

# N32H787

# Product Brief

The N32H787 series adopts a high-performance dual-core architecture. The ARM Cortex-M7 core is the main core, running at frequencies up to 600MHz, supporting double-precision floating-point operations and DSP instructions. The Cortex-M4 core is the auxiliary core, running at frequencies up to 300MHz. It has (2/4MB) of on-chip FLASH, integrates up to 1504KB of SRAM (including 1024KB TCM SRAM and 480KB SRAM) + 4KB Backup SRAM, integrates 3 12-bit 5Mps ADCs, 4 high-speed comparators, 6 12-bit DACs, and features multiple high-speed communication interfaces including U(S)ART, I2C, xSPI, SPI, USBFS Dual Role, USBHS Dual Role, CAN-FD, SDRAM, FEMC, SDMMC, and 10/100/1000M Ethernet. It supports digital camera interface (DVP), MIPI, TFT-LCD graphic interface, JPEG hardware encoder/decoder and GPU. The chip has a built-in high-performance encryption algorithm hardware acceleration engine supporting AES/TDES and SHA algorithms, supports TRNG true random number generator, and supports CRC8/16/32. It supports up to 166 GPIOs and is available in UFBGA169, LQFP176, LQFP208, and TFBGA240+25 packages.

## Key Features

- **Dual-Core Architecture CPU (Cortex-M7 and Cortex-M4F)**
  - **ARM Cortex-M7**
    - 32-bit ARM Cortex-M7 core, double-precision floating-point unit, supports DSP instructions and MPU
    - Built-in 32KB instruction cache and 32KB data cache with ECC
    - Maximum frequency 600MHz, 1284 DMIPS
  - **ARM Cortex-M4F**
    - 32-bit ARM Cortex-M4F core + FPU, single-cycle hardware multiply-divide instructions, supports DSP instructions and MPU
    - Built-in 16KB instruction cache and 16KB data cache with parity checking, supports Flash acceleration unit with 0 wait state program execution
    - Maximum frequency 300MHz, 375 DMIPS
- **Encrypted Memory**
  - 2M/4M Byte on-chip Flash, supports encrypted storage with automatic program decryption during execution
  - 1504KB built-in SRAM with ECC support
    - 1024KB TCM SRAM, configurable as D-TCM, I-TCM or SRAM
    - 480KB on-chip SRAM
- **Operating Modes**
  - Run mode
  - SLEEP mode: AXI enabled, AHB enabled
  - Stop0 mode: SRAM, TCM, RTC, LSE, IWDG enabled

- Stop2 mode: Flash in standby mode, SRAM, TCM, RTC, LSE, IWDG, Backup SRAM, backup registers enabled, I/O state maintained
- Standby mode: Backup SRAM, RTC, IWDG, LSE, backup registers enabled, SRAM and TCM disabled
- VBAT mode: Backup SRAM, RTC, LSE, backup registers enabled
- **Clock**
  - 4MHz~48MHz external high-speed crystal
  - 4MHz~50MHz external clock input
  - 32.768KHz external low-speed crystal
  - Three built-in high-speed PLLs
  - Built-in MSI clock supporting 31.25K/62.5K/125K/250K/500K/1M/2M/4M/8M/16MHz configurations
  - Internal high-speed RC 64MHz
  - Internal low-speed RC 32KHz
- **Reset**
  - Supports power-on/power-down/external pin reset
  - Supports watchdog reset and software system reset
  - Supports programmable voltage detection
- **High-Speed Communication Interfaces**
  - 8 USART interfaces/7 UART interfaces, supporting ISO7816, IrDA, LIN
  - 2 LPUART interfaces
  - 7 SPI interfaces, supporting master/slave modes, up to 50 MHz
  - 10 I2C interfaces, up to 3.4 MHz, configurable master/slave modes, supports dual address response in slave mode
  - 1 USBHS Dual Role interface with built-in high-speed PHY
  - 1 USBFS Dual Role interface
  - 8 CAN-FD bus interfaces
  - 2 Ethernet MAC interfaces: ETH1 supports 10M/100M/1000M rates, ETH2 supports 10M/100M rates, both support IEEE 1588 time synchronization protocol
- **High-Performance Analog Interfaces**
  - 3 12-bit 5Msps ADCs, supporting 12-bit/10-bit resolution with hardware oversampling up to 16-bit, up to 55 external single-ended input channels, 5 internal single-ended input channels, supporting single-ended and differential modes
  - 4 high-speed analog comparators
  - 6 12-bit DACs: 2 1Msps DACs supporting buffered/unbuffered external output (internal output only supports unbuffered mode; simultaneous internal/external output requires buffer enabled), 4 DACs supporting only internal chip output with 15Msps sampling rate and unbuffered output
  - 2 MCO outputs, configurable to output SYSCLK, HSE, MSI, LSE, LSI, HSI64 or PLL clock division
  - 1 reference voltage VREFBUF (configurable: 1.5V/1.8V/2.048V/2.5V)

- 1 temperature sensor
- **Audio Interfaces**
  - 4 I2S interfaces, supporting half/full duplex modes, audio sampling rates from 8KHz to 192KHz
  - 8 PDM digital microphone interfaces built into DSMU
- **Memory Expansion Interfaces**
  - 1 FEMC (Flexible External Memory Controller) interface, 100 MHz bus rate, SRAM/PSRAM/Nor Flash supporting 16/32-bit data width, NAND Flash supporting 8/16-bit data width
  - 1 xSPI interface, supporting 1/2/4/8-bit data width, master/slave configurable, up to 133 MHz, usable for expanding SRAM, PSRAM and Flash, supports XIP
  - 1 SDRAM interface, up to 133 MHz
  - 2 SDMMC interfaces, supporting SD/SDIO 3.0, eMMC 4.51 format, up to 104MHz
- **Image Processing Interfaces**
  - 2 digital camera interfaces (DVP), supporting 8/10/12/16bit, up to 110MHz
  - 1 MIPI display controller (DSI) with built-in D-PHY
  - 1 TFT-LCD display interface, supporting up to 24-bit parallel digital RGB LCD with all signal interfaces for direct connection to various LCD and TFT panels, resolution up to 1920x1080
  - Built-in 2.5D graphics processor supporting image scaling, rotation, mixing, anti-aliasing, texture mapping, etc.
  - Hardware JPEG encoder/decoder
- **Maximum support for 166 GPIOs, low-speed GPIOs support 5V tolerance (under VDD=3.3V±10% condition)**
- **Motor control Cordic accelerator, supporting trigonometric and hyperbolic functions, supports floating-point input and output**
- **Delta Sigma Module Unit (DSMU)**
- **Built-in filter algorithm accelerator FMAC, supporting FIR and IIR filtering**
- **3 high-speed DMA controllers, each supporting 8 channels, 1 MDMA supporting 16 channels, fully configurable channel source and destination addresses**
- **RTC real-time clock, supporting perpetual calendar with leap year, alarm events, periodic wake-up, internal/external clock calibration**
- **Timers**
  - 2 16-bit ultra-high precision timers (SHRTIM1/SHRTIM2), highest control precision 100ps, each with 1 master timer and 6 16-bit slave timer units. Each timer unit has 2 independent channels, supporting 12 independent PWM outputs or 6 pairs of complementary PWM outputs
  - 4 16-bit advanced timers, supporting input capture, complementary output, quadrature encoder input, etc., highest control precision 3.3ns; each timer has 6 independent channels, 4 of which support 4 pairs of complementary PWM outputs
  - 10 16-bit general-purpose timers (GTIMA13), each with 4 independent channels, supporting input capture, output compare, PWM generation
  - 4 32-bit basic timers (BTIM1~4)

- 5 16-bit low-power timers (LPTIM1~5), operational in Stop2 mode
- 2x 24-bit SysTick, 2x 14-bit window watchdogs (WWDG), 2x 12-bit independent watchdogs (IWDG)

● **Programming**

- Supports SWD/JTAG online debugging interfaces
- Supports USB, UART Bootloader

● **Security Features**

- FLASH has up to 4 encryption partitions, supporting storage encryption
- Supports write protection (WRP), multiple read protection (RDP) levels (L0/L1/L2)
- Built-in cryptographic hardware acceleration engine, supporting AES/TDES, SHA, SM4 algorithms
- TRNG true random number generator, CRC8/16/32 computation
- Supports secure boot, encrypted program download, secure update, external high and low-speed clock failure detection
- Supports tamper detection

● **Supports 128-bit UCID in OTP**

● **Operating Conditions**

- Operating voltage range: 2.3V~3.6V
- Chip junction temperature range: -40°C~125°C

● **Certification**

- USB IF
- IEC61508 SIL2

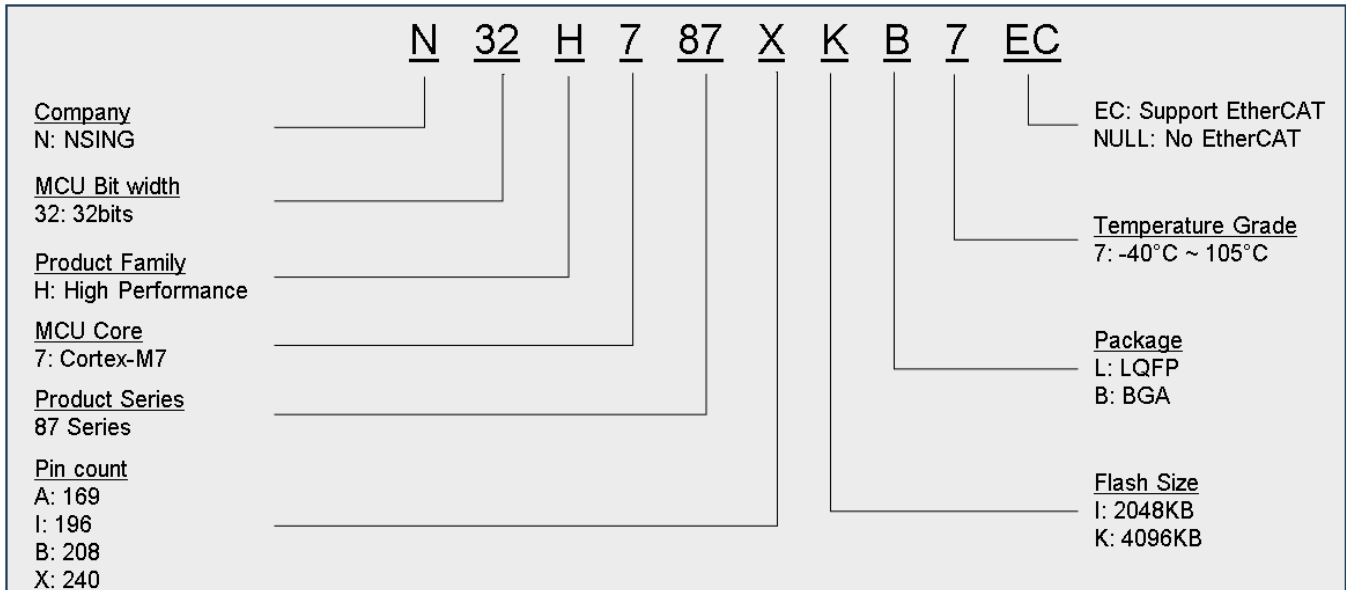
● **Package**

- UFBGA169(7mmx7mm)
- LQFP176(24mm x 24mm)
- LQFP208(28mmx28mm)
- TFBGA240+25(14mmx14mm)

● **Ordering Model**

Series	Model
N32H787xxx7	N32H787AKB7, N32H787AIB7, N32H787IKL7, N32H787IIL7, N32H787BKL7, N32H787BIL7, N32H787XKB7, N32H787XIB7

# 1 Naming Convention



## 2 Product Model and Resource Configuration

Table 2-1 N32H787 Series Resource Configuration

Device Model		N32H787A KB7	N32H787A IB7	N32H787I KL7	N32H787I IL7	N32H787B KL7	N32H787B IL7	N32H787XK B7	N32H787X IB7
Flash (KB)		4096	2048	4096	2048	4096	2048	4096	2048
SRAM (KB)	TCM	1024							
	System RAM	480							
	Backup RAM	4							
Core	M7	600MHz							
	M4	300MHz							
Operating Voltage		2.3V~3.6V							
DCDC (step-down)		Yes							
Coprocessor	Cordic	Yes							
	DSMU	Yes							
	FMAC	Yes							
Timers	SHRTIM	2							
	ADTIM	4							
	GPTIM	10							
	BSTIM	4							
	LPTIM	5							
	SysTick timer	2							
	WWDG	2*14bit							
	IWDG	2*12bit							
	RTC	Yes							
Communica tion Interfaces	SPI/I2S	6/4				7/4			
	I2C	8				10			
	USART	6				7		8	
	UART	5				7			
	LPUART	2							
	USBHS Dual Role	1							
	USBFS Dual Role	1							
	CAN FD	8							
	10/100M ETH	1							
	10/100/100 0M ETH	1							
Expanded Storage	SDRAM	Yes							
	xSPI	1							
	FEMC	Yes							
	SDMMC	2							
Analog	12bit ADC	3							
	12bit DAC Number of channels	2+4 <sup>(1)</sup> 2 External channels							

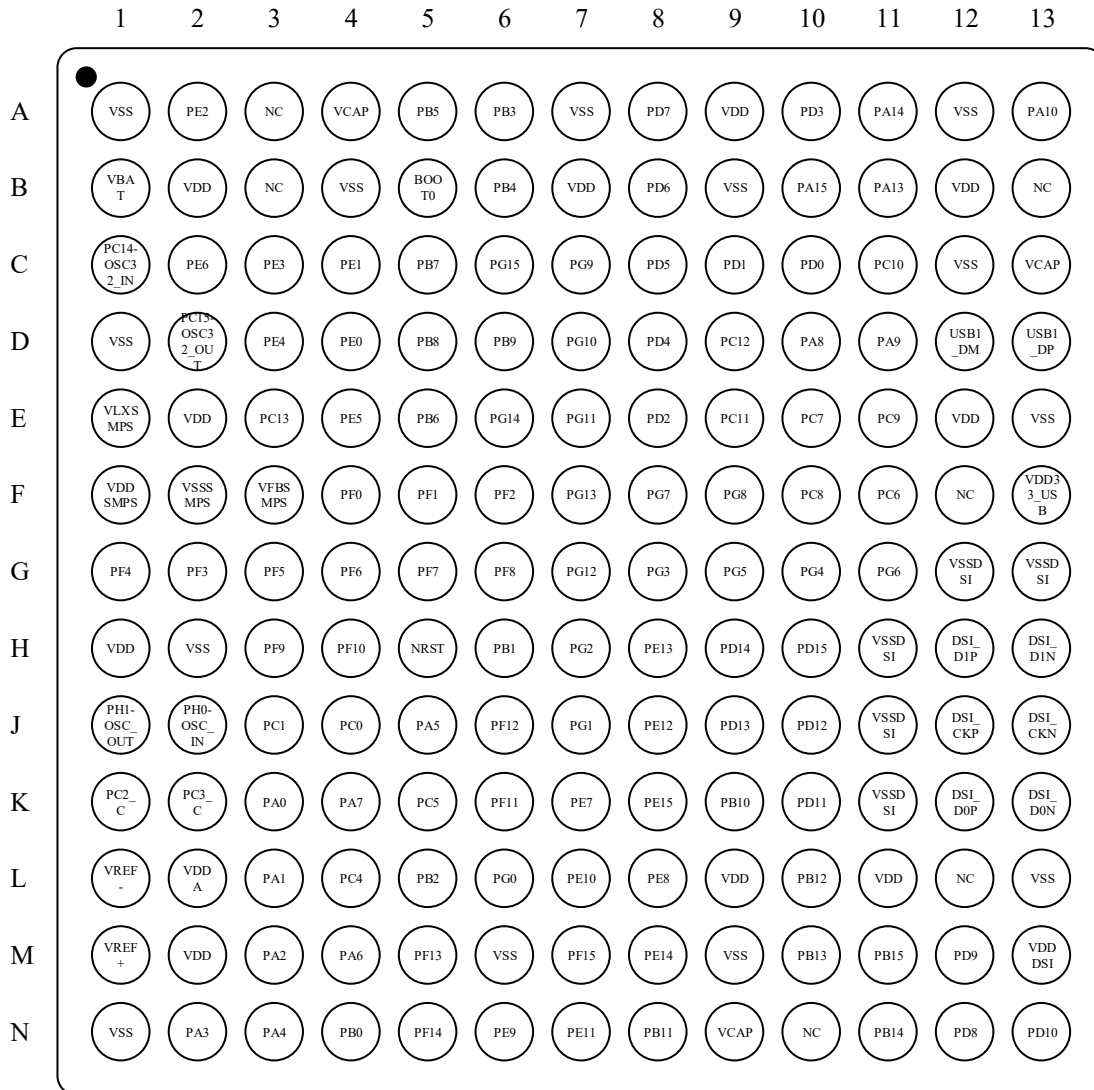
	Comparator	4		
	VREFBUF	Yes		
Imaging	LCDC	Yes		
	MIPI	Yes		
	GPU	Yes		
	JPEG	Yes		
	DVP	2		
GPIO		112	139	166
DMA Number of channels		3 24Channel		
MDMA Number of channels		1 16Channel		
Algorithm Support		DES/3DES, AES, SHA1/SHA224/SHA256, CRC8/16/CRC32		
Security Protection		Read/write protection (RDP/WRP), storage encryption, secure boot		
Package	UFBGA169	LQFP176	LQFP208	TFBGA240+25

*Note: 4 DACs only support internal connection and cannot output to GPIO*

### 3 Package

#### 3.1 UFBGA169 Package

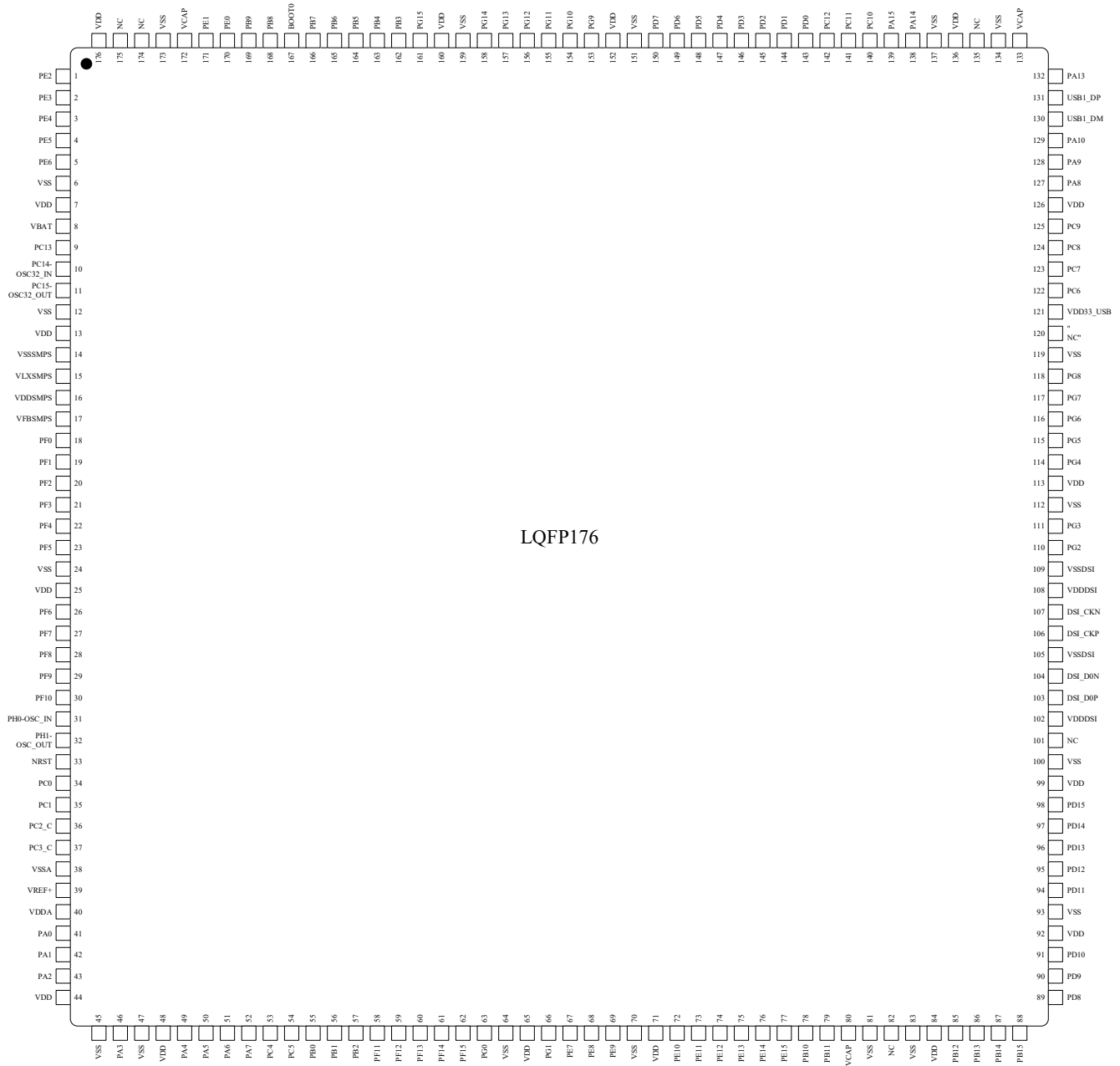
##### 3.1.1 UFBGA169 Pin Distribution



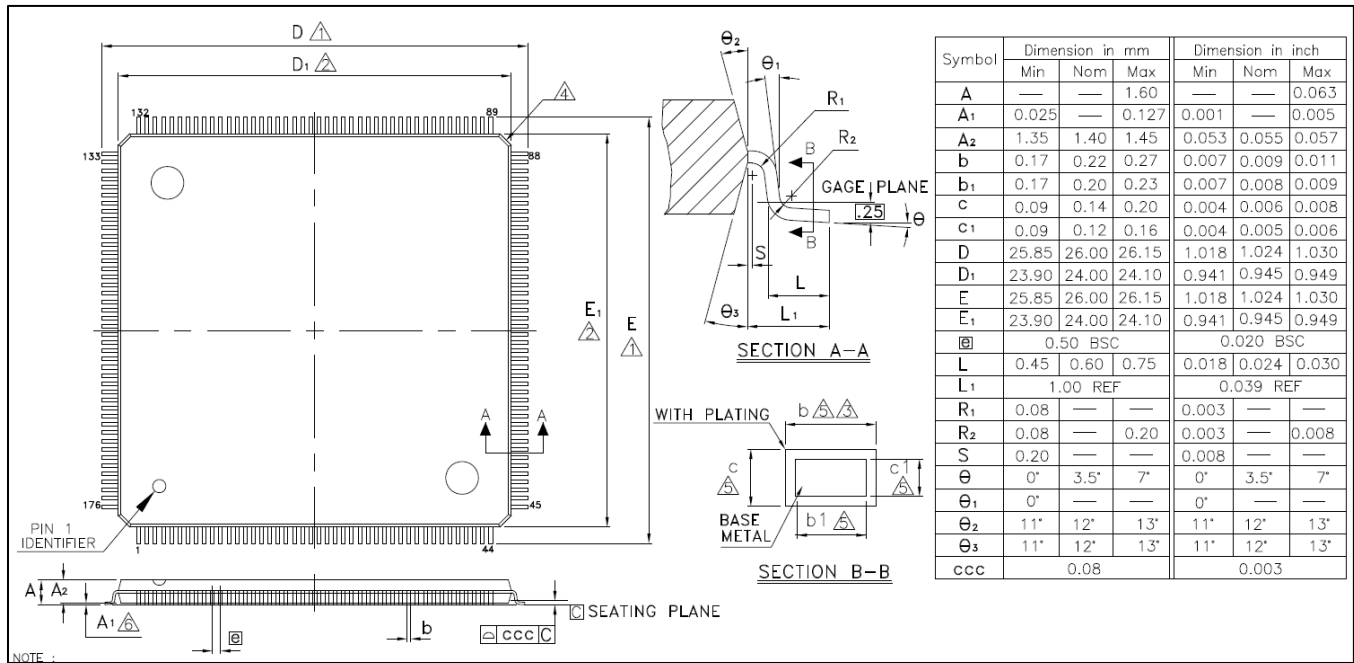


## 3.2 LQFP176 Package

### 3.2.1 LQFP176 Pin Distribution

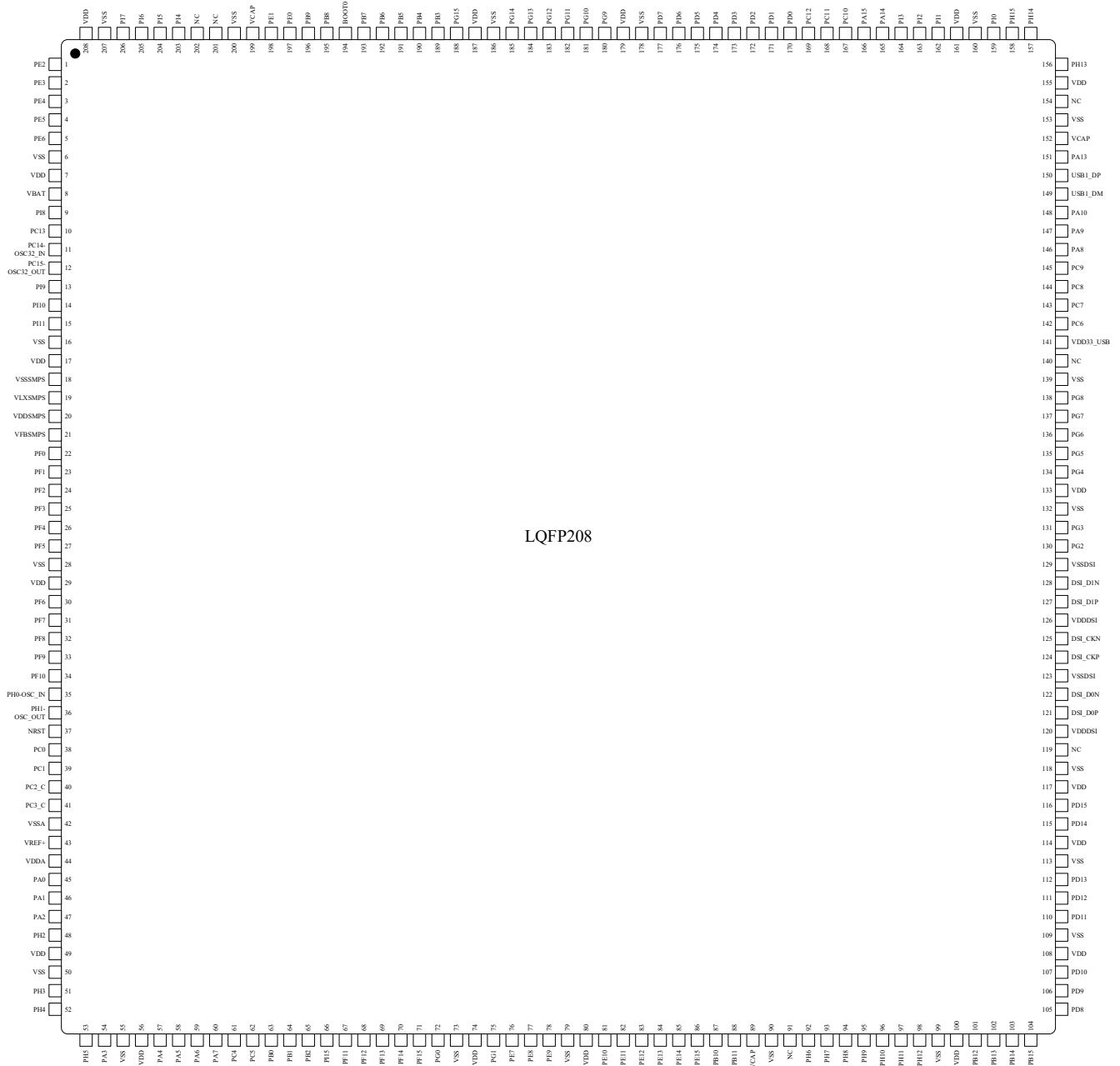


### 3.2.2 LQFP176 Package Size

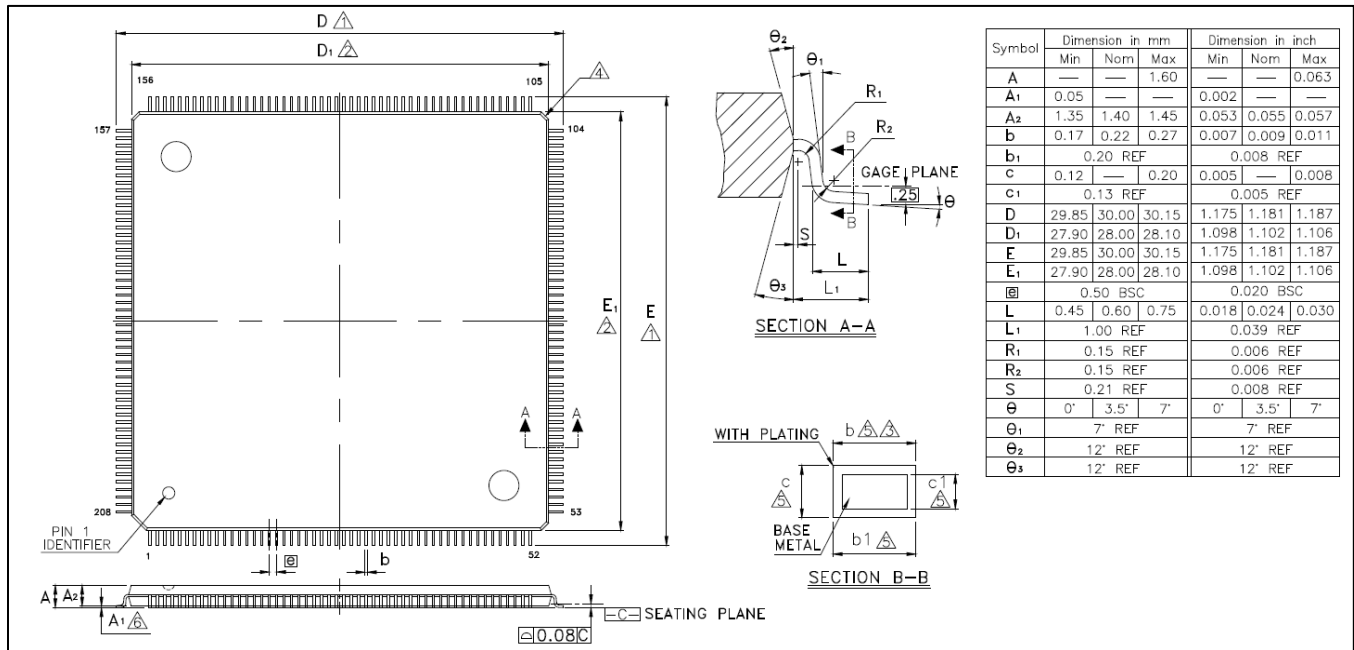


### 3.3 LQFP208 Package

#### 3.3.1 LQFP208 Pin Distribution

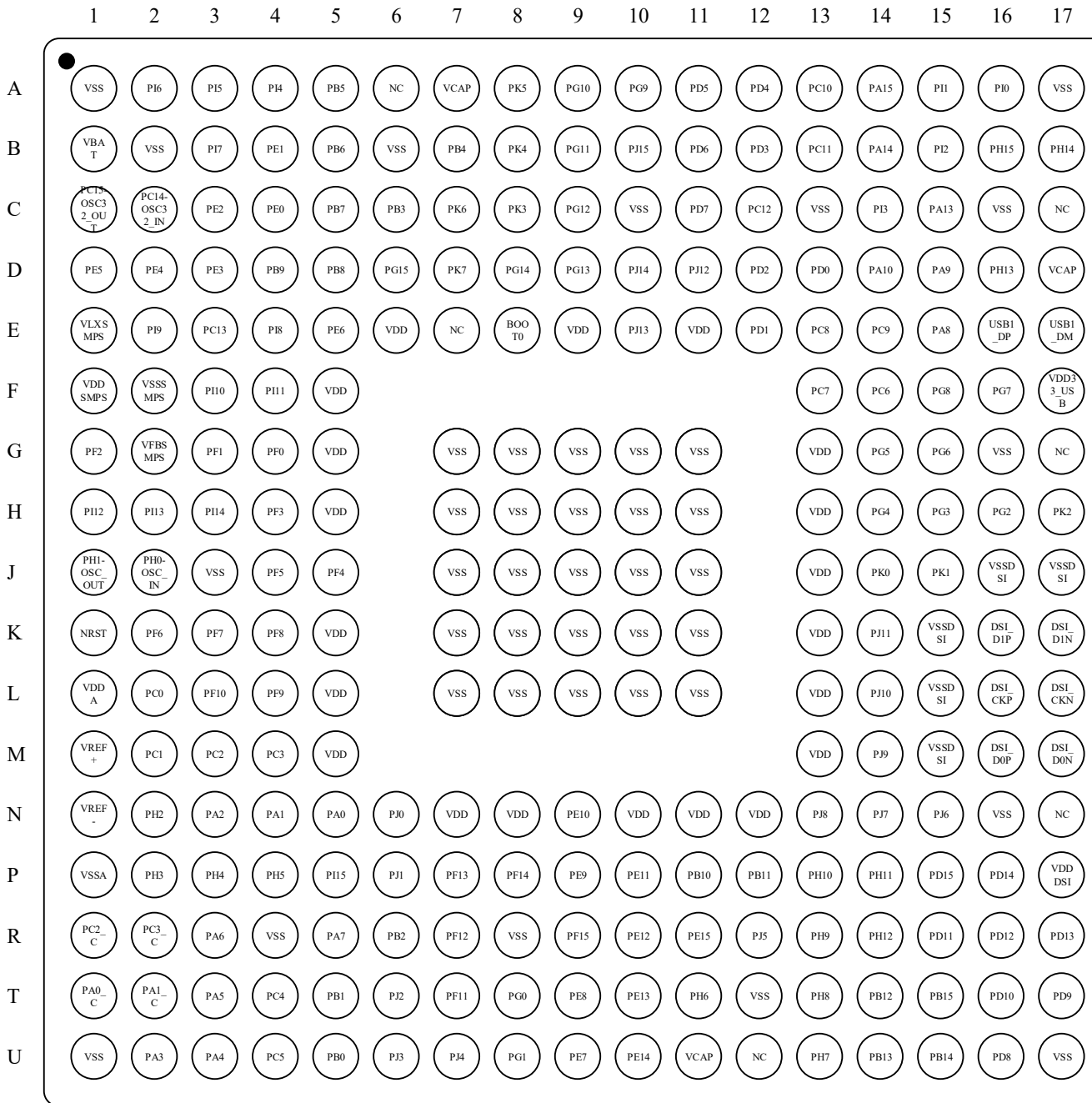


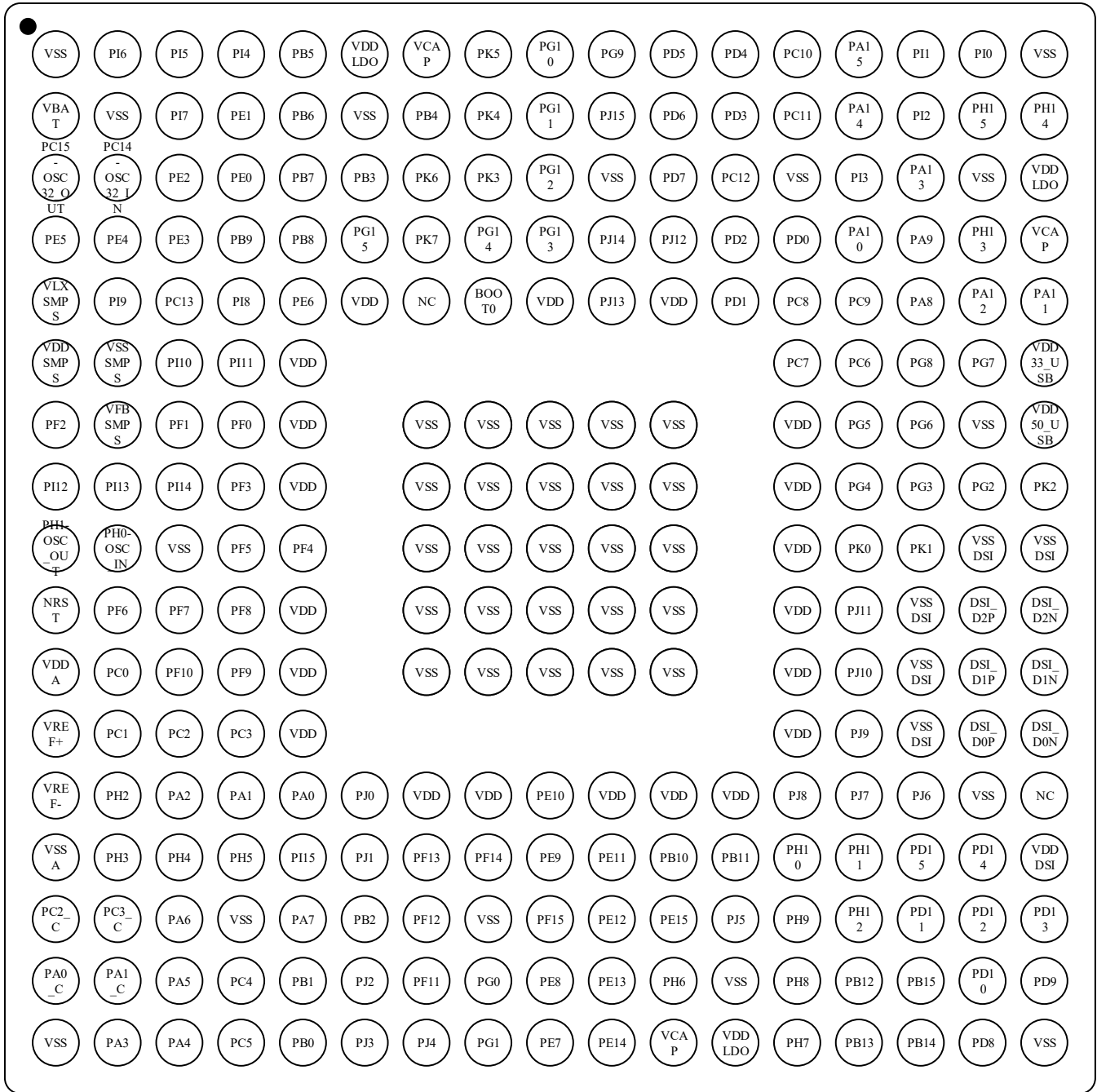
### 3.3.2 LQFP208 Package Size

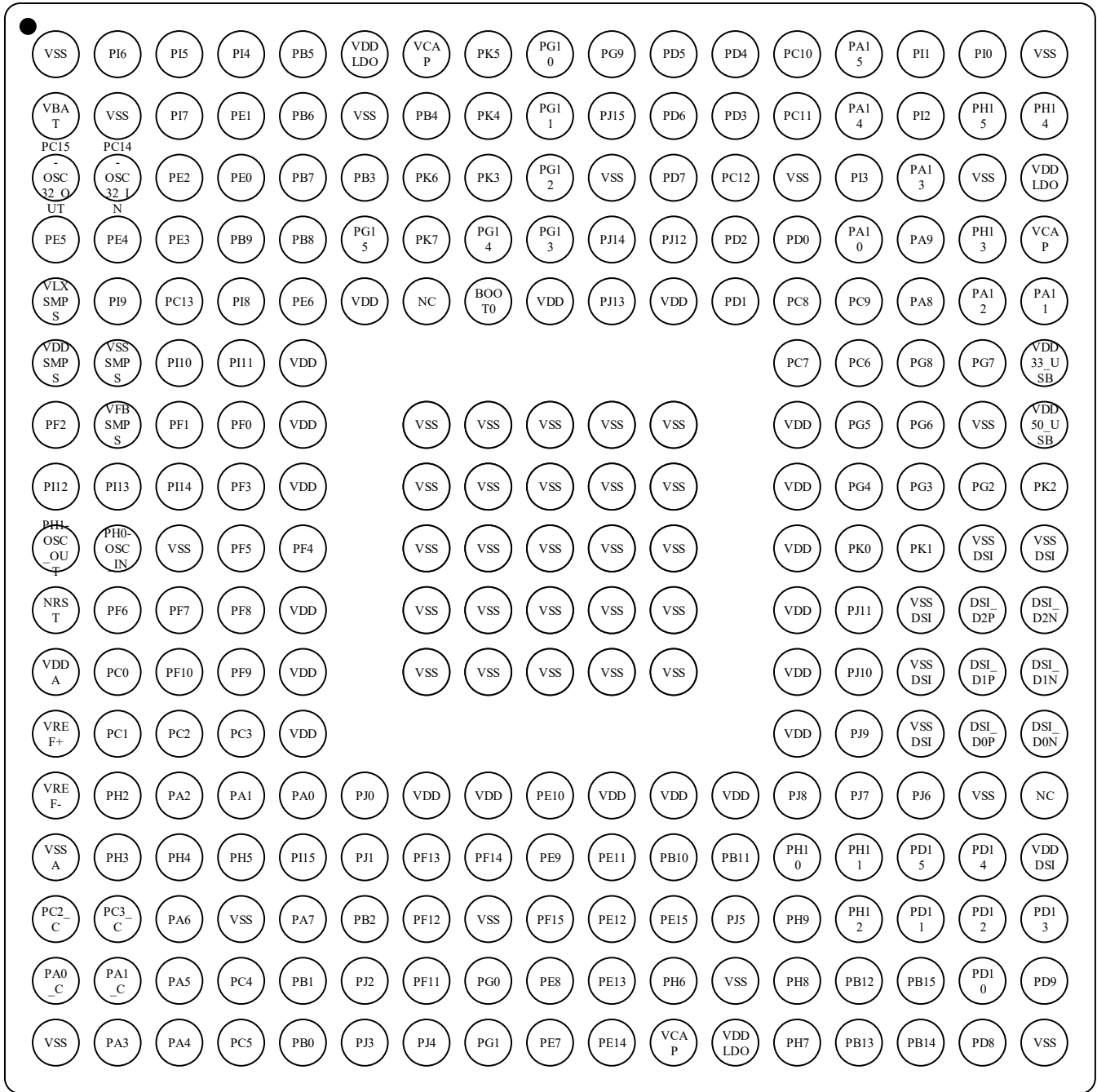


### 3.4 TFBGA240+25 Package

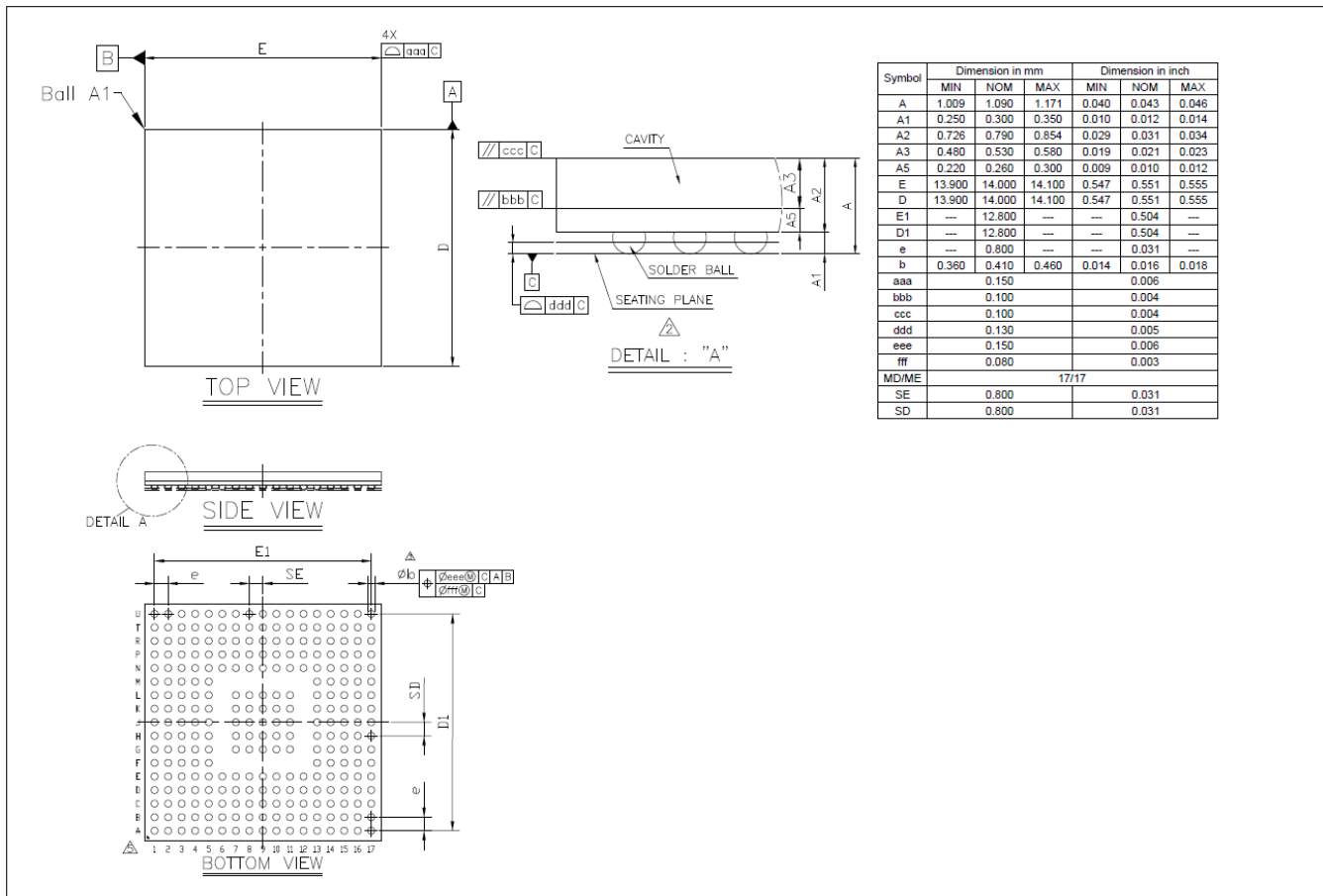
#### 3.4.1 TFBGA240+25 Pin Distribution







### 3.4.2 TFBGA240+25 Package Size





## 4 Version History

Version	Date	Changes
V1.0.0	2025.4.23	First release

## 5 Disclaimer

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