

Porting Guide

STM32F407/417 Series to N32H487 Series

Introduction

The migration guide primarily outlines the disparities between the STM32F407/417 series and the N32H487 series, facilitating a seamless transition from developing with the STM32F407/417 series to the N32H487 series.

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1 Overview

The N32H487 series is the latest high-performance general-purpose secure MCU product developed by Nsing Technologies based on the Cortex-M4 core. It supports multiple packaging forms such as LQFP64, LQFP100, and LQFP128, and is compatible with the corresponding packaging pins of the STM32F407/417 series.

This guide mainly introduces the differences in resources and IO functions between two series of chips, as follows:

- Resource Differences: Introduce the differences in resources such as general basic modules, communication peripherals, analog peripherals, timers, etc. under various corresponding packaging
- Hardware differences: Introduction includes differences in pin layout and functional mapping
- Minimum System Design: N32H487 Minimum System Design Considerations
- Main functional differences: Introduce the main functional differences of each module

2 Resource Differences

2.1 LQFP100 Packaging Resource Differences

The comparison of resource differences between STM32F407/417 LQFP100 package and N32H487 LQFP100 package is shown in the following table:

Device model		STM32F407VET6 STM32F407VGT6 STM32F407VGT7	STM32F417VET6 STM32F417VGT6 STM32F417VGT7	N32H487VEL7
FLASH(KB)		512	1024	512
SRAM (KB)	General SRAM	112+16		160
	CCM SRAM	64		32
	Backup SRAM	4		4
Core		Cortex-M4F		Cortex-M4F
Maximum frequency		168MHz		240MHz
Work environment		1.8~3.6V/-40~85°C/105°C		1.8~3.6V/-40~105°C
Storage Expansion	FEMC	Address Data Bus Reuse Mode		Address Data Bus Reuse Mode
	SDIO	Yes		Yes
	xSPI	-		Yes
DMA		2*8CH		2*8CH
DVP		Yes		Yes
Timer	Advance d	2*16bit		3*16bit
	General	8*16bit+2*32bit		7*16bit+3*16bit
	Basic	2*16bit		2*32bit
	Lower power	-		2*16bit
	SysTick	1		1
	IWDG	1*12bit		1*12bit
	WWDG	1*7bit		1*14bit
Communication interface	SPI	3		6
	I2S	2		2
	I2C	3		4
	USART	4		4
	UART	2		4
	CAN	2*CAN		3*FDCAN
	Ethernet	Yes		Yes
	USB FS	Yes		Yes
	USB HS	Yes		Yes
RTC		Yes		Yes
Tamper pins		1		3
CORDIC		-		Yes
FMAC		-		Yes
GPIO		82		85
Wakeup pins		1		5
12bit ADC		3		4
ADC channels		16		42
12bit DAC		Yes		2
DAC channels		2		2
VREFBUF		-		Yes
Algorithm support		TRNG、CRC32	TRNG、CRC32、 DES/3DES、AES、 SHA1/SHA224/SHA 256、MD5、HMAC	DES/3DES、AES、SHA1/SHA224/SHA256、 SM3、SM4、MD5、CRC16/CRC32、TRNG

Safety protection	RDP、PCROP、WRP	Read write protection (RDP/WRP), storage encryption, partition protection, secure boot
Package	LQFP100	LQFP100

2.2 LQFP144 Packaging Resource Differences

The comparison of resource differences between STM32F407/417 LQFP144 package and N32H487 LQFP144 package is shown in the following table:

Device model		STM32F407ZET6 STM32F407ZGT6 STM32F407ZGT7	STM32F417ZET6 STM32F417ZGT6	N32H487ZEL7
FLASH(KB)		512	1024	512
SRAM (KB)	General SRAM	112+16		160
	CCM SRAM	64		32
	Backup SRAM	4		4
Core		Cortex-M4F		Cortex-M4F
Maximum frequency		168MHz		240MHz
Work environment		1.8~3.6V/-40~ 85°C/105°C	1.8~3.6V/-40~85°C	1.8~3.6V/-40~105°C
Storage Expansion	FEMC	Yes		Yes
	SDIO	Yes		Yes
	xSPI	-		Yes
DMA		2*8CH		2*8CH
DVP		Yes		Yes
Timer	Advanced	2*16bit		3*16bit
	General	8*16bit+2*32bit		7*16bit+3*16bit
	Basic	2*16bit		2*32bit
	Lower power	-		2*16bit
	SysTick	1		1
	IWDG	1*12bit		1*12bit
	WWDG	1*7bit		1*14bit
Communica tion interface	SPI	3		6
	I2S	2		2
	I2C	3		4
	USART	4		4
	UART	2		4
	CAN	2*CAN		3*FDCAN
	Ethernet	Yes		Yes
	USB FS	Yes		Yes
	USB HS	Yes		Yes
RTC		Yes		Yes
Tamper pins		1		3
CORDIC		-		Yes
FMAC		-		Yes
GPIO		114		118
Wakeup pins		1		5
12bit ADC		3		4
ADC channels		24		42
12bit DAC		Yes		2
DAC channels		2		2
VREFBUF		-		Yes

Algorithm support	TRNG、CRC32	TRNG、CRC32、 DES/3DES、AES、 SHA1/SHA224/SHA256、MD5、HMAC	DES/3DES、AES、 SHA1/SHA224/SHA256、SM3、SM4、 MD5、CRC16/CRC32、TRNG
Safety protection	RDP、PCROP、WRP		Read write protection (RDP/WRP), storage encryption, partition protection, secure boot
Package	LQFP100		LQFP100

3 Hardware Differences

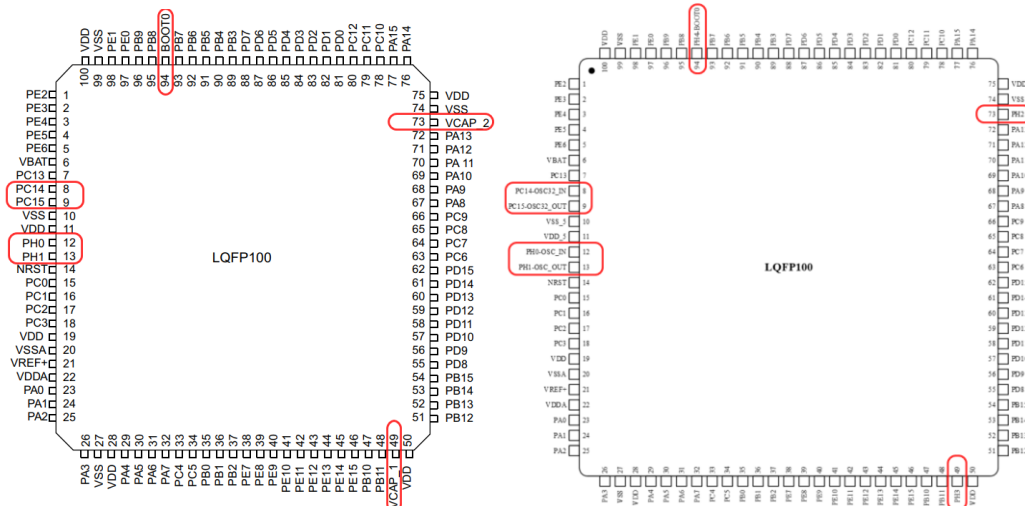
3.1 Pin Layout

The N32H487 series is basically compatible with the STM32F407/417 series pins, with the following specific differences:

- STM32F407/417 PC14/PC15 can also be used as a low-speed clock port, which is different from N32H487 only in terms of pin naming.
- STM32F407/417 PH0/PH1 can also be used as a high-speed clock port, which is different from N32H487 only in terms of pin naming.
- N32H487 does not have VCAP_1/VCAP_2 pins and does not require external capacitors. The corresponding pins have been changed to GPIO PH3/PH2.
- The N32H487 BOOT0 pin can be reused as GPIO PH4.
- The N32H487 LQFP144 package does not support PDR_ON function, and the corresponding pin has been changed to GPIO PH5.

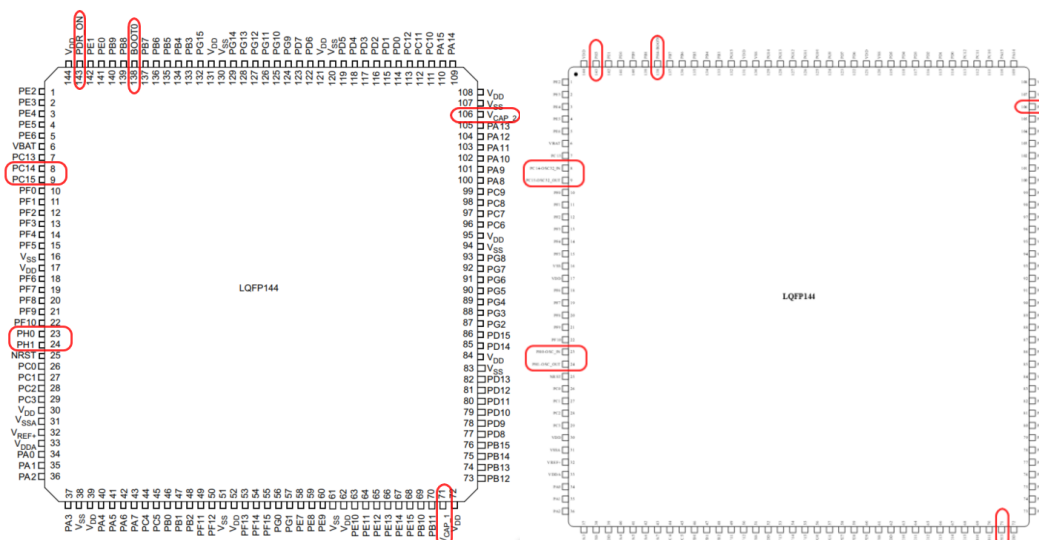
3.1.1 LQFP100

On the left is the pin distribution diagram of STM32F407/417 series LQFP100, and on the right is the pin distribution diagram of N32H487 series LQFP100:



3.1.2 LQFP144

On the left is the pin distribution diagram of STM32F407/417 series LQFP144, and on the right is the pin distribution diagram of N32H487 series LQFP144:



3.2 Pin Function Mapping

The N32H487 series provides more peripheral multiplexing functionality on each pin, making practical applications more flexible. Some of the pin functions have differences or do not meet the requirements. Based on the multiplexing function of STM32F407/417, the main differences are as follows:

- The RTS_DE, TX, and RX signals of the N32H487 series USART3, USART5, and UART8 can be mapped to any IO
- The TX and RX signals of the N32H487 series FDCAN1, FDCAN2, and FDCAN3 can be mapped to any IO
- N32H487 series supports XSPI
- N32H487 series supports LPTIM

The differences in pin reuse function are detailed in the table below. Based on the reuse function of STM32F407/417 series, the highlighted red parts are the pins with differences or that do not meet the function requirements:

LQFP100	LQFP144	Pin name	Pins Reuse function	
			STM32F407/417	N32H487
1	1	PE2	TRACECLK ETH_MII_TXD3 FSMC_A23 EVENTOUT	FEMC_A23 ETH_MII_TX_D3 GTIM2_CH1 SPI4_SCK ATIM3_CH1 USART4_TX DVP_HSYNC EVENTOUT
2	2	PE3	TRACED0 FSMC_A19 EVENTOUT	FEMC_A19 GTIM2_CH2 SPI4_NSS ATIM3_CH2 USART4_RX DVP_VSYNC EVENTOUT
3	3	PE4	TRACED1 FSMC_A20 EVENTOUT DCMI_D4	FEMC_A20 DVP_D4 GTIM2_CH3 SPI4_NSS ATIM3_CH1N

LQFP100	LQFP144	Pin name	Pins Reuse function	
			STM32F407/417	N32H487
				DVP_PIXCLK EVENTOUT
4	4	PE5	TRACED2 FSMC_A21 EVENTOUT TIM9_CH1 DCMI_D6	FEMC_A21 GTIM5_CH1 DVP_D6 GTIM2_CH4 SPI4_MISO ATIM3_CH2N DVP_D0 EVENTOUT
5	5	PE6	TRACED3 FSMC_A22 EVENTOUT TIM9_CH2 DCMI_D7	FEMC_A22 GTIM5_CH2 DVP_D7 SPI4_MOSI ATIM3_CH3N DVP_D1 LPTIM2_IN1 EVENTOUT WKUP3 RTC_TAMP3
6	6	VBAT	VBAT	VBAT
7	7	PC13	EVENTOUT RTC_OUT RTC_TAMP1 RTC_TS	RTC_OUT1 ATIM1_CH1N ATIM1_BKIN ATIM2_CH4N LPTIM2_ETR XSPI_RXDS ATIM3_BKIN EVENTOUT WKUP2 RTC_TAMP1
8	8	PC14	EVENTOUT OSC32_IN	GTIM7_CH3 EVENTOUT OSC32_IN
9	9	PC15	EVENTOUT OSC32_OUT	GTIM7_CH4 EVENTOUT OSC32_OUT
-	10	PF0	FSMC_A0 EVENTOUT I2C2_SDA	FEMC_A0 I2C2_SDA ATIM3_CH1 XSPI_NSS1 UART8_CTS EVENTOUT
-	11	PF1	FSMC_A1 EVENTOUT I2C2_SCL	FEMC_A1 I2C2_SCL ATIM3_CH2 XSPI_CLK EVENTOUT
-	12	PF2	FSMC_A2 EVENTOUT I2C2_SMBA	FEMC_A2 I2C2_SMBA ATIM3_CH3 XSPI_IO0

LQFP100	LQFP144	Pin name	Pins Reuse function	
			STM32F407/417	N32H487
				EVENTOUT ADC1_IN13
-	13	PF3	FSMC_A3 EVENTOUT ADC3_IN9	FEMC_A3 ATIM3_CH4 I2C3_SCL XSPI_IO1 EVENTOUT ADC3_IN17
-	14	PF4	FSMC_A4 EVENTOUT ADC3_IN14	FEMC_A4 ATIM3_CH1N I2C3_SDA XSPI_IO2 GTIM5_CH1 I2C3_SCL EVENTOUT ADC3_IN0
-	15	PF5	FSMC_A5 EVENTOUT ADC3_IN15	FEMC_A5 ATIM3_CH2N XSPI_IO3 GTIM5_CH2 I2C3_SDA EVENTOUT ADC3_IN13
10	16	VSS	VSS	VSS
11	17	VDD	VDD	VDD
-	18	PF6	FSMC_NIORD EVENTOUT TIM10_CH1 ADC3_IN4	GTIM6_CH1 GTIM4_ETR GTIM3_CH4 I2C2_SCL GTIM4_CH1 XSPI_IO3 SPI5_NSS UART7_RX DVP_D14 EVENTOUT ADC2_IN16
-	19	PF7	FSMC_NREG EVENTOUT TIM11_CH1 ADC3_IN5	GTIM7_CH1 ATIM3_BKIN GTIM4_CH2 XSPI_IO2 FEMC_A1 SPI5_SCK UART7_TX GTIM8_ETR EVENTOUT ADC1_IN15
-	20	PF8	FSMC_NIOWR EVENTOUT TIM13_CH1 ADC3_IN6	GTIM9_CH1 ATIM3_BKIN2 GTIM4_CH3 XSPI_IO0 FEMC_A24 SPI5_MISO EVENTOUT

LQFP100	LQFP144	Pin name	Pins Reuse function	
			STM32F407/417	N32H487
				ADC2_IN1
-	21	PF9	FSMC_CD EVENTOUT TIM14_CH1 ADC3_IN7	GTIM10_CH1 ATIM3_BKIN GTIM8_CH1 SPI2_SCK GTIM4_CH4 XSPI_IO1 FEMC_A25 SPI5_MOSI DVP_D15 EVENTOUT ADC4_IN17
-	22	PF10	FSMC_INTR EVENTOUT ADC3_IN8	ATIM3_BKIN2 GTIM8_CH2 SPI2_SCK XSPI_CLK FEMC_A0 DVP_D11 EVENTOUT ADC4_IN0
12	23	PH0	EVENTOUT OSC_IN	I2C2_SDA SPI2_NSS/I2S2_WS ATIM1_CH3N USART2_RX GTIM5_CH3 ATIM3_CH1N EVENTOUT OSC_IN ADC1_IN10
13	24	PH1	EVENTOUT OSC_OUT	I2C2_SCL SPI2_SCK/I2S2_CK USART2_TX GTIM5_CH4 ATIM3_CH2N EVENTOUT OSC_OUT ADC2_IN10
14	25	NRST	NRST	NRST
15	26	PC0	EVENTOUT OTG_HS_ULPI_STP ADC123_IN10	LPTIM1_IN1 ATIM1_CH1 UART7_RX I2C3_SCL DVP_D2 USART4_TX XSPI_RXDS DVP_D15 GTIM10_CH1 EVENTOUT ADC12_IN6
16	27	PC1	ETH_MDC EVENTOUT ADC123_IN11	ETH_MDC LPTIM1_OUT ATIM1_CH2 UART7_TX

LQFP100	LQFP144	Pin name	Pins Reuse function	
			STM32F407/417	N32H487
				XSPI_IO4 SPI3_MOSI/I2S3_SD SPI2_MOSI/I2S2_SD I2C3_SDA USART4_RX GTIM10_CH2 EVENTOUT ADC12_IN7
17	28	PC2	SPI2_MISO I2S2ext_SD ETH_MII_TXD2 EVENTOUT OTG_HS_ULPI_DIR ADC123_IN12	SPI2_MISO ETH_MII_TX_D2 I2S2_AUX_SD LPTIM1_IN2 ATIM1_CH3 ATIM3_CH2 XSPI_IO5 SPI3_NSS/I2S3_WS GTIM10_CH3 UAR7_TX EVENTOUT ADC12_IN8
18	29	PC3	SPI2_MOSI I2S2_SD ETH_MII_TX_CLK EVENTOUT OTG_HS_ULPI_NXT ADC123_IN13	SPI2_MOSI/I2S2_SD ETH_MII_TX_CLK LPTIM1_ETR ATIM1_CH4 ATIM1_BKIN2 XSPI_IO6 SPI3_SCK/I2S3_CK GTIM10_CH4 UAR7_RX EVENTOUT ADC12_IN9
19	30	VDD	VDD	VDD
20	31	VSSA	VSSA	VSSA
21	32	VREF+	VREF+	VREF+
22	33	VDDA	VDDA	VDDA
23	34	PA0/WKUP	ETH_MII_CRS EVENTOUT TIM2_CH1_ETR TIM5_CH1 TIM8_ETR UART4_TX USART2_CTS WKUP ADC123_IN0	USART2_CTS UART6_TX ETH_MII_CRS GTIM1_CH1_ETR GTIM4_CH1 ATIM2_ETR ATIM2_BKIN SPI3_MISO ATIM3_CH3N EVENTOUT ADC12_IN3 WKUP1 RTC_TAMP2
24	35	PA1	ETH_RMII_REF_CLK ETH_MII_RX_CLK EVENTOUT TIM5_CH2 TIM2_CH2	USART2_RTS_DE UART6_RX ETH_RMII_REF_CLK ETH_MII_RX_CLK GTIM4_CH2

LQFP100	LQFP144	Pin name	Pins Reuse function	
			STM32F407/417	N32H487
			UART4_RX USART2_RTS ADC123_IN1	GTIM1_CH2 GTIM8_CH1N SPI4_MOSI DVP_HSYNC SPI3_MOSI/I2S3_SD SPI6_SCK ATIM3_CH4N EVENTOUT ADC12_IN4 RTC_REFIN
25	36	PA2	ETH_MDIO EVENTOUT TIM5_CH3 TIM9_CH1 TIM2_CH3 USART2_TX ADC123_IN2	USART2_TX GTIM4_CH3 GTIM5_CH1 GTIM1_CH3 ETH_MDIO GTIM8_CH1_ETR XSPI_NSS0 UART7_TX I2S_CKIN DVP_VSYNC SPI6_NSS EVENTOUT ADC1_IN5 WKUP4 LSCO
26	37	PA3	ETH_MII_COL EVENTOUT TIM5_CH4 TIM9_CH2 TIM2_CH4 USART2_RX OTG_HS_ULPI_D0 ADC123_IN3	USART2_RX GTIM4_CH4 GTIM5_CH2 GTIM1_CH4 ETH_MII_COL GTIM8_CH2 XSPI_CLK UART7_RX I2S2_MCK DVP_PIXCLK MCO2 EVENTOUT ADC1_IN2
27	38	VSS	VSS	VSS
28	39	VDD	VDD	VDD
29	40	PA4	SPI1_NSS SPI3_NSS I2S3_WS EVENTOUT DCMI_HSYNC USART2_CK OTG_HS_SOF ADC12_IN4 DAC_OUT1	SPI1_NSS SPI3_NSS/I2S3_WS USART2_CK DVP_HSYNC USB_HS_SOF GTIM2_CH2 DVP_D0 XSPI_NSS1 I2C2_SCL SPI6_MISO GTIM7_CH1 LPTIM2_IN2 USART1_TX

LQFP100	LQFP144	Pin name	Pins Reuse function	
			STM32F407/417	N32H487
				EVENTOUT ADC2_IN17 DAC1_OUT
30	41	PA5	SPI1_SCK EVENTOUT TIM2_CH1_ETR TIM8_CH1N OTG_HS_ULPI_CK ADC12_IN5 DAC_OUT2	SPI1_SCK GTIM1_CH1_ETR ATIM2_CH1N DVP_D1 XSPI_CLK I2C2_SDA SPI6_MOSI USART1_RX XSPI_IO0 GTIM7_CH2 EVENTOUT ADC2_IN13 DAC2_OUT
31	42	PA6	SPI1_MISO EVENTOUT TIM8_BKIN TIM13_CH1 TIM3_CH1 TIM1_BKIN DCMI_PIXCLK ADC12_IN6	SPI1_MISO ATIM2_BKIN GTIM9_CH1 DVP_PIXCLK GTIM2_CH1 ATIM1_BKIN XSPI_IO3 UART7_CTS I2S2_MCK SDIO_CMD DVP_D2 XSPI_IO0 EVENTOUT ADC2_IN0
32	43	PA7	SPI1_MOSI ETH_MII_RX_DV ETH_RMII_CRS_DV EVENTOUT TIM8_CH1N TIM14_CH1 TIM3_CH2 TIM1_CH1N ADC12_IN7	SPI1_MOSI ATIM2_CH1N GTIM7_CH1 GTIM2_CH2 ETH_MII_RX_DV ATIM1_CH1N ETH_RMII_CRS_DV GTIM10_CH1 XSPI_IO2 DVP_D3 XSPI_IO1 MCO1 GTIM9_CH2 EVENTOUT ADC2_IN2
33	44	PC4	ETH_RMII_RX_D0 ETH_MII_RX_D0 EVENTOUT ADC12_IN14	ETH_RMII_RX_D0 ETH_MII_RX_D0 ATIM1_ETR I2C2_SCL USART1_TX XSPI_IO7 DVP_D4 XSPI_IO2

LQFP100	LQFP144	Pin name	Pins Reuse function	
			STM32F407/417	N32H487
				UART7_TX I23_SCL LPTIM2_OUT ATIM3_CH3N EVENTOUT ADC2_IN5
34	45	PC5	ETH_RMII_RX_D1 ETH_MII_RX_D1 EVENTOUT ADC12_IN15	ETH_RMII_RX_D1 ETH_MII_RX_D1 GTIM8_BKIN ATIM1_CH4N USART1_RX DVP_D5 XSPI_IO3 UART7_RX I2C3_SDA GTIM5_ETR EVENTOUT ADC2_IN11 WKUP5
35	46	PB0	ETH_MII_RXD2 EVENTOUT TIM3_CH3 TIM8_CH2N TIM1_CH2N OTG_HS_ULPI_D1 ADC12_IN8	GTIM2_CH3 ATIM2_CH2N ETH_MII_RX_D2 ATIM1_CH2N XSPI_IO1 SPI5_SCK SPI3_MOSI/I2S3_SD SDIO_D1 DVP_D6 USART4_TX EVENTOUT ADC3_IN12 ADC1_IN1
36	47	PB1	ETH_MII_RXD3 EVENTOUT TIM3_CH4 TIM8_CH3N TIM1_CH3N OTG_HS_ULPI_D2 ADC12_IN9	GTIM2_CH4 ATIM2_CH3N ETH_MII_RX_D3 ATIM1_CH3N XSPI_IO0 UART7_RTS_DE SPI5_NSS SDIO_D2 DVP_D7 USART4_RX EVENTOUT ADC1_IN12 ADC3_IN1
37	48	PB2	EVENTOUT BOOT1	RTC_OUT2 LPTIM1_OUT GTIM4_CH1 ATIM3_CH1 I2C3_SMBA XSPI_IO5 GTIM1_CH4 SPI3_MOSI/I2S3_SD

LQFP100	LQFP144	Pin name	Pins Reuse function	
			STM32F407/417	N32H487
				SDIO_CLK DVP_D3 UART6_TX SPI1_NSS GTIM6_ETR EVENTOUT ADC2_IN12
-	49	PF11	EVENTOUT DCMI_D12	DVP_D12 ATIM3_ETR FEMC_NE4 SPI5_MOSI EVENTOUT
-	50	PF12	FSMC_A6 EVENTOUT	FEMC_A6 ATIM3_CH1 DVP_D4 EVENTOUT
-	51	VSS	VSS	VSS
-	52	VDD	VDD	VDD
-	53	PF13	FSMC_A7 EVENTOUT	FEMC_A7 ATIM3_CH2 I2C4_SMBA DVP_D5 MCO1 EVENTOUT
-	54	PF14	FSMC_A8 EVENTOUT	FEMC_A8 ATIM3_CH3 I2C4_SCL DVP_D6 MCO2 EVENTOUT
-	55	PF15	FSMC_A9 EVENTOUT	FEMC_A9 ATIM3_CH4 I2C4_SDA DVP_D7 EVENTOUT
-	56	PG0	FSMC_A10 EVENTOUT	FEMC_A10 ATIM3_CH1N UART7_TX GTIM7_CH2 EVENTOUT
-	57	PG1	FSMC_A11 EVENTOUT	FEMC_A11 ATIM3_CH2N UART7_RX GTIM7_CH3 EVENTOUT
38	58	PE7	FSMC_D4 EVENTOUT TIM1_ETR	FEMC_D4 ATIM1_ETR UART7_RX UART6_RX SPI1_SCK GTIM4_CH2 GTIM9_CH4 EVENTOUT

LQFP100	LQFP144	Pin name	Pins Reuse function	
			STM32F407/417	N32H487
				ADC3_IN4
39	59	PE8	FSMC_D5 EVENTOUT TIM1_CH1N	FEMC_D5 ATIM1_CH1N GTIM4_CH3 UART7_TX SDIO_D0 SPI1_MISO EVENTOUT ADC34_IN6
40	60	PE9	FSMC_D6 EVENTOUT TIM1_CH1	FEMC_D6 ATIM1_CH1 GTIM4_CH4 SDIO_D1 SPI1_MOSI EVENTOUT ADC3_IN2
-	61	VSS	VSS	VSS
-	62	VDD	VDD	VDD
41	63	PE10	FSMC_D7 EVENTOUT TIM1_CH2N	FEMC_D7 ATIM1_CH2N XSPI_CLK SDIO_D2 SPI2_NSS/I2S2_WS ATIM1_CH1N GTIM2_CH1 GTIM9_CH1 USART4_TX EVENTOUT ADC34_IN14
42	64	PE11	FSMC_D8 EVENTOUT TIM1_CH2	FEMC_D8 ATIM1_CH2 SPI4_NSS XSPI_NSS0 SPI5_NSS SDIO_D3 SPI2_SCK/I2S2_CK USART4_RX EVENTOUT ADC34_IN15
43	65	PE12	FSMC_D9 EVENTOUT TIM1_CH3N	FEMC_D9 ATIM1_CH3N SPI4_SCK XSPI_IO0 SPI5_SCK SDIO_CLK SPI2_MISO GTIM7_CH4 EVENTOUT ADC34_IN16
44	66	PE13	FSMC_D10 EVENTOUT TIM1_CH3	FEMC_D10 ATIM1_CH3 SPI4_MISO

LQFP100	LQFP144	Pin name	Pins Reuse function	
			STM32F407/417	N32H487
				XSPI_IO1 SPI5_MISO SPI2_MOSI/I2S2_SD SDIO_CMD EVENTOUT ADC3_IN3
45	67	PE14	FSMC_D11 EVENTOUT TIM1_CH4	FEMC_D11 ATIM1_CH4 SPI4_MOSI ATIM1_BKIN2 XSPI_IO2 SPI5_MOSI EVENTOUT ADC4_IN5
46	68	PE15	FSMC_D12 EVENTOUT TIM1_BKIN	FEMC_D12 ATIM1_BKIN ATIM1_CH4N XSPI_IO3 I2C1_SDA USART4_RX GTIM10_CH1 EVENTOUT ADC4_IN2
47	69	PB10	SPI2_SCK I2S2_CK ETH_MII_RX_ER EVENTOUT TIM2_CH3 USART3_TX OTG_HS_ULPI_D3 I2C2_SCL	SPI2_SCK/I2S2_CK I2C2_SCL ETH_MII_RX_ER GTIM1_CH3 UART7_RX XSPI_CLK ATIM1_BKIN SDIO_D7 FEMC_D11 DVP_D4 EVENTOUT
48	70	PB11	ETH_RMII_TX_EN ETH_MII_TX_EN EVENTOUT TIM2_CH4 USART3_RX OTG_HS_ULPI_D4 I2C2_SDA	I2C2_SDA ETH_RMII_TX_EN ETH_MII_TX_EN GTIM1_CH4 UART7_TX XSPI_NSS0 I2S_CKIN FEMC_D12 DVP_D5 EVENTOUT ADC12_IN14
49	71	VCAP_1	-	LPTIM2_IN1 UART8_CTS ATIM3_BKIN ATIM2_CH4N DVP_D12 GTIM5_CH1 EVENTOUT PH3

LQFP100	LQFP144	Pin name	Pins Reuse function	
			STM32F407/417	N32H487
50	72	VDD	VDD	VDD
51	73	PB12	SPI2_NSS I2S2_WS ETH_RMII_TXD0 ETH_MII_TXD0 EVENTOUT TIM1_BKIN USART3_CK CAN2_RX OTG_HS_ULPI_D5 OTG_HS_ID I2C2_SMBA	SPI2_NSS/I2S2_WS I2C2_SMBA USART3_CK ATIM1_BKIN ETH_RMII_TX_D0 ETH_MII_TX_D0 USB_HS_ID GTIM4_ETR UART7_RTS_DE SPI4_NSS GTIM9_CH3 EVENTOUT ADC1_IN11 ADC4_IN1
52	74	PB13	SPI2_SCK I2S2_CK ETH_RMII_TXD1 ETH_MII_TXD1 EVENTOUT TIM1_CH1N USART3_CTS CAN2_TX OTG_HS_ULPI_D6 OTG_HS_VBUS	SPI2_SCK/I2S2_CK USART3_CTS ATIM1_CH1N ETH_RMII_TX_D1 ETH_MII_TX_D1 UART7_CTS SPI4_SCK ATIM1_CH2 GTIM10_CH2 GTIM9_CH4 EVENTOUT USB_HS_VBUS ADC3_IN5
53	75	PB14	SPI2_MISO I2S2ext_SD EVENTOUT TIM1_CH2N TIM12_CH1 TIM8_CH2N USART3_RTS OTG_HS_DM	SPI2_MISO ATIM1_CH2N GTIM8_CH1 ATIM2_CH2N I2S2_AUX_SD GTIM9_CH2 USART4_CK DVP_D13 EVENTOUT USB_HS_DM ⁽⁶⁾ ADC4_IN4 ADC1_IN0
54	76	PB15	SPI2_MOSI I2S2_SD EVENTOUT TIM1_CH3N TIM8_CH3N TIM12_CH2 OTG_HS_DP RTC_REFIN	SPI2_MOSI/I2S2_SD ATIM1_CH3N ATIM2_CH3N GTIM8_CH2 GTIM8_CH1N ATIM2_CH4 UART8_CTS DVP_D14 EVENTOUT USB_HS_DP ⁽⁶⁾ RTC_REFIN ADC2_IN15 ADC4_IN3

LQFP100	LQFP144	Pin name	Pins Reuse function	
			STM32F407/417	N32H487
55	77	PD8	FSMC_D13 EVENTOUT USART3_TX	FEMC_D13 ETH_MII_DV ETH_RMII_CRD_DV SPI3_NSS/I2S3_WS ATIM1_CH3 GTIM10_CH1 EVENTOUT ADC4_IN12
56	78	PD9	FSMC_D14 EVENTOUT USART3_RX	FEMC_D14 ETH_MII_RX_D0 ETH_RMII_RX_D0 SPI3_SCK/I2S3_CK ATIM1_CH3N GTIM9_CH3 GTIM7_ETR GTIM10_CH2 EVENTOUT ADC4_IN13
57	79	PD10	FSMC_D15 EVENTOUT USART3_CK	FEMC_D15 USART3_CK ETH_MII_RX_D1 ETH_RMII_RX_D1 ATIM1_CH4 ATIM3_ETR EVENTOUT ADC34_IN7
58	80	PD11	FSMC_CLE FSMC_A16 EVENTOUT USART3_CTS	FEMC_CLE/FEMC_A16 USART3_CTS GTIM4_ETR I2C4_SMBA ETH_MII_RX_D2 SPI3_MISO USART4_TX I2C1_SCL GTIM10_CH3 EVENTOUT ADC34_IN8
59	81	PD12	FSMC_ALE FSMC_A17 EVENTOUT TIM4_CH1 USART3_RTS	FEMC_ALE/FEMC_A17 GTIM3_CH1 ETH_MII_RX_D3 SPI3_MOSI/I2S3_SD GTIM6_CH1 EVENTOUT ADC34_IN9
60	82	PD13	FSMC_A18 EVENTOUT TIM4_CH2	FEMC_A18 GTIM3_CH2 XSPI_RXDS GTIM6_CH2 EVENTOUT ADC34_IN10
-	83	VSS	VSS	VSS
-	84	VDD	VDD	VDD

LQFP100	LQFP144	Pin name	Pins Reuse function	
			STM32F407/417	N32H487
61	85	PD14	FSMC_D0 EVENTOUT TIM4_CH3	FEMC_D0 GTIM3_CH3 I2C4_SCL ATIM2_CH1 GTIM10_CH4 GTIM6_CH3 EVENTOUT ADC34_IN11
62	86	PD15	FSMC_D1 EVENTOUT TIM4_CH4	FEMC_D1 GTIM3_CH4 SPI2_NSS I2C4_SDA ATIM2_CH2 ATIM2_CH1N GTIM8_CH1 GTIM6_CH4 EVENTOUT
-	87	PG2	FSMC_A12 EVENTOUT	FEMC_A12 ATIM3_CH3N SPI1_SCK I2C2_SCL GTIM5_ETR EVENTOUT
-	88	PG3	FSMC_A13 EVENTOUT	FEMC_A13 ATIM3_BKIN I2C4_SCL SPI1_MISO ATIM3_CH4N I2C2_SDA EVENTOUT
-	89	PG4	FSMC_A14 EVENTOUT	FEMC_A14 ATIM3_BKIN2 I2C4_SDA SPI1_MOSI GTIM6_ETR EVENTOUT
-	90	PG5	FSMC_A15 EVENTOUT	FEMC_A15 ATIM3_ETR SPI1_NSS UART7_CTS EVENTOUT
-	91	PG6	FSMC_INT2 EVENTOUT	FEMC_INT2 ATIM3_BKIN I2C3_SMBA UART7_RTS_DE DVP_D12 EVENTOUT
-	92	PG7	FSMC_INT3 EVENTOUT USART6_CK	FEMC_INT3 USART4_CK I2C3_SCL UART7_TX DVP_D13 EVENTOUT

LQFP100	LQFP144	Pin name	Pins Reuse function	
			STM32F407/417	N32H487
-	93	PG8	ETH_PPS_OUT EVENTOUT USART6_RTS	USART4_RTS_DE ETH_PPS_OUT I2C3_SDA UART7_RX FEMC_NE3 XSPI_NSS1 EVENTOUT
-	94	VSS	VSS	VSS
-	95	VDD	VDD	VDD
63	96	PC6	I2S2_MCK EVENTOUT TIM8_CH1 TIM3_CH1 DCMI_D0 USART6_TX SDIO_D6	I2S2_MCK ATIM2_CH1 SDIO_D6 USART4_TX DVP_D0 GTIM2_CH1 I2C4_SCL SPI2_NSS/I2S2_WS USART2_CTS FEMC_A16 ATIM2_CH2 EVENTOUT
64	97	PC7	I2S3_MCK EVENTOUT TIM8_CH2 TIM3_CH2 DCMI_D1 USART6_RX SDIO_D7	I2S3_MCK ATIM2_CH2 SDIO_D7 USART4_RX DVP_D1 GTIM2_CH2 I2C4_SDA SPI2_SCK/I2S_CK USART2_RTS_DE FEMC_A17 ATIM2_CH2N GTIM8_CH2 EVENTOUT
65	98	PC8	EVENTOUT TIM8_CH3 TIM3_CH3 DCMI_D2 USART6_CK SDIO_D0	ATIM2_CH3 SDIO_D0 GTIM2_CH3 USART4_CK DVP_D2 ATIM3_CH3 I2C3_SCL SPI2_MISO USART2_TX EVENTOUT
66	99	PC9	I2S_CKIN EVENTOUT TIM8_CH4 TIM3_CH4 DCMI_D3 I2C3_SDA SDIO_D1 MCO2	I2S_CKIN MCO2 ATIM2_CH4 SDIO_D1 I2C3_SDA DVP_D3 GTIM2_CH4 ATIM2_BKIN2 SPI2_MOSI/I2S2_SD

LQFP100	LQFP144	Pin name	Pins Reuse function	
			STM32F407/417	N32H487
				USART2_RX FEMC_NOE ATIM2_CH3N GTIM8_CH3 EVENTOUT
67	100	PA8	EVENTOUT TIM1_CH1 USART1_CK OTG_FS_SOF I2C3_SCL MCO1	MCO1 USART1_CK ATIM1_CH1 I2C3_SCL I2C2_SDA I2S2_MCK I2C2_SMBA GTIM3_ETR SDIO_D1 EVENTOUT ADC3_IN18
68	101	PA9	EVENTOUT TIM1_CH2 DCMI_D0 USART1_TX OTG_FS_VBUS I2C3_SMBA	USART1_TX ATIM1_CH2 I2C3_SMBA DVP_D0 I2C2_SCL I2S3_MCK GTIM8_BKIN GTIM1_CH3 SPI2_SCK/I2S2_CK SDIO_D2 I2C4_SCL I2C1_SCL EVENTOUT ADC4_IN18
69	102	PA10	EVENTOUT TIM1_CH3 DCMI_D1 USART1_RX OTG_FS_ID	USART1_RX ATIM1_CH3 DVP_D1 GTIM10_BKIN I2C2_SMBA SPI2_MISO GTIM1_CH4 ATIM2_BKIN I2C2_SDA I2S2_AUX_SD SPI5_MOSI I2C4_SDA FEMC_NWE EVENTOUT PVD_IN
70	103	PA11	EVENTOUT TIM1_CH4 USART1_CTS CAN1_RX OTG_FS_DM	USART1_CTS ATIM1_CH4 USB_FS_DM SPI2_MOSI/I2S2_SD ATIM1_CH1N GTIM3_CH1 ATIM1_BKIN2 SPI4_MISO

LQFP100	LQFP144	Pin name	Pins Reuse function	
			STM32F407/417	N32H487
				USART4_TX ATIM2_CH3N EVENTOUT
71	104	PA12	EVENTOUT TIM1_ETR USART1_RTS CAN1_TX OTG_FS_DP	USART1_RTS_DE ATIM1_ETR USB_FS_DP GTIM9_CH1 I2S_CKIN ATIM1_CH2N GTIM3_CH2 SPI4_MOSI USART4_RX SPI2_NSS EVENTOUT
72	105	PA13	EVENTOUT JTMS-SWDIO	JTMS-SWDIO GTIM9_CH1N I2C4_SCL I2C1_SCL IR_OUT USART3_CTS GTIM3_CH3 UART6_TX GTIM8_CH3 EVENTOUT
73	106	VCAP_2	VCAP_2	USART4_RTS_DE USART1_RX GTIM3_CH4 GTIM9_CH3 DVP_D13 EVENTOUT PH2
74	107	VSS	VSS	VSS
75	108	VDD	VDD	VDD
76	109	PA14	EVENTOUT JTCK-SWCLK	JTCK-SWCLK LPTIM1_OUT I2C4_SMBA I2C1_SDA ATIM2_CH2 ATIM1_BKIN USART2_TX UART6_RX GTIM8_CH4 EVENTOUT
77	110	PA15	SPI3_NSS SPI1_NSS I2S3_WS EVENTOUT TIM2_CH1_ETR JTDI	JTDI SPI3_NSS/I2S3_WS GTIM1_CH1_ETR SPI1_NSS ATIM2_CH1 I2C1_SCL USART2_RX UART6_RTS_DE ATIM1_BKIN UART1_TX

LQFP100	LQFP144	Pin name	Pins Reuse function	
			STM32F407/417	N32H487
				USART2_CTS ATIM2_CH1N ATIM3_ETR EVENTOUT
78	111	PC10	SPI3_SCK I2S3_CK EVENTOUT DCMI_D8 UART4_TX USART3_TX SDIO_D2	SPI3_SCK/I2S3_CK UART6_TX SDIO_D2 DVP_D8 ATIM2_CH1N XSPI_NSS1 GTIM9_CH4 EVENTOUT
79	112	PC11	SPI3_MISO I2S3ext_SD EVENTOUT DCMI_D4 UART4_RX USART3_RX SDIO_D3	UART6_RX SPI3_MISO SDIO_D3 DVP_D4 I2S3_AUX_SD ATIM2_CH2N I2C3_SDA XSPI_CLK GTIM10_ETR ATIM3_CH2 EVENTOUT
80	113	PC12	SPI3_MOSI I2S3_SD EVENTOUT DCMI_D9 UART5_TX USART3_CK SDIO_CK	SDIO_CLK DVP_D9 SPI3_MOSI/I2S3_SD USART3_CK GTIM4_CH2 ATIM2_CH3N I2C2_SDA XSPI_IO0 ATIM2_CH2N ATIM3_CH3 EVENTOUT
81	114	PD0	FSMC_D2 EVENTOUT CAN1_RX	FEMC_D2 ATIM2_CH4N SPI4_MISO SPI3_MOSI UART6_TX XSPI_IO1 ATIM3_CH4 EVENTOUT
82	115	PD1	FSMC_D3 EVENTOUT CAN1_TX	FEMC_D3 ATIM2_CH4 ATIM2_BKIN2 SPI2_NSS/I2S2_WS UART6_RX XSPI_IO2 I2C1_SDA EVENTOUT
83	116	PD2	EVENTOUT TIM3_ETR DCMI_D11	GTIM2_ETR SDIO_CMD DVP_D11

LQFP100	LQFP144	Pin name	Pins Reuse function	
			STM32F407/417	N32H487
			UART5_RX SDIO_CMD	ATIM2_BKIN SPI3_NSS/I2S3_WS XSPI_IO3 ATIM2_CH3N SPI2_MOSI ATIM1_CH4 ATIM2_CH4N ATIM3_CH4 GTIM5_CH2 EVENTOUT
84	117	PD3	FSMC_CLK EVENTOUT USART2_CTS	FEMC_CLK USART2_CTS GTIM1_CH1_ETR XSPI_NSS0 SPI2_SCK/I2S2_CK DVP_D5 EVENTOUT
85	118	PD4	FSMC_NOE EVENTOUT USART2_RTS	FEMC_NOE USART2_RTS_DE GTIM1_CH2 XSPI_IO4 EVENTOUT
86	119	PD5	FSMC_NWE EVENTOUT USART2_TX	FEMC_NWE USART2_TX XSPI_IO5 GTIM6_CH1 ATIM1_CH4N EVENTOUT
-	120	VSS	VSS	VSS
-	121	VDD	VDD	VDD
87	122	PD6	FSMC_NWAIT EVENTOUT USART2_RX	FEMC_NWAIT USART2_RX GTIM1_CH4 XSPI_IO6 SPI3_MOSI/I2S3_SD DVP_D0 GTIM9_ETR EVENTOUT
88	123	PD7	FSMC_NE1 FSMC_NCE2 EVENTOUT USART2_CK	USART2_CK FEMC_NE1/FEMC_NCE2 GTIM1_CH3 XSPI_IO7 EVENTOUT
-	124	PG9	FSMC_NE2 FSMC_NCE3 EVENTOUT USART6_RX	USART4_RX FEMC_NE2/FEMC_NCE3 SPI3_SCK USART1_TX GTIM8_CH1N DVP_VSYNC SPI2_MOSI GTIM6_CH2 SPI2_MISO EVENTOUT

LQFP100	LQFP144	Pin name	Pins Reuse function	
			STM32F407/417	N32H487
-	125	PG10	FSMC_NCE4_1 FSMC_NE3 EVENTOUT	FEMC_NE3 XSPI_IO2 DVP_D2 GTIM7_CH1 EVENTOUT
-	126	PG11	ETH_MII_TX_EN ETH_RMII_TX_EN FSMC_NCE4_2 EVENTOUT	ETH_MII_TX_EN ETH_RMII_TX_EN XSPI_IO3 SPI4_SCK DVP_D3 GTIM7_CH2 EVENTOUT
-	127	PG12	FSMC_NE4 EVENTOUT USART6_RTS	FEMC_NE4 USART4_RTS_DE XSPI_D1 SPI4_MISO GTIM7_CH3 EVENTOUT
-	128	PG13	ETH_MII_TX_D0 ETH_RMII_TX_D0 FSMC_A24 EVENTOUT USART6_CTS	FEMC_A24 USART4_CTS ETH_MII_TX_D0 ETH_RMII_TX_D0 XSPI_CLK SPI4_MOSI GTIM7_CH4 EVENTOUT
-	129	PG14	ETH_MII_TX_D1 ETH_RMII_TX_D1 FSMC_A25 EVENTOUT USART6_TX	FEMC_A25 USART4_TX ETH_MII_TX_D1 ETH_RMII_TX_D1 XSPI_D0 SPI4_NSS SPI2_MISO I2C1_SCL GTIM6_CH3 ATIM2_CH4 EVENTOUT
-	130	VSS	VSS	VSS
-	131	VDD	VDD	VDD
-	132	PG15	EVENTOUT DCMI_D13 USART6_CTS	USART4_CTS DVP_D13 GTIM6_CH4 I2C1_SDA SPI6_NSS ATIM2_CH4N USART1_RX EVENTOUT
89	133	PB3	TRACESWO SPI3_SCK SPI1_SCK I2S3_CK EVENTOUT	JTDO SPI3_SCK/I2S3_CK GTIM1_CH2 SPI1_SCK GTIM3_ETR ATIM2_CH1N

LQFP100	LQFP144	Pin name	Pins Reuse function	
			STM32F407/417	N32H487
			TIM2_CH2 JTDO	USART2_TX GTIM2_ETR USART1_RX I2C2_SDA USART2_RTS_DE ATIM2_BKIN EVENTOUT
90	134	PB4	SPI1_MISO SPI3_MISO I2S3ext_SD EVENTOUT TIM3_CH1 NJTRST	NJTRST SPI3_MISO GTIM2_CH1 SPI1_MISO I2S3_AUX_SD GTIM9_CH1_ETR ATIM2_CH2N USART2_RX GTIM10_BKIN I2C3_SDA SDIO_D0 ATIM2_ETR LPTIM2_IN1 USART2_TX EVENTOUT
91	135	PB5	SPI1_MOSI SPI3_MOSI I2S3_SD ETH_PPS_OUT EVENTOUT TIM3_CH2 DCMI_D10 CAN2_RX OTG_HS_ULPI_D7 I2C1_SMBA	I2C1_SMBA ETH_PPS_OUT GTIM2_CH2 SPI1_MOSI SPI3_MOSI/I2S3_SD DVP_D10 GTIM9_BKIN ATIM2_CH3N USART2_CK I2C3_SDA GTIM10_CH1 LPTIM1_IN1 UART5_CTS USART2_RX EVENTOUT
92	136	PB6	EVENTOUT TIM4_CH1 DCMI_D5 USART1_TX CAN2_TX I2C1_SCL	I2C1_SCL GTIM3_CH1 DVP_D5 USART1_TX GTIM9_CH1N ATIM2_CH1 ATIM2_ETR ATIM2_BKIN2 LPTIM1_ETR ETH_PPS_OUT FEMC_NE2/FEMC_NCE3 EVENTOUT
93	137	PB7	FSMC_NL EVENTOUT TIM4_CH2 DCMI_VSYNC	I2C1_SDA FEMC_NADV DVP_VSYNC USART1_RX

LQFP100	LQFP144	Pin name	Pins Reuse function	
			STM32F407/417	N32H487
			USART1_RX I2C1_SDA	GTIM3_CH2 GTIM10_CH1N ATIM2_BKIN GTIM2_CH4 I2C4_SDA LPTIM1_IN2 ETH_MII_TXD3 UART6_CTS EVENTOUT PVD_IN
94	138	BOOT0	VPP	GTIM4_CH1 GTIM10_CH1N USART1_TX EVEVTOUT PH4
95	139	PB8	ETH_MII_TXD3 EVENTOUT TIM4_CH3 TIM10_CH1 DCMI_D6 CAN1_RX I2C1_SCL SDIO_D4	GTIM3_CH3 SDIO_D4 GTIM6_CH1 DVP_D6 ETH_MII_TX_D3 I2C1_SCL GTIM9_CH1 ATIM2_CH2 ATIM1_BKIN SPI5_MOSI FMEC_NWAIT GTIM9_CH4 EVENTOUT
96	140	PB9	SPI2_NSS I2S2_WS EVENTOUT TIM4_CH4 TIM11_CH1 DCMI_D7 CAN1_TX I2C1_SDA SDIO_D5	SPI2_NSS/I2S2_WS GTIM3_CH4 GTIM7_CH1 SDIO_D5 DVP_D7 I2C1_SDA GTIM10_CH1 ATIM2_CH3 ATIM1_CH3N FEMC_NE1/FEMC_NCE2 EVENTOUT IR-OUT
97	141	PE0	FSMC_NBL0 EVENTOUT TIM4_ETR DCMI_D2	GTIM3_ETR FEMC_NBL0 DVP_D2 ATIM3_ETR ATIM3_CH4N GTIM9_CH1 USART1_TX EVENTOUT
98	142	PE1	FSMC_NBL1 EVENTOUT DCMI_D3	FEMC_NBL1 DVP_D3 GTIM10_CH1 ATIM3_CH4 USART1_RX

LQFP100	LQFP144	Pin name	Pins Reuse function	
			STM32F407/417	N32H487
				EVENTOUT
-	143	PDR_ON	PDR_ON	EVENTOUT PH5
100	144	VDD	VDD	VDD

4 Minimum System Design

The minimum system design for N32H487 has the following considerations, which can be referred to in the hardware design guide "CN_UG_N32H47X&N32H48X Series Hardware Design Guide":

● Power supply

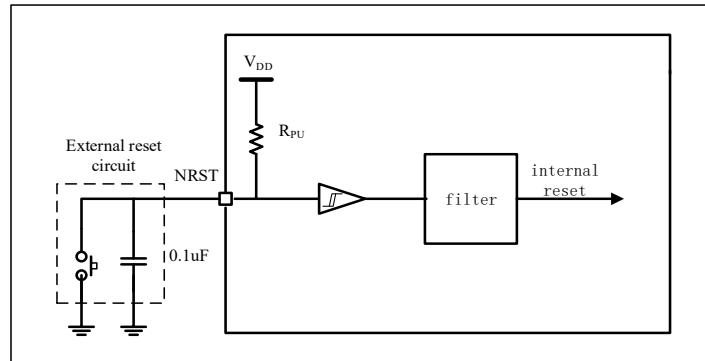
VDD is the main power supply for MCU and must be powered by a stable external power supply with a voltage range of 1.8V~3.6V. A 0.1uF decoupling capacitor should be placed nearby for all VDD pins, and an additional 10uF decoupling capacitor should be added to one VDD pin. Please refer to the hardware design guide for the specific design of decoupling capacitors.

VDDA is an analog power supply that provides power to ADC, DAC, and COMP. It is recommended to place a 0.1uF and a 10uF capacitor on the VDDA input pin.

VREF+ serves as the reference voltage, providing reference levels for ADC and DAC. When VREF+ uses the built-in reference source VREFBUF, it is recommended to place a 0.1uF and a 1uF capacitor near the VREF+ pin. When VREF+ is powered externally, it is recommended to place a 0.1uF and a 10uF capacitor near the VREF+ pin.

● External pin reset circuit

When a low level (external reset) appears on the NRST pin, a system reset will occur. The external NRST pin reset reference circuit is as follows:



Note: The reset pin NRST cannot be left hanging during design. The external capacitor 0.1uF is given as a typical reference value. If the reset time needs to be accelerated, the NRST pin can be pulled up. In addition, users can decide whether to add a reset button according to their actual product needs.

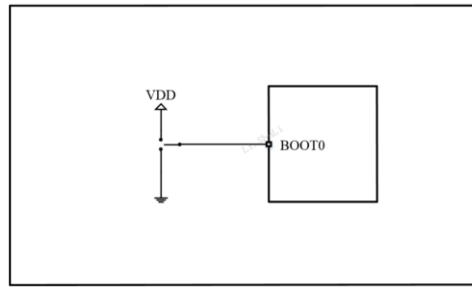
● External clock circuit

The N32H487 series MCU includes two external clocks: an external high-speed clock HSE (4MHz~32MHz) and an external low-speed clock LSE (typically using 32.768KHz).

HSE and LSE are configured with corresponding load capacitors based on the crystal oscillator characteristics. For details, please refer to the external clock characteristic description in the relevant data manual.

● Boot pin connection

The following figure shows the external connections required for selecting a boot memory for the N32H487 series chip. Please refer to the relevant sections of the user manual for the startup mode.



5 Main Functional Differences

The following table only lists the main differences. For other detailed functions, please refer to the data manual and user manual:

Device model	STM32F407/417 series	N32H487 series
System		
System Clock	Main frequency 168M, AHB bus up to 168M	Main frequency 200M, AHB bus up to 200M
External clock source	HSE 4-26M (Bypass 1-50M)	HSE 4-32M (Bypass 1-50M)
Internal clock source	HSI(16M)、LSI(32K)	HSI(8M)、LSI(32K)
operation temperature	-40~85°C or -40~105°C	-40~105°C
External interrupt	➢ 16 configurable external pin interrupts ➢ 7 configurable peripheral interrupts	➢ 16 configurable external pin interrupts, supporting full pin mapping ➢ 16 configurable peripheral interrupts
BOR	➢ Three configurable gears	➢ Five configurable gears
PVD	➢ Eight configurable gears	➢ Two configurable detection voltage intervals ➢ Each detection voltage interval supports 8 configurable gears
low power mode	➢ Four low-power modes: Sleep mode Stop mode Standby mode VBAT mode	➢ Four low-power modes: Sleep mode Stop mode Standby mode VBAT mode
Low speed clock output	➢ Not supported	➢ Supports low-speed clock output in Stop0/Standby mode
Standby wake-up	➢ 1 configurable wake-up pin	➢ 5 configurable wake-up pins
Storage		
FLASH	➢ Maximum 1024KB ➢ Page size 16KB (4 pieces) ➢ Page size 64KB (1 piece) ➢ Page size 128KB (7 pieces)	➢ Maximum 512KB ➢ Page size 8KB ➢ Support ECC verification
SRAM	➢ 112KB Universal SRAM1 ➢ 16KB Universal SRAM2 ➢ 64KB CCM SRAM, can only be used for data storage and only supports CPU access ➢ 4KB Backup SRAM	➢ 160KB general-purpose SRAM, supporting parity check ➢ 32KB CCM SRAM, supporting ECC ➢ 4KB Backup SRAM, supports ECC
Expanded storage	➢ XSPI: Not supported ➢ FSMC: Support PC Card ➢ SDIO: Compatible with SD 2.0, SDIO 2.0, MMC 4.2 Support CE-ATA V1.1	➢ XSPI: 1/2/4/8-bit data cable The size of the data can be configured during read and write operations ➢ FEMC Not supported PC Card ➢ SDIO: Compatible with SD 2.0、SDIO 2.0、MMC 4.2 Not supported CE-ATA
Peripherals		
Advanced Timer	➢ Name: TIM1/8 ➢ The highest resolution is 5.95ns ➢ 4 comparison outputs, including 4 external input/output channels and 3 pairs of complementary output channels	➢ Name: ATIM1/2/3 ➢ The highest resolution is 5ns ➢ 9-way comparison output ➢ Four external input/output channels ➢ Four complementary output channels
General Timer	➢ Name: TIM2/3/4/5/9/10/11/12/13/14 ➢ TIM2/3/4/5/12/13/14 maximum resolution 11.9ns ➢ TIM9/10/11 maximum resolution 5.95ns ➢ TIM2/5 supports 32-bit counting ➢ TIM3/4/9/10/11/12/13/14 supports 16 bit counting ➢ TIM2/3/4/5 supports 4 comparison outputs, including 4 external input/output channels ➢ TIM9/10/11/12/13/14 supports 2 comparison outputs, including 2 external input/output	➢ Name: GTIM1~10 ➢ GTIM1-7 has a maximum resolution of 5.56ns ➢ GTIM8-10 with a maximum resolution of 5ns ➢ GTIM1~10 supports 16 bit counting ➢ GTIM1-7 supports 4 comparison outputs, including 4 external input/output channels ➢ GTIM8/9/10 supports 5 comparison outputs, including 4 external input/output channels and 1 pair of complementary output channels ➢ GTIM8/9/10 supports brake input

	channels	
Basic timer	➤ Name: TIM6/7 ➤ The highest resolution is 11.9ns ➤ Supports 16 bit counting	➤ Name: BTIM1/2 ➤ The highest resolution is 5.56ns ➤ Supports 32-bit counting
LPTIM	➤ Not supported	➤ 2
WWDG	➤ 7bit	➤ 14bit
IWDG	➤ Freezing is not supported	➤ Support freezing IWDG in low-power mode
SPI	➤ 3*SPI ➤ Maximum 75MHz	➤ 6*SPI ➤ Maximum 60MHz
I2S	➤ 2 * I2S, supports full duplex communication	➤ 2 * I2S, supports full duplex communication
I2C	➤ 3*I2C ➤ Maximum 400KHz	➤ 4*I2C ➤ Maximum 1MHz
USART	➤ 4*USART ➤ Pin swapping is not supported ➤ Does not support RS-485 hardware flow control	➤ 4*USART ➤ Support pin swapping ➤ Supports RS-485 hardware flow control ➤ USART3 TX/RX/RTS de supports full pin mapping
UART	➤ 2*UART ➤ Pin swapping is not supported ➤ Does not support RS-485 hardware flow control	➤ 4*UART ➤ Support pin swapping ➤ Supports RS-485 hardware flow control ➤ UART5/8 TX/RX/RTS de supports full pin mapping
CAN	➤ Only supports CAN 2.0A/B ➤ Not supporting full pin mapping	➤ Supports CAN 2.0A/B and FDCAN ➤ Support full pin mapping
USB FS	➤ 1*USB FS OTG	➤ 1*USB FS Device
USB HS	➤ 1*USB HS OTG ➤ Built in FS PHY ➤ HS requires an external PHY chip	➤ 1*USB HS DualRole
DVP	➤ 8/10/12/14 bit data	➤ 8/10/12/16 bit data
Ethernet	➤ Adhere to the IEEE 802.3-2002 standard	➤ Adhere to the IEEE 802.3-2015 standard
RTC	➤ Two intrusion detection pins ➤ One timestamp triggers the input pin	➤ 3 intrusion detection pins: PC13/PE6/PA0 ➤ 16 external interrupts EXTI0~15 can be configured as timestamp trigger sources
ADC	➤ 3*ADC ➤ Up to 24 external channels ➤ Single channel maximum 2.4MSPS	➤ 4*ADC ➤ Up to 51 external channels ➤ Maximum 4.7MSPS
DAC	➤ 2*DAC ➤ Up to 2 external channels	➤ 8*DAC ➤ Up to 4 external channels
VREFBUF	➤ Not supported	➤ Can be configured with 2.048, 2.5, and 2.9V ➤ Configurable output
Algorithm	➤ Supported CRC32 ➤ STM32F415支持DES/3DES ➤ STM32F415支持AES128/192/256 ➤ STM32F415支持SHA1/224/256 ➤ STM32F415支持MD5/HMAC	➤ Supported CRC16/32 ➤ Supported AES128/192/256 ➤ Supported DES/3DES ➤ Supported SM4 ➤ Supported SHA1/224/256 ➤ Supported MD5 ➤ Supported SM3
Secure	➤ RDP ➤ PCROP ➤ WRP	➤ RDP ➤ WRP ➤ Storage encryption ➤ Partition protection ➤ Safe startup
Pin		
GPIO	➤ Does not support digital filtering ➤ Other differences can be found in the pin function mapping	➤ Configurable digital filtering ➤ Other differences can be found in the pin function mapping

6 Version History

Version	Date	Changes
V1.0.0	2024.11.12	Initial version

7 Disclaimer

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