N32G003x4/x5 Datasheet

N32G003 series based on 32-bit ARM Cortex-M0, runup to 48MHz, up to 29.5KB embedded flash, 3KB SRAM, 1x12bit 1Msps ADC, 1xCOMP, 2xUART, 1xI2C, 1xSPI.

Key features

- **Core**
  - A 32-bit ARM Cortex-M0 core, Single-cycle hardware multiply instruction
  - Run up to 48MHz
- **Encrypted memory**
  - Up to 29.5KByte embedded Flash memory, data 100,000 cycling and 10 years retention
  - Up to 3KB SRAM
- **Power consumption mode**
  - Run mode: all peripherals are configurable
  - Stop mode: TIM6, IWDG can be configured to work, SRAM data is maintained, and all IO states are maintained
  - Power Down mode: All power supply off, support NRST, PA1_WKUP0, PA2_WKUP1 wake-up
- **Clock**
  - HSI: Internal high-speed RC OSC 48MHz/40MHz(optional)
  - LSI: Internal low-speed RC OSC 32KHz
  - MCO: Support 1-way clock output, configurable HSI or LSI clock output that can be divided.
- **Reset**
  - Support power-on/power-off/external pin reset
  - Support programmable low voltage detection and reset
  - Support watchdog reset, software reset
- **Communication interface**
  - 2xUART, which supports asynchronous mode, multiprocessor communication mode, single-wire half-duplex mode
  - 1xSPI, rate up to 12MHz
  - 1xI2C, rate up to 1MHz, which can be configured in master/slave mode
- **Analog interface**
  - 1x12bit 1Msps high-speed ADC , up to 9 external single-ended input channels and 1 internal channel connected to the 1.2V reference
  - 1xhigh-speed analog comparator, positive terminal input supports four adjustable dropout voltages of 0mV/100mV/200mV/ 300mV
- **Support up to 18 GPIOs that support multiplexing.**
- **1xBeeper, support complementary output**
- **Timer counter**
  - 1x16-bit advanced timer counters, support input capture, output compare, each timer has 4 independent channels, 3 of which support 6 complementary PWM output

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- 1x16-bit general purpose timer counters, each timer has 2 independent channels, supports input capture/output compare/PWM output
- 1x16-bit basic timer counter, supports STOP wake-up low-power mode
- 1x24-bit SysTick
- 1x12-bit Independent watchdog (IWDG)

- **Programming mode**
  - Support SWD online debugging interface
- **Security features**
  - CRC16 calculation
  - Support multiple read protection(RDP) levels (L0/L1/L2)
- **96-bit UID and 128-bit UCID**
- **Working conditions**
  - Operating Voltage Range: 2V~5.5V
  - Operating Temperature Range: -40℃~105℃
  - ESD: ±4KV (HBM model), ±1KV (CDM model)
- **Package**
  - QFN20(3mm x 3mm)
  - TSSOP20(6.5mm x 4.4mm)
  - TSSOP20-1(6.5mm x 4.4mm)
  - SOP8(4.9mm x 3.9mm)

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1 Product introduction

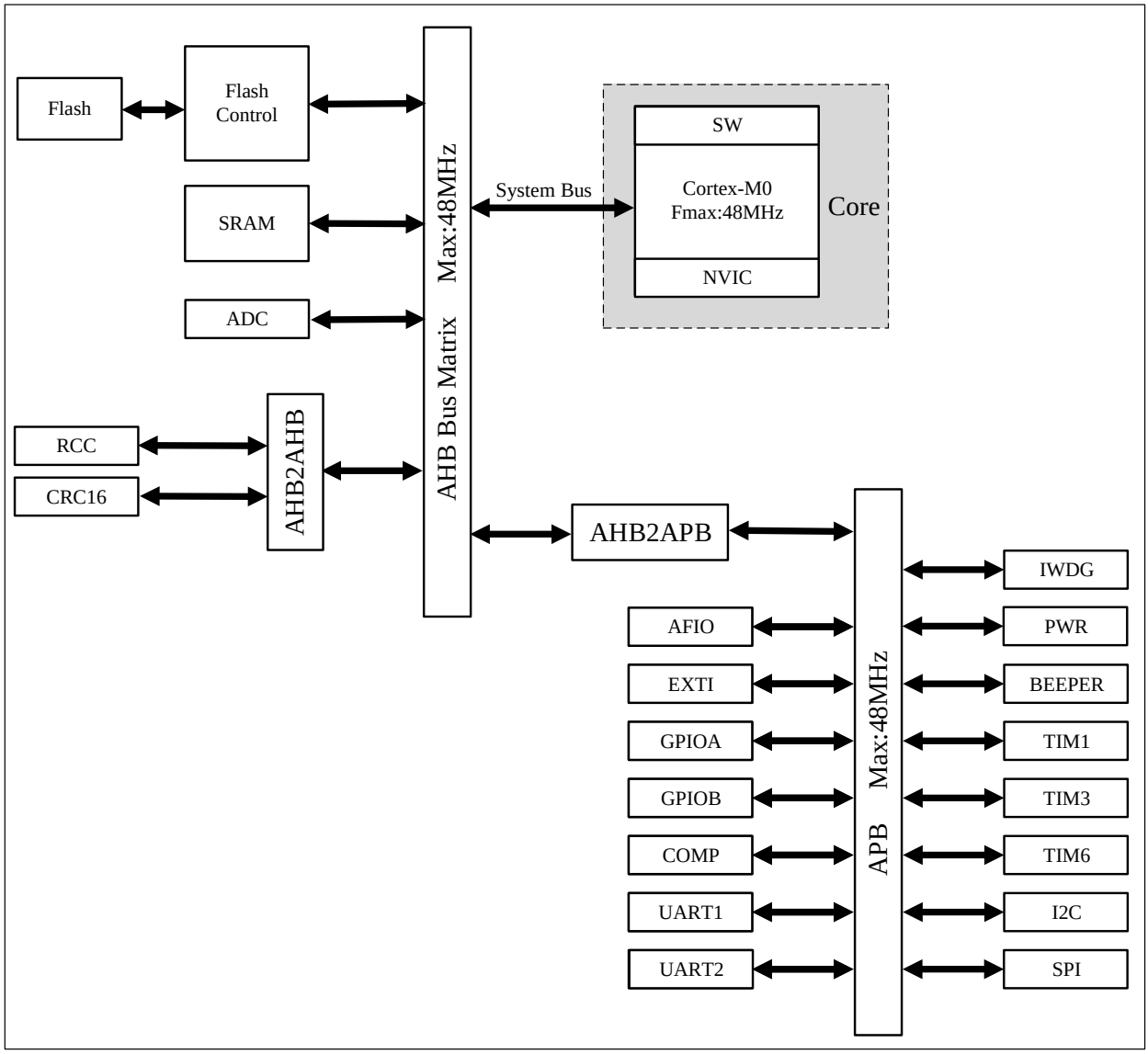
N32G003 series microcontroller products use 32-bit ARM Cortex-M0® core, the highest operating frequency is 48MHz, integrated up to 29.5KB memory Flash, up to 3KB SRAM; Built-in a high-speed AHB bus, a low-speed peripheral bus APB and bus matrix, support up to 18 general-purpose I/O, provide a wealth of high-performance analog interfaces, including a 12-bit 1Msps ADC, support up to 9 external input channels, 1 high-speed comparator, and provide a variety of digital communication interfaces, including 2xUART, 1xI2C, 1xSPI.

The N32G003 series can operate stably in the temperature range of -40℃ to +105℃, supply voltage from 2V to 5.5V, and provide a variety of power modes for users to choose from, meeting the requirements of low-power applications. This series is available in different packages with 20 pins.

N32G003 series microcontrollers are suitable for low-power electronic cigarettes, security, smart home, motor control, power management system and other application scenarios.

Figure 1-1 shows the bus block diagram of this series of products.

Figure 1-1 N32G003 Block Diagram



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1.1 Devices list

Table 1-1 N32G003 Series Resource Configuration

Part Number		N32G003J5A7	N32G003F5Q7/F4Q7	N32G003F5S7/F4S7	N32G003F5S7-1
Flash capacity (KB)		29.5	29.5/16	29.5/16	29.5
SRAM capacity (KB)		3	3	3	3
CPU frequency		ARM Cortex-M0 @ 48MHz			
Working environment		2~5.5V/-40~105℃			
Timer	General	1	1	1	1
	Advanced	1	1	1	1
	Basic	1	1	1	1
Communication interface	SPI	1	1	1	1
	I2C	1	1	1	1
	UART	2	2	2	2
GPIO		6	18		
12bit ADC		1x12bit	1x12bit	1x12bit	1x12bit
Number of channels		8Channel	9Channel	9Channel	9Channel
COMP		1	1	1	1
Beeper		1	1	1	1
Algorithm support		CRC16			
Security protection		Read protection（RDP）			
Package		SOP8	QFN20	TSSOP20	TSSOP20-1

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2 Function Introduction

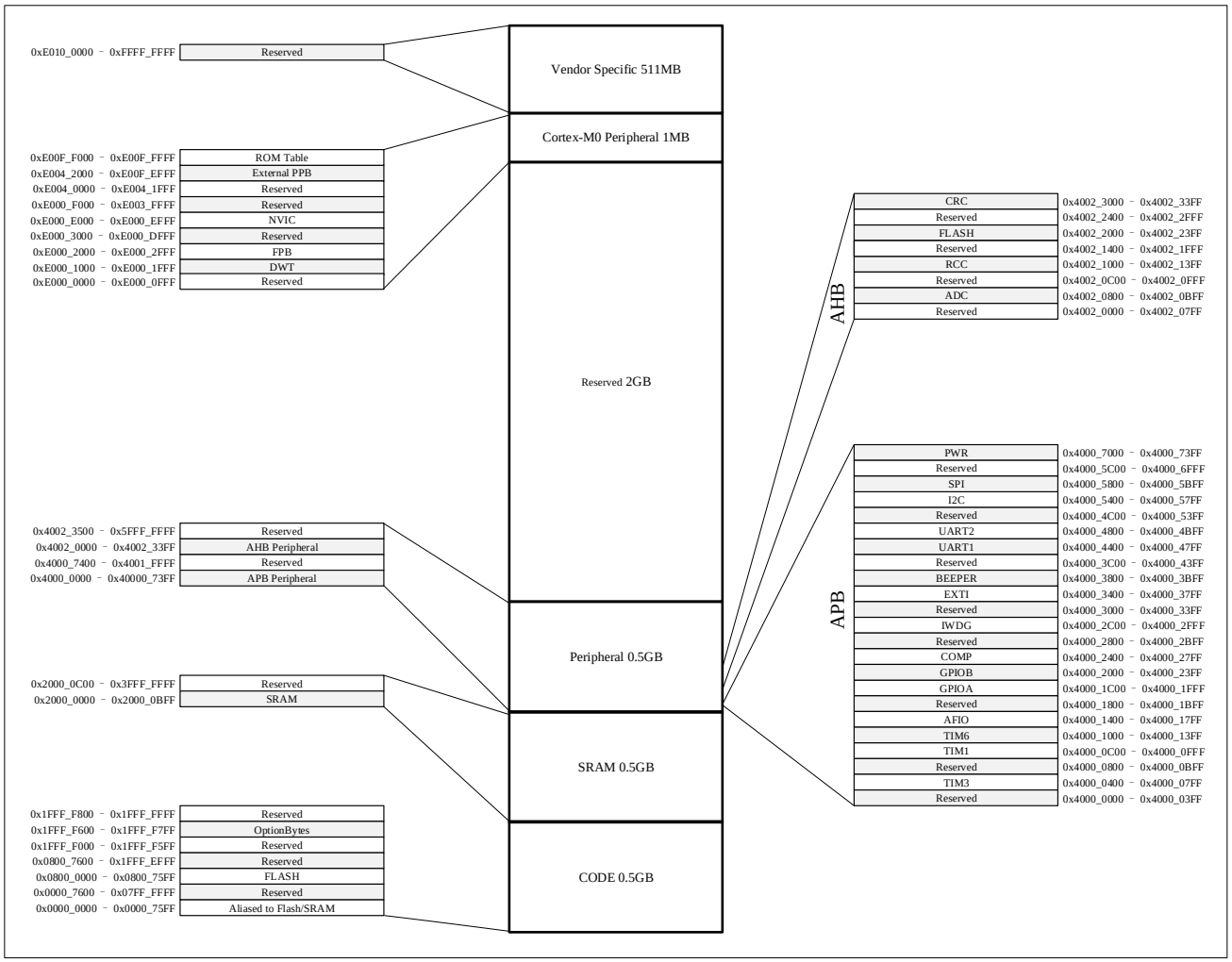
2.1 Processor core

The N32G003 family integrates the latest generation of embedded ARM Cortex®-M0 processors.

2.2 Storage

N32G003 series devices include embedded Flash memory and embedded SRAM, following figure shows the memory address mapping.

Figure 2-1 Memory map



2.2.1 Embedded FLASH memory

Integrated 29.5K bytes embedded FLASH, used to store programs and data, page size of 512byte, supporting page erasing, word writing, word reading, half word reading, byte reading operations.

2.2.2 Embedded SRAM

Integrated 3K bytes embedded SRAM. In STOP mode the SRAM data can be retained.

2.2.3 Nested vector interrupt controller (NVIC)

The Nested Vector Interrupt Controller (NVIC) is closely linked to the processor core, enabling low latency interrupt processing and efficient processing of late interrupts. The nested vector interrupt controller manages interrupts

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including core exceptions.

- 16 maskable interrupt channels (not including 16 Cortex®-M0 neutral line);
- 4 programmable priorities (using 2 bit interrupt priorities);
- Low latency exception and interrupt handling;
- Power management control;
- Realization of system control register;

2.3 External interrupt/event controller (EXTI)

The external interrupt/event controller contains 20 edge detectors for generating interrupt/event requests. Each input line can be independently configured as an event or interrupt, as well as three trigger types of rising edge, falling edge or bilateral edge, or can be shielded independently. The suspend register holds interrupt requests for status lines, and interrupt requests can be cleared by writing '1' to the corresponding bit of the suspend register..

2.4 Clock system

The device is available in a variety of clocks to choose from, including an internal high-speed RC oscillator HSI (48MHz or 40MHz) and an internal low-speed clock LSI (32KHz).

The HSI oscillator clock source is used to drive the system clock (SYSCLK).

The 32KHz low-speed internal RC is used as the secondary clock source, which can be selected to drive the independent watchdog (IWDG), TIM6 (for wake-up STOP mode).

Multiple prescalers can be used to configure the frequency of AHB and APB. The maximum frequency of AHB and APB is 48MHz.

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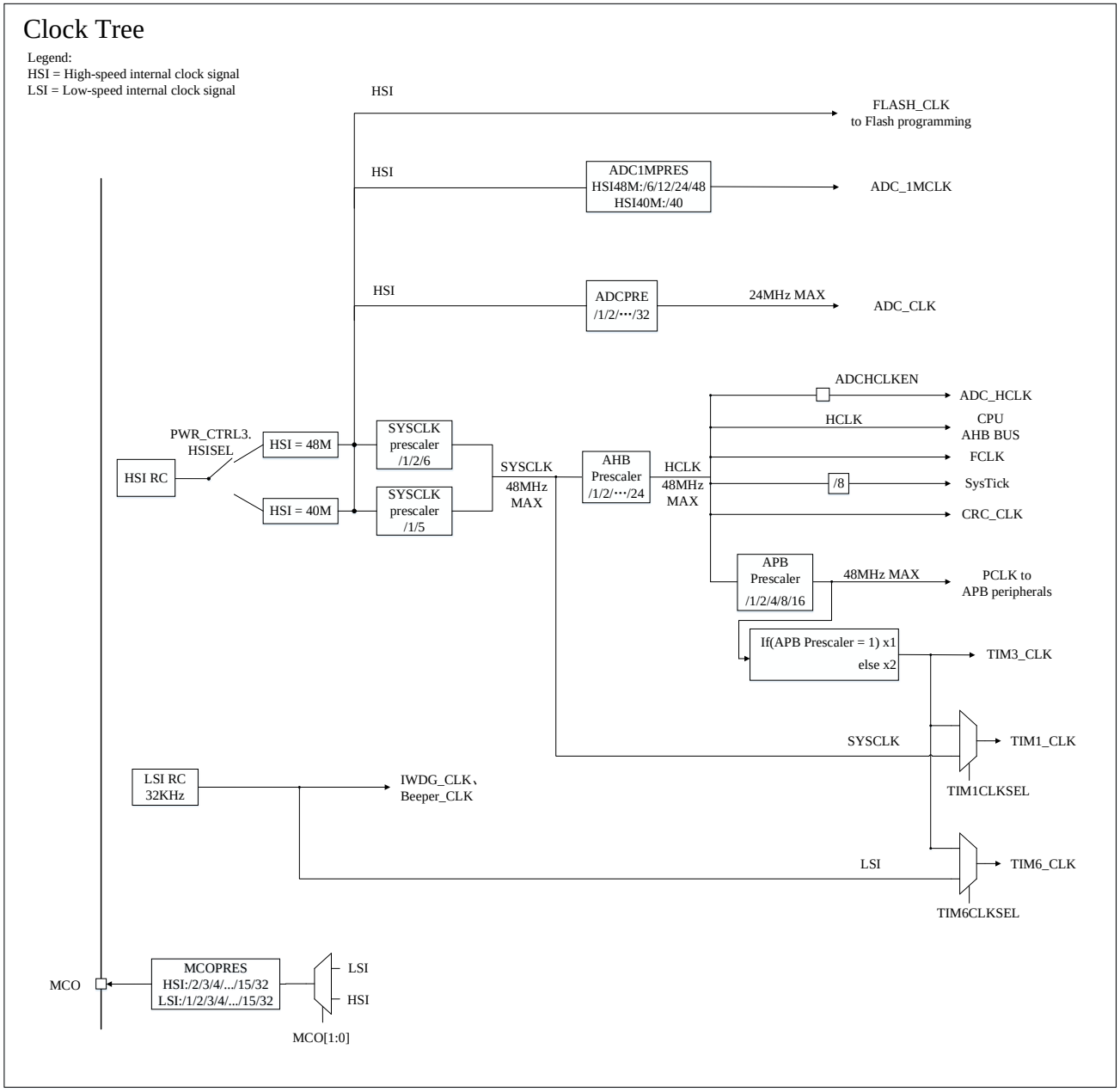
Figure 2-2 Clock Tree



2.5 Boot mode

Boot from the FLASH Memory 0x08000000.

2.6 Power supply scheme

- VDD area: The voltage input range is 2V~5.5V, which mainly provides power input for Main Regulator, IO and clock reset system.
- VDDD area: The voltage regulator supplies power for the CPU, AHB, APB, SRAM, FLASH and most digital peripheral interfaces.

PWR is the power control module of the entire device, its main function is to control N32G003 to enter different power modes and can be awakened by other events or interrupts. N32G003 supports RUN, STOP and PD modes.

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2.7 Programmable voltage detector

Integrated power-on reset (POR) and power-down reset (PDR) circuits are integrated to ensure that the system operates when the supply exceeds 2V, and when V_{DD} falls below the set threshold ($V_{POR/PDR}$), the device is placed in a reset state without using an external reset circuit. There is also a programmable voltage monitor (PVD) in the device that monitors the V_{DD} supply and compares to the threshold V_{PVD}, which generates an interrupt when V_{DD} is below or above the threshold V_{PVD}, and the interrupt handler can issue a warning message. The PVD function needs to be enabled through the program. For values for $V_{POR/PDR}$ and V_{PVD}, refer to Table 4-6.

2.8 Low power mode

N32G003 is in RUN mode after system reset or power-on reset. When the CPU does not need to run(e.g. while waiting for an external event), you can choose to enter a low power mode to save power. It is up to the user to choose the best low-power mode between low power, short start-up time, and available wake-up sources.

N32G003 has the following two low power modes:

- STOP mode (most of the clocks are turned off, the voltage regulator is still running in low power mode)
- PD mode (V_{DDD} power down mode, V_{DD} retention, 2 WAKEUP IO and NRST can wake up)
- In addition, the following methods can also reduce the power consumption in RUN mode:
  - Reduce the system clock frequency
  - Turn off the unused peripheral clocks on the APB and AHB buses
  - Configure PWR_CTRL4.STBFLH in RUN mode allows FLASH to enter deep standby mode.

2.9 Timer and watchdog

The N32G003 supports up to 1 advanced timer, 1 general-purpose timer, 1 base timer, as well as 1 watchdog timer and 1 system tick timer.

The following table compares the functions of advanced timer, general-purpose timer and basic timer:

Table 2-1 Comparison of Timer functions

Timer	Counter resolution	Counter type	Prescaler factor	Capture/ compare channels	Complementary output
TIM1	16bit	Up, down, up/down	Any integer between 1 and 65536	4	Y
TIM3	16bit	Up, down, up/down	Any integer between 1 and 65536	2	N
TIM6	16bit	Up	Any integer between 1 and 65536	0	N

2.9.1 Basic timer (TIM6)

The basic timer contains a 16-bit counter, it also provides the ability to wake the system from a low-power mode.

The main functions of the basic timer include:

- 16-bit auto-reload up-counting counters.
- 16-bit programmable prescaler. (The frequency division factor can be configured with any value between 1 and 65536)
- The events that generate the interrupt are as follows:

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- Update event

- Support STOP mode wake-up: When the clock source is configured as LSI, STOP mode can be awakened by updating interrupts (connected to EXTI19).

2.9.2 General-purpose timer (TIM3)

The general-purpose timers (TIM3) is mainly used in the following occasions: counting the input signal, measuring the pulse width of the input signal and generating the output waveform, etc.

The main functions of the general-purpose timer include:

- 16-bit auto-reload counters. (It can realize up-counting, down-counting, up/down counting)
- 16-bit programmable prescaler. (The frequency division factor can be configured with any value between 1 and 65536)
- TIM3 up to 2 channels
- Channel's working modes: PWM output, ouput compare, one-pulse mode output, input capture
- The events that generate the interrupt are as follows:
  - Update event
  - Trigger event
  - Input capture
  - Output compare
- Timer can be controlled by external signal
- Timers are linked internally for timer synchronization or chaining
- Supports capturing internal comparator output signals

2.9.3 Advanced timer (TIM1)

The advanced control timers (TIM1) is mainly used in the following occasions: counting the input signal, measuring the pulse width of the input signal and generating the output waveform, etc.
Advanced timers have complementary output function with dead-time insertion and break function. Suitable for motor control.

The main functions of the advanced timer include:

- 16-bit auto-reload counters. (It can realize up-counting, down-counting, up/down counting)
- 16-bit programmable prescaler. (The frequency division factor can be configured with any value between 1 and 65536)
- Programmable Repetition Counter
- TIM1 up to 5 channels.
- 4 capture/compare channels, the working modes are PWM output, ouput compare, one-pulse mode output, input capture.
- The events that generate the interrupt are as follows:
  - Update event
  - Trigger event
  - Input capture
  - Output compare
  - Break input
- Complementary outputs with adjustable dead-time
  - For TIM1, channel 1,2,3 support this feature

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- Timer can be controlled by external signal
- Timers are linked internally for timer synchronization or chaining
- TIM1_CC5 for COMP blanking

2.9.4 SysTick timer (Systick)

This timer is dedicated to real-time operating systems and can also be used as a standard decrement counter.

It has the following characteristics:

- 24 bit decrement counter
- Automatic reloading function
- A maskable system interrupt is generated when the counter is 0
- Programmable clock source

2.9.5 Watchdog (WDG)

Support for one watchdog independent watchdog (IWDG). It provides increased security, time accuracy.

Independent Watchdog (IWDG)

The independent watchdog is based on a 12-bit decrement counter and a 3-bit prescaler. It is driven by a separate low-speed RC oscillator that remains active even if the master clock fails and operates in STOP modes.Once activated, if the dog is not fed (clears the watchdog counter) within the set time, the IWDG generates a reset when the counter counts to 0x000. It can be used to reset the entire system in the event of an application problem, or as a free timer to provide time-out management for applications. The option byte can be configured to start the watchdog software or hardware. Reset and low power wake up are available.

2.10 I^2C bus interface

The device integrates up to one independent I2C bus interfaces, which provide multi-master function and control all I2C bus-specific timing, protocol, arbitration and timeout. Supports multiple communication rate modes (up to 1MHz), I2C modules have a variety of uses, including CRC code generation and verification.

The functions of the I2C interface are described as follows:

- This module can be used as master device or slave device;
- I2C master device function;
  - Generate a clock;
  - Generate start and stop signals;
- Function of I2C slave device
  - Programmable address detection;
  - The I2C interface supports 7-bit or 10-bit addressing and dual-slave address response capability in 7-bit slave mode.
  - Stop bit detection;
- Generate and detect 7-bit / 10-bit addresses and broadcast calls;
- Support different communication speeds;
  - Standard speed (up to 100 kHz);
  - Fast (up to 400 kHz);
  - Fast + (up to 1MHz);
- Status flags:
  - Transmitter/receiver mode flag;

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- Byte transfer complete flag;
- I2C bus busy flag;

- Error flags:
  - Arbitration is missing in Master mode
  - Acknowledge (ACK) error after address/data transfer;
  - Error start or stop condition detected
  - Overrun or underrun when clock extending is disable;
- Interrupt vectors: event interrupt and error interrupt;
- Optional extend clock function
- Generation or verification of configurable PEC(Packet error detection)
  - In transmit mode, the PEC value can be transmitted as the last byte
  - PEC error check for the last received byte

2.11 Universal asynchronous transceiver (UART)

In the N32G003 series, two universal asynchronous transceivers (UART1 and UART2) are integrated.

UART1 and UART2 interfaces support asynchronous communication mode, multiprocessor communication mode, single-wire half-duplex communication mode.

Main features of USART are as follows:

- Full-duplex asynchronous communication
- Supports NRZ standard format
- Supports single-wire half-duplex communication
- Configurable baud rate
- Support serial data frame structure with 8 or 9 data bits, 1 or 2 stop bits
- Generation and checking of supported parity bits
- Support multi-processor communication mode, can enter mute mode, wake up by idle detection or address mark detection
- Support data overflow error detection, frame error detection, noise error detection, parity error detection
- 8 interrupt requests:
  - Transmit data register empty
  - Transmit complete
  - Receive data register full
  - Idle line detected
  - Data overflow detected
  - Frame error
  - Noise error
  - Parity error

Mode configuration:

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UART modes	UART1	UART2
Asynchronous mode	support	support
Multiprocessor communication	support	support
Half Duplex (Single wire mode)	support	support

2.12 Serial peripheral interface (SPI)

Supports 1 SPI interface. SPI allows the chip to communicate with external devices in half/full-duplex, synchronous, serial manner. This interface can be configured in master mode and provide a communication clock (SCK) for external slave devices. Interfaces can also operate in a multi-master configuration. It can be used for a variety of purposes, including two-wire simplex simultaneous transmission using a single bidirectional data line.

The main functions of SPI interfaces are as follows:

- Full duplex mode and simplex synchronous mode.
- Support master mode, slave mode and multi-master mode.
- Supports 8-bit or 16-bit data frame format.
- Data bit sequence programmable.
- NSS management by hardware or software.
- Clock polarity and phase programmable.

2.13 General purpose input/output interface (GPIO)

Supports 18 GPIO, divided into 2 groups (GPIOA/GPIOB), GPIOA have 16 pins, GPIOB has 2 pins. Each GPIO pin can be configured by software as output (push-pull or open drain), input (with or without pull-up or pull-down) or alternate peripheral function ports (output/input), most GPIO pins are shared with digital or analog reuse peripherals, some IO pins are also reused with clock pins. Except for ports with analog input function, all GPIO pins have the ability to pass through a large current.

GPIO ports have the following features:

- GPIO port can be configured with the following modes by software:
  - Input floating
  - Input pull-up
  - Input pull-down
  - Analog function
  - Open drain output and pull-up/pull-down can be configured
  - Push-pull output and pull-up/pull-down can be configured
  - Push-pull alternate function and pull-up/pull-down can be configured
  - Open-drain alternate function and pull-up/pull-down can be configured
- Individual bit setting or bit clearing function
- All I/O support external interrupt function
- All I/O support low power mode wake up, rising or falling edge configurable
  - 18 EXTI can be used for wake up in STOP mode, and all I/O can be reused as EXTI
  - NRST(PA0)/PA1/PA2 three wake up IOs can be used for PD mode wake up, I/O filtering time maximum 1us
- Supports software remapping I/O alternate function

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- Support GPIO lock mechanism, reset the lock state to clear

Each I/O port bit can be programmed arbitrarily, but the I/O port register must be accessed as a 32-bit word (16-bit half-word or 8-bit byte are not allowed).

2.14 Analog/digital converter (ADC)

The 12-bit ADC is a high-speed analog-to-digital converter using successive approximation.It can measure 10 channel signal source. It has 9 external and 1 internal channel.Each channel of the A/D conversion performed in single,continuous or scan mode. ADC measurements are stored (left-aligned/ right-aligned) in 16-bit data registers. The application can detect that the input voltage is within user-defined high/low thresholds by analog watchdog and the maximum frequency of the input clock to the ADC is 24MHz.

The main features of ADC are described as follows:

- Supports 1 ADC, supports single-ended inputs, and can measure 9 external and 1 internal sources
- Supports 12-bit resolution with a maximum sampling rate of 1MSPS
- ADC clock source is divided into working clock source and timing clock source
  - HSI as the ADC_CLK working clock source, up to 24M.
  - HSI as the ADC_1MCLK timing clock source for internal timing functions, the frequency must be configured to 1MHz.
- Supports timer trigger ADC sampling
- Interrupts when conversion ends, and simulated watchdog events occur
- Support 2 conversion modes
  - Single conversion
  - Continuous conversion
- Scan mode supports up to any 5 channels, each channel has an independent result data register buffer
- All channel sampling intervals can be programmed uniformly
- Regular conversion has external triggering options
- ADC power supply requirements: 2.4V to 5.5V
- ADC input conversion range: $0 \leq V_{IN} \leq VDD$.

2.15 Analog comparator (COMP)

One comparator is embedded and can be used as a separate device (all comparator ports are led to I/O), or it can be combined with a timer to form cycle-by-cycle current control in motor control applications with the PWM output from the timer.

The main functions of comparator are as follows:

- Operate votage 2.4~5.5V
- A comparator with substraction,support positive port input voltage(500mV~VDD-200mV) minus a reference voltage(300/200/100/0mV)
- Support filter clock
- Output polarity can be configured high and low
- The hysteresis configuration can be configured with none, low, medium, or high
- The comparison result can be output to the I/O port or trigger timer, which is used to capture events, OCREF_CLR events, brake events, and generate interrupts
- Input channel can select I/O ports

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- Can be equipped with read-only or read-write, it needs to be reset to unlock when locked
- Support blanking (Blanking), configurable blanking source to generate blanking, ,
- Filter window size can be configured
- Filter threshold size can be configured
- Sampling frequency for filtering can be configured

2.16 Beeper

The beeper module supports complementary outputs and can generate periodic signals to drive external passive buzzers. Used to generate a beep or the alarm to sound.

2.17 Cyclic redundancy check calculation unit (CRC)

Integrated CRC16 functions, the cyclic redundancy check (CRC) calculation unit is based on a fixed generation polynomial to obtain any CRC calculation results. In many applications, CRC-based techniques are used to verify data transfer or storage consistency.

The CRC has the following features:

- CRC16: supports polynomials $X^{16} + X^{15} + X^2 + X^0$
- CRC16 calculation time: 1 AHB clock cycle (HCLK)
- The initial value for cyclic redundancy computing is configurable

2.18 Unique device serial number (UID)

N32G003 series products have two built-in unique device serial numbers of different lengths, which are 96-bit Unique Device ID (UID) and 128-bit Unique Customer ID (UCID). These two device serial numbers are stored in the system configuration block of flash memory. The information they contain is written at the time of delivery and is guaranteed to be unique to any of the N32G003 series microcontrollers under any circumstances and can be read by user applications or external devices through the CPU or SWD interface and cannot be modified.

The 96-bit UID is usually used as a serial number or password. When writing flash memory, this unique identifier is combined with software encryption and decryption algorithm to further improve the security of code in flash memory.

UCID is 128-bit, which complies with the definition of national technology chip serial number. It contains the information related to chip production and version.

2.19 Serial wire SWD debug port (SWD)

Embedded ARM SWD interface.

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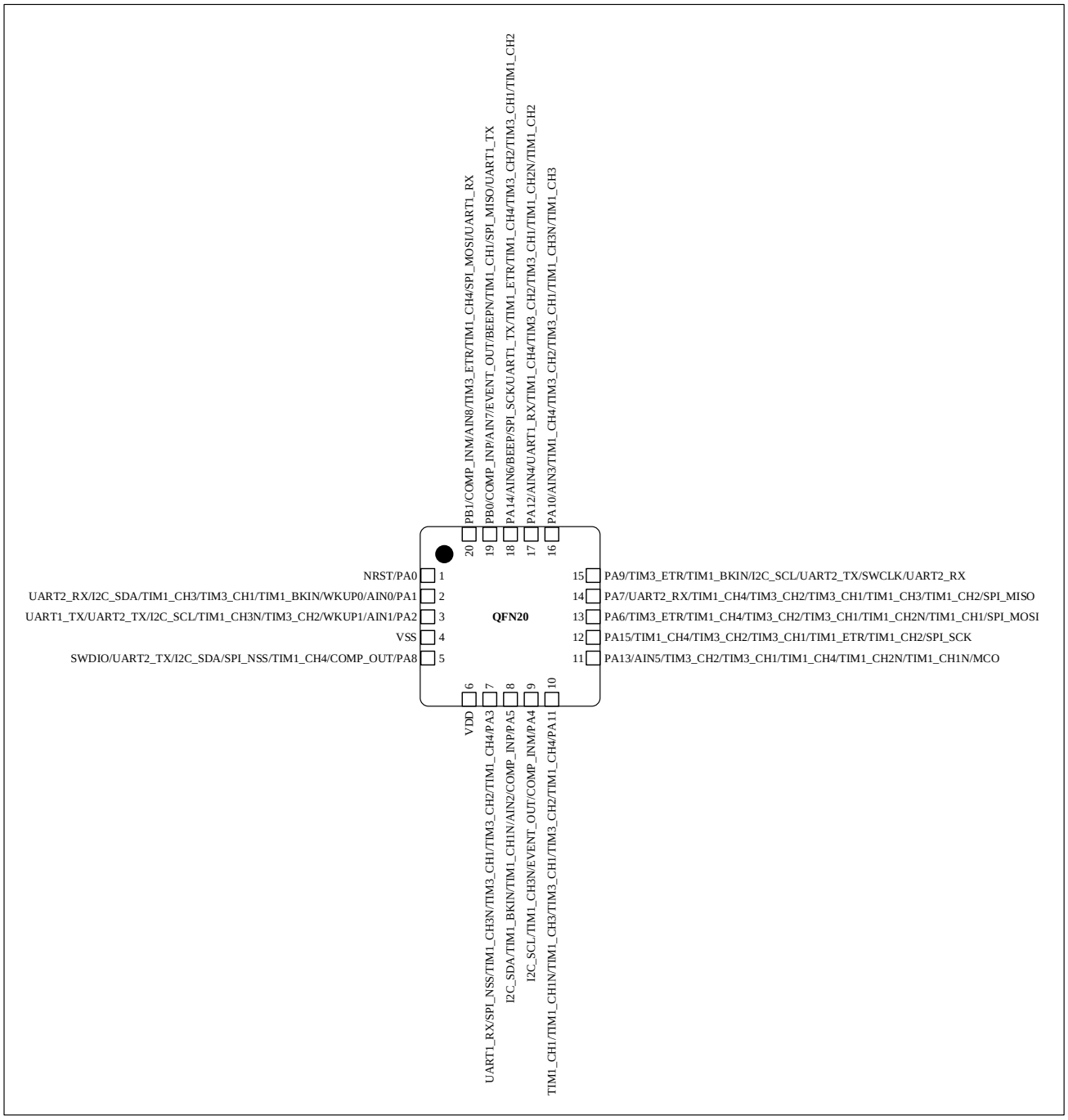
3 Pin and description

3.1 Pinouts

3.1.1 QFN20

Figure 3-1 N32G003 Series QFN20 pinout



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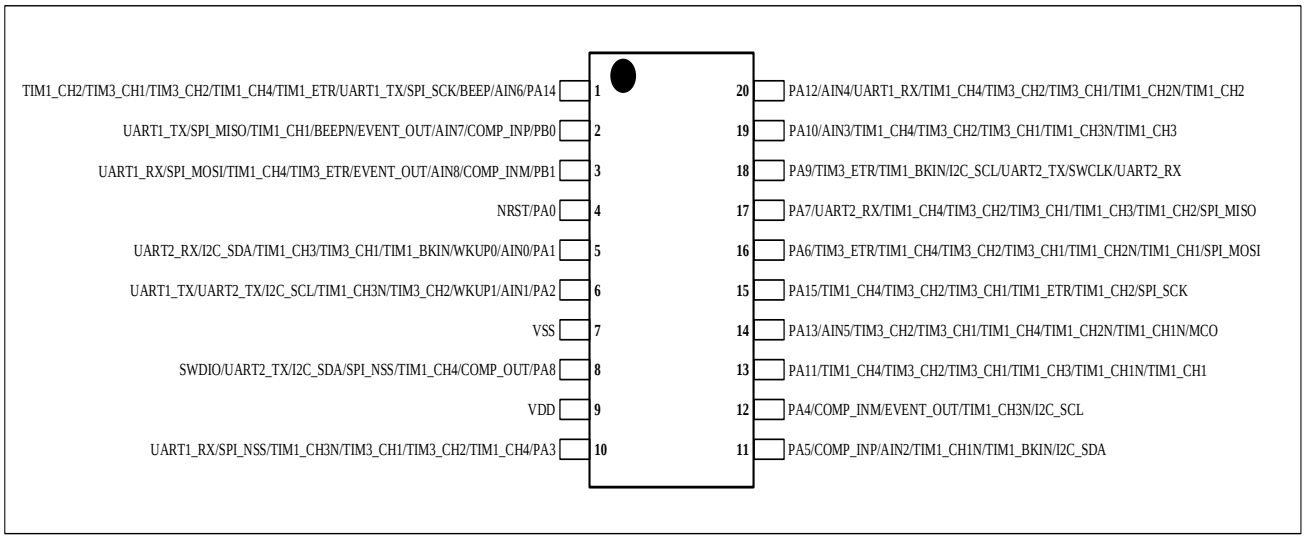
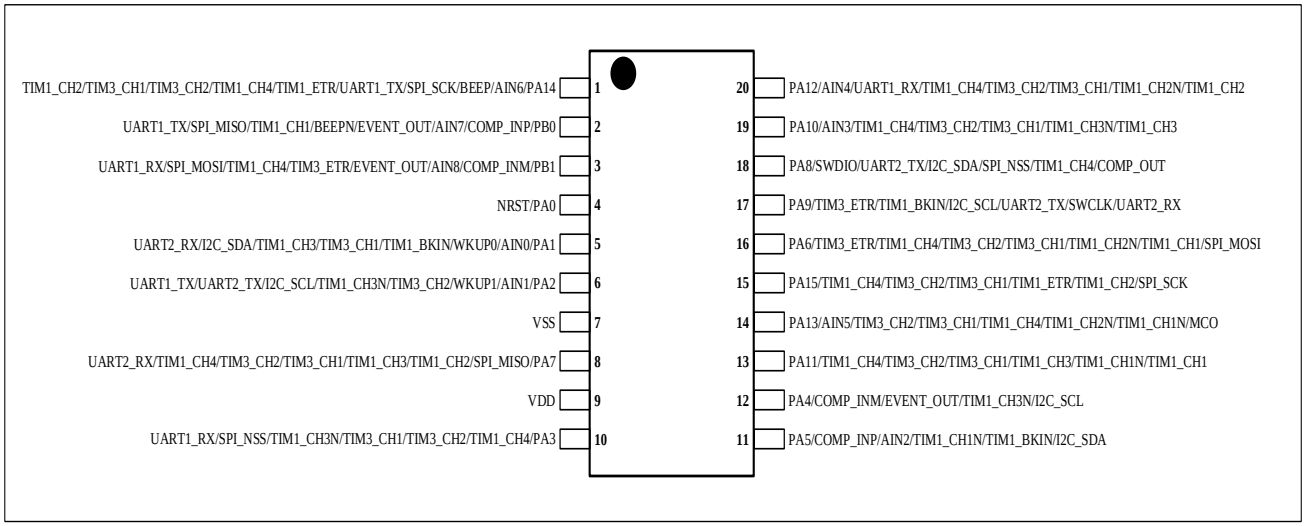
3.1.2 TSSOP20

Figure 3-2 N32G003 Series TSSOP20 pinout



3.1.3 TSSOP20-1

Figure 3-3 N32G003 Series TSSOP20-1 pinout



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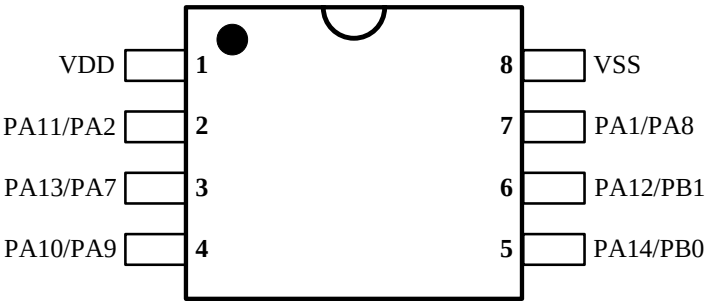
3.1.4 SOP8

Figure 3-4 N32G003 Series SOP8 pinout



1	VDD	
2	PA2	AIN1/WKUP1/TIM2_CH2/TIM1_CH3N/I2C_SCL/UART2_TX/UART1_TX
	PA11	TIM1_CH4/TIM2_CH2/TIM2_CH1/TIM1_CH3/TIM1_CH1N/TIM1_CH1
3	PA7	UART2_RX/TIM1_CH4/TIM2_CH2/TIM2_CH1/TIM1_CH3/TIM1_CH2/SPI_MISO
	PA13	AIN5/TIM2_CH2/TIM2_CH1/TIM1_CH4/TIM1_CH2N/TIM1_CH1N/MCO
4	PA9	TIM2_ETR/TIM1_BKIN/I2C_SCL/UART2_TX/SWCLK
	PA10	AIN3/TIM1_CH4/TIM2_CH2/TIM2_CH1/TIM1_CH3N/TIM1_CH3
5	PA14	AIN6/BEEP/SPI_SCK/UART1_TX/TIM1_ETR/TIM1_CH4/TIM2_CH2/TIM2_CH1/TIM1_CH2
	PB0	COMP_INP/AIN7/EVENT_OUT/BEEPN/TIM1_CH1/SPI_MISO/UART1_TX
6	PA12	AIN4/UART1_RX/TIM1_CH4/TIM2_CH2/TIM2_CH1/TIM1_CH2N/TIM1_CH2
	PB1	COMP_INM/AIN8/EVENT_OUT/TIM2_ETR/TIM1_CH4/SPI_MOSI/UART1_RX
7	PA1	AIN0/WKUP0/TIM1_BKIN/TIM2_CH1/TIM1_CH3/I2C_SDA/UART2_RX
	PA8	COMP_OUT/TIM1_CH4/SPI_NSS/I2C_SDA/UART2_TX/SWDIO
8	VSS	

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3.2 Pin definition

Table 3-1 Pin Definition

Package				Pin name(function after reset)	Type(1)	I/O structure(2)	Alternate functions	
SOP8	TSSOP20	TSSOP20-1	QFN20				Alternate functions	Additional functions
5	1	1	18	PA14	I/O	TC	TIM1_CH2 TIM3_CH1 TIM3_CH2 TIM1_CH4 TIM1_ETR UART1_TX SPI_SCK BEEP	AIN6
5	2	2	19	PB0	I/O	TC	UART1_TX SPI_MISO TIM1_CH1 BEEPN EVENT_OUT	AIN7 COMP_INP
6	3	3	20	PB1	I/O	TC	UART1_RX SPI_MOSI TIM1_CH4 TIM3_ETR EVENT_OUT	AIN8 COMP_INM
-	4	4	1	NRST/PA0(3)	I/O	RST/TC	Can be configured as an NRST pin or a normal IO pin	
7	5	5	2	PA1	I/O	TC	UART2_RX I2C_SDA TIM1_CH3 TIM3_CH1 TIM1_BKIN WKUP0	AIN0
2	6	6	3	PA2	I/O	TC	UART1_TX UART2_TX I2C_SCL TIM1_CH3N TIM3_CH2 WKUP1	AIN1
8	7	7	4	VSS	S	-	Power ground	
7	8	18	5	PA8(3) (SWDIO)	I/O	TC	SWDIO UART2_TX I2C_SDA SPI_NSS TIM1_CH4 COMP_OUT	-
1	9	9	6	VDD	S	-	Power supply	

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-	10	10	7	PA3	I/O	TC	UART1_RX SPI_NSS TIM1_CH3N TIM3_CH1 TIM3_CH2 TIM1_CH4	-
-	11	11	8	PA5	I/O	TC	I2C_SDA TIM1_BKIN TIM1_CH1N	AIN2 COMP_INP
-	12	12	9	PA4	I/O	TC	I2C_SCL TIM1_CH3N EVENT_OUT	COMP_INM
2	13	13	10	PA11	I/O	TC	TIM1_CH1 TIM1_CH1N TIM1_CH3 TIM3_CH1 TIM3_CH2 TIM1_CH4	-
3	14	14	11	PA13	I/O	TC	MCO TIM1_CH1N TIM1_CH2N TIM1_CH4 TIM3_CH1 TIM3_CH2	AIN5
-	15	15	12	PA15	I/O	TC	SPI_SCK TIM1_CH2 TIM1_ETR TIM3_CH1 TIM3_CH2 TIM1_CH4	-
-	16	16	13	PA6	I/O	TC	SPI_MOSI TIM1_CH1 TIM1_CH2N TIM3_CH1 TIM3_CH2 TIM1_CH4 TIM3_ETR	-

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3	17	8	14	PA7	I/O	TC	SPI_MISO TIM1_CH2 TIM1_CH3 TIM3_CH1 TIM3_CH2 TIM1_CH4 UART2_RX	-
4	18	17	15	PA9[3] (SWCLK)	I/O	TC	SWCLK UART2_TX I2C_SCL TIM1_BKIN TIM3_ETR UART2_RX[4]	-
4	19	19	16	PA10	I/O	TC	TIM1_CH3 TIM1_CH3N TIM3_CH1 TIM3_CH2 TIM1_CH4	AIN3
6	20	20	17	PA12	I/O	TC	TIM1_CH2 TIM1_CH2N TIM3_CH1 TIM3_CH2 TIM1_CH4 UART1_RX	AIN4

1. *I = input, O = output, S = power, HiZ = High resistance*
2. *TC: Standard 5V I/O, RST: bidirectional reset pin with built-in weak pull-up resistor*
3. *During and immediately after the reset, the multiplexing function is not enabled, and the I/O port is configured as an analog input mode (PMODE[1:0]=2'b11). But there are a few exception signals:*
   - *PA0 is configured as a normal GPIO or NRST pin via an option byte*
   - *After reset, the default state of the pins related to the debugging system is the SWD function, and the SWD pin is configured to input pull-up or pull-down mode:*
     - *PA9: SWCLK is configured as input pull-down mode*
     - *PA8: SWDIO is configured as input pull-up mode*
4. *Version A chips do not support PA9 multiplexing to UART2_RX*

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4 Electrical characteristics

4.1 Parameter conditions

All voltages are based on VSS unless otherwise specified.

4.1.1 Minimum and maximum values

Unless otherwise specified, all minimums and maximums will be guaranteed under the worst ambient temperature, supply voltage and clock frequency conditions by performing tests on 100% of the product on the production line at ambient temperatures T_A=25 ℃.

Note at the bottom of each form that data obtained through characterization results, design simulation and/or process characteristics will not be tested on the production; Base on characterization, the minimum and maximum values are obtained by taking the average of the samples tested and adding or subtracting three times the standard distribution (mean ±3∑).

4.1.2 Typical numerical values

Unless otherwise specified, typical data is based on T_A=25 ℃ and V_{DD}=3.3V (2V ≤ VDD ≤ 5.5V voltage range). These data are only used for design guidance and not tested.

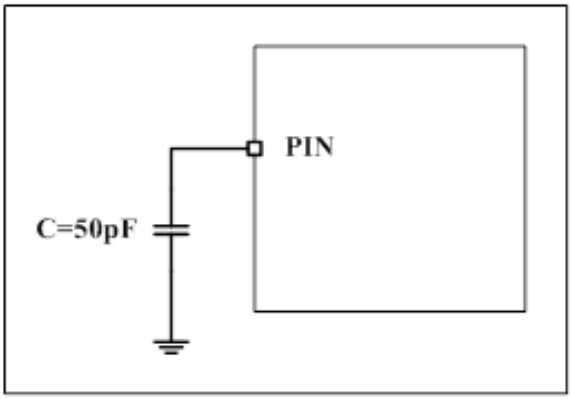
4.1.3 Typical curves

Unless otherwise specified, typical curves are for design guidance only and have not been tested.

4.1.4 Loading capacitor

The load conditions when measuring the pin parameters are shown in Figure 4-1.

Figure 4-1 pin loading conditions



4.1.5 Pin input voltage

The measurement method of the input voltage on the pin is shown in Figure 4-2.

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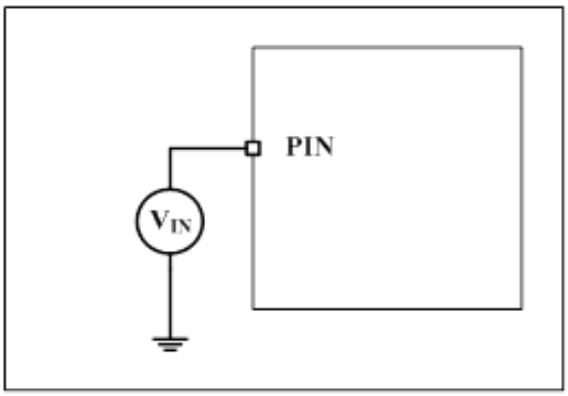
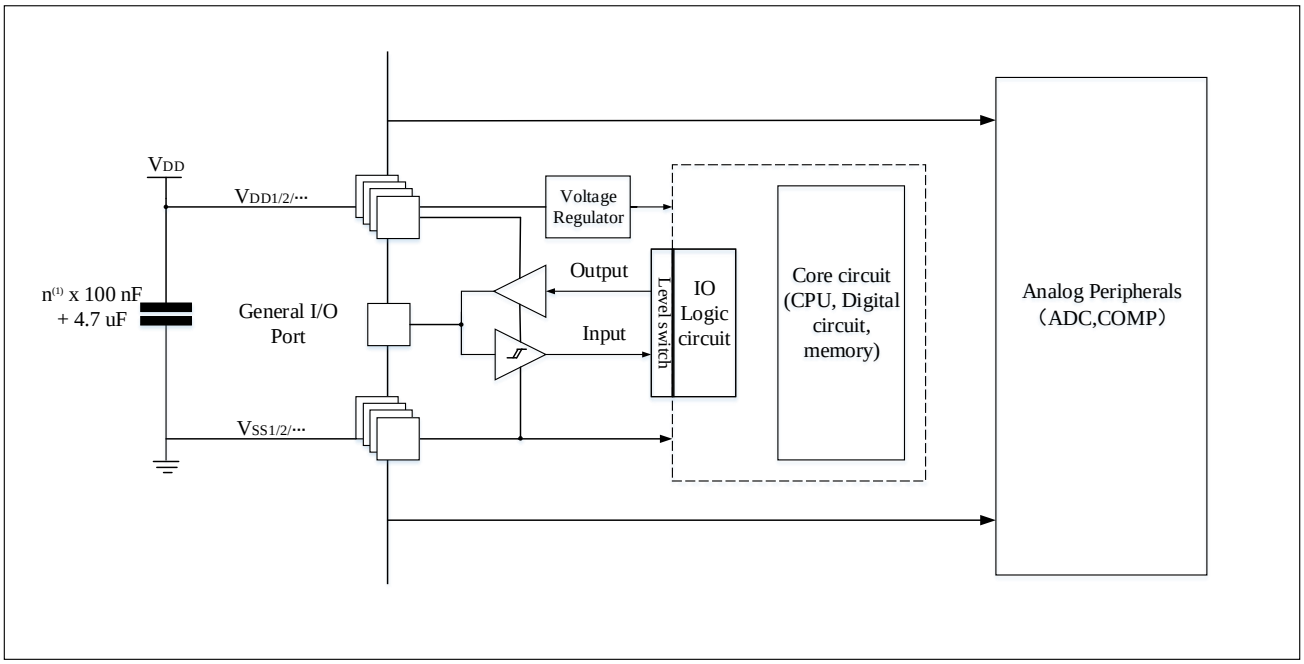
Figure 4-2 Pin input voltage



4.1.6 Power supply scheme

Figure 4-3 Power supply scheme

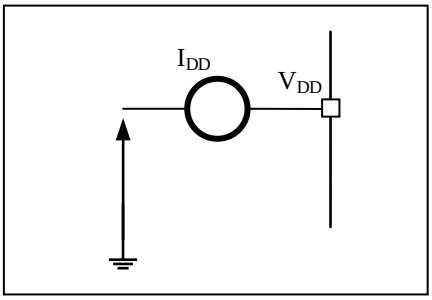


1. *n is the count of VDD.*

Note: Please refer to the hardware design guide for the capacitor connection method.

4.1.7 Current consumption measurement

Figure 4-4 Current consumption measurement



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4.2 Absolute maximum ratings

The load applied to the device may permanently damage the device if it exceeds the values given in the Absolute maximum rating list (Table 4-1, Table 4-2, Table 4-3). The maximum load that can be sustained is only given here, and it does not mean that the functional operation of the device under such conditions is correct. The reliability of the device will be affected when the device works for a long time under the maximum condition.

Table 4-1 Voltage characteristics

Symbol	Parameter	Min	Max	Unit
V_{DD}- V_{SS}	External supply voltage(including V_{DDA} and V_{DD})(1)	-0.3	6.5	V
V_{IN}	Input voltage on any I/O and control pins	-0.3	Min (V_{DD} + 0.3, 6.5)	
$\lvert \Delta V_{DDx} \rvert$	Voltage difference between different power supply pins	-	50	mV
$\lvert V_{SSx}$- $V_{SS} \rvert$	Voltage difference between different ground pins	-	50	
$V_{ESD(HBM)}$	ESD electrostatic discharge voltage (human body model)	See section 4.3.9		

1. All power (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to an external power supply within the allowable range.

Table 4-2 Current characteristics

Symbol	Parameter	Max	Unit
I_{VDD}	Total current into V_{DD}/V_{DDA} power lines(1)	200	mA
I_{VSS}	Total current out of V_{SS} ground lines(1)	200	
I_{IO}	Output current sunk by any I/O and control pin	16	
	Output current source by any I/O and control pins	-16	
$I_{INJ(PIN)}$ (2)	Injected current of NRST pin	0/-5	
	Injected current of other pins	+/-5	

1. All power supply (V_{DD}) and ground (V_{SS}) pins must always be connected to the external allowable range of the power supply system.
2. Reverse injection of current can interfere with the analog performance of the device. See Section 4.3.16.

Table 4-3 Temperature characteristics

Symbol	Parameter	Value	Unit
T_{STG}	Storage temperature range	-65 ~ + 150	℃
T_J	Maximum junction temperature	125	℃

4.3 Operating conditions

4.3.1 General operating conditions

Table 4-4 General operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
f_{HCLK}	AHB clock frequency	-	0	48	MHz
f_{PCLK}	APB clock frequency	-	0	48	
V_{DD}	Standard operating voltage	-	2	5.5	V
	When using an ADC, analog partial operating voltage	-	2.4	5.5	V
	When using an COMP, analog partial operating voltage	-	2.4	5.5	V

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T_A	Temperature range	7 suffix version	-40	105	°C
T_J	Junction temperature range	7 suffix version	-40	125	°C

4.3.2 Operating conditions at power-up and power-down

The parameters given in the following table are based on testing under the ambient temperature listed in Table 4-4.

Table 4-5 Operating conditions at power-up and power-down

Symbol	Parameter	Conditions	Min	Max	Unit
t_{VDD}	V_{DD} rising time rate	From 0 to V_{DD}	20	∞	μs/V
	V_{DD} falling time rate	From V_{DD} to 0	50	∞	μs/V

4.3.3 Reset and power control module features

The parameter test conditions in the following table are based on Table 4-4.

Table 4-6 Reset and power control module features

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{PVD}	Rising	PVD[3:0]=0	1.68	1.88	2.08	V
	Falling	PVD[3:0]=0	1.58	1.78	1.98	
	Rising	PVD[3:0]=1	1.88	2.08	2.28	
	Falling	PVD[3:0]=1	1.78	1.98	2.18	
	Rising	PVD[3:0]=2	2.08	2.28	2.48	
	Falling	PVD[3:0]=2	1.98	2.18	2.38	
	Rising	PVD[3:0]=3	2.28	2.48	2.68	
	Falling	PVD[3:0]=3	2.18	2.38	2.58	
	Rising	PVD[3:0]=4	2.48	2.68	2.88	
	Falling	PVD[3:0]=4	2.38	2.58	2.78	
	Rising	PVD[3:0]=5	2.68	2.88	3.08	
	Falling	PVD[3:0]=5	2.58	2.78	2.98	
	Rising	PVD[3:0]=6	2.86	3.08	3.3	
	Falling	PVD[3:0]=6	2.76	2.98	3.2	
	Rising	PVD[3:0]=7	3.06	3.28	3.5	
	Falling	PVD[3:0]=7	2.96	3.18	3.4	
	Rising	PVD[3:0]=8	3.26	3.48	3.7	
	Falling	PVD[3:0]=8	3.16	3.38	3.6	
	Rising	PVD[3:0]=9	3.46	3.68	3.9	
	Falling	PVD[3:0]=9	3.36	3.58	3.8	
	Rising	PVD[3:0]=10	3.66	3.88	4.1	
	Falling	PVD[3:0]=10	3.56	3.78	4	
	Rising	PVD[3:0]=11	3.82	4.08	4.34	
	Falling	PVD[3:0]=11	3.72	3.98	4.24	
	Rising	PVD[3:0]=12	4.02	4.28	4.54	
	Falling	PVD[3:0]=12	3.92	4.18	4.44	
	Rising	PVD[3:0]=13	4.22	4.48	4.74	
	Falling	PVD[3:0]=13	4.12	4.38	4.64	

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	Rising	PVD[3:0]=14	4.42	4.68	4.94	
	Falling	PVD[3:0]=14	4.32	4.58	4.84	
	Rising	PVD[3:0]=15	4.62	4.88	5.14	
	Falling	PVD[3:0]=15	4.52	4.78	5.04	
$V_{PVDhyst}$(1)	PVD hysteresis	-	80	100	125	mV
V_{LVR}	Rising	LVR[3:0]=0	1.68	1.88	2.08	V
	Falling	LVR[3:0]=0	1.58	1.78	1.98	
	Rising	LVR[3:0]=1	1.88	2.08	2.28	
	Falling	LVR[3:0]=1	1.78	1.98	2.18	
	Rising	LVR[3:0]=2	2.08	2.28	2.48	
	Falling	LVR[3:0]=2	1.98	2.18	2.38	
	Rising	LVR[3:0]=3	2.28	2.48	2.68	
	Falling	LVR[3:0]=3	2.18	2.38	2.58	
	Rising	LVR[3:0]=4	2.48	2.68	2.88	
	Falling	LVR[3:0]=4	2.38	2.58	2.78	
	Rising	LVR[3:0]=5	2.68	2.88	3.08	
	Falling	LVR[3:0]=5	2.58	2.78	2.98	
	Rising	LVR[3:0]=6	2.86	3.08	3.3	
	Falling	LVR[3:0]=6	2.76	2.98	3.2	
	Rising	LVR[3:0]=7	3.06	3.28	3.5	
	Falling	LVR[3:0]=7	2.96	3.18	3.4	
	Rising	LVR[3:0]=8	3.26	3.48	3.7	
	Falling	LVR[3:0]=8	3.16	3.38	3.6	
	Rising	LVR[3:0]=9	3.46	3.68	3.9	
	Falling	LVR[3:0]=9	3.36	3.58	3.8	
	Rising	LVR[3:0]=10	3.66	3.88	4.1	
	Falling	LVR[3:0]=10	3.56	3.78	4	
	Rising	LVR[3:0]=11	3.82	4.08	4.34	
	Falling	LVR[3:0]=11	3.72	3.98	4.24	
	Rising	LVR[3:0]=12	4.02	4.28	4.54	
	Falling	LVR[3:0]=12	3.92	4.18	4.44	
	Rising	LVR[3:0]=13	4.22	4.48	4.74	
	Falling	LVR[3:0]=13	4.12	4.38	4.64	
	Rising	LVR[3:0]=14	4.42	4.68	4.94	
	Falling	LVR[3:0]=14	4.32	4.58	4.84	
	Rising	LVR[3:0]=15	4.62	4.88	5.14	
	Falling	LVR[3:0]=15	4.52	4.78	5.04	
$V_{LVRhyst}$(1)	LVR hysteresis	-	80	100	125	mV
$V_{POR/PDR}$	VDD Power on/down Reset threshold	-	1.487	1.53	1.659	V
$T_{RSTTEMPO}$(1)	Reset temporization	-	76	150	250	us

1. Guaranteed by design, not tested in production.

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4.3.4 Internal reference voltage

The parameter test conditions in the following table are based on Table 4-4.

Table 4-7 Internal reference voltage

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{REFINT}	Internal reference voltage	-Temperature drift characteristics at 40 ℃<TA<+105 ℃(2)	-	-	60	mV
		T_A = 25℃， VDD=5.0V(3)	1.18	1.21	1.22	V
$T_{S\_vrefint}$(1)	When reading the internal reference voltage, the sampling time of the ADC	PLS[3:0]=0001 (Rising edge), f_{ADC_CLK}=24M	15.8	-	126.7	μs

1. The shortest sampling time is obtained through multiple loops in the application.
2. Guaranteed by design, not tested in production.
3. Tested in production.

4.3.5 Power supply current characteristics

Current consumption is a combination of several parameters and factors, including operating voltage, ambient temperature, load of I/O pins, software configuration of the product, operating frequency, I/O pin flip rate, program location in memory, and code executed.

The measurement method of current consumption is illustrated in Figure 4-4.

All of the current consumption measurements given in this section are while executing a reduced set of code.

4.3.5.1 Maximum current consumption

The chip test conditions are as follows:

- All I/O pins are in input mode and connected to a static level——V_{DD} or V_{SS} (no load).
- All peripherals are in the off state, unless otherwise specified.
- The access time of flash memory is adjusted to the frequency of f_{HCLK} (0~24MHz is 0 waiting period, 24~48MHz is 1 waiting period).
- The command prefetch function is enabled (Note: this parameter must be set before setting the clock and bus frequency division).
- When the peripheral is turned on: $f_{PCLK} = f_{HCLK}$.

The parameter test conditions in the following table are based on Table 4-4.

Table 4-8 Typical current consumption in RUN mode when running code from FLASH

Symbol	Parameter	Conditions	f_{HCLK}	Typ(1)	Unit
				T_A = 105℃	
I_{DD}	Supply current in RUN mode	External clock (2), Enable all peripherals	48MHz	4.92	mA
			40MHz	4.03	
			24MHz	3.0	
			8MHz	2.01	
		External clock (2), Disable all peripherals	48MHz	4.0	
			40MHz	3.3	
			24MHz	2.51	
			8MHz	1.8	

1. Guaranteed by characterization, not tested in production.

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4.3.5.2 Typical current consumption

The chip test conditions are as follows:

- All I/O pins are in input mode and connected to a static level—V_{DD} or V_{SS} (no load).
- All peripherals are in the off state, unless otherwise specified.
- The access time of flash memory is adjusted to the frequency of f_{HCLK} (0~24MHz is 0 waiting period, 24~48MHz is 1 waiting period).
- The command prefetch function is enabled (Note: this parameter must be set before setting the clock and bus frequency division).
- When the peripheral is turned on: f_{PCLK}= f_{HCLK}, f_{ADCCLK} = f_{PCLK}/2.

The parameter test conditions in the following table are based on Table 4-4.

Table 4-9 Typical current consumption in RUN mode when running code from FLASH

Symbol	Parameter	Conditions	f_{HCLK}	Typ(1)		Unit
				Enable all peripherals(2)	Disable all peripherals	
I_{DD}	Current in RUN mode	Internal high-speed RC oscillator (HSI)	48MHz	4.91	3.99	mA
			40MHz	4.02	3.28	
			24MHz	2.98	2.49	
			8MHz	1.94	1.74	

1. The typical value is obtained by testing at T_A=25℃ V_{DD}=3.3V.

4.3.5.3 Low power mode current consumption

The microcontroller is under the following conditions:

- All I/O pins are in input mode and are connected to a static level —V_{DD} or V_{SS} (no load).
- All peripherals are disabled unless otherwise noted.

Table 4-10 Typical current consumption in STOP and PD mode(V_{DD}=3.3V)

Symbol	Parameter	Condition	Typ(1)		Max	Unit
			T_A=25℃	T_A=105℃		
I_{DD_STOP}	Current in STOP mode	LSI=32KHz, HCLK off, 3KB SRAM hold, all GPIO status hold, register hold.	1.5	6.1	-	uA
I_{DD_PD}	Current in PD mode	All functional modules are turned off and support 2-way IO wake-up	0.5	1.2	-	uA

1. Typical/Maximum values are tested at TA=25℃.

Table 4-11 Typical current consumption in STOP and PD mode (V_{DD}=5.0V)

Symbol	Parameter	Condition	Typ(1)		Max(2)	Unit
			T_A=25℃	T_A=105℃	T_A=25℃	
I_{DD_STOP}	Current in STOP mode	LSI=32KHz, HCLK off, 3KB SRAM hold, all GPIO status hold, register hold.	2	6.8	5	uA
I_{DD_PD}	Current in PD mode	All functional modules are turned off and support 2-way IO wake-up.	0.9	1.9	1	uA

1. Guaranteed by design and comprehensive evaluation, not tested in production.

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2. Tested in production.

4.3.6 Internal clock source characteristics

The characteristic parameters given in the following table were measured using ambient temperature and supply voltage in accordance with Table 4-4.

4.3.6.1 High-speed internal (HSI) RC oscillator

Table 4-12 HSI Oscillator characteristics (1) (2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI}	Frequency	HSI=48M , V_{DD}=3.3V, T_A = 25℃, After calibration	47.52(3)	48	48.48(3)	MHz
		HSI=40M , V_{DD}=3.3V, T_A = 25℃, After calibration	39.6(3)	40	40.4(3)	MHz
DuCy（HSI）	Duty cycle	-	45	-	55	%
ACC_{HSI}	The temperature drift of the HSI oscillator(4)	V_{DD}=3.3V, T_A = -40~105℃, Temperature drift	-3.5	-	1.5	%
		V_{DD}=3.3V, T_A = -20~85℃, Temperature drift	-2.5	-	1	%
		V_{DD}=3.3V, T_A = 0~70℃, Temperature drift	-1.5	-	1	%
$t_{SU(HSI)}$	HSI startup Time	-	2	-	7	μs
$I_{DD(HSI)}$	HSI power consumption	-	-	250	400	μA

1. Unless otherwise specified, V_{DD} = 3.3V, T_A = -40~105℃.
2. Guaranteed by design, not tested in production.
3. Production calibration accuracy, excluding welding effects. Welding brings about 1% frequency deviation range.
4. Frequency deviation includes the effect of welding, data is from sample testing, not tested in production.

4.3.6.2 Low-speed internal (LSI) RC oscillator

Table 4-13 LSI Oscillator characteristics (1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSI}(2)	Frequency	V_{DD}=3.3V, T_A = 25℃, After calibration	31	32	33	KHz
		V_{DD} =2V ~5.5V, T_A = -40~105℃	26	32	38	KHz
$t_{SU(LSI)}$ (2)	LSI Startup Time		-	30	80	μs
$I_{DD(LSI)}$ (2)	LSI driving current		-	0.3	-	μA

1. Unless otherwise specified, V_{DD} = 3.3V, T_A = -40~105℃.
2. Guaranteed by design, not tested in production.

4.3.7 Low-power mode wake-up time

The wake-up time listed in Table 4-20 is measured during the wake-up phase of an 48MHz HSI RC oscillator. The clock source used when waking up depends on the current operating mode:

- STOP or PD mode: clock source is RC oscillator

The parameter test conditions in the following table are based on Table 4-4.

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Table 4-14 Low-power mode wake-up time

Symbol	Parameter	Typ	Unit
t_{WUSTOP}(1)	Wake up from STOP mode	22	us
t_{WUPD}(1)	Wake up from PD mode	200	us

1. The measurement of the wake-up time is from the start of the wake-up event to the user program reading the first instruction.

4.3.8 FLASH characteristics

Unless otherwise specified, all characteristic parameters are obtained at T_A = -40~105℃.

Table 4-15 FLASH characteristics

Symbol	Parameter	Conditions	Min(1)	Typ(1)	Max(1)	Unit
t_{PROG}	Word programming time(32-bit)	T_A = -40~105℃	144.5	175	185	μs
t_{ERASE}	Page erase time(512Bytes)	T_A = -40~105℃	-	2.27	-	ms
t_{ME}	Mass erase time	T_A = -40~105℃； BOOT UNLOCK	-	70.6	-	ms
		T_A = -40~105℃； BOOT LOCK	-	132.8	-	ms
I_{DD}	Current(1)	Read, f_{HCLK}=48MHz, V_{DD}=3.3V	-	2	2.4	mA
		Write, f_{HCLK}=48MHz, V_{DD}=3.3V	-	-	1.2	mA
		Erase, f_{HCLK}=48MHz, V_{DD}=3.3V	-	-	0.6	mA
		PD/STOP mode, V_{DD}=3.3~3.6V	-	-	150	μA

1. Guaranteed by design, not tested in production.

Table 4-16 Flash endurance and data retention period

Symbol	Parameter	Conditions	Min(1)	Unit
N_{END}	Endurance(Note: erasing and writing cycle)	T_A = -40~105 ℃	100	kcycles
t_{RET}	Data retention	T_A = 105 ℃, after 1000 erasing cycle(1)	10	years

1. Guaranteed by characterization, not tested in production.

4.3.9 Electrical sensitivity

Based on three different tests (ESD, LU), a specific measurement method is used to test the strength of the chip to determine its performance in terms of electrical sensitivity.

Electrostatic discharge (ESD)

Electrostatic discharge (a positive pulse followed by a negative pulse one second later) is applied to all pins of all samples.

Table 4-17 ESD characteristics

Symbol	Parameter	Conditions	Class	Max(1)	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A = +25 ℃, In accordance with MIL-STD-883K Method 3015.9	2	4000	V

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$V_{ESD(CDM)}$	Electrostatic discharge voltage (charged device model)	T_A = +25 ℃, In accordance with ESDA/JEDEC JS-002-2018	II	1000	

1. Guaranteed by characterization, not tested in production.

Staic Latch-up(LU)

To evaluate the locking performance, two complementary static latch-up tests were performed on six samples:

- Supply voltage exceeding limit for each power pin.
- Current is injected into each input, output, and configurable I/O pin.

This test conforms to EIA/JESD78E IC latch standard.

Table 4-18 Static Latch-up characteristics

Symbol	Parameter	Conditions	Class
LU	Static Latch-up	T_A = +105 ℃, conforming to JESD78E	II level A

4.3.10I/O port characteristics

Generic input/output characteristics

The parameter test conditions in the following table are based on Table 4-4. All I/O ports are CMOS and TTL compatible.

Table 4-19 I/O static characteristics

Symbol	Parameter	VDD	Conditions	Min	Max	Unit
V_{IL}	Low level input voltage	5	-	-	0.3×VDD	V
		3.3	-	-	0.8	
		2	-	-	0.2×VDD	
V_{IH}	High level input voltage	5	-	0.7×VDD	-	
		3.3	-	2.0	-	
		2	-	0.8×VDD	-	
V_{hys}	Schmitt trigger voltage hysteresis (1)	5/3.3/2	-	0.1×VDD	-	V
I_{lkg}(2)	Input leakage current IIH	5/3.3/2	-	-	1	µA
	Input leakage current IIL	5/3.3/2	-	-1	-	
V_{OH}	Output high level voltage	5	High driving Imin=16mA low driving Imin=8mA	VDD-0.8	-	V
		3.3	High driving Imin=8mA low driving Imin=4mA	2.4	-	
		2	High driving Imin=4mA low driving Imin=2mA	VDD-0.45	-	
V_{OL}	Output low level voltage	5	High driving Imin=16mA low driving Imin=8mA	-	0.7	
		3.3	High driving Imin=8mA low driving Imin=4mA	-	0.45	
		2	High driving Imin=4mA low driving Imin=2mA	-	0.4	
R_{PU}	Weak pull-up equivalent resistor	5/3.3/2	-	20	100	kΩ
R_{PD}	Weak pull-down equivalent resistor	5/3.3/2	-	20	100	kΩ
C_{IO}	I/O pin capacitance	5/3.3/2	-	-	10	pF

1. The hysteresis voltage of the Schmitt trigger switching level. Guaranteed by characterization, not tested in production.
2. If there is negative current in the adjacent pin, the leakage current may be higher than the maximum value.

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Input and output AC characteristics

The parameter test conditions in the following table are based on Table 4-4.

Table 4-20 I/O AC characteristics

VDD	Conditions			Rise/Fall Time (ns)			Propagation Delay (ns)		
	Driving Strength	Slew Rate Control	CLoading(pf)	Min	Typ	Max	Min	Typ	Max
5V(4.5~5.5)	Low (DR=1)	Slow (SR=1)	25	2.56	3.68	6.01	3.96	5.87	9.57
			50	4.76	6.87	11.3	5.01	7.32	11.8
			100	9.24	12.2	21.9	7.46	10.7	17.1
		Fast (SR=0)	25	2.4	3.47	5.71	3.34	5	8.18
			50	4.66	6.72	11.1	4.56	6.69	10.9
			100	9.19	13.3	21.8	7.02	10.1	16.2
	High (DR=0)	Slow (SR=1)	25	1.59	2.28	3.6	3.56	5.33	8.8
			50	2.54	3.65	5.96	4.16	6.17	10.1
			100	4.7	6.83	11.2	5.22	7.64	12.3
		Fast (SR=0)	25	1.32	1.89	3.05	3	4.57	7.58
			50	2.38	3.44	5.65	3.54	5.3	8.7
			100	4.63	6.66	11	4.57	6.72	10.8
3.3V(2.7~3.6)	Low (DR=1)	Slow (SR=1)	25	3.32	5.02	9.31	4.74	7.32	13.6
			50	6.06	9.23	17.4	6.27	9.57	17.7
			100	11.7	17.9	33.6	9.31	14	25.8
		Fast (SR=0)	25	3.06	4.67	8.79	4.17	6.52	12.2
			50	5.91	9.02	17	5.69	8.75	16.2
			100	11.7	17.8	33.5	8.73	13.2	24.3
	High (DR=0)	Slow (SR=1)	25	2.08	3.16	5.84	3.93	6.12	11.4
			50	3.34	5.05	9.27	4.72	7.3	13.6
			100	5.97	9.16	17.2	6.25	9.54	17.6
		Fast (SR=0)	25	1.75	2.66	4.91	3.41	5.41	10.2
			50	3	4.62	8.67	4.16	6.51	12.2
			100	5.87	8.92	16.8	5.66	8.72	16.2
1.8V(1.62~2)	Low (DR=1)	Slow (SR=1)	25	6.08	10.2	18.1	8.41	14.5	26.6
			50	11	18.4	32.9	11	18.9	34.5
			100	21	35	64	16.3	27.6	49.5
		Fast (SR=0)	25	5.58	9.34	16.7	7.38	12.8	23.7
			50	10.6	17.7	32.3	9.98	17.2	31.6
			100	20.8	34.6	63.5	15.2	25.9	43.7
	High (DR=0)	Slow (SR=1)	25	3.77	6.37	11.4	7.05	12.2	22.5
			50	6.11	10.3	18.2	8.42	14.5	26.6
			100	10.9	18.3	32.7	11.4	18.9	34.5
		Fast (SR=0)	25	3.24	5.49	9.8	6.14	10.7	20
			50	5.61	9.4	16.5	7.41	12.9	23.8
			100	10.6	17.6	32	10	17.2	31.6

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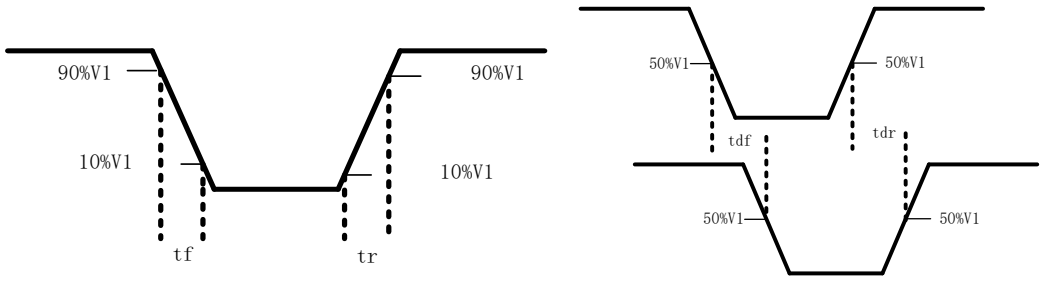
Figure 4-5 I/O AC characteristic definition



4.3.11NRST pin characteristics

NRST pin is integrated with pull-up resistor. Unless otherwise specified, the parameter test conditions in the following table are based on Table 4-4.

Table 4-21 NRST pin characteristics

Symbol	Parameter	VDD	Conditions	Min	Typ	Max	Unit
$V_{IL(NRST)}$(1)	NRST low level input voltage	2V~5.5V	-	-	-	0.3VDD	V
$V_{IH(NRST)}$(1)	NRST high level input voltage	2V~5.5V	-	0.75VDD	-	-	
$V_{hys(NRST)}$	NRST schmitt trigger voltage hysteresis	2V~5.5V	-	115	220	315	mV
$V_{OL(NRST)}$(1)	NRST output low level voltage	5V	High driving Imin=16mA low driving Imin=8mA	-	-	0.7	V
		3.3V	High driving Imin=8mA low driving Imin=4mA	-	-	0.45	
		2V	High driving Imin=4mA low driving Imin=2mA	-	-	0.4	
$V_{OH(NRST)}$(1)	NRST output high level voltage	5V	High driving Imin=16mA low driving Imin=8mA	VDD-0.8	-	-	
		3.3V	High driving Imin=8mA low driving Imin=4mA	2.4	-	-	
		2V	High driving Imin=4mA low driving Imin=2mA	VDD-0.45	-	-	
R_{PU}	Weak pull-up equivalent resistor (2)	2V~5.5V	-	30	60	70	kΩ
$V_{F(NRST)}$(1)	NRST input filter pulse	2V	-	-	-	100	ns
		3V~3.6V	-	-	-	100	
		4.5V~5.5V	-	-	-	50	
$V_{NF(NRST)}$(1)	NRST input unfiltered pulse	2V	-	650	-	-	ns
		3V~3.6V	-	300	-	-	
		4.5V~5.5V	-	200	-	-	

1. Guaranteed by design, note tested in production
2. The pull-up resistor is designed as true resistor for a not switchable PMOS implementation, The resistance of this PMOS switch is very small (about 10%).

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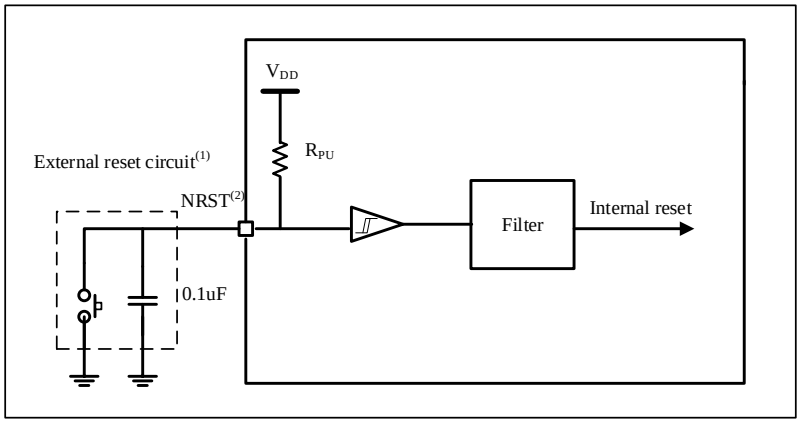
Figure 4-6 NRST pin protection recommended circuit design



1. The reset network is to prevent parasitic reset.
2. The user must ensure that the potential of the NRST pin can be lower than the maximum $V_{IL\ (NRST)}$, otherwise the MCU cannot be reset.

4.3.12 TIM characteristics

The parameters listed are guaranteed by design.

Table 4-22 TIMx (1) characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{res(TIM)}$	Timer resolution time	-	1	-	$t_{TIMxCLK}$
		$f_{TIMxCLK}$= 48MHz	20.8	-	ns
f_{EXT} (2)	Timer external clock frequency on CH1 to CH4	-	0	$f_{TIMxCLK}/2$	MHz
		$f_{TIMxCLK}$= 48MHz	0	24	MHz
Res_{TIM}	Timer resolution	-	-	16	Bits
$t_{COUNTER}$	Select the internal clock, 16-bit counter clock cycle	-	1	65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$= 48MHz	0.0208	1365	µs
t_{MAX_COUNT}	Maximum count	-	-	65536x65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$= 48MHz	-	89.478	s

1. x can be 1, 3, 6.
2. TIM1 is CH1~CH4, TIM3 is CH1~CH2, TIM6 is not applicable

4.3.13 IWDG characteristics

Table 4-23 IWDG counting maximum and minimum reset time (LSI = 32KHz)

Prescaler	IWDG_PREDIV.PD[2:0]	Min(1) IWDG_RELV.REL[11:0]=0	Max(1) IWDG_RELV.REL[11:0]=0xFFF	Unit
/4	000	0.125	512	ms
/8	001	0.25	1024	
/16	010	0.5	2048	
/32	011	1	4096	
/64	100	2	8192	
/128	101	4	16384	
/256	11x	8	32768	

1. Guaranteed by design, not tested in production.

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4.3.14I2C characteristics

Unless otherwise specified, the parameters use ambient temperature, f_{PCLK} frequency, and V_{DD} supply voltage in accordance with Table 4-4.

The I^2C interface of the N32G003 product conforms to the standard I^2C communication protocol, but has the following limitations: SDA and SCL are not "true" open leak pins, and when configured for open leak output, the PMOS tube between the pin and V_{DD} is closed, but still exists.

I^2C interface features are are shown in the following table. See Section 4.3.10 for details about the features of the input/output multiplexing function pins (SDA and SCL).

Table 4-24 I2C interface characteristics

Symbol	Parameter	Standard model		Fast mode		Fast+ mode		Unit
		Min	Max	Min	Max	Min	Max	
f_{SCL}	I2C interface frequency	0	100	0	400	0	1000	KHz
$t_{h(STA)}$	Start condition holding time(1)	4.0	-	0.6	-	0.26	-	μs
$t_{w(SCLL)}$	SCL clock low time(1)	4.7	-	1.3	-	0.5	-	μs
$t_{w(SCLH)}$	SCL clock high time(1)	4.0	-	0.6	-	0.26	-	μs
$t_{su(STA)}$	Setup time of repeated starting conditions(1)	4.7	-	0.6	-	0.26	-	μs
$t_{h(SDA)}$	SDA data hold time(1)	-	3.4	-	0.9	-	0.4	μs
$t_{su(SDA)}$	SDA setup time(1)	250	-	100	-	50	-	ns
$t_{r(SDA)}$ $t_{r(SCL)}$	SDA and SCL rising time(1)	-	1000	20+0.1Cb	300	-	120	ns
$t_{f(SDA)}$ $t_{f(SCL)}$	SDA and SCL falling time(1)	-	300	20+0.1Cb	300	-	120	ns
$t_{su(STO)}$	Stop condition setup time(1)	4.0	-	0.6	-	0.26	-	μs
$t_{w(STO:STA)}$	Time from stop condition to start condition (bus idle) (1)	4.7	-	1.3	-	0.5	-	μs
C_b	Capacity load per bus (1)	-	400	-	400	-	200	pf
t_{SP}	Spike width suppressed by analog filters in standard and fast modes	0	35	0	35	0	35	ns
$t_{v(SDA)}$	Data validity time(1)	3.45	-	0.9	-	0.45	-	μs
$t_{v\ (ACK)}$	Response validity time (1)	3.45	-	0.9	-	0.45	-	μs

1. Guaranteed by design, not tested in production.
2. To achieve the maximum frequency of standard mode I2C, f_{PCLK} must be greater than 2MHz.To achieve the maximum frequency of fast mode I2C, f_{PCLK} must be greater than 4MHz.

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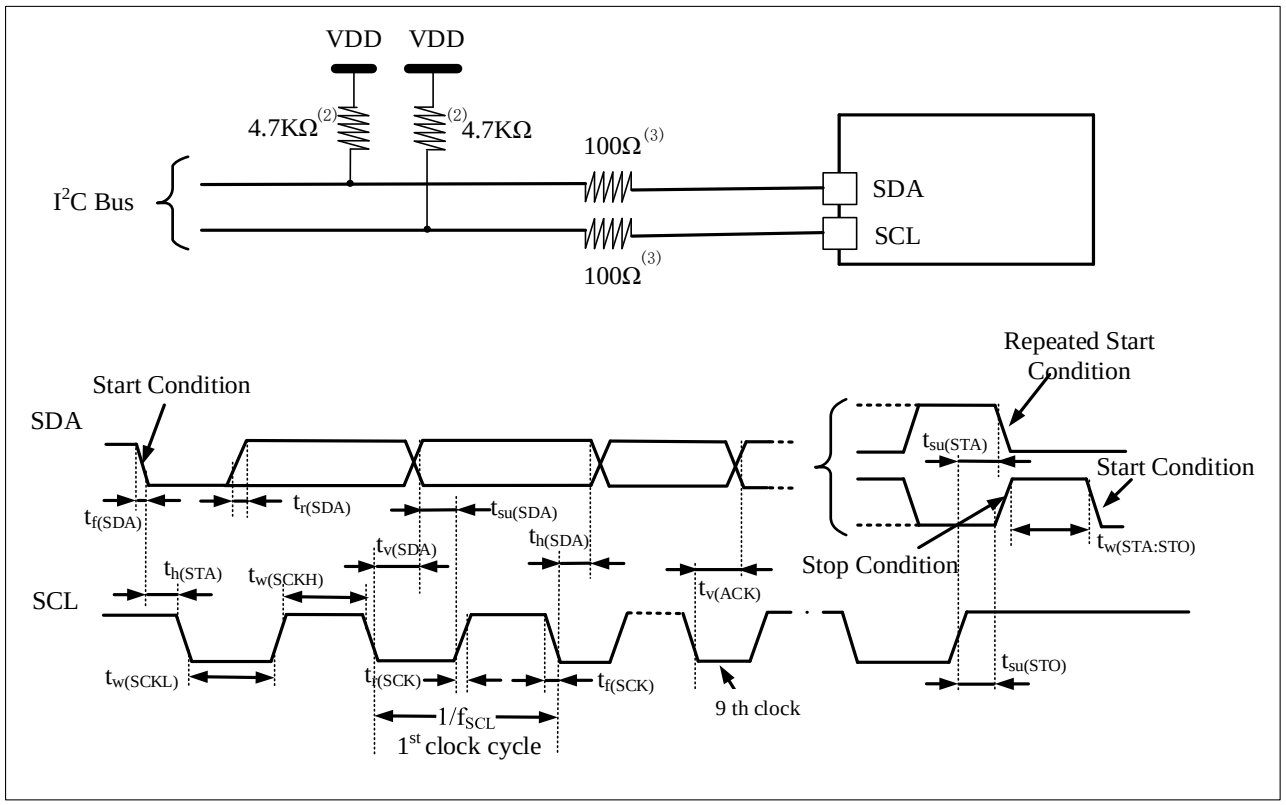
Figure 4-7 I2C bus AC waveform and measurement circuit (1)



1. The measuring point is set at $0.3V_{DD}$ and $0.7V_{DD}$.
2. The pull-up resistance depends on the I2C interface speed.
3. The resistance value depends on the actual electrical characteristics. The signal line can be directly connected without serial resistance..

4.3.15SPI characteristics

Unless otherwise specified, the parameters use ambient temperature, f_{PCLK} frequency, and V_{DD} supply voltage in accordance with Table 4-4.

See Section 4.3.10 for details about the features of the input/output multiplexing function pins (NSS, SCLK, MOSI, MISO)

Table 4-25 SPI characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
f_{SCLK} $1/t_{c(SCLK)}$	SPI clock frequency	Master mode	-	12	MHz
		Slave mode	-	12	
$t_{r(SCLK)}t_{f(SCLK)}$	SPI clock rising and falling time	Load capacitance: C = 30pF	-	15	ns
DuCy(SCLK)	SPI slave input clock duty cycle	SPI Slave mode	30	70	%
$t_{su(NSS)}$ (1)	NSS setup time	Slave mode	$4t_{PCLK}$	-	ns
$t_{h(NSS)}$(1)	NSS hold time	Slave mode	$2t_{PCLK}$	-	ns
$t_{w(SCLKH)}$(1) $t_{w(SCLKL)}$(1)	SCLK high and low time	Master mode	t_{PCLK}	t_{PCLK} + 2	ns
$t_{su(MI)}$(1)	Data entry setup time	Master mode	5	-	ns
$t_{su(SI)}$(1)		Slave mode	5	-	

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$t_{h(MI)}$(1)	Data entry hold time	Master mode	5	-	ns
$t_{h(SI)}$(1)		Slave mode	4	-	
$t_{a(SO)}$(1)(2)	Data output access time	Slave mode	0	$3t_{PCLK}$	ns
$t_{dis(SO)}$(1)(3)	Disabled time for data output	Slave mode	2	10	ns
$t_{v(SO)}$(1)	Valid time of data output	Slave mode (after the enabled edge)	-	5	ns
$t_{v(MO)}$(1)		Master mode (after the enabled edge)	-	5	
$t_{h(SO)}$(1)	Data output hold time	Slave mode (after the enabled edge)	15	-	ns
$t_{h(MO)}$(1)		Master mode (after the enabled edge)	2	-	

1. Guaranteed by design, not tested in production.
2. The minimum value means the minimum time to drive the output, and the maximum value means the maximum time to get the data correctly.
3. The minimum value means the minimum time to turn off the output, and the maximum value means the maximum time to put the data wire in the high resistance state.

Figure 4-8 SPI sequence diagram - slave mode and CLKPHA=0

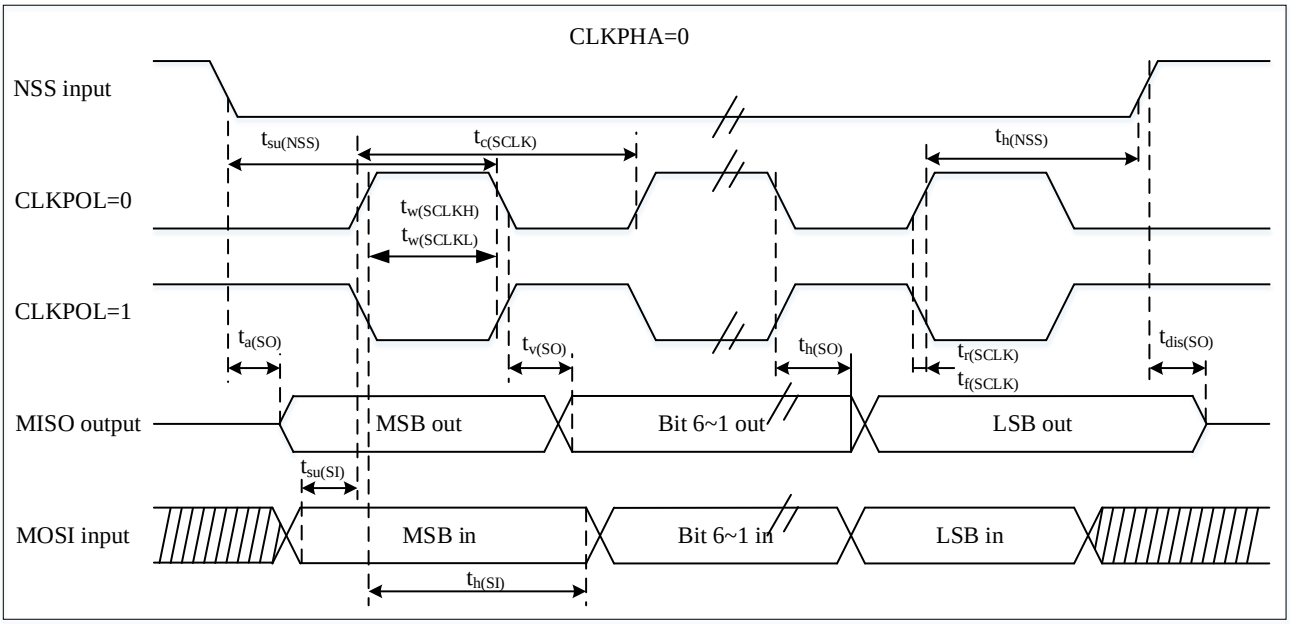

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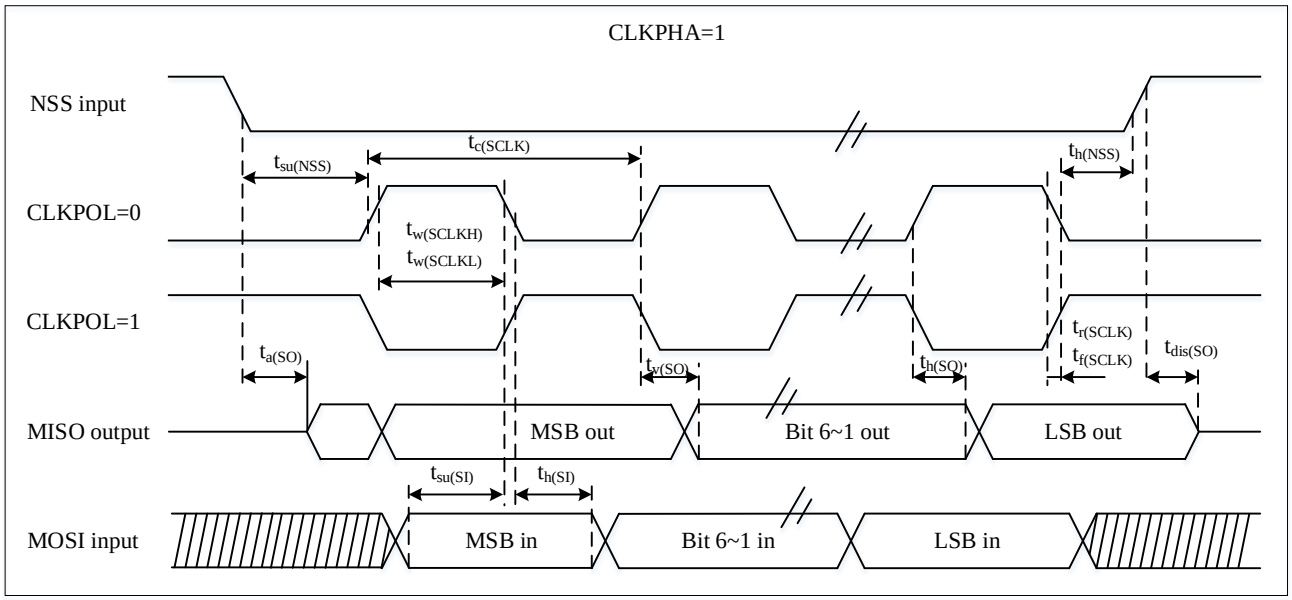
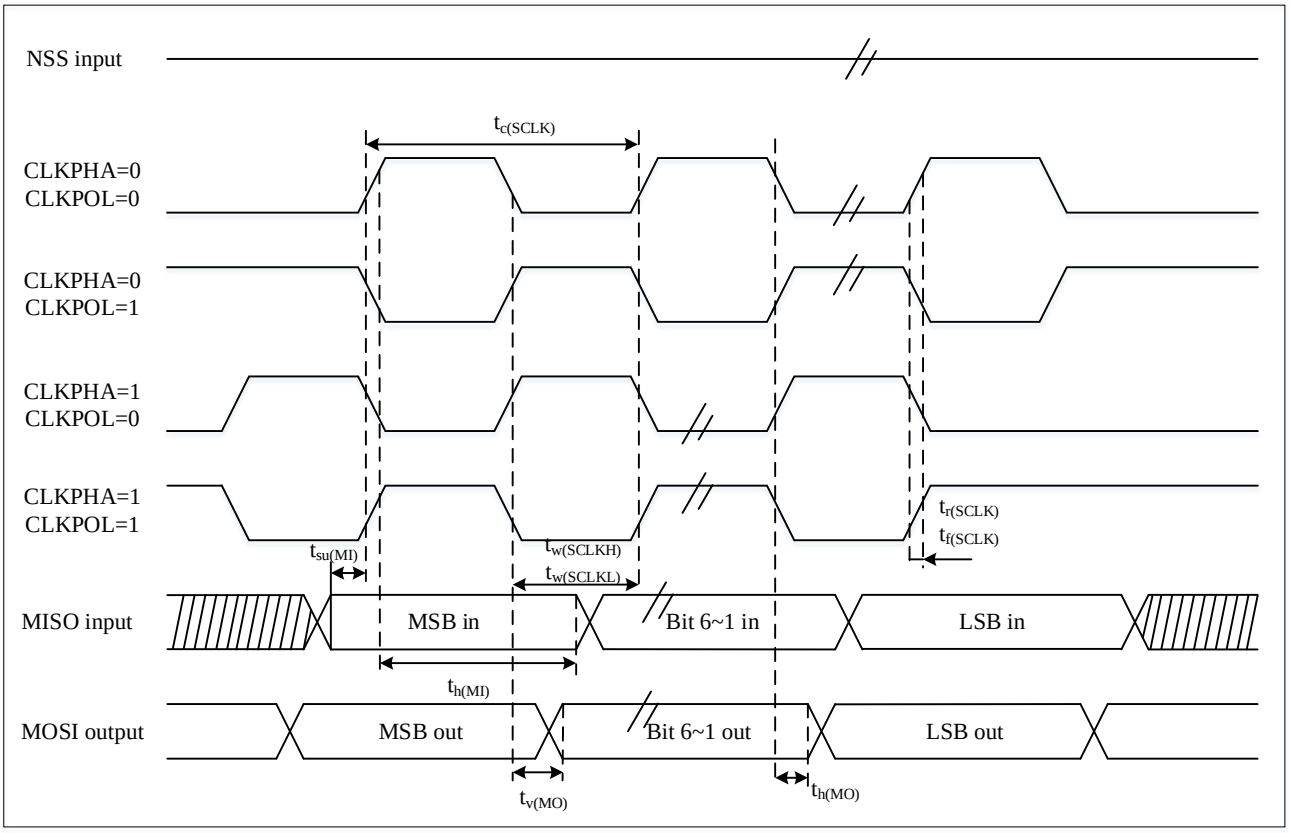
Figure 4-9 SPI sequence diagram - slave mode and CLKPHA=1(1)



1. The measurement points were set at the CMOS level of 0.3 V_{DD} and 0.7 V_{DD}.

Figure 4-10 SPI timing diagram-master mode (1)



1. The measurement points are set at CMOS level: 0.3 V_{DD} and 0.7 V_{DD}.

4.3.16ADC electrical parameters

Unless otherwise specified, following table parameters are measured using ambient temperature, f_{HCLK} frequency, and V_{DD} supply voltage in accordance with the conditions in Table 4-4.

Note: It is recommended to perform a calibration at each power-on.

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Table 4-26 ADC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DD}(1)	Supply voltage	-	2.4	-	5.5	V
V_{REF+}	Positive reference voltage	-	V_{DD}			V
f_{ADC}	ADC clock frequency	-	-	-	24	MHz
f_s(1)	Sampling rate	-	0.03	-	1	Msps
V_{AIN}	Conversion voltage range	-	0	-	V_{REF+}	V
R_{AIN}(1)	External input impedance	-	See formula 1			Ω
R_{ADC}(1)	ADC input resistance	V_{DD} =3.3 V	600	750	975	Ω
		V_{DD} =5.0V	360	450	585	Ω
C_{ADC}(1)	Internal sample and hold capacitor	-	22	26	30	pF
SNDR	Signal noise distortion ration	V_{DD} =3.3V	57	58.5	73	dB
		V_{DD} =5.0V	57.7	58.9	74	dB
T_S(1)	Sampling cycle	-	8	-	3034	$1/f_{ADC}$
t_{STAB}(1)	Power-on time	-	32	-	-	$1/f_{ADC}$
t_{CONV}(1)	Conversion time	-	12			$1/f_{ADC}$
I_{ADC}	ADC current consumption	-	-	1.67	6	mA

1. Guaranteed by design, not tested in production.

Formula 1: Maximum R_{AIN} formula

$$R_{AIN} < \frac{T_S}{f_{ADC} \times C_{ADC} \times \ln(2^{N+2})} - R_{ADC}$$

The above formula (Formula 1) is used to determine the maximum external impedance so that the error can be less than 1/4 LSB. Where N=12 (representing 12-bit resolution).

Table 4-27 ADC sampling time(V_{DD} = 3.3V) 1)

Resolution	Rin（kΩ）	Minimum sampling time (ns)
12-bit	1	500
	1.2	583
	2	833
	3.6	1250
	8.26	2333
	10	3000
	18	5000
	26.9	7583
	35.9	10000
	61.9	15833

1. Guaranteed by design, not tested in production.

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Table 4-28 ADC sampling time (V_{DD} = 5.0V) (1)

Resolution	Rin（kΩ）	Minimum sampling time (ns)
12-bit	0.6	500
	0.9	583
	1.9	833
	3.5	1250
	7.8	2333
	10.5	3000
	18.4	5000
	28.6	7583
	38.2	10000
	61.3	15833

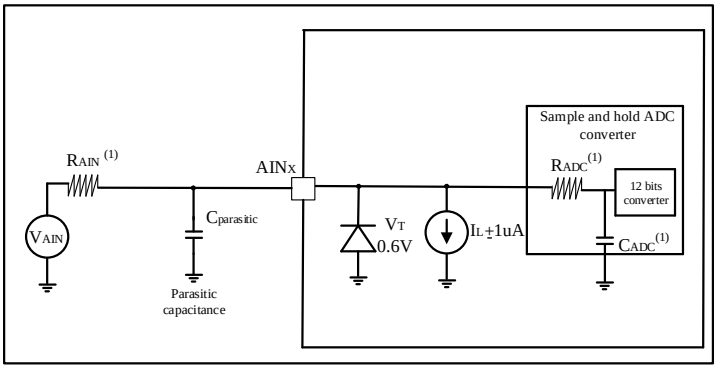
1. Guaranteed by design, not tested in production.

Table 4-29 ADC accuracy - limited test conditions (1)

Symbol	Parameter	Conditions	Typ	Max(2)	Unit
EG	Gain error	V_{REF+} = 3.3V, T_A = 25 ℃, sample rate = 1MSPS, Vin = 0.05V_{DDA} ~ 0.95V_{DDA}	±2	±5	LSB
EO	Offset error		±2	-	
ED	Differential linearity error		±0.6	±2.3	
EL	Integral linearity error		±1.5	±3.69	
ENOB	Effective number of bits		10.3	-	Bits
EG	Gain error	V_{REF+} = 5.0V, T_A = 25 ℃, sample rate = 1MSPS, Vin = 0.05V_{DDA} ~ 0.95V_{DDA}	±2	±5	LSB
EO	Offset error		±2	-	
ED	Differential linearity error		±0.6	±2.2	
EL	Integral linearity error		±1.5	±3.3	
ENOB	Effective number of bits		10.4	-	Bits

1. The relationship between the negative injection current and ADC accuracy: the need to avoid negative current is injected on any standard analog input pin, as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (between the pin and ground) on the standard analog pin that may produce negative injection current.
2. Guaranteed by characterization, not tested in production.

Figure 4-11 ADC typical connection diagram



1. For values of R_{AIN}, R_{ADC}, and C_{ADC}, see Table 4-26.
2. Cparasitic indicates parasitic capacitance on PCB (related to welding and PCB layout quality) and pads (approximately 7pF).A larger Cparasitic value would reduce the accuracy of the conversion and the solution was to reduce f_{ADC}.

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4.3.17COMP characteristics

Unless otherwise specified, following table parameters are measured using ambient temperature, f_{HCLK} frequency, and V_{DD} supply voltage in accordance with the conditions in Table 4-4.

Table 4-30 COMP characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DD}	Analog Supply voltage	Normal mode		2.4	-	5.5	V
		With subtractor mode		2.4	-	5.5	
V_{IN}	Input voltage range	VIN		0	-	VDD	
		VIN - 100mV/200mV/300mV		500	-	VDD-200	mV
t_{START}(1)	Comparator start setup time	Normal mode		-	-	5	us
		With subtractor mode		-	-	15	
t_d	Propagation delay for 200mV step with 100mV overdrive	Falling edge		-	304	-	ns
		Rising edge		-	268	-	
V_{OFFSET}	Comparator input offset error	VIN		-	±4	±15	mV
		VIN - 100mV		-	±20	±50	
		VIN - 200mV		-	±20	±50	
		VIN - 300mV		-	±20	±50	
V_{hys}	Comparator hysteresis	No hysteresis		-	0	-	mV
		Low hysteresis		-	10	-	
		Medium hysteresis		-	20	-	
		High hysteresis		-	30	40	
I_{DD}	Comparator current consumption	Normal mode	Static	-	-	50	µA
			With 50kHz ±100 mV overdrive square signal	-	-	50	
		With subtractor mode	Static	-	-	500	
			With 50 kHz ±100 mV overdrive square signal	-	-	500	

1. Guaranteed by design, not tested in production.

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5 Package Information

5.1 QFN20

Figure 5-1 QFN20 package outline

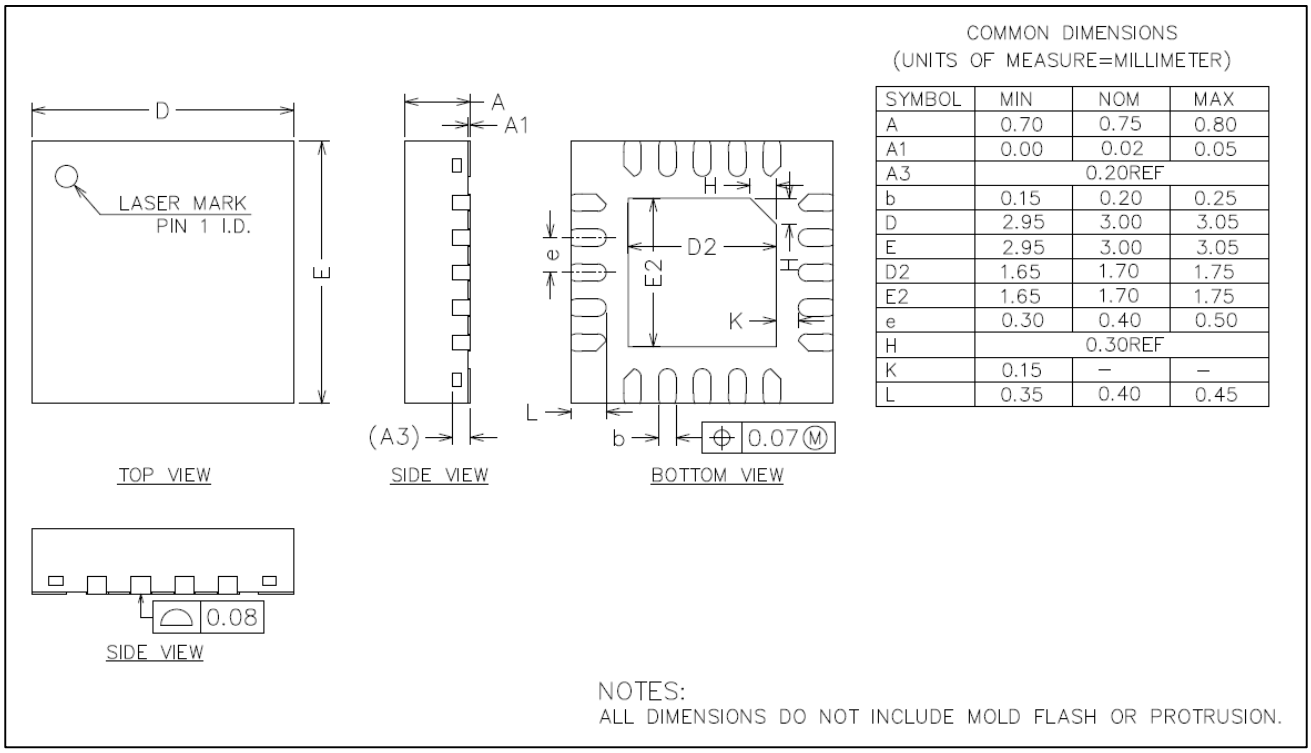
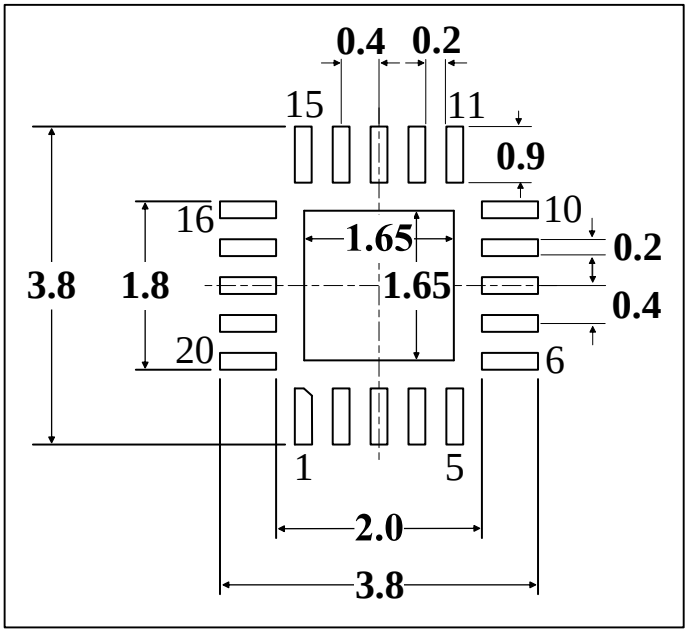


Figure 5-2 QFN20 Recommended Footprint(1)



1. Dimensions are expressed in millimeters

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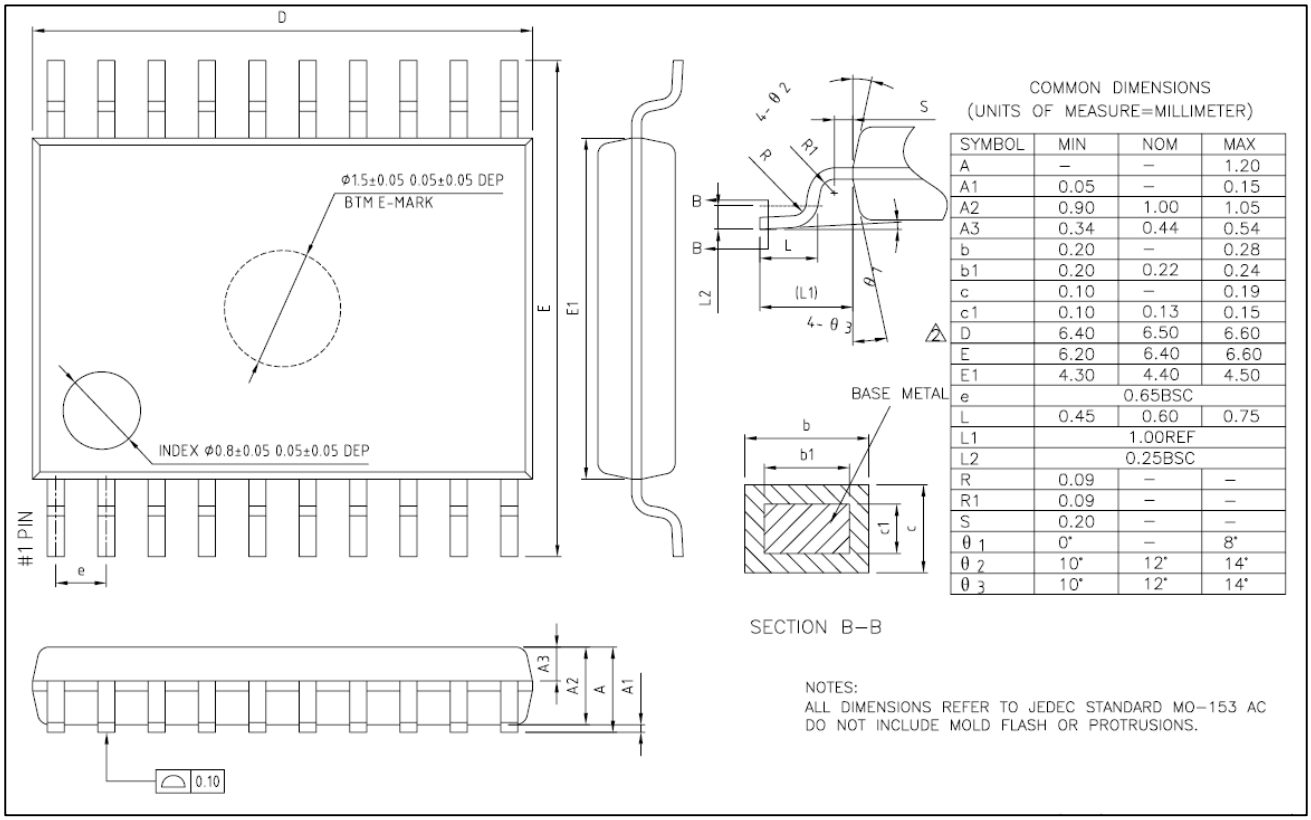
5.2 TSSOP20/TSSOP20-1

Figure 5-3 TSSOP20/TSSOP20-1 package outline

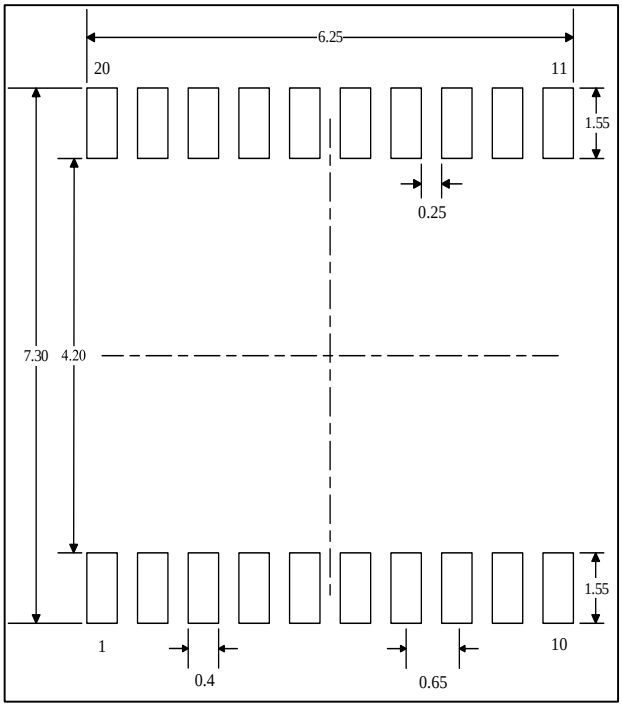


COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	–	–	1.20
A1	0.05	–	0.15
A2	0.90	1.00	1.05
A3	0.34	0.44	0.54
b	0.20	–	0.28
b1	0.20	0.22	0.24
c	0.10	–	0.19
c1	0.10	0.13	0.15
D	6.40	6.50	6.60
E	6.20	6.40	6.60
E1	4.30	4.40	4.50
e		0.65BSC	
L	0.45	0.60	0.75
L1		1.00REF	
L2		0.25BSC	
R	0.09	–	–
R1	0.09	–	–
S	0.20	–	–
θ 1	0°	–	8°
θ 2	10°	12°	14°
θ 3	10°	12°	14°

NOTES:
ALL DIMENSIONS REFER TO JEDEC STANDARD MO-153 AC
DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.

Figure 5-4 TSSOP20/TSSOP20-1 Recommended Footprint(1)



1. Dimensions are expressed in millimeters

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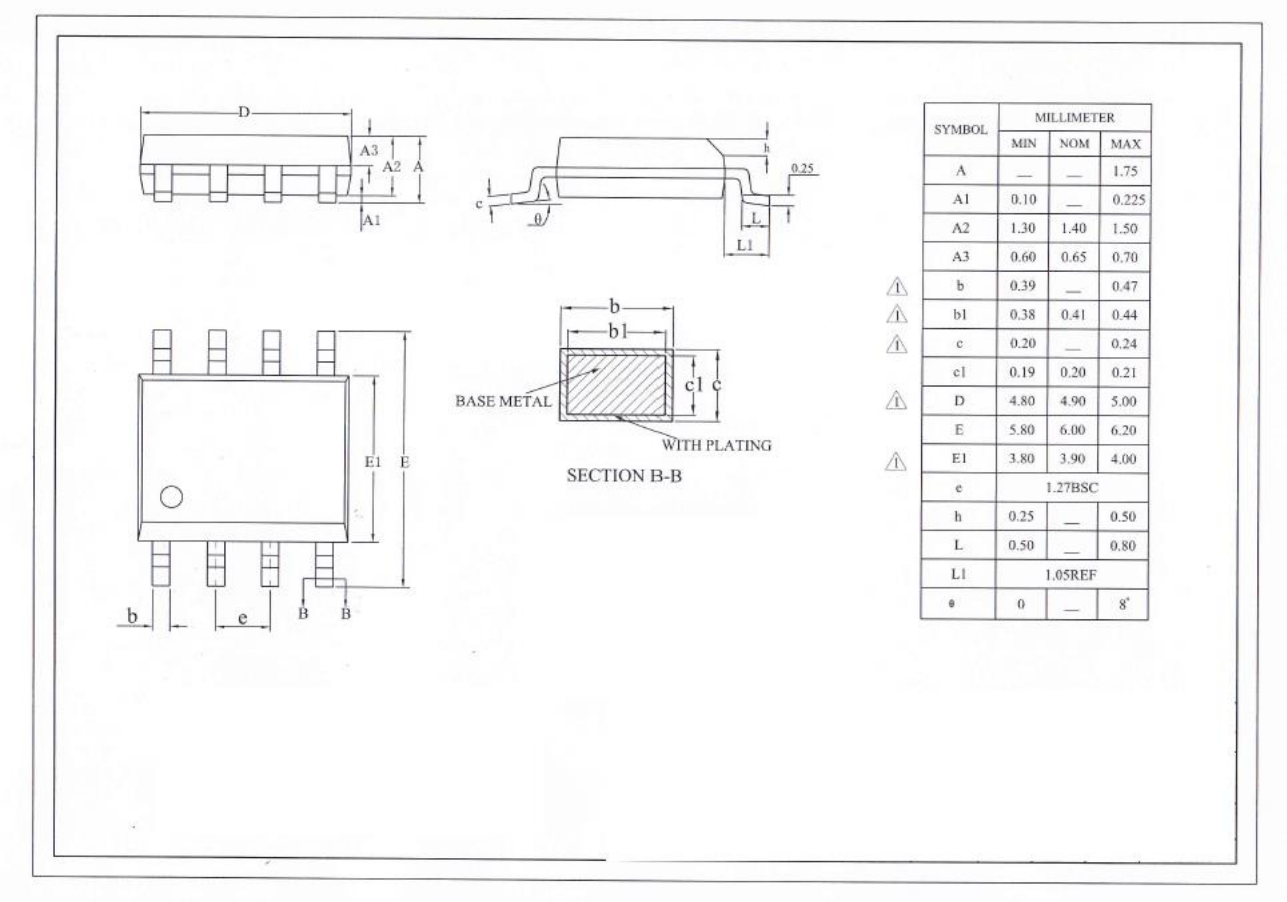
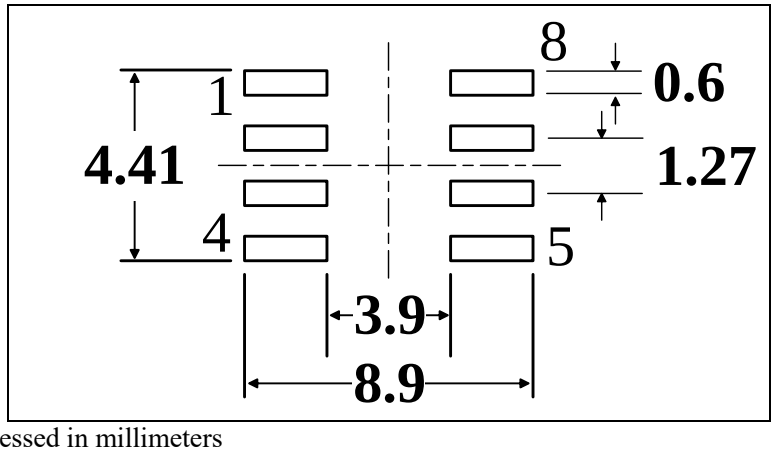
5.3 SOP8

Figure 5-5 SOP8 package outline



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.75
A1	0.10	—	0.225
A2	1.30	1.40	1.50
A3	0.60	0.65	0.70
b	0.39	—	0.47
b1	0.38	0.41	0.44
c	0.20	—	0.24
c1	0.19	0.20	0.21
D	4.80	4.90	5.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	1.27BSC		
h	0.25	—	0.50
L	0.50	—	0.80
L1	1.05REF		
θ	0	—	8°

Figure 5-6 SOP8 Recommended Footprint(1)



1. Dimensions are expressed in millimeters

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5.4 Marking Information

Figure 5-7 QFN20 Marking information

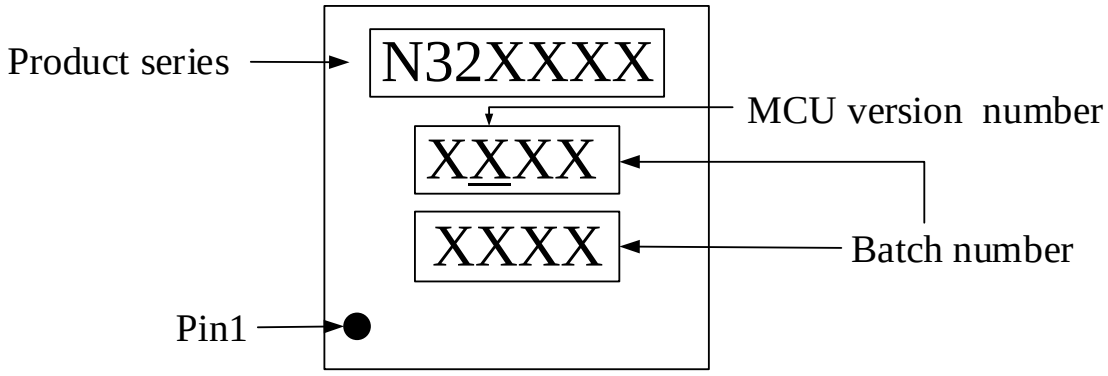


Figure 5-8 TSSOP20 Marking information

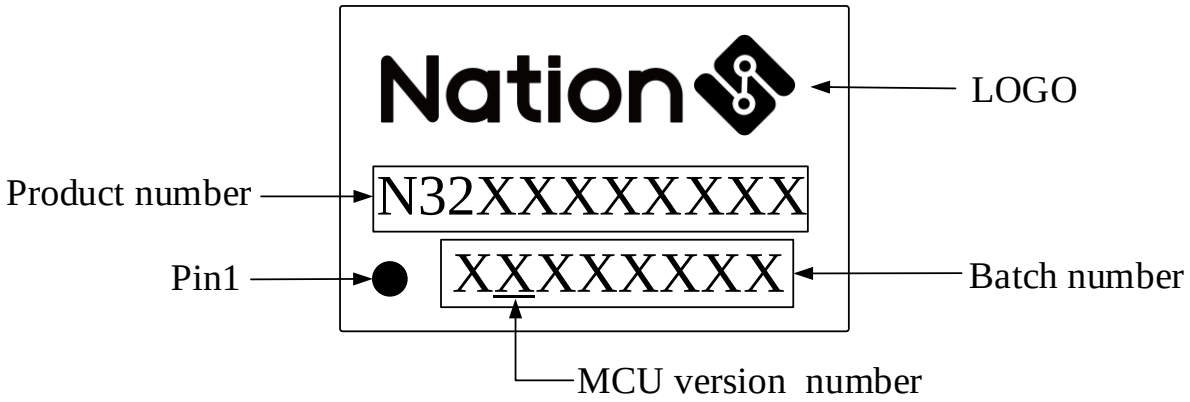
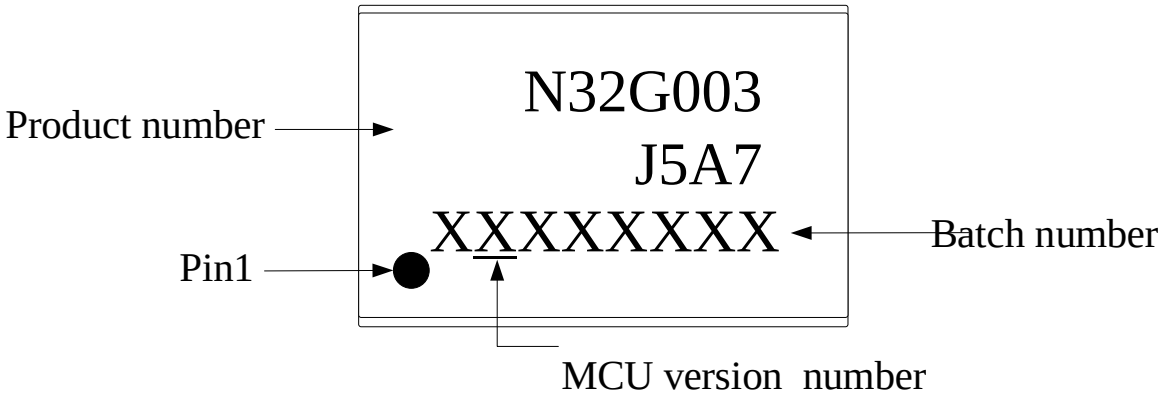


Figure 5-9 SOP8 Marking information



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6 Ordering Information

Figure 6-1 N32G003 Series Part Number Information

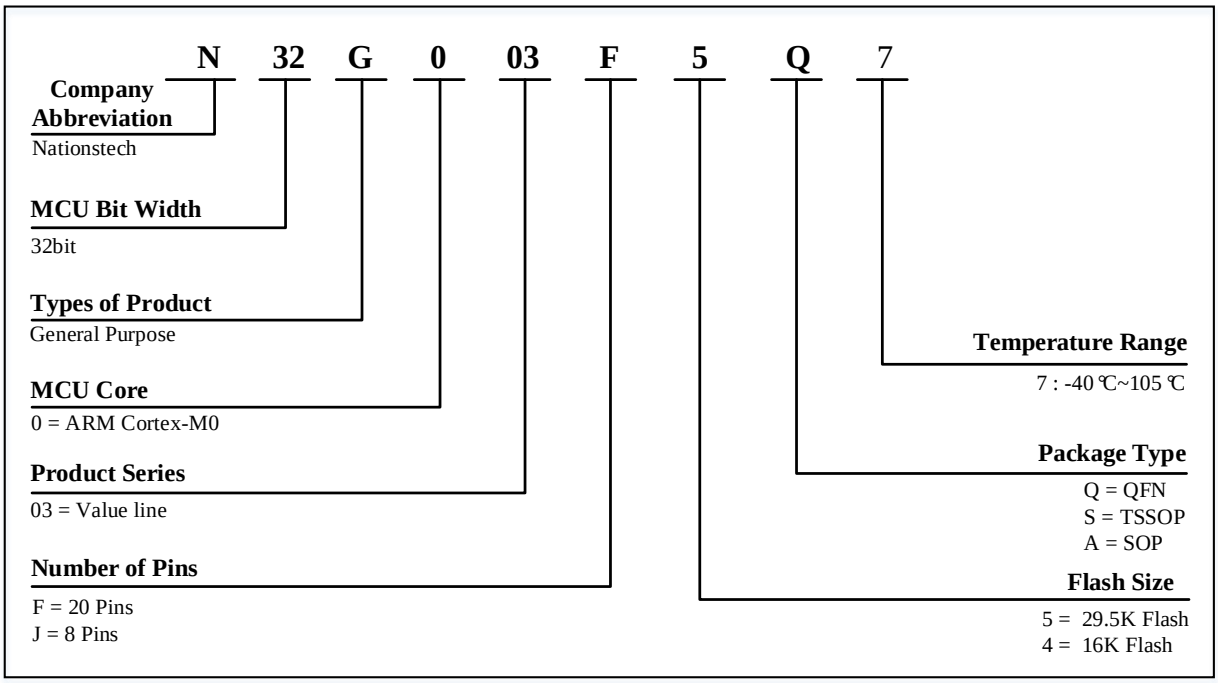

Table 6-1 N32G003 Series Ordering Code

Ordering Code[1]	Package	Size	Packaging[2]	SPQ[3]	Temperature range
N32G003F5S7	TSSOP20	6.5mm x 4.4mm	Tube	70	-40℃～105℃
N32G003F5S7-1	TSSOP20-1	6.5mm x 4.4mm	Tube	70	-40℃～105℃
N32G003F5Q7	QFN20	3mm x 3mm	Tray	490	-40℃～105℃
N32G003F4S7	TSSOP20	6.5mm x 4.4mm	Tube	70	-40℃～105℃
N32G003F4Q7	QFN20	3mm x 3mm	Tray	490	-40℃～105℃
N32G003J5A7	SOP8	4.9mm x 3.9mm	Tube	100	-40℃～105℃

1. For the latest detailed-ordering information, please refer to the Selection Guide.
2. The packaging provided is the basic packaging. If user has any other requirements, please contact Naitons.
3. Minimum packaging quantity.

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7 Version history

Date	Version	Remark
2022.10.26	V1.0	Initial release
2023.7.14	V1.1.0	1. PA9 adds UART2_RX multiplexing function 2. Added N32G003F4S7\N32G003F4Q7 model chips 3. Modified Table 4-6,Table 4-28 data
2025.1.7	V1.2.0	1. Modified Table 4-11,Table 4-27 data
2025.6.20	V1.2.1	1. Add pad drawing, modify order code information, modify silkscreen description, update package outline drawing
2026.3.2	V1.3.0	1. Add N32G003J5A7 and N32G003F5S7-1 2. Modify electrical data parameters.

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