N32G033 series

32-bit ARM Cortex®-M0 microcontroller

User manual V1.2.0

Contents

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1 Abbreviations In The Text

1.1 Describes The List Of Abbreviations Used In The Register Table

The following abbreviations are used in the description of registers:

read/write(rw)	Software can read and write this bit.
read-only(r)	Software can only read this bit.
write-only(w)	Software can only write this bit, and reading this bit will return the reset value.
read/clear(rc_w1)	Software can read this bit or clear it by writing' 1', and writing' 0' has no effect on this bit.
read/clear(rc_w0)	Software can read this bit or clear it by writing' 0', and writing' 1' has no effect on this bit.
read/clear by read(rc_r)	Software can read this bit. Reading this bit will automatically clear it to' 0'. Writing' 0' has no effect on this bit.
read/set(rs)	Software can read or set this bit. Writing' 0' has no effect on this bit.
read-only write trigger(rt_w)	Software can read this bit and write' 0' or' 1' to trigger an event, but it has no effect on this bit value.
read-write, automatic clear(rw1_ac)	Read-Write, automatic clear this bit: Writing '1' to wait for the operation to complete will automatically clear the bit. Writing' 0' has no effect on this bit..
toggle(t)	Software can only flip this bit by writing' 1', and writing' 0' has no effect on this bit.
Reserved(Res.)	Reserved bits, the default value must be kept unchanged.

1.2 Available Peripherals

For all models of N32G033 microcontroller series, the existence and number of a peripheral, please refer to the data sheet of the corresponding model.

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2 Memory and Bus Architecture

2.1 System Architecture

2.1.1 Bus Architecture

The main system consists of the following parts:

- Two main drive units:
  - Cortex®-M0 core system bus
  - General purpose DMA
- Five passive units
  - Embedded SRAM
  - Embedded Flash memory
  - ADC
  - AHB to AHB bridge, it connects some AHB devices
  - AHB to APB bridges (AHB2APB), which connect all APB devices

These are connected to each other through a multi-level AHB bus architecture, as shown in Figure 2-1:

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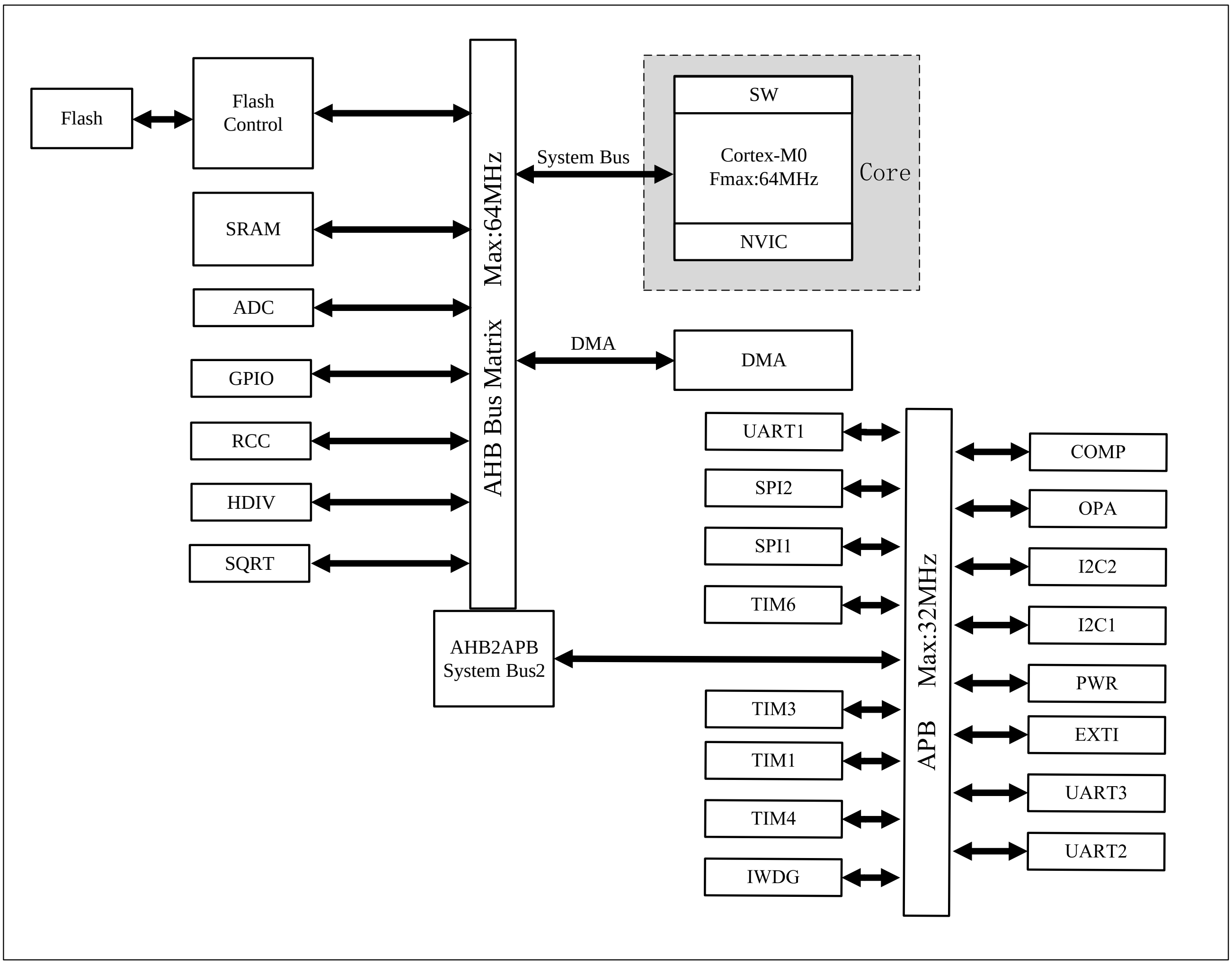
Figure 2-1 Bus Architecture



- CPU System bus: It connects the kernel Sbus of the Cortex®-M0 to bus matrix, and is used for instruction pre-fetch, data loading (constant loading and debug access) and AHB/APB peripheral access.
- DMA bus: The DMA's AHB master interface is connected to the bus matrix, which coordinates access from the kernel and DMA to SRAM, Flash and peripherals.
- The bus matrix coordinates access arbitration between the kernel system bus and the DMA master bus. The arbitration uses a Round Robin algorithm.
- The system consists of one AHB2APB Bridges. APB1 contains 17 APB peripherals and the maximum speed of PCLK is 32MHz.

2.1.2 Bus Address Mapping

The address mapping includes all AHB and APB peripherals, Flash, SRAM, System Memory, etc. The specific mapping is as follows:

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Figure 2-2 Bus Address Map

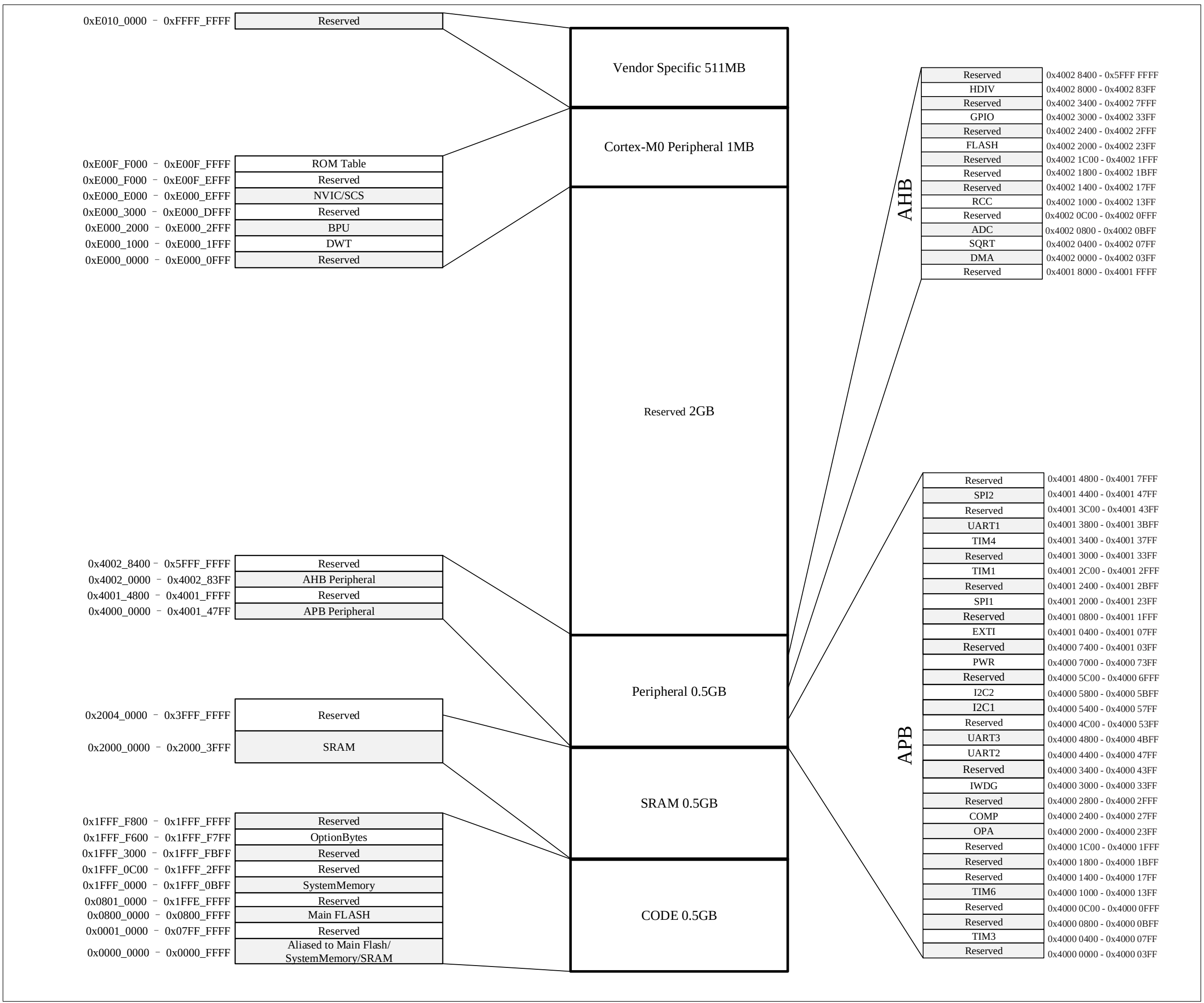

Table 2-1 List of Peripheral Register Addresses

Address Range	Peripheral	Bus
0x4002 8000 - 0x5FFF FFFF	Reserved	AHB
0x4002 8000 - 0x4002 83FF	HDIV	
0x4002 3400 - 0x4002 7FFF	Reserved	
0x4002 3000 - 0x4002 33FF	IOM	
0x4002 2400 - 0x4002 2FFF	Reserved	
0x4002 2000 - 0x4002 23FF	FLASH	
0x4002 1400 - 0x4002 1FFF	Reserved	
0x4002 1000 - 0x4002 13FF	RCC	
0x4002 0C00 - 0x4002 0FFF	Reserved	
0x4002 0800 - 0x4002 0BFF	ADC	
0x4002 0400 - 0x4002 07FF	SQRT	
0x4002 0000 - 0x4002 03FF	DMA	

Address Range	Peripheral	Bus
0x4001 8000 - 0x4001 FFFF	Reserved	
0x4000 0000 - 0x4000 03FF	Reserved	APB
0x4000 0400 - 0x4000 07FF	TIM3	
0x4000 0800 - 0x4000 0BFF	Reserved	
0x4000 0C00 - 0x4000 0FFF	Reserved	
0x4000 1000 - 0x4000 13FF	TIM6	
0x4000 1400 - 0x4000 17FF	Reserved	
0x4000 1800 - 0x4000 1BFF	Reserved	
0x4000 1C00 - 0x4000 1FFF	Reserved	
0x4000 2000 - 0x4000 23FF	OPA	
0x4000 2400 - 0x4000 27FF	COMP	
0x4000 2800 - 0x4000 2FFF	Reserved	
0x4000 3000 - 0x4000 33FF	IWDG	
0x4000 3400 - 0x4000 43FF	Reserved	
0x4000 4400 - 0x4000 47FF	UART2	
0x4000 4800 - 0x4000 4BFF	UART3	
0x4000 4C00 - 0x4000 53FF	Reserved	
0x4000 5400 - 0x4000 57FF	I2C1	
0x4000 5800 - 0x4000 5BFF	I2C2	
0x4000 5C00 - 0x4000 6FFF	Reserved	
0x4000 7000 - 0x4000 73FF	PWR	
0x4000 7400 - 0x4001 03FF	Reserved	
0x4001 0400 - 0x4001 07FF	EXTI	
0x4001 0800 - 0x4001 1FFF	Reserved	
0x4001 2000 - 0x4001 23FF	SPI1	
0x4001 2400 - 0x4001 2BFF	Reserved	
0x4001 2C00 - 0x4001 2FFF	TIM1	
0x4001 3000 - 0x4001 33FF	Reserved	
0x4001 3400 - 0x4001 37FF	TIM4	
0x4001 3800 - 0x4001 3BFF	UART1	
0x4001 3C00 - 0x4001 43FF	Reserved	
0x4001 4400 - 0x4001 47FF	SPI2	
0x4001 4800 - 0x4001 7FFF	Reserved	

2.1.3 Boot Management

2.1.3.1 Boot address

During system startup, you can select the BOOT mode after the reset through the BOOT0 pin and the user option byte BOOT configuration. The value of the BOOT pin will be re-sampled after the system is reset or exits from the Power Down

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mode. After a startup delay has elapsed, the CPU fetches the top-of-stack value from address 0x0000_0000 and executes the code from the reset vector address indicated by address 0x0000_0004. Because of the Cortex®-M0 always gets the top-of-stack value and reset vector from addresses 0x0000_0000 and 0x0000_0004, so boot is only suitable for booting from the CODE area, and address remapping is designed for boot space. There are three boot modes to choose from:

- Boot from Main Flash:
  - Main Flash memory is mapped to the boot space (0x0000_0000);
  - Main Flash memory is accessible in two address areas, 0x0000_0000 or 0x0800_0000;
- Boot from System Memory:
  - System Memory is mapped to boot space (0x0000_0000);
  - System Memory can be accessed in two address areas, 0x0000_0000 or 0x1FFF_0000;
- Boot from the embedded SRAM:
  - The embedded SRAM is mapped to boot space (0x0000_0000);
  - The embedded SRAM is accessible in two address areas, 0x0000_0000 or 0x2000_0000;

2.1.3.2 **Boot configuration**

Three different BOOT modes can be selected through the BOOT0 pin and the user option byte BOOT configuration.

Table 2-2 List of Boot Mode

Boot mode select pin					**Boot mode**	**Specifies the start address for accessing memory space in boot mode**		
nBOOT1	nBOOT0	BOOT0 pin	nSWBOOT0	BOOT0 _CFG		Main Flash	System Memory	SRAM
X	X	0	1	1	Main Flash start	0x0000_0000 0x0800_0000	0x1FFF_0000	0x2000_0000
X	1	X	0					
1	X	1	1		System Memory start	0x08000000	0x0000_0000 0x1FFF_0000	0x2000_0000
1	0	X	0					
0	X	1	1		SRAM start	0x08000000	0x1FFF_0000	0x0000_0000 0x2000_0000
0	0	X	0					
X	X	1	1	0	Main Flash start	0x0000_0000 0x0800_0000	0x1FFF_0000	0x2000_0000
X	1	X	0					
1	X	0	1		System Memory start	0x08000000	0x0000_0000 0x1FFF_0000	0x2000_0000
1	0	X	0					
0	X	0	1		SRAM start	0x08000000	0x1FFF_0000	0x0000_0000 0x2000_0000
0	0	X	0					

Note: BOOT0 and GPIO are multiplexed, and there default settings during power-on are controlled by the BOOT0_CFG value.

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2.1.3.3 Embedded boot loader

The embedded boot loader is stored in System Memory for reprogramming Flash Memory through UART1. The UART1 interface can operate on an internal 64MHz oscillator (HSI). For further details, please refer to bootstrap manual.

2.2 Memory System

The program memory, data memory, registers and I/O ports are organized in the same 4GB linear address space. Data bytes are stored in the memory in Little Endian format. The lowest numbered byte in a word is regarded as the least significant byte of the word, while the highest numbered byte is the most significant byte. The specifications of program memory and data memory are as follows.

2.2.1 FLASH Specification

The Flash consists of a main memory block and an information block, which are described below:

- The maximum main memory block is 64KB, also known as main Flash memory, which contains 128 pages for storing and running user programs and storing data.
- The information area is 5KB, including 10 Pages, and consists of system memory area (3KB), system configuration area (1.5KB) and option byte area (0.5KB).
  - The System Memory area is 3KB, including 6 Pages, also known as System Memory, and is used for storing and running the BOOT loader
  - The system configuration area is 1.5KB, including 3 Pages.
  - The Option Byte area is 0.5KB, including 1 Page, also known as Option Byte, with an effective space of 26B, Both the BOOT program and user program can read, write and erase this area.

2.2.1.1 Flash memory module organization

Both the main memory block and the information block are allocated to bus address space memory

Table 2-3 Flash Bus Address List

Memory Area	Page Name	Address Range	Size
The main memory area	Page 0	0x0800_0000 – 0x0800_01FF	0.5KB
	Page 1	0x0800_0200 – 0x0800_03FF	0.5KB
	Page 2	0x0800_0400 – 0x0800_05FF	0.5KB
	⋮	⋮	⋮
	Page 127	0x0800_FE00 – 0x0800_FFFF	0.5KB
Information area	System memory area	0x1FFF_0000 – 0x1FFF_0BFF	3KB
	System configuration area	0x1FFF_F000 – 0x1FFF_F5FF	1.5KB
	Option byte area	0x1FFF_F600 – 0x1FFF_F619	26B
Memory area interface register	FLASH_AC	0x4002_2000 – 0x4002_2003	4B
	FLASH_KEY	0x4002_2004 – 0x4002_2007	4B
	FLASH_OPTKEY	0x4002_2008 – 0x4002_200B	4B
	FLASH_STS	0x4002_200C – 0x4002_200F	4B
	FLASH_CTRL	0x4002_2010 – 0x4002_2013	4B

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Memory Area	Page Name	Address Range	Size
	FLASH_ADD	0x4002_2014 – 0x4002_2017	4B
	FLASH_OB2	0x4002_2018 – 0x4002_201B	4B
	FLASH_OB	0x4002_201C – 0x4002_201F	4B
	FLASH_WRP	0x4002_2020 – 0x4002_2023	4B
	Reserved	0x4002_2024 – 0x4002_204F	44B
	FLASH_VTOR	0x4002_2050 – 0x4002_2053	4B

The Flash memory is organized into 64-bit wide memory units, which can store codes and data constants.

Information is divided into three parts:

- The system memory area is used to store the bootloader in the system memory. The bootloader uses UART1 serial interface to program the Flash memory.
- System configuration area,contains basic information about the chip.
- The option byte area.

The writing to the main memory and information block is managed by embedded Flash programming/erasing controller.

There are two ways to protect Flash memory from illegal access (read, write and erase):

- Page write protection (WRP)
- Readout protection (RDP)

When the Flash memory write operation is executed, any read operation to the Flash memory will stall the bus, and the read operation can only be performed correctly after the write operation is completed. This means that code or data fetches cannot be made while a program/erase operation is ongoing.

When performing Flash programming operations (write or erase), the internal RC oscillator (HSI) must be turned on .

Note: In the low power consumption mode, all Flash memory operations are suspended.

2.2.1.2 Read and write operation

The Flash operation only supports 32-bit operation, and the Flash should be erased before the write operation, and the minimum block size for erasing is one page 0.5KB. Write operation is divided into erasing and programming phases.

When reading Flash, the number of waiting cycles for reading can be configured by the register. When using, it needs to be calculated in combination with the clock frequency of SYSCLK interface. For example, when SYSCLK <= 32MHz, the minimum number of waiting periods is 0; When 32MHz< SYSCLK <= 64MHz, the minimum number of waiting periods is 1.

2.2.1.3 Unlock Flash

After reset, the Flash module is protected and cannot be written into the FLASH_CTRL register to prevent accidental operation of Flash memory due to electrical disturbances and other reasons. By writing a specific sequence of key values into the FLASH_KEY register, you can unlock the FLASH_CTRL register. The specific sequence is: Firstly, writing KEY1 = 0x45670123 in the FLASH_KEY register. Secondly, writing the key value KEY2 = 0xCDEF89AB in the FLASH_KEY register.

If there is an error in sequence or key value, a bus error will be returned and the FLASH_CTRL register will be locked until the next reset.

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Software can check the FLASH_CTRL.LOCK bit to confirm whether the Flash is unlocked. If normal locking is required, software can set the FLASH_CTRL.LOCK bit to 1. After that, the Flash can be unlocked by writing the correct key sequence to the FLASH_KEY register.

2.2.1.4 Erase and program

2.2.1.4.1 **Erase of main memory area and data FLASH area**

The main memory area can be erased page by page or whole. The data FLASH area only can be erased by page.

- **Page Erase**

  Page Erase process:

  – Check the FLASH_ STS.BUSY bit to confirm that there are no other Flash operations in progress;

  – Set the FLASH_CTRL.PER bit to '1';

  – Select the page to be erased with the FLASH_ADD register;

  – Set the FLASH_CTRL.START bit to '1';

  – Wait for the FLASH_ STS.BUSY bit to change to '0';

  – Read out the content of the erased page and verify it.

- **Mass Erase**

  Mass Erase process:

  – Check the FLASH_ STS.BUSY bit to confirm that there are no other Flash operations in progress;

  – Set the FLASH_CTRL.MER bit to '1';

  – Set the FLASH_CTRL.START bit to '1';

  – Wait for the FLASH_ STS.BUSY bit to change to '0';

  – Read out all pages and verify them.

2.2.1.4.2 **Main memory area programming**

Programming the main storage area can write 32 bits at a time. When FLASH_CTRL.PG is set to '1', writing a word to a flash address will initiate programming once; Writing any half word of data will result in a bus error. During the programming process (FLASH_STS.BUSY is '1'), any read or write operation to the flash memory will cause the CPU to pause until the flash programming is completed.

Main memory programming process:

- Check the FLASH_ STS.BUSY bit to confirm that there are no other Flash operations in progress;
- Set the FLASH_CTRL.PG bit to '1';
- Write the word to be programmed at the specified address;
- Wait for the FLASH_ STS.BUSY bit to change to '0';
- Read the written address and verify the data.

Note: When the FLASH_STS.BUSY bit is '1', you cannot write to any register.

Note: After writing data to two addresses in programming, it is necessary to add 3 __NOP() to prevent the bus from reading

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Flash data and causing programming failure.

2.2.1.4.3 **Option byte erase and programming**

The option byte area is programmed differently from the main memory block. The number of option bytes is limited to 13 bytes (2 bytes for write protection, 2 bytes for readout protection, 7 byte for configuration and 2 bytes for storing user data). After unlocking the Flash, you must write KEY1 and KEY2 respectively (refer to 2.2.1.3) to the FLASH_OPTKEY register, and then set the FLASH_CTRL.OPTWE bit to '1'. At this time, the option byte area can be programmed: set the FLASH_CTRL.OPTPG bit to '1' and then write a word to the specified address.

When programming the word in the option byte area, use the low byte in the half-word and automatically calculate the high byte (the high byte is the complement of the low byte), before starting the programming operation, this ensures that the option byte and its complement are always correct.

Option byte erase process:

- Check the FLASH_ STS.BUSY bit to confirm that there are no other Flash operations in progress;
- Unlock the FLASH_CTRL.OPTWE bit;
- Set the FLASH_CTRL.OPTER bit to '1';
- Set the FLASH_CTRL.START bit to '1';
- Wait for the FLASH_ STS.BUSY bit to change to '0';
- Read the erased option byte and verify it.

Note: The option byte erase process does not require configuring the FLASH_ADD register. If the page start address of the non option byte area is written to the FLASH_ADD register, a FLASH_STS.WRPERR error will occur.

Option byte area programming process:

- Check the FLASH_ STS.BUSY bit to confirm that there are no other Flash operations in progress;
- Set the FLASH_CTRL.OPTWE bit to '1';
- Set the FLASH_CTRL.OPTPG bit to '1';
- Writing the word to be programmed to the specified address;
- Wait for the FLASH_ STS.BUSY bit to change to '0';
- Read the written address and verify the data.

2.2.1.5 **Option byte**

Option byte block is mainly used to configure read-write protection, boot mode configuration, software/hardware watchdog, and bus address space is allocated to the option byte block for read-write access. They consist of 13 options bytes :2 byte for write protection, 2 bytes for readout protection, 7 byte for configuration option, 2 bytes defined by user. The option byte block also contains the complement codes corresponding to these 13 option bytes. These complement codes need to be automatically calculated by hardware when the option bytes are written in the bus, and written into Flash together, and used for verification when the option bytes are read.

By default, the option byte block is always read-accessible and write-protected. To write (program/erase) the option byte block, first unlock the Flash, then unlock the option byte: write the correct key-value sequence (KEY1 = 0x45670123, KEY2 = 0xCDEF89AB) into the FLASH_OPTKEY, and then write operation to the option byte block will be allowed. If

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the sequence is wrong or the key value is wrong, a bus error will be returned and the option byte will be locked until the next reset. To lock the option byte normally, write '0' to the FLASH_CTRL.OPTWE bit by software, and then the option byte can be unlocked by writing the correct key value sequence in the FLASH_OPTKEY.

After each system reset, the option byte data is read out from the option byte block and stored it in the option byte register (FLASH_OB/ FLASH_OB2/FLASH_WRP) with read-only property. At the same time, the option byte complement data read out together will be used to verify whether the option byte data is correct. If it does not match, an option byte error flag (FLASH_OB.OBERR) will be generated. When an option byte error occurs, the corresponding option byte is forced to 0xFF. When the option byte and its complement are both 0xFF (the state after erasing), the above verification steps are skipped and verification is not required.

Table 2-4 Option Byte List

Address	[31:24] Corresponding complement code	[23:16] Option byte	[15:8] Corresponding complement code	[7:0] Option byte
0x1FFF_F600	nUSER4	USER4	nRDP1	RDP1
0x1FFF_F604	nUSER0[15:8]	USER0[15:8]	nUSER0[7:0]	USER0[7:0]
0x1FFF_F608	nUSER1[15:8]	USER1[15:8]	nUSER1[7:0]	USER1[7:0]
0x1FFF_F60C	nUSER3	USER3	nUSER2	USER2
0x1FFF_F610	nData1	Data1	nData0	Data0
0x1FFF_F614	nWRP1	WRP1	nWRP0	WRP0
0x1FFF_F618	-	-	nRDP2	RDP2

- Readout protection L1 level option byte: RDP1
  - Protect the code stored in the Flash memory;
  - When the correct value is written, it is not allowed to read the Flash memory;
  - The result of whether RDP1 is turned on or not can be inquired through FLASH_OB[1];
- User configuration option 0: USER0
  - USER0 [15:0], IWDG_SW configuration options, can be queried through FLASH_OB [2]
  - USER0=16'h5aa5: Hardware watchdog
  - USER0! =16'h5aa5: Software watchdog
- User Configuration Option 1: USER1
  - USER1 [15:0], PF3_SRST configuration options, can be queried through FLASH_OB [3]
  - USER1=16'h5aa5: PF3 is a regular GPIO
  - USER1! =16'h5aa5: PF3 is NRST
- User Configuration Option 2: USER2
  - USER2，Power on delay reset control, can be queried through FLASH-OB [11:4]
- User configuration option 3: USER3
  - USER3[7:4]: Reserved

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- USER3[3]: BOOT0_CFG configuration options, which can be queried through FLASH_OB[15]

  0: BOOT0 Pin pull down is effective

  1: BOOT0 Pin Pull Up Effective

- USER3[2]: nSWBOOT0_SEL configuration option, which can be queried through FLASH_OB[14]

  0: nBOOT0 configuration selection uses BOOT mode selection

  1: BOOT0 Pin is used to select BOOT mode

- USER3 [1]: nBOOT1 configuration option, which can be queried through FLASH_OB[13]

- USER3 [0]: nBOOT0 configuration option, which can be queried through FLASH_OB[12]

- User Configuration Option 4: USER4
  - USER4[7:2]: Reserved
  - USER4[1:0]: Used to select the serial port pin for boot, which can be queried through FLASH_OB[21:20]
- 2 bytes of user data: Datax
  - Data1 (stored in FLASH_OB2[15:8]);
  - Data0 (stored in FLASH_OB2[7:0]);
- Write protection option byte: WRP0 ~ 1, which can be inquired through the register FLASH _WRP [15:0]
  - WRP0: Write protection for pages 0 to 63, bit[0] corresponds to Page (0 to 7)..., bit[7] corresponds to Page (56~63);
  - WRP1: Write protection for pages 64~127, bit[0] corresponds to Page (64~71)..., bit[7] corresponds to Page (120~127);
- Readout protection L2 level option byte: RDP2
  - Add protection function on the basis of L1, refer to the detailed description of readout protection in section 2.2.1.7;
  - The result of whether RDP2 is turned on or not can be inquired through FLASH_OB[31];

2.2.1.6 **Write protection**

Write protection can be configured for all pages of the Flash main memory area (maximum 64KB), to prevent accidental write operations caused by programcrashes or electrical disturbances. The basic unit of write protection is as follows: for Page 0 to 127, every 8 pages is a basic protection unit. Write protection can be configured by setting WRP0 and WRP1 in the option byte block; After each configuration, a system reset is required for the configured value to be reloaded to take effect. If an attempt is made to program or erase a protected page, a protection error flag will be returned in the FLASH_STS.

The system information area contains the following blocks:

- The system memory block (3KB) in the system information area stores the boot program and cannot be changed.
- The system configuration block (1.5KB) in the system information area stores the basic information of the chip and cannot be changed.
- The option byte block (0.5KB) in the system information area stores the user-configurable option byte information. The write protection of the option byte block is achieved by writing 0 to the FLASH_CTRL.OPTWE bit by software, and after that, you can write the correct key value sequence to FLASH_OPTKEY to release the write protection of

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the option byte.

2.2.1.7 **Readout protection**

The user code in Flash can be protected against unauthorized reading by setting readout protection. Readout protection is set by configuring RDP bytes in the option byte block. Three different readout protection levels can be configured, as shown in the following Table

Table 2-5 Read Protection Configuration List

Read Protection Status	RDP1	nRDP1	nRDP2	RDP2
L0 level	0xA5	0x5A	RDP2! = 0xCC || nRDP2! = 0x33	
L2 level	0xXX	0xXX	0x33	0xCC
L1 level	Not the above two configurations			

- L0 level:
  - In unprotected state(RDP1 == 0xA5 & nRDP1 == 0x5A) && (RDP2!= 0xCC | nRDP2!= 0x33);
  - The main memory area, data flash area and option bytes can be read arbitrarily;
  - The main memory area, data flash area and options bytes can be programmed and erase, with configurable read/write protection.
- L1 level:
  - The corresponding ~ ((RDP1 == 0xA5 & nRDP1 == 0x5A) && (RDP2!= 0xCC | nRDP2!= 0x33)) | (RDP2 == 0xCC & nRDP2 == 0x33));
  - Allow read operations on the main storage area from user code/SRAM code;
  - All pages of the main storage area can be programmed through code executed in the main flash memory to achieve functions such as IAP or data storage
  - All main storage pages are not allowed to perform write or erase operations in debug mode
  - Cannot load code into built-in SRAM through SWD
  - When the read protected option byte is rewritten to the unprotected L0 level, the entire main storage area will be automatically erased. The process is as follows: (Erasing the option byte block will not cause an automatic erase operation, as the erase result is 0xFF, which is still in the L1 level protection state)
    - Write the correct key value sequence into FLASH_OPTKEY to unlock the option byte block;
    - The bus initiates a command to erase the entire option byte area (Page erase);
    - Bus write 0xA5 to readout protection option byte;
    - Internally, automatically erase all main memory areas;
    - Internally, automatically write 0xA5 to readout protection option byte;
    - When the system is reset (such as software reset, etc.), the option byte block (including the new RDP value 0xA5) will be reloaded into the system, and the readout protection will be released;
- L2 level: Except that SRAM boot disabled, debug mode disabled, option byte write/page erase disabled and the protection level cannot be modified (irreversible), other features are the same as L1 level. The L2 level is realized by

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configuring another option byte, RDP2. No matter what the value of RDP1 is, as long as it satisfies (RDP2==0xCC & nRDP2==0x33), it is L2 level.

2.2.1.8 Permission protection

- Flash main memory area permissions:
  - Under L0 level: The main storage area can be read; The main storage area can be configured with write protection properties for each Page;
  - Under L1/2 level:
    - When executed in SWD debug mode, all Pages is not allowed (W/R/PE) operations;
    - All Pages can be programmed through the code executed in the main Flash memory area (implementing functions such as IAP or data memory);
    - All Pages can configure the write protection property of each Page;
    - When the L1 level is modifiedto the L0 level, all Flash main memory and data flash will be automatically erased;
- Flash option byte area permission:
  - Under the L0/L1 level:all accesses are allowed (W/R/PE);
  - Under L2 level: except for debug mode, all other modes allow read-only access to the Flash option byte area.
- Flash system memory area permissions:
  - The code executed in the system memory area/user program area/SRAM area allows read access (R).
  - Access is not allowed through debugging interfaces;
  - At the L1/L2 level, access is not allowed through the debugging interface;
  - At the L1/L2 level, SRAM startup jumps to system memory and code execution is not allowed to access (W/R/PE). Other situations allow access (W/R/PE).
- Flash system configuration area:
  - Read-only;

Table 2-6 Flash Read-write-erase(1) Permission Control Table

Protect Level	**Boot Mode** / Perform user / Access area	System Memory/Main Flash: SWD	System Memory/Main Flash: System Memory/ Main Flash/SRAM	Modify protection level
L0 level	Flash main memory area	Read-Write-Erase	Read-Write-Erase	Allow to change to L1 or L2
	Flash main memory area mass erase	Allow	Allow	

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	Flash option byte area	Read-Write-Erase	Read-Write-Erase	
	Flash system memory area	Prohibit	Read-only	
	System configuration area	Read-only	Read-only	
	SRAM（All）	Read and write	Read and write	
L1 level	Flash main memory area	Prohibit	Read-Write-Erase	Allow to change to L0 or L2. When changed to L0, the main storage area will be automatically erased.
	Flash main memory area mass erase	Prohibit	Allow	
	Flash option byte area	Read-Write-Erase	Read-Write-Erase	
	Flash system memory area	Prohibit	Read-only	
	System configuration area	Read-only	Read-only	
	SRAM（All）	Read-only	Read and write	
L2 level	Flash main memory area	The SWD interface is disabled.	Read-Write-Erase	No modifications are allowed.
	Flash main memory area mass erase		Allow	
	Flash option byte area		Read-only	
	Flash system memory area		Read-only	
	System configuration area		Read-only	
	SRAM（All）		Read and write	
Protect	**Boot Mode**	SRAM		Modify protection

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Level	Perform user / Access area	SWD	System Memory/ Main Flash/SRAM	level
L0 level	Flash main memory area	Read-Write-Erase	Read-Write-Erase	Allow to change to L1 or L2
	Flash main memory area mass erase	Allow	Allow	
	Flash option byte area	Read-Write-Erase	Read-Write-Erase	
	Flash system memory area	Prohibit	Read-only	
	System configuration area	Read-only	Read-only	
	SRAM（All）	Read and write	Read and write	
L1 level	Flash main memory area	Prohibit	Read-Write-Erase	Allow to change to L0 or L2. When changed to L0, the main storage area will be automatically erased.
	Flash main memory area mass erase	Prohibit	Allow	
	Flash option byte area	Read-Write-Erase	Read-Write-Erase	
	Flash system memory area	Prohibit	Prohibit	
	System configuration area	Read-only	Read-only	
	SRAM（All）	Read-only	Read and write	
L2 level	Flash main memory area	L2 protection level, cannot boot from SRAM		No modification is allowed. SWD is banned.
	Flash main memory area mass erase			
	Flash option byte area			
	Flash system memory area			

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	System configuration area		
	SRAM（All）		

Note: (1)Erase here refers to Flash page erase.

2.2.2 SRAM

SRAM is mainly used for operation to store variables and data or stacks during program execution. The maximum capacity is 6KB.

SRAM supports read-write access of byte, half-word and word.

SRAM supports code execution and can run programs at full speed in SRAM. The maximum address range of SRAM is 0x2000 0000 to 0x2000 17FF.

In RUN /STOP mode, data can be retained normally.

The main features are as follows:

- The maximum capacity is 6KB in total.
- Supports byte/half word/word reading and writing.
- CPU/DMA can be accessed.
- The CPU BUS can be remapped to SRAM to run the program at full speed.

2.2.3 FLASH Register Description

All register operations must be performed in words (32 bits).

2.2.3.1 Flash register overview

Table 2-7 Flash Register Overview

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x00	FLASH_AC	Reserved																													LATENCY		
0x04	FLASH_KEY	FKEY																															
0x08	FLASH_OPTKEY	OPTKEY																															
0x0c	FLASH_STS	Reserved																										EOP	WRPERR	Reserved	PGERR	Reserved	BUSY
0x10	FLASH_CTRL	Reserved																				EOPITE	Reserved	ERRITE	OPTWE	Reserved	LOCK	START	OPTER	OPTPG	MER	PER	PG
0x14	FLASH_ADD	FADD																															
0x18	FLASH_OB2	Reserved																Data1								Data0							
0x1c	FLASH_OB	RDPRT2	Reserved									BOOT_SEL		Reserved				BOOT0_CF	nSWBOOT0	nBOOT1	nBOOT0	POR_DELAY								NRST_PF3	IWDG_SW	RDPRT1	OBERR

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0x20	FLASH_WRP	Reserved	WRP
0x50	FLASH_VTOR	VTOR_EN	VTOR_VALUE

2.2.3.2 Flash access control register (FLASH_AC)

Address offset: 0x00

Reset value: 0x0000 0002

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved														LATENCY	
														rw	rw

Bit Field	Name	Description
31:2	Reserved	Reserved,the reset value must be maintained.
1:0	LATENCY	Time delay These bits represent the ratio of the SYSCLK (system clock) cycle to the flash access time 00: Zero periodic delay, when 0 < SYSCLK ≤ 32MHz 01: A periodic delay, when 32MHz < SYSCLK ≤ 64MHz 10/11: Reserved

2.2.3.3 Flash key register (FLASH_KEY)

Address offset: 0x04

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
FKEY[31:16]															
w	w	w	w	w	w	w	w	w	w	w	w	w	w	w	w

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FKEY[15:0]															
w	w	w	w	w	w	w	w	w	w	w	w	w	w	w	w

Bit Field	Name	Description
31:0	FKEY	Used to unlock the FLASH_CTRL.LOCK bit.

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2.2.3.4 Flash OPTKEY register (FLASH_OPTKEY)

Address offset: 0x08

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
OPTKEY [31:16]															
w	w	w	w	w	w	w	w	w	w	w	w	w	w	w	w

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OPTKEY [15:0]															
w	w	w	w	w	w	w	w	w	w	w	w	w	w	w	w

Bit field	Name	Description
31:0	OPTKEY	Used to unlock the FLASH_CTRL.OPTWE bit.

2.2.3.5 Flash status register (FLASH_STS)

Address offset: 0x0C

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved										EOP	WRPERR	Reserved	PGERR	Reserved	BUSY
										rc_w1	rc_w1		rc_w1		r

Bit Field	Name	Description
31:6	Reserved	Reserved,the reset value must be maintained
5	EOP	End of the operation When the Flash operation (programming/erasing) is complete, the hardware sets this to '1' and writing '1' clears this state. *Note: EOP status is set for each successful programming or erasure.*
4	WRPERR	Write protection error When attempting to program a write protected Flash address, hardware sets this to '1' and writing '1' clears this state.
3	Reserved	Reserved,the reset value must be maintained
2	PGERR	Programming errors When trying to program to an address whose content is not '0xFFFF_FFFF', the hardware sets this to '1'. Writing '1' clears this state. *Note: Before programming, the FLASH_CTRL.START bit must be cleared.*

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Bit Field	Name	Description
1	Reserved	Reserved,the reset value must be maintained
0	BUSY	Busy This bit indicates that a Flash operation is in progress.This bit is set to '1' at the start of the Flash operation; This bit is cleared to '0' at the end of the operation or when an error occurs.

2.2.3.6 Flash control register (FLASH_CTRL)

Address offset: 0x10

Reset value: 0x0000 0080

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved			EOPITE	Reserved	ERRITE	OPTWE	Reserved	LOCK	START	OPTER	OPTPG	Reserved	MER	PER	PG
			rw		rw	rw		rw	rw	rw	rw		rw	rw	rw

Bit Field	Name	Description
31:13	Reserved	Reserved,the reset value must be maintained
12	EOPITE	Allow operation completion interrupt. This bit allows an interrupt to be generated when the FLASH_STS.EOP bit becomes '1'. 0: Forbid interruption. 1: Interrupts are allowed.
11	Reserved	Reserved,the reset value must be maintained
10	ERRITE	Allow error status to be interrupted This bit allows interrupts in the event of Flash errors (when FLASH_STS.PGERR/ FLASH_STS.WRPERR is set to '1'). 0: Forbid interruption. 1: Interrupts are allowed.
9	OPTWE	Allows option bytes to be written When the bit is' 1 ', programmatic manipulation of the option byte is allowed. When the correct key sequence is written to the FLASH_OPTKEY register, the bit is set to '1'. Software can clear this bit.
8	Reserved	Reserved,the reset value must be maintained
7	LOCK	Lock This bit can only be written as '1'.When the bit is' 1 ', Flash and FLASH_CTRL are locked. Hardware clears this bit to '0' after detecting a correct unlock sequence. After an unsuccessful unlock operation, this bit cannot be changed until the next

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Bit Field	Name	Description
		system reset.
6	START	Start An erase operation is triggered when the bit is' 1 '.This bit can only be set by software to '1' and cleared to '0' when FLASH_STS.BUSY changes to '1'.
5	OPTER	Erase option bytes 0: Disable option bytes erase mode; 1: Enable option bytes erase mode.
4	OPTPG	Program option bytes 0: Disable option bytes program mode; 1: Enable option bytes program mode.
3	Reserved	Reserved,the reset value must be maintained
2	MER	Mass erase 0: Disable mass erase mode; 1: Enable mass erase mode.
1	PER	Page erase 0: Disable mass erase mode; 1: Enable mass erase mode.
0	PG	Program 0: Disable Program mode; 1: Enable Program mode.

Note: Please refer to Section 2.2.1.4 for programming and erasing.

2.2.3.7 Flash address register (FLASH_ADD)

Address offset: 0x14

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
FADD[31:16]															
w	w	w	w	w	w	w	w	w	w	w	w	w	w	w	w

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FADD[15:0]															
w	w	w	w	w	w	w	w	w	w	w	w	w	w	w	w

Bit Field	Name	Description
31:0	FADD	Flash memory address Select the address to program when programming and the page to erase when erasing. *Note: When the FLASH_STS.BUSY bit is '1', this register cannot be written.*

2.2.3.8 Flash address register (FLASH_OB2)

Address offset: 0x18

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Reset value: 0x0000 FFFF

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Data1								Data0							
r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r

Bit Field	Name	Description
31:16	Reserved	Reserved,the reset value must be maintained
15:8	Data1[7:0]	Data1 *Note: This bit is read-only.*
7:0	Data0[7:0]	Data0 *Note: This bit is read-only.*

2.2.3.9 Flash option byte register (FLASH_OB)

Address offset: 0x1C

Reset value: 0x0FFF FFFC

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RDPRT2	Reserved									BOOT_SEL[1:0]		Reserved			
r										r	r				

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BOOT0_CFG	nSWBOOT0	nBOOT1	nBOOT0	POR_DELAY[7:0]								NRST_PF3	IWDG_SW	RDPRT1	OBERR
r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r

Bit Field	Name	Description
31	RDPRT2	Readout protection level L2 0: Readout protection L2 is disabled. 1: Readout protection L2 is enabled. *Note: This bit is read-only.*
30:22	Reserved	Reserved,the reset value must be maintained
21:20	BOOT_SEL	BOOT serial communication pin selection 11b: PA9, PA10 (default) 00b: PA13, PA14 01b: PF0, PF1 10b: PA2, PA3
19:16	Reserved	Reserved,the reset value must be maintained

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Bit Field	Name	Description
15	BOOT0_CFG	BOOT0 power-on default state 0: High level default, pulled low effective 1: Low level default, pulled high effective
14	nSWBOOT0	For the usage rules, see 2.1.3.2 Boot configuration.
13	nBOOT1	For the usage rules, see 2.1.3.2 Boot configuration.
12	nBOOT0	For the usage rules, see 2.1.3.2 Boot configuration.
11:4	POR_DELAY[7:0]	The delay time for CPU reset after triggering POR. After the initial power on of the system is completed, Cortex ®- The system reset delay of M0 can be configured through this bit to control the reset delay time of the kernel. 0x00: Maximum delay time …. 0xFF: No delay Delay time=(1/fLSI) × (0xFF - POR-DELAY).
3	NRST_PF3	PF3 pin configuration. 0: Ordinary IO pin 1: NRST pin *Note: This bit is read-only.*
2	IWDG_SW	Watchdog Settings 0: Hardware watchdog. 1: Software watchdog. *Note: This bit is read-only.*
1	RDPRT1	Readout protection level L1 0: The L1 level of readout protection is disabled. 1: L1 readout protection is enabled. *Note: This bit is read-only.*
0	OBERR	Option byte error When this bit is '1', the option byte does not match its inverse. *Note: This bit is read-only.*

2.2.3.10 Flash write protection register (FLASH_WRP)

Address offset: 0x20

Reset value: 0xFFFF FFFF

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WRPT[15:0]															
r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r

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Bit Field	Name	Description
31:16	Reserved	Reserved,the reset value must be maintained
15:0	WRPT	Write protection This register contains the write protection option byte loaded by option byte area. 0: Write protection takes effect. 1: Write protection is invalid. *Note: These bits are read-only.*

2.2.3.11 Flash VTOR register (FLASH_VTOR)

Address offset: 0x50

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
VTOR_EN	VTOR_VALUE[30:16]														
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VTOR_VALUE[15:0]															
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Bit Field	Name	Description
31	VTOR_EN	Interrupt vector remapping enable. 1: enable 0: disable
30:0	VTOR_VALUE	Used for interrupt vector remapping, storing the base address of the interrupt vector table. These bits are valid when VTOR_EN = 1. Interrupt address = VTOR_VALUE + offset address. *Note: This function is only valid when the offset address is less than 0x100.*

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3 Power Control (PWR)

3.1 General Description

The PWR is power management unit to control status of different modules in different power modes. Its major function is to control MCU to enter different power modes and wakeup when events or interrupts happen. MCU support the RUN and STOP Mode. PWR controls voltage regulator, Clock sources, Resets and Flash/SRAM/GPIO status in different power modes.

3.1.1 Power Supply

MCU has an external V_{DD} supply. Embedded voltage regulator is used to supply the internal 1.5V digital power supplies. Voltage regulator has two modes, normal mode and low power mode.

- V_{DD}: 2.0V~5.5V, which mainly provides power input for MR, IO and clock reset system.
- V_{DDA}: 2.0V~5.5V, which mainly provides power for most analog peripherals. For details, please refer to the electrical characteristics section of the relevant data sheet.
- VDDA and VSSA must be connected to VDD and VSS respectively.

Voltage regulator operates in several different modes, depending on the application:

- RUN mode: The voltage regulator provides power in normal power mode.
- STOP mode: The voltage regulator provides power in low power mode and the output voltage can be configured to 1.5V or 1.2V by software.

Table 3-1 Power Domain Descriptions

Power Domain	Work mode	voltage (v)	Driven Module	Note
VDDA	External pin	2～5.5V	ADC, COMP, DAC, OPA	Connect to VDD on the PCB
VDD	External pin	2～5.5V	POR_VDD/PDR_VDD, PVD, MR, LSI, HSI_LDO	-
VDDD	Low power	1.5	-	stop mode
	Active	1.5		run mode
VDDD_HSI	Active	1.5	HSI	-
BG1.2v	Active	1.2	Internal Benchmark	2% accuracy over the entire temperature range
BG3.6v	Active	3.6	ADC Reference Value Usage	2% accuracy over the entire temperature range
BG1.8v	Active	1.8	VBG(1.8V),1/2AVDD,1/4AVDD: OPA's VCM Usage	2% accuracy over the entire temperature range

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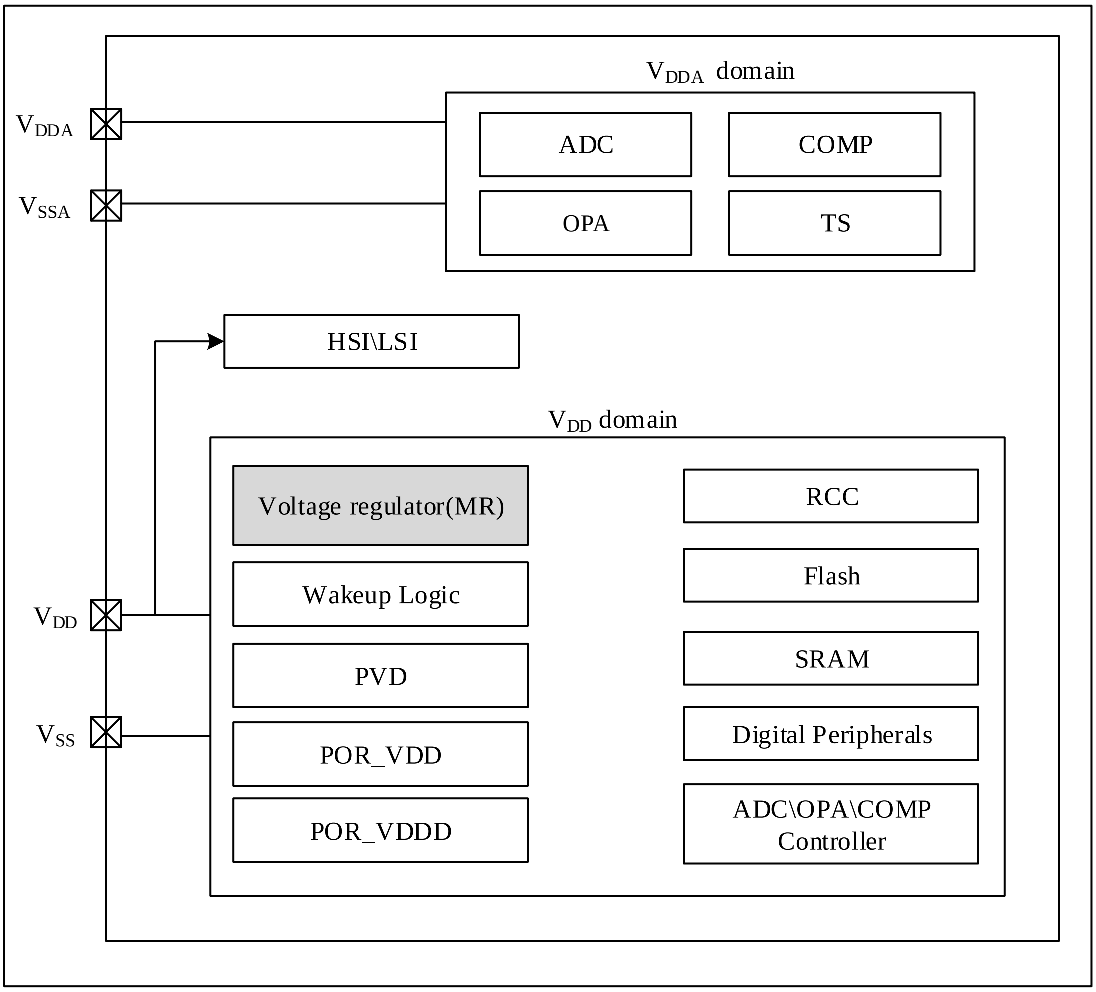
Figure 3-1 Power Supply Block Diagram



3.1.2 Power Supply Supervisor

3.1.2.1 Power on reset (POR) and power down reset (PDR)

Power on reset (POR) and power down reset (PDR) circuits are integrated inside the chip. When VDD/VDDA is below the specified limit voltage VPOR/VPDR, the system remains in a reset state without an external reset circuit. Refer to the electrical characteristics section of the data sheet for details on power-on and power-off resets.

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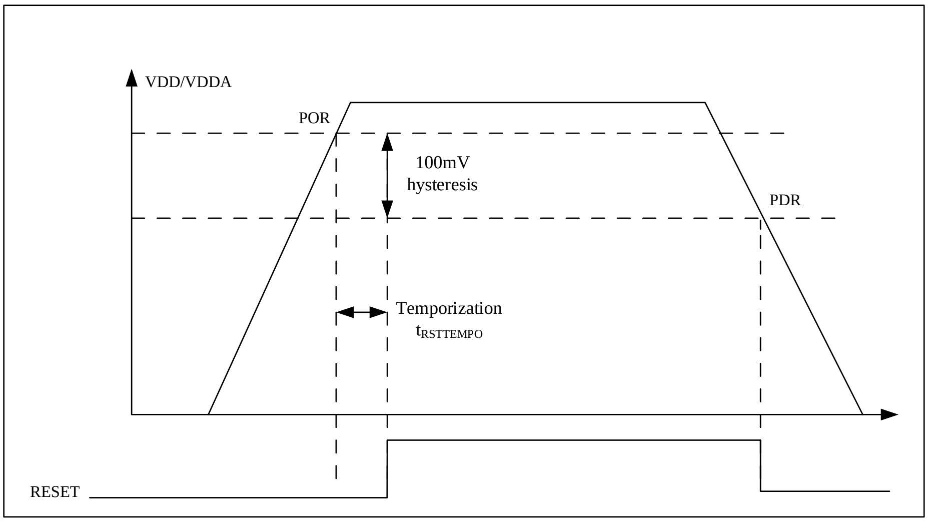
Figure 3-2 Power on Reset/Power down Reset Waveform



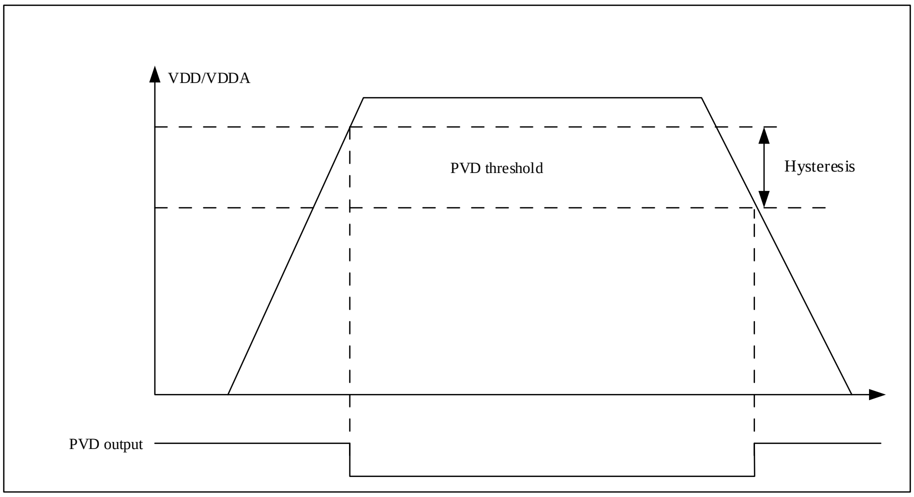
3.1.2.2 Programmable voltage detector (PVD)

The PVD monitors the power supply by comparing the V_{DD} voltage with the relevant bits in the power control register (PWR_CTRL). PWR_CTRL.PLS select the threshold of the monitoring voltage. Enable PVD by setting the PWR_CTRL.PVDEN.

The PWR_CTRLSTS.PVDO flag is used to indicate whether the V_{DD} is above/below the PVD voltage threshold. This event is connected internally to EXTI line7 and produces an interrupt if the interrupt is enabled in the external interrupt register. A PVD break occurs when the V_{DD} drops below the PVD threshold and/or when the V_{DD} rises above the PVD threshold, according to the rise/fall edge trigger setting of EXTI line 7. This feature can be used to perform emergency shutdown tasks.

- 15 software-selectable steps between 2.0V and 5V.
- Voltage hysteresis range: +/-100mV
- Supports programmable filtering (based on the LSI clock, configurable from 1 to 32 cycles / 30 to 1024 µs, default ~300 µs, implemented internally by PWR).

Figure 3-3 PVD Threshold Diagram



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3.2 Low-Power Mode

The MCU has two power modes: RUN, STOP. Different mode has different performance and power consumption. A summary of MCU power modes is shown below.

Table 3-2 Power Modes

Mode	Condition	Enter	Exit
RUN	CPU is running all peripherals are configurable.	Power up, system reset, or wakeup from other power modes.	Enter other low-power modes.
STOP	CPU enters deep SLEEP. peripherals clock are disabled,Voltage regulator runs in LP mode. HSI is disabled. LSI is enabled. Flash enters deep standby mode. SRAM/All registers are retained, All IO are retained . After waking up, The system clock configuration is retained. and the code continues to execute from the stopped point.	WFI/WFE: 1）SLEEPDEEP = 1, no pending interrupts/events.	Any interrupts wakeup event through EXTI

Note:

1. *IWDG (Independent Watchdog) can be configured to trigger either an interrupt or a system reset. It supports wake-up via interrupt or can be configured to perform a reset (in the same manner as NRST).*
2. *All EXTI lines are capable of wake-up. All GPIO pins can be mapped to EXTI0~6, with the ability to record up to 7 groups of wake-up sources (PA0~PA3: Group 1, PA4~PA7: Group 2, PA8~PA11: Group 3, PA12~PA15: Group 4, PB0~PB3: Group 5, PB4~PB8: Group 6, PF0~PF3: Group 7).*
3. *In RUN mode, the GPIO input filter width is configurable from 0 to 8 filter clock cycles. The filter clock (provided by RCC) can be configured with a division factor ranging from 1 to 16.*
4. *In STOP mode, the EXTI0~6 input filter can be enabled, with a fixed filter width of 2 LSI clock cycles.*

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The operating enabled status of different modules in different power consumption modes are shown in the following table:

Table 3-3 Peripheral Running Status

Main Blocks	Run/Active	Stop mode	
		Status	Wakeup capability
Cortex-M0	Y	-	-
FLASH	Y	-	-
SRAM	Y	Y（RET）	-
POR/PDR	Y	Y	Y
PVD	O	O	O
DMA	O	-	-
UART1	O	-	-
UART2	O	-	-
UART3	O	O	O
I2C1/2	O	-	-
SPI1/2/3	O	-	-
AD Timer	O	-	-
GP Timer	O	-	-
BS Timer	O	O	O
HSI	O	-	-
LSI	O	Y	-
IWDG	O	O	O
ADC	O	-	-
COMP	O	O	O
OPA	O	-	-
SysTick	O	-	-
GPIOs	O	O	O

Notes:

(1) Y: Yes (Enable), O: Optional (Disabled by default, Enabled by software), -: Not available.

3.2.1 STOP Mode

STOP mode is based on the Cortex®-M0 deep sleep mode combined with peripheral clock gating. The HSI is disabled. The LSI can be configured to enable. All GPIO states, SRAM and all registers are retained. Flash is in deep sleep mode. After waking up, the HSI is turned on, and the code starts from where it hangs.

3.2.1.1 Entering STOP mode

To enter the STOP mode, user needs to set SCB_SCR.SLEEPDEEP = 1.

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If a FLASH operation is in progress, entry into STOP mode will be delayed until the memory access completes.

If an APB area is being accessed, entry into STOP mode will be delayed until the APB access completes.

In STOP mode, the following peripherals can be used:

- Independent Watchdog (IWDG): Once enabled, it continues operating until a reset is generated.
- TIM6 / PVD / COMP peripherals can be configured for wake-up.
- UART3 is optional; if UART3 is used for wake-up, only event wake-up is supported.
- ADC should be disabled before entering STOP mode to avoid unnecessary power consumption.

3.2.1.2 Exiting STOP mode

When an interrupt or wake-up event wakes up STOP mode, the system clock configuration remains unchanged, codes resumed from suspended location.

3.3 Debug Support

3.3.1 Peripheral Debug Support

In addition to supporting debug in low power mode, it also supports some peripherals to stop operating in debug state (TIM1, TIM3, TIM4, TIM6, I2C1, I2C2, IWDG). For specific operations and features, please refer to the description of the other bit fields of the DBG_CTRL register in Chapter 3.4.5

3.4 PWR Registers

3.4.1 PWR Register Overview

Table 3-4 PWR Register Overview

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
000h	PWR_CTRL	Reserved									NRSTCNT				PVDCNT					Reserved	IWDGRSTEN	Reserved			PLS[3:0]				PVDEN	Reserved			
004h	PWR_CTRLSTS	Reserved																													PVDO	Reserved	
008h	PWR_CTRL2	Reserved																			MRLPDLY												MRLPEN
00Ch	DBG_CTRL	Reserved													TIM6STP	Reserved	I2C2TIMOUT	I2C1TIMOUT	Reserved	TIM4STP	TIM3STP	Reserved	TIM1STP	Reserved	IWDGSTP	Reserved							

3.4.2 Power Control Register（PWR_CTRL）

Address offset: 0x00

Reset value: 0x00785000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved									NRSTCNT				PVDCNT		
									rw				rw		

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PVDCNT		Reserved	IWDGRSTEN	Reserved			PLS[3:0]				PVDEN	Reserved			
rw			rw				rw				rw				

Bit field	Name	Description
31:23	Reserved	Reserved, must be kept at the reset value.
22:19	NRSTCNT	NRST Pin Filter Width The filter width is NRSTCNT*(T_{sysclk}*2) *Note:* *1. all 0 mean bypass* *2. In STOP mode, bypass*
18:14	PVDCNT	PVD Filter Width The filter width is PVDCNT*T_{LSI} *Note:* *1. all 0 mean bypass*
13	Reserved	Reserved, must be kept at the reset value.
12	IWDGRSTEN	IWDG Reset Enable Control 0: IWDG reset request does not generate a system reset; 1: IWDG reset request generates a system reset.
11:9	Reserved	Reserved, must be kept at the reset value.
8:5	PLS[3:0]	PVD Warning Voltage Level Selection

PWR_CTRL.PLS	Voltage
0000	Reserved
0001	2.0V
0010	2.2V
0011	2.4V
0100	2.6V
0101	2.8V
0110	3.0V
0111	3.2V

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Bit field	Name	Description	
		1000	3.4V
		1001	3.6V
		1010	3.8V
		1011	4.0V
		1100	4.2V
		1101	4.4V
		1110	4.6V
		1111	4.8V
4	PVDEN	PVD Enable Control 0: Disable PVD; 1: Enable PVD.	
3:0	Reserved	Reserved, must be kept at the reset value.	

3.4.3 Power Control Status Register（PWR_CTRLSTS）

Address offset: 0x04

Reset value: 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
													PVDO		
													r		

Bit field	Name	Description
31:3	Reserved	Reserved, must be kept at the reset value.
2	PVDO	PVD Module Detection Output 0: No PVD event; 1: PVD event has occurred.
1:0	Reserved	Reserved, must be kept at the reset value.

3.4.4 Power Control Register 2（PWR_CTRL2）

Address offset: 0x08

Reset value: 0x000007E1

Note: This register is write-protected. Before modification, you must first write the value 32'h5710_3616 to this

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address, and then proceed with the write operation.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved			MRLPDLY												MRLPEN

Bit field	Name	Description
31:13	Reserved	Reserved, must be kept at the reset value.
12:1	MRLPDLY	MR LP Control Enable After the system enters STOP mode, the enabling of MR LP is delayed. Delay time = MRLPDLY*(T_{sysclk}*2)
0	MRLPEN	MR LOWPOWER Mode Control 0: Permanently enabled; 1: MR LOWPOWER is automatically controlled.

3.4.5 Debug Control Register（DBG_CTRL）

Address offset：0x0C

Reset value：0x00000000

Note: Only POR/PDR can reset this register. Software write access to this register is only possible when a debugger is connected.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved													TIM6STP	Reserved	I2C2TIMOUT
													rw		rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
I2C1TIMOUT	Reserved	TIM4STP	TIM3STP	Reserved	TIM1STP	Reserved	IWDGSTP	Reserved							
rw		rw	rw		rw		rw								

Bit field	Name	Description
31:19	Reserved	Reserved, must be kept at the reset value.
18	TIM6STP	Halts the TIM6 counter when the core halts. Set or cleared by software (function takes effect upon setting). 0: Disable; 1: Enable.

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Bit field	Name	Description
17	Reserved	Reserved, must be kept at the reset value.
16	I2C2TIMOUT	Halts the SMBUS timeout mode of I2C2 when the core halts. Set or cleared by software. 0: Operates the same as in normal mode; 1: Freeze the SMBUS timeout control.
15	I2C1TIMOUT	Halts the SMBUS timeout mode of I2C1 when the core halts. Set or cleared by software. 0: Operates the same as in normal mode; 1: Freeze the SMBUS timeout control.
14	Reserved	Reserved, must be kept at the reset value.
13	TIM4STP	Halts the TIM4 counter when the core halts. Set or cleared by software (function takes effect upon setting). 0: Disable; 1: Enable.
12	TIM3STP	Halts the TIM3 counter when the core halts. Set or cleared by software (function takes effect upon setting). 0: Disable; 1: Enable.
11	Reserved	Reserved, must be kept at the reset value.
10	TIM1STP	Halts the TIM1 counter when the core halts. Set or cleared by software (function takes effect upon setting). 0: Disable; 1: Enable.
9	Reserved	Reserved, must be kept at the reset value.
8	IWDGSTP	Stops the watchdog when the core enters debug mode. Set or cleared by software. 0: Watchdog counter continues to operate normally; 1: Watchdog counter stops working.
7:0	Reserved	Reserved, must be kept at the reset value.

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4 Reset and clock control (RCC)

4.1 Reset Control Unit

Supports the following two types of reset:

- Power Reset
- System Reset

4.1.1 Power reset

A power reset occurs when the following events take place:

- Power-on/Power-down Reset (POR/PDR reset)

The power reset will reset all registers. (See Figure 3-1 Power Block Diagram)

The reset source ultimately acts upon the NRST pin and remains low during the reset process. The reset entry vector is fixed at address 0x0000_0004. For further details, refer to Table 5-1 Vector Table..

4.1.2 System reset

A system reset is generated when any of the following events occur:

- Low level on the NRST pin (external reset)
- Independent watchdog timer termination (IWDG reset)
- Software reset (SW reset)
- EMC/GLITCH reset
- M0 core lockdown reset

The reset source can be identified by examining the reset flag in the Control/Status Register (RCC_CTRLSTS).

The system reset signal provided to the chip is output on the NRST pin. The pulse generator ensures each reset pulse (external or internal) has a minimum duration of 20µs. For external reset, the reset pulse is generated when the NRST pin is pulled low.

The reset circuit is illustrated below:

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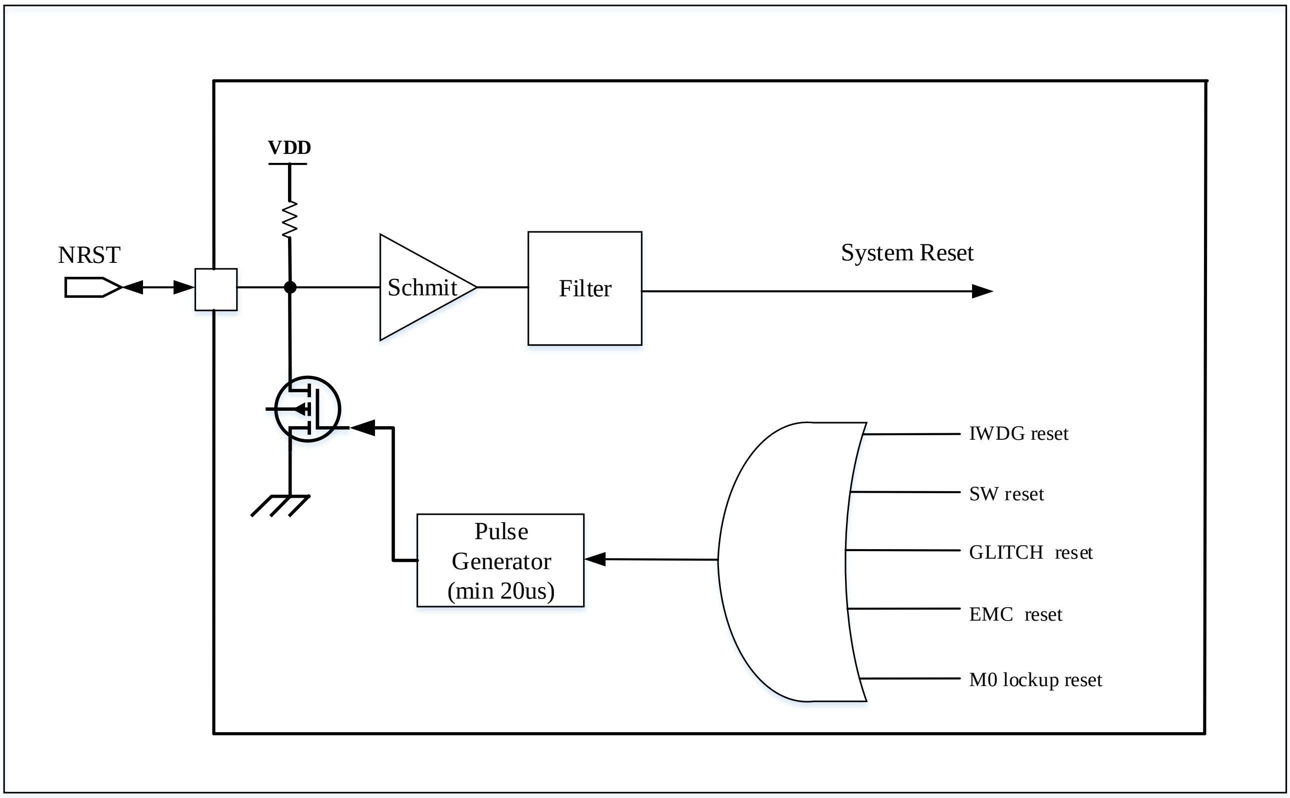
Figure 4-1 System reset generation



4.1.2.1 Software reset

A software reset can be generated by setting the SYSRESETREQ bit in Cortex®-M0 Application Interrupt and Reset Control Register. Refer to Cortex®-M0 technical reference manual for further information.

4.2 Clock control unit

Two distinct clock sources may be employed to drive the system clock (SYSCLK):

- HSI oscillator clock
- LSI oscillator clock

Multiple prescalers are available to configure the frequencies for AHB and APB. The maximum AHB frequency is 64MHz, while the maximum APB frequency is 32MHz.

Except where noted below, all peripheral clocks derive from either AHB or APB:

- By configuring RCC_CFG.TIMXCLKSEL, one of the following may be selected as the operating clock source for TIM1/3/4:
  - HCLK
  - SYSCLK
- By configuring RCC_CFG.TIM6CLKSEL, one of the following may be selected as the TIM6 clock source:
  - SYSCLK
  - LSI

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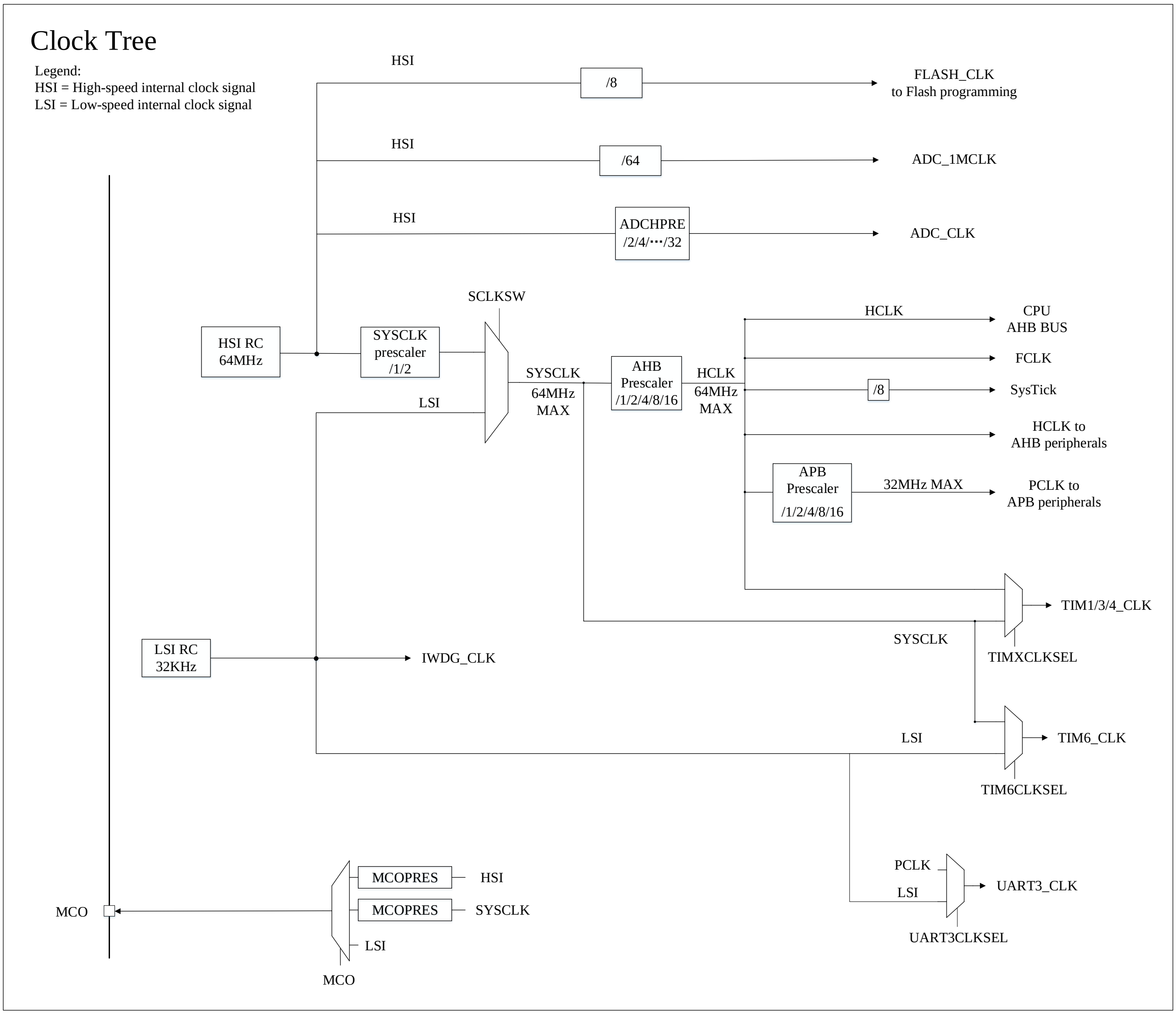
- By configuring RCC_CFG.UART3CLKSEL, one of the following may be selected as the UART3 clock source:
  - APB CLK
  - LSI
- The IWDG clock source is the LSI oscillator
- The Flash memory programming interface clock is always the HSI clock
- The ADC operating clock is HSI divided by 2/4/8/16/32

4.2.1 Clock Tree Diagram

Figure 4-2 Clock Tree



1. The maximum frequency available for the system clock is 64MHz.

2. For more details about the internal clock source characteristics, please refer to the "Electrical Characteristics" section in the product datasheet.

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4.2.2 HSI clock

The HSI (High-Speed Internal) clock signal is generated by an internal 64MHz RC oscillator and may be used directly as the system clock. The HSI RC oscillator provides a clock source without requiring any external components.

Users may adjust the HSI frequency using the RCC_CTRL.HSITRIM[9:0] bits.

The RCC_CTRL.HSIRDF bit indicates whether the HSI RC oscillator is stable. During initialisation, the HSI RC output clock remains disabled until this bit is set via hardware. The HSI clock can be enabled or disabled by setting the RCC_CTRL.HSIEN bit.

4.2.3 LSI clock

The LSI RC can provide a clock for the IWDG in STOP mode. The LSI clock frequency is approximately 32 kHz. For further details, please refer to the Electrical Characteristics section of the datasheet.

The RCC_CLKINT.LSIRDF bit flag indicates whether the LSI clock is stable.

The LSI will not be disabled after power-up.

4.2.4 System clock (SYSCLK) selection

Following a system reset, the HSI oscillator is selected as the system clock.

When the LSI clock source is ready, switching between clock sources is possible.

The LSI is set as the system clock via RCC_CFG.SCLKSW, and RCC_CFG.SCLKSTS determines whether the current system clock is HSI or LSI.

4.2.5 Watchdog clock

If the IWDG is initiated via hardware options or software, the clock is supplied to the IWDG once the LSI oscillator has stabilised.

4.2.6 Clock output(MCO)

The microcontroller clock output (MCO) function permits clock signals to be output to external MCO pins.

The corresponding GPIO port register must be configured for the desired function. The following three clock signals may be selected as the MCO clock:

- SYSCLK divided by the selected divisor
- HSI divided by the selected divisor
- LSI value

The clock selection is controlled by the RCC_CFG.MCO[1:0] bits..

4.2.7 LSI calibration

- Enabling Conditions

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Support when the system is active, the software initiates calibration counting. This requires first enabling the corresponding clock and verifying stable clock output.

- Clock Calibration Counter Operation

Upon calibration commencement, the first counter employs the LSI clock for counting. Counting concludes after completing RCC_CTRL.LSICALLEN[1:0] cycles, generating a count-done signal.

Concurrently during this count, the second counter operates using the HSI clock. Upon reaching Done, it stores the count result in a register for CPU interrogation.

- Calibration Procedure

1. Wait for HSI and LSI to be in ready state
2. Configure RCC_CTRL.LSICALLEN[1:0] to set LSI counting period to N (N configurable as 128, 256, 512, 1024)
3. Configure RCC_CTRL.LSICALEN to 1 to enable LSI calibration counting
4. Wait for RCC_CTRL.LSICALCF to go high, indicating counting completion; read the count result from RCC_LSICAL
5. Calculate the measured frequency using the formula: Measured frequency = 64,000,000 * N / RCC_LSICAL, Adjust the TRIM value based on the deviation between the measured frequency and 32 kHz.

4.3 RCC registers

4.3.1 RCC register overview

Table 4-1 RCC register overview

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
000h	RCC_CTRL	Reserved									HSITRIM[9:0]										Reserved	LSICALCF	LSICALLEN[1:0]		LSICALEN	Reserved						HSIRDF	HSIEN
004h	RCC_CFG	Reserved	MCOPRES[2:0]			MCO[1:0]		Reserved									SYSPRES	Reserved		TIMXCLKSEL	TIM6CLKSEL	UART3CLKSEL	APBPRES[2:0]			Reserved	AHBPRES[2:0]			Reserved		SCLKSTS	SCLKSW
008h	RCC_CLKINT	Reserved													HSIRDCLR	Reserved	LSIRDCLR	Reserved													HSIRDF	Reserved	LSIRDF
00Ch	RCC_APBRST	OPARST	Reserved	COMPRST	Reserved										UART3RST	UART2RST	UART1RST	TIM6RST	TIM4RST	TIM3RST	TIM1RST	Reserved	SPI2RST	SPI1RST	Reserved						I2C2RST	I2C1RST	IOMRST
010h	RCC_AHBPCLKEN	Reserved																			ADCEN	Reserved				HDIVEN	Reserved	SQRTEN	Reserved				DMAEN
014h	RCC_APBPCLKEN	OPAEN	COMPFILTEN	COMPEN	Reserved										UART3EN	UART2EN	UART1EN	TIM6EN	TIM4EN	TIM3EN	TIM1EN	Reserved	SPI2EN	SPI1EN	Reserved					PWREN	I2C2EN	I2C1EN	IOMEN
01Ch	RCC_CTRLSTS	Reserved																				LKUPRSTF	Reserved	EMCGBNF	EMCGBF	GLITCHRSTF	IWDGRSTF	SFTRSTF	PORRSTF	PINRSTF	Reserved		RMRSTF

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020h	RCC_AHBPRST	Reserved	ADCRST	Reserved	HDIVRST	Reserved	SQRTRST	Reserved									
024h	RCC_CFG2	Reserved	ADCHPRE[2:0]														
02Ch	RCC_LSICAL	Reserved	HSICALCNT														
030h	RCC_EMCCTRL	LKUPRSTEN	Reserved	GBNSW	GBNRST	GBNDET	Reserved	GBNDETSEL	GBSW	GBRST	GBDET	Reserved	GBNDETSEL	GVSW	GVRST	GVDET	GVDETSEL
034h	RCC_LSCTRL	Reserved	TRIMSEL	LSITRIM[8:0]													
038h	RCC_TIMFILTCFG	IOFLITCLK	Reserved	TIM4FILTCLK	Reserved	TIM3FILTCLK	Reserved	TIM1FILTCLK									

4.3.2 Clock Control Register (RCC_CTRL)

Address offset: 0x00

Reset value: 0x00400603

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved									HSITRIM[9:0]						
									rw						

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HSITRIM[9:0]			Reserved	LSICALCF	LSICALLEN[1:0]		LSICALEN	Reserved						HSIRDF	HSIEN
rw				r	rw		rw							r	rw

Bit field	Name	Description
31:23	Reserved	Reserved, the reset value must be maintained.
22:13	HSITRIM[9:0]	HSI clock trim value Default 10'b10_0000_0000, written by software to calibrate the frequency of the internal HSI RC oscillator. HSITRIM[9:4] for coarse adjustment, adjustment step about 960KHz; HSITRIM[3:0] for fine adjustment, adjustment step about 160KHz. *Note: The reset value of HSI tirm will be different for each MCU after leaving the factory, and the actual value of the MCU shall prevail.*
12	Reserved	Reserved, the reset value must be maintained.
11	LSICALCF	Clock calibration complete flag 0: Calibration incomplete 1: Calibration complete
10:9	LSICALLEN[1:0]	Clock calibration length Counts HSI clock cycles over LSICALLEN LSI cycles 00: 128 LSI cycles 01: 256 LSI cycles 10: 512 LSI cycles

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Bit field	Name	Description
		11: 1024 LSI cycles
8	LSICALEN	Clock Calibration Enable 0: Disabled 1: Enabled
7:2	Reserved	Reserved, the reset value must be maintained.
1	HSIRDF	HSI Clock Ready Flag 0: Not ready 1: Ready
0	HSIEN	HSI Clock Enable 0: Disabled 1: Enabled HSI is enabled by default after power-up and serves as the system clock. When switching LSI to act as the system clock, disable HSI after the switch is complete.

4.3.3 Clock Configuration Register (RCC_CFG)

Address offset: 0x04

Reset value: 0x20000400

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved	MCOPRES[2:0]			MCO[1:0]		Reserved									SYSPRES
		rw			rw										rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved		TIMXCLKSEL	TIM6CLKSEL	UART3CLKSEL	APBPRES[2:0]			Reserved	AHBPRES[2:0]			Reserved		SCLKSTS	SCLKSW
		rw	rw	rw		rw				rw				r	rw

Bit field	Name	Description
31	Reserved	Reserved, the reset value must be maintained.
30:28	MCOPRES[2:0]	MCO Output SYSCLK, HSI Division Configuration 010: 2 division 011: 3 division … 111: 7 division Other configurations are not permitted
27:26	MCO[1:0]	MCO Output Clock Selection 00: No clock output 01: Select output LSI 10: Select output SYSCLK division value 11: Select output HSI division value

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Bit field	Name	Description
25:17	Reserved	Reserved, the reset value must be maintained.
16	SYSPRES	SYSCLK Division Configuration 0: No division 1: 2-division
15:14	Reserved	Reserved, the reset value must be maintained.
13	TIMXCLKSEL	TIM1/3/4 Operating Clock Source Selection 0: hclk 1: sysclk
12	TIM6CLKSEL	TIM6 Operating Clock Source Selection 0: sysclk 1: LSI If TIM6 is required to operate during system STOP state, the TIM6 operating clock source must be configured as LSI
11	UART3CLKSEL	UART3 operating clock source selection 0: APB CLK 1: LSI If UART3 is required to operate during system STOP state, the UART3 operating clock source must be configured as LSI
10:8	APBPRES[2:0]	APB clock division configuration 100: HCLK divided by 2 101: HCLK divided by 4 110: HCLK divided by 8 111: HCLK divided by 16 Other values: No division *Note: When modifying the division factor, ensure the APB CLK frequency does not exceed 32 MHz*
7	Reserved	Reserved, the reset value must be maintained.
6:4	AHBPRES[2:0]	AHB Clock Division Configuration 100: SYSCLK divided by 2 101: SYSCLK divided by 4 110: SYSCLK divided by 8 111: SYSCLK divided by 16 Other values: No division *Note: When modifying the division factor, ensure the APB CLK frequency does not exceed 32 MHz*
3:2	Reserved	Reserved, the reset value must be maintained.
1	SCLKSTS	System Clock Switching State 0: HSI as current SYSCLK clock source 1: LSI as current SYSCLK clock source
0	SCLKSW	System Clock Switch Control 0: SYSCLK clock source selects HSI 1: SYSCLK clock source selects LSI

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4.3.4 Clock Status Register (RCC_CLKINT)

Address offset: 0x08

Reset value: 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved													HSIRDCLR	Reserved	LSIRDCLR
													w		w

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved													HSIRDF	Reserved	LSIRDF
													r		r

Bit field	Name	Description
31:19	Reserved	Reserved, the reset value must be maintained.
18	HSIRDCLR	HSIRDF Clear 0: No effect 1: Clear HSIRDF flag
17	Reserved	Reserved, the reset value must be maintained.
16	LSIRDCLR	LSIRDF Clear 0: No effect 1: Clear LSIRDF flag
15:3	Reserved	Reserved, the reset value must be maintained.
2	HSIRDF	HSI Ready Flag 0: Not ready 1: Ready
1	Reserved	Reserved, the reset value must be maintained.
0	LSIRDF	LSI Ready Flag 0: Not ready 1: Ready

4.3.5 APB Peripheral Reset Register (RCC_APBRST)

Address offset: 0x0C

Reset value: 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
OPARST	Reserved	COMPRST	Reserved										UART3RST	UART2RST	UART1RST
rw		rw											rw	rw	rw
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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TIM6RST	TIM4RST	TIM3RST	TIM1RST	Reserved	SPI2RST	SPI1RST	Reserved	I2C2RST	I2C1RST	IOMRST
rw	rw	rw	rw		rw	rw		rw	rw	rw

Bit field	Name	Description
31	OPARST	OPA Soft Reset 0: Clear reset 1: Generate reset
30	Reserved	Reserved, the reset value must be maintained.
29	COMPRST	COMP Soft Reset 0: Clear reset 1: Generate reset
28:19	Reserved	Reserved, the reset value must be maintained.
18	UART3RST	UART3 Soft Reset 0: Clear reset 1: Generate reset
17	UART2RST	UART2 Soft Reset 0: Clear reset 1: Generate reset
16	UART1RST	UART1 Soft Reset 0: Clear reset 1: Generate reset
15	TIM6RST	TIM6 Soft Reset 0: Clear reset 1: Generate reset
14	TIM4RST	TIM4 Soft Reset 0: Clear reset 1: Generate reset
13	TIM3RST	TIM3 Soft Reset 0: Clear reset 1: Generate reset
12	TIM1RST	TIM1 Soft Reset 0: Clear reset 1: Generate reset
11	Reserved	Reserved, the reset value must be maintained.
10	SPI2RST	SPI2 Soft Reset 0: Clear reset 1: Generate reset
9	SPI1RST	SPI1 Soft Reset 0: Clear reset 1: Generate reset
8:3	Reserved	Reserved, the reset value must be maintained.
2	I2C2RST	I2C2 Soft Reset

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Bit field	Name	Description
		0: Clear reset 1: Generate reset
1	I2C1RST	I2C1 Soft Reset 0: Clear reset 1: Generate reset
0	IOMRST	IOM Soft Reset 0: Clear reset 1: Generate reset

4.3.6 AHB Peripheral Clock Enable Register (RCC_AHBPCLKEN)

Address offset: 0x10

Reset value: 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved			ADCEN	Reserved				HDIVEN	Reserved	SQRTEN	Reserved				DMAEN
			rw					rw		rw					rw

Bit field	Name	Description
31:13	Reserved	Reserved, the reset value must be maintained.
12	ADCEN	ADC Bus Clock Enable 0: Disabled 1: Enabled
11:8	Reserved	Reserved, the reset value must be maintained.
7	HDIVEN	HDIV Bus Clock Enable 0: Disabled 1: Enabled
6	Reserved	Reserved, the reset value must be maintained.
5	SQRTEN	SQRT Bus Clock Enable 0: Disabled 1: Enabled
4:1	Reserved	Reserved, the reset value must be maintained.
0	DMAEN	DMA Bus Clock Enable 0: Disabled 1: Enabled

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4.3.7 APB Peripheral Clock Enable Register (RCC_APBPCLKEN)

Address offset: 0x14

Reset value: 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
OPAEN	COMPFILTEN	COMPEN	Reserved										UART3EN	UART2EN	UART1EN
rw	rw	rw											rw	rw	rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TIM6EN	TIM4EN	TIM3EN	TIM1EN	Reserved	SPI2EN	SPI1EN	Reserved					PWREN	I2C2EN	I2C1EN	IOMEN
rw	rw	rw	rw		rw	rw						rw	rw	rw	rw

Bit field	Name	Description
31	OPAEN	OPA Bus Clock Enable 0: Disabled 1: Enabled
30	COMPFILTEN	COMP Filter clock enable 0: Disabled 1: Enabled
29	COMPEN	COMP Bus Clock Enable 0: Disabled 1: Enabled
28:19	Reserved	Reserved, the reset value must be maintained.
18	UART3EN	UART3 Bus Clock Enable 0: Disabled 1: Enabled
17	UART2EN	UART2 Bus Clock Enable 0: Disabled 1: Enabled
16	UART1EN	UART1 Bus Clock Enable 0: Disabled 1: Enabled
15	TIM6EN	TIM6 Bus Clock Enable 0: Disabled 1: Enabled
14	TIM4EN	TIM4 Bus Clock Enable 0: Disabled 1: Enabled
13	TIM3EN	TIM3 Bus Clock Enable 0: Disabled 1: Enabled

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Bit field	Name	Description
12	TIM1EN	TIM1 Bus Clock Enable 0: Disabled 1: Enabled
11	Reserved	Reserved, the reset value must be maintained.
10	SPI2EN	SPI2 Bus Clock Enable 0: Disabled 1: Enabled
9	SPI1EN	SPI1 Bus Clock Enable 0: Disabled 1: Enabled
8:4	Reserved	Reserved, the reset value must be maintained.
3	PWREN	PWR Bus Clock Enable 0: Disabled 1: Enabled
2	I2C2EN	I2C2 Bus Clock Enable 0: Disabled 1: Enabled
1	I2C1EN	I2C1 Bus Clock Enable 0: Disabled 1: Enabled
0	IOMEN	IOM Bus Clock Enable 0: Disabled 1: Enabled

4.3.8 Control/Status Register (RCC_CTRLSTS)

Address offset: 0x1C

Reset value: 0x00000018

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved				LKUPRSTF	Reserved	EMCGBNF	EMCGBF	GLITCHRSTF	IWDGRSTF	SFTRSTF	PORRSTF	PINRSTF	Reserved		RMRSTF
				r		r	r	r	r	r	r	r			rw

Bit field	Name	Description
31:12	Reserved	Reserved, the reset value must be maintained.

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Bit field	Name	Description
11	LKUPRSTF	CPU Lockup Triggered System Reset Flag 0: No reset generated 1: Reset generated RMRSTF written as 1, this bit cleared
10	Reserved	Reserved, the reset value must be maintained.
9	EMCGBNF	EMC GBN Triggered System Reset Flag 0: No reset generated 1: Reset generated RMRSTF written as 1, this bit cleared
8	EMCGBF	EMC GB Triggered System Reset Flag 0: No reset generated 1: Reset generated RMRSTF written as 1, this bit cleared
7	GLITCHRSTF	GLITCH Triggered System Reset Flag 0: No reset generated 1: Reset generated RMRSTF written as 1, this bit cleared
6	IWDGRSTF	IWDGTriggered System Reset Flag 0: No reset generated 1: Reset generated RMRSTF written as 1, this bit cleared
5	SFTRSTF	Software Reset Triggered System Reset Flag 0: No reset generated 1: Reset generated RMRSTF written as 1, this bit cleared
4	PORRSTF	POR Reset Flag 0: No reset generated 1: Reset generated
3	PINRSTF	NRST PINTriggered System Reset Flag 0: No reset generated 1: Reset generated RMRSTF written as 1, this bit cleared
2:1	Reserved	Reserved, the reset value must be maintained.
0	RMRSTF	Clear Reset Flag 0: Do not clear reset flag 1: Clear all reset flags in RCC_CTRLSTS

4.3.9 AHB Peripheral Reset Register (RCC_AHBPRST)

Address offset: 0x20

Reset value: 0x00000000

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved			ADCRST	Reserved				HDIVRST	Reserved	SQRTRST	Reserved				
			rw					rw		rw					

Bit field	Name	Description
31:13	Reserved	Reserved, the reset value must be maintained.
12	ADCRST	ADC Soft Reset 0: Clear reset 1: Generate reset
11:8	Reserved	Reserved, the reset value must be maintained.
7	HDIVRST	HDIV Soft Reset 0: Clear reset 1: Generate reset
6	Reserved	Reserved, the reset value must be maintained.
5	SQRTRST	SQRT Soft Reset 0: Clear reset 1: Generate reset
4:0	Reserved	Reserved, the reset value must be maintained.

4.3.10 Clock Configuration Register 2 (RCC_CFG2)

Address offset: 0x24

Reset value: 0x00000003

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved													ADCHPRE[2:0]		
													rw		

Bit field	Name	Description
31:3	Reserved	Reserved, the reset value must be maintained.
2:0	ADCHPRE[2:0]	ADC Operating Clock Division Configuration 001: HSI clock divided by 2

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Bit field	Name	Description
		011: HSI clock divided by 4 100: HSI clock divided by 8 101: HSI clock divided by 16 110: HSI clock divided by 32 Other: HSI clock divided by 32

4.3.11 Clock Calibration Count Register (RCC_LSICAL)

Address offset: 0x2C

Reset value: 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved								HSICALCNT							
								r							

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HSICALCNT															
r															

Bit field	Name	Description
31:24	Reserved	Reserved, the reset value must be maintained.
23:0	HSICALCNT	Number of cycles generated by HSI (fixed at 64MHz) within the RCC_CTRL.LSICALLEN[1:0] clock calibration period

4.3.12 EMC Control Register (RCC_EMCCTRL)

Address offset: 0x30

Reset value: 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
LKUPRSTEN	Reserved							GBNSW	GBNRST	GBNDET	Reserved			GBNDETSEL	
rw								rw	rw	rw				rw	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GBSW	GBRST	GBDET	Reserved			GBDETSEL		GVSW	GVRST	GVDET	GVDETSEL				
rw	rw	rw				rw		rw	rw	rw	rw				

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Bit field	Name	Description
31	LKUPRSTEN	CPU Lockup Trigger Reset Enable 0: Disabled 1: Enabled
31:24	Reserved	Reserved, the reset value must be maintained.
23	GBNSW	Upon EMC GBN occurrence, system clock source switches from HSI to LSI 0: Switch disabled 1: Switch enabled
22	GBNRST	Upon EMC GBN occurrence, generates system reset 0: No reset generated 1: Generate reset
21	GBNDET	EMC GBN detection enabled 0: Disabled 1: Enabled
20:18	Reserved	Reserved, the reset value must be maintained.
17:16	GBNDETSEL	EMC GBN detection mode selection 0 is the maximum hysteresis interval, 3 is the minimum hysteresis interval, and they decrease sequentially
15	GBSW	When EMC GB occurs, system clock source switches from HSI to LSI 0: Switch disabled 1: Switch enabled
14	GBRST	When EMC GB occurs, generate system reset 0: Do not generate reset 1: Generate reset
13	GBDET	EMC GB Detection Enable 0: Disabled 1: Enabled
12:10	Reserved	Reserved, the reset value must be maintained.
9:8	GBDETSEL	EMC GB detection mode selection 0 is the maximum hysteresis interval, 3 is the minimum hysteresis interval, and they decrease sequentially
7	GVSW	Upon GLITCH occurrence, system clock source switches from HSI to LSI 0: Switch disabled 1: Switch enabled
6	GVRST	Upon GLITCH occurrence, generate system reset 0: Do not generate reset 1: Generate reset
5	GVDET	GLITCH detection enabled 0: Disabled 1: Enabled *Note: After enabling the GVDET bit, a delay of 10us or more is required to enable the GVRST bit and GVSW bit.*
4:0	GVDETSEL	GLITCH detection mode selection Bit2 is the actual highest bit, 0 is the highest sensitivity, 0x1F is the lowest sensitivity, and they

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Bit field	Name	Description
		decrease in sequence

4.3.13 LSI Calibration Control Register (RCC_LSCTRL)

Address offset: 0x34

Reset value: 0x00000140

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved						TRIMSEL	LSITRIM[8:0]								
						rw	rw								

Bit field	Name	Description
31:10	Reserved	Reserved, the reset value must be maintained.
9	TRIMSEL	LSI TRIM Source Selection 0: Derived from AFEC 1: Derived from RCC_LSCTRL.LSITRIM[8:0]
8:0	LSITRIM[8:0]	LSI Clock Trim Value Default: 9'b1_0100_0000, software-programmable for calibrating the internal LSI RC oscillator frequency. Adjustment step: 100Hz. *Note: The reset value of HSI tirm will be different for each MCU after leaving the factory, and the actual value of the MCU shall prevail.*

4.3.14 Filter Clock Configuration Register (RCC_TIMFILTCFG)

Address offset: 0x38

Reset value: 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
IOFLITCLK				Reserved							TIM4FILTCLK				
rw											rw				

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved			TIM3FILTCLK					Reserved			TIM1FILTCLK				
			rw								rw				

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Bit field	Name	Description
31:28	IOFLITCLK	IOM Filter Unit Operating Clock Division Control (Based on HCLK) 0000: No division 0001: 2-division 0010: 3-division … 1110: 15-division 1111: 16-division
27:21	Reserved	Reserved, the reset value must be maintained.
20:16	TIM4FILTCLK	TIM4 Filter Unit Operating Clock Division Control (based on TIM4 Operating Clock) 00000: No division 00001: 2-division 00010: 3-division … 11110: 31-division 11111: 32-division
15:13	Reserved	Reserved, the reset value must be maintained.
12:8	TIM3FILTCLK	TIM3 filter unit operating clock division control (based on TIM3 operating clock) 00000: No division 00001: 2-division 00010: 3-division … 11110: 31-division 11111: 32-division
7:5	Reserved	Reserved, the reset value must be maintained.
4:0	TIM1FILTCLK	TIM1 filter unit operating clock division control (based on TIM1 operating clock) 00000: No division 00001: 2-division 00010: 3-division … 11110: 31-division 11111: 32-division

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5 Interrupts and Events

5.1 Nested Vectored Interrupt Controller

Features

- 21 maskable interrupt channels.
- 4 programmable priority levels (using 2-bit interrupt priority);
- Low-latency exception and interrupt handling;
- Power management control;
- Implementation of system control registers;

The nested vectored interrupt controller (NVIC) is closely linked to the processor core, enabling low latency interrupt processing and efficient processing of late interrupts. The nested vectored interrupt controller manages interrupts including core exceptions.

5.1.1 SysTick Calibration Value Register

The system tick calibration value is fixed at 8000. When the system tick clock is set to 8MHz (the maximum value of HCLK/8), 1ms time base is generated.

5.1.2 Interrupt and Exception Vectors.

Table 5-1 Vector Table

Position	Priority	Priority Type	Name	Description	Address
-	-	-	-	Reserved	0x0000 0000
-	-3	Fixed	Reset	Reset	0x0000 0004
-	-2	Fixed	NMI	Non-maskable interrupt. RCC clock security system (CSS) is connected to the NMI vector.	0x0000 0008
-	-1	Fixed	HardFault	All types of errors (fault)	0x0000 000C
-	3	Settable	SVCall	System services invoked by SWI directives	0x0000 002C
-	5	Settable	PendSV	System service requests that can be pending	0x0000 0038
-	6	Settable	SysTick	System tick timer	0x0000 003C
0	7	Settable	WWDG	Window watchdog interrupt	0x0000 0040
1	8	Settable	FLASH	Flash global interrupt	0x0000 0044
2	9	Settable	EXTI0_6	EXTI0_6 (ALL GPIO MUX group connected to EXTI lines 0-6) interrupt	0x0000 0048
3	10	Settable	COMP	Comparator interrupt (connected to EXTI line 8)	0x0000 004C
4	11	Settable	UART1	UART1 interrupt	0x0000 0050
5	12	Settable	UART2	UART2 interrupt	0x0000 0054

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Position	Priority	Priority Type	Name	Description	Address
6	13	Settable	TIM1_BRK_UP_TRG_COM	TIM1 brake, update, trigger, and communication interruption	0x0000 0058
7	14	Settable	TIM1_CC	TIM1 capture comparison interrupted	0x0000 005C
8	15	Settable	ADC	ADC global interrupt, segmented ADC management	0x0000 0060
9	16	Settable	SPI1	SPI1 global interrupt	0x0000 0064
10	17	Settable	IWDG	IWDG interrupt	0x0000 0068
11	18	Settable	TIM4	TIM4 global interrupt, 32-bit GP	0x0000 006C
12	19	Settable	TIM3	TIM3 global interrupt, 16-bit GP	0x0000 0070
13	20	Settable	TIM6	TIM6 Timer, Basic Timer (EXTI line 9)	0x0000 0074
14	21	Settable	UART3	UART3 interrupt	0x0000 0078
15	22	Settable	SPI2	SPI2 global interrupt	0x0000 007C
16	23	Settable	I2C1_EV	I2C1 event interrupt	0x0000 0080
17	24	Settable	I2C1_ER	I2C1 error interrupt	0x0000 0084
18	25	Settable	I2C2_EV	I2C2 event interrupt	0x0000 0088
19	26	Settable	I2C2_ER	I2C2 error interrupt	0x0000 008C
20	27	Settable	DMA	DMA global interrupt	0x0000 0090

5.2 Extended Interrupt/Event Controller (EXTI)

5.2.1 Introduction

The extended interrupt/event controller contains 11 edge detection circuits that generate interrupt/event triggers. Each input line can be independently configured with pulse or pending input types, and 3 trigger event types including rising edge, falling edge or double edges, which can also be independently shielded. Interrupt requests that hold the state line in the pending register can be cleared by writing '1' in the corresponding bit of the pending register.

5.2.2 Main Features

The main features of EXTI controller are as follows:

- Support 11 software interrupt/event requests.
- Interrupts/events corresponding to each input line can be configured to trigger or mask independently.
- Each interrupt line has an independent state bit.
- Support for pulse or pending input types.
- 3 trigger events are supported: rising edge, falling edge, and double edge.
- Wake up MCU to exit low power mode.

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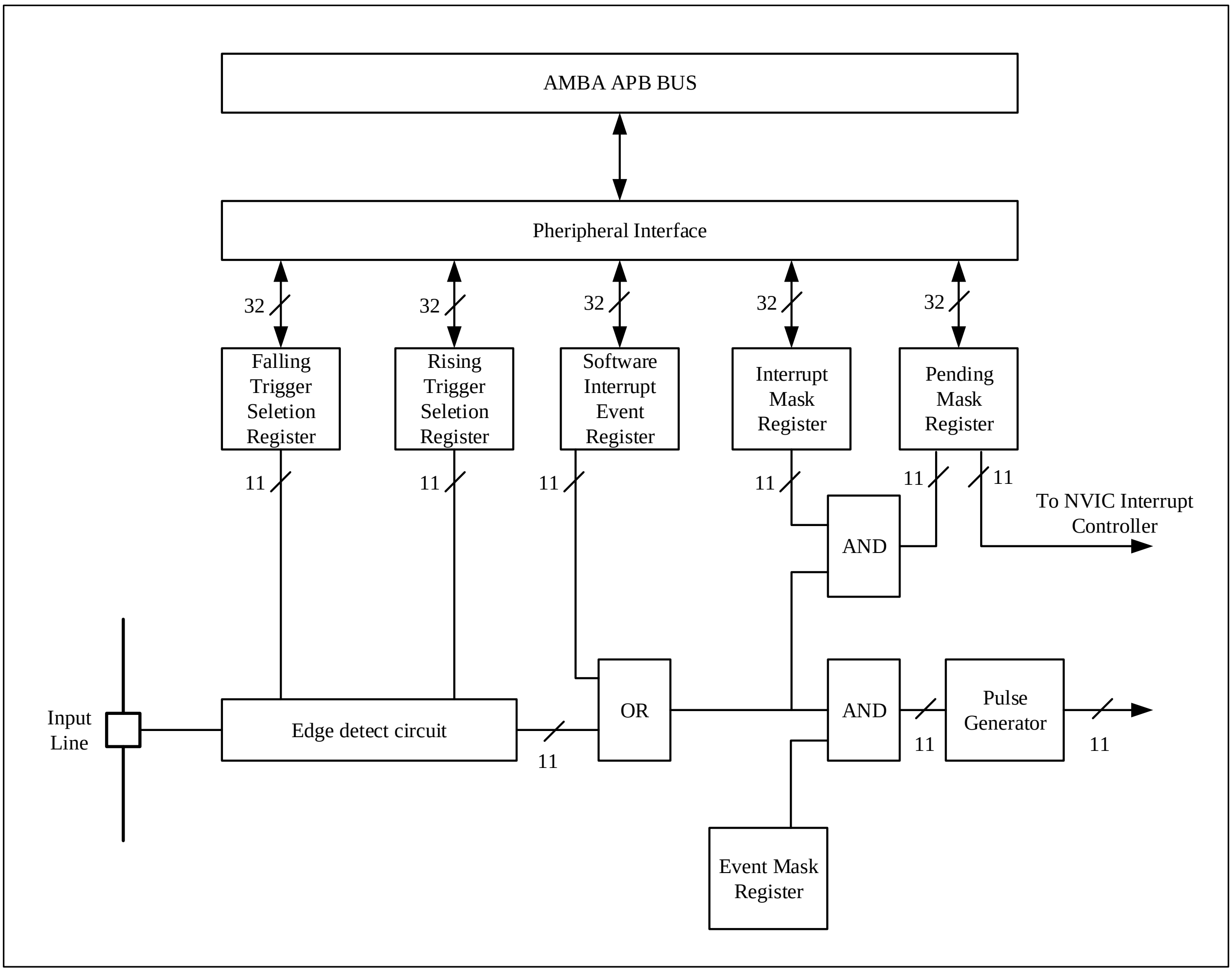
Figure 5-1 Extenal Interrupt/Event Controller Block Diagram



5.2.3 Functional Description

The EXTI contains 11 interrupt lines. To generate interrupts, the NVIC interrupt channel of the extended interrupt controller must be configured to enable the appropriate interrupt lines. Select rising edge, falling edge, or double edges trigger event types by edge trigger configuration registers EXTI_RT_CFG and EXTI_FT_CFG, and write '1' to the corresponding bit of interrupt masking register EXTI_IMASK to allow interrupt requests. When a preset edge trigger polarity is detected on the external interrupt line, an interrupt request is generated and the corresponding pending bit is set to '1'. Writing '1' to the corresponding bit of the pending register clears the interrupt request.

To generate an event, the corresponding event line must be configured and enabled. According to the desired edge detection polarity, set up the rise/fall edge trigger configuration register, while writing '1' in the corresponding bit of the event masking register to allow interrupt requests. When a preset edge occurs on an event line, an event request pulse is generated and the corresponding pending bit is not set to '1'.

In addition, interrupt/event requests can also be generated by software by writing a '1' in the software interrupt/event register.

- Hardware interrupt configuration, select and configure 11 lines as interrupt sources as required:
  - Configure the mask bit (EXTI_IMASK) for 11 interrupt lines.

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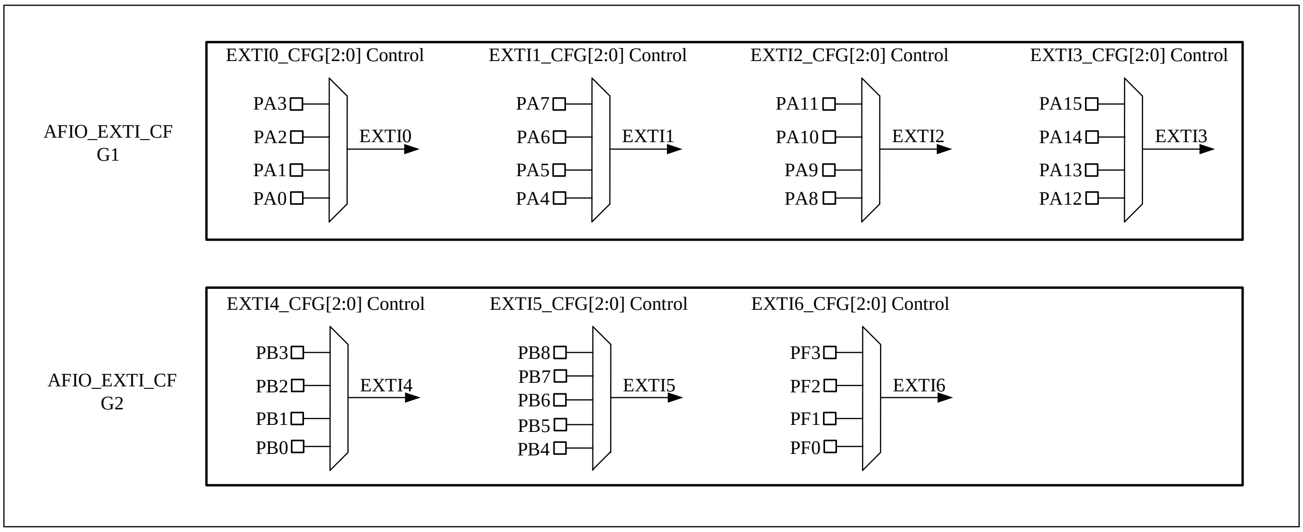
- Configure the Trigger Selection bits of the selected interrupt line (EXTI_RT_CFG and EXTI_FT_CFG);
- Configure the enable and mask bits of the NVIC interrupt channel corresponding to the external interrupt controller so that the requests in the 11 interrupt lines can be correctly responded to.

- Hardware event configuration: Select 11 lines as event sources as required:
  - Configure the mask bit (EXTI_EMASK) for 11 event lines.
  - Configure the Trigger Selection bits for the selected event line (EXTI_RT_CFG and EXTI_FT_CFG).
- Software interrupt/event configuration, select 11 lines as software interrupt/event lines as required:
  - Configure 11 interrupt/event line mask bits (EXTI_IMASK and EXTI_EMASK).
  - Configure the request bit of the software interrupt event register (EXTI_SWIE).

5.2.4 EXTI Line Mapping

Figure 5-2 External Interrupt Generic I/O Mapping



To configure external interrupts/events on GPIO lines, the AFIO clock must be enabled first. Connect the universal I/O ports to 7 external interrupt/event lines as shown in the diagram above. The connection mode of the other 4 EXTI lines is as follows:

- EXTI line 7 is connected to the PVD output
- EXTI line 8 is connected to the COMP interrupt/wake-up event
- EXTI line 9 is connected to the TIM6 interrupt/wake-up event
- EXTI line 10 is connected to the UART3 wake-up event

Note: When using COMP interrupts and TIM6 interrupts, the associated EXTI can only be configured as a rising edge trigger.

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5.3 EXTI Registers

5.3.1 EXTI Register Overview

Table 5-2 EXTI Register Overview

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x00	EXTI_EMASK	Reserved																					EMASKx										
0x04	EXTI_IMASK	Reserved																					IMASKx										
0x08	EXTI_FT_CFG	Reserved																					FT_CFGx										
0x0c	EXTI_RT_CFG	Reserved																					RT_CFGx										
0x10	EXTI_PEND	Reserved																					PENDx										
0x14	EXTI_SWIE	Reserved																					SWIEx										

5.3.2 EXTI Event Mask Register (EXTI_EMASK)

Address offset: 0x00

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved					EMASKx										
					rw										

BitField	Name	Description
31:11	Reserved	Reserved, the reset value must be maintained.
10:0	EMASKx	Event mask on line x (x = 0, 1, 2, …, 9, 10) 0: Masking the event requests from line x. 1: Not masking the event requests from line x.

5.3.3 EXTI Interrupt Mask Register (EXTI_IMASK)

Address offset: 0x04

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

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15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved					IMASKx										
					rw										

BitField	Name	Description
31:11	Reserved	Reserved, the reset value must be maintained.
10:0	IMASKx	Interrupt mask on line x (x = 0, 1, 2, …, 9, 10) 0: Masking the interrupt requests from line x. 1: Not masking the interrupt requests from line x.

5.3.4 EXTI Falling Edge Trigger Configuration Register (EXTI_FT_CFG)

Address offset: 0x08

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved					FT_CFGx										
					rw										

BitFild	Name	Description
31:11	Reserved	Reserved, the reset value must be maintained.
10:0	FT_CFGx	The falling edge on line x triggers the configuration bit (x = 0, 1, 2, …, 9, 10) 0: Disable falling edge triggering (interrupts and events) on input line x 1: Enable falling edge triggering (interrupts and events) on input line x

5.3.5 EXTI Rising Edge Trigger Configuration Register (EXTI_RT_CFG)

Address offset: 0x0C

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved					RT_CFGx										
					rw										

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BitField	Name	Description
31:11	Reserved	Reserved, the reset value must be maintained.
10:0	RT_CFGx	The rising edge on line x triggers the configuration bit (x = 0, 1, 2, …, 9, 10) 0: Disable rising edge triggering (interrupts and events) on input line x 1: Enable rising edge triggering (interrupts and events) on input line x

5.3.6 EXTI Pending Register (EXTI_PEND)

Address offset: 0x10

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved					PENDx										
					rc_w1										

BitField	Name	Description
31:11	Reserved	Reserved, the reset value must be maintained.
10:0	PENDx	Pending bit on line x (x = 0, 1, 2, …, 9, 10) 0: No pending request has occurred 1: A pending trigger request occurred This bit is set to '1' when a selected edge trigger event occurs on the external interrupt line. It can be cleared by writing '1' to the bit, or by changing the polarity of the edge detection.

5.3.7 EXTI Software Interrupt Event Register (EXTI_SWIE)

Address offset: 0x14

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved					SWIEx										
					rw										

BitField	Name	Description
31:11	Reserved	Reserved, the reset value must be maintained.
10:0	SWIEx	Software interrupt on line x (x = 0, 1, 2, …, 9, 10)

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BitField	Name	Description
		When the bit is' 0 ', writing '1' sets the corresponding pending bit in EXTI_PEND. If this interrupt is allowed in EXTI_IMASK and EXTI_EMASK, an interrupt will be generated. *Note: This bit can be cleared to '0' by writing '1' to clear the corresponding bit of EXTI_PEND.*

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6 GPIO and AFIO

6.1 Overview

GPIO refers to General Purpose Input/Output, AFIO refers to Alternate Function Input/Output. The chip supports up to 29 GPIOs, divided into three groups (GPIOA/GPIOB/GPIOF), Group A has 16 ports per group, Group B has 9 ports per group, and Group F has a total of 4 ports. GPIO ports share pins with other multiplexed peripherals, allowing users to configure them flexibly according to their needs. Each GPIO pin can be independently configured as an output, input, or a multiplexed peripheral function port. Apart from analog input pins, all other GPIO pins have the capability to handle high current.

The GPIO main features:

- GPIO ports can be individually configured by software into the following modes
  - Input floating
  - Input pull-up
  - Input pull-down
  - Analog
  - Push-pull output with selectable pull-up/pull-down
  - Push-pull alternate function with selectable pull-up/pull-down
  - Open-drain alternate function with selectable pull-up/pull-down (Only I2C related multiplexing support)
- Individual bit set/clear function
- All I/O support external interrupt
- All I/O support low-power mode wake-up, with configurable rising or falling edge
  - All EXTIs can be awakened, all GPIO can be configured to EXTI0~6, and 7 wake-up sources can be recorded (PA0~PA3: Group 1, PA4~PA7: Group 2, PA8~PA11: Group 3, PA12~PA15: Group 4, PB0~PB3: Group 5, PB4~PB8: Group 6, PF0~PF3: Group 7)
- Supports software remapping of I/O alternate functions
- Supports GPIO locking mechanism, lock state can be cleared by reset mode

Each I/O port bit can be programmed arbitrarily, but the registers must be accessed in 32-bit words (not allowing 16-bit half-word or 8-bit byte access). The following diagram illustrates the basic structure of an I/O port.

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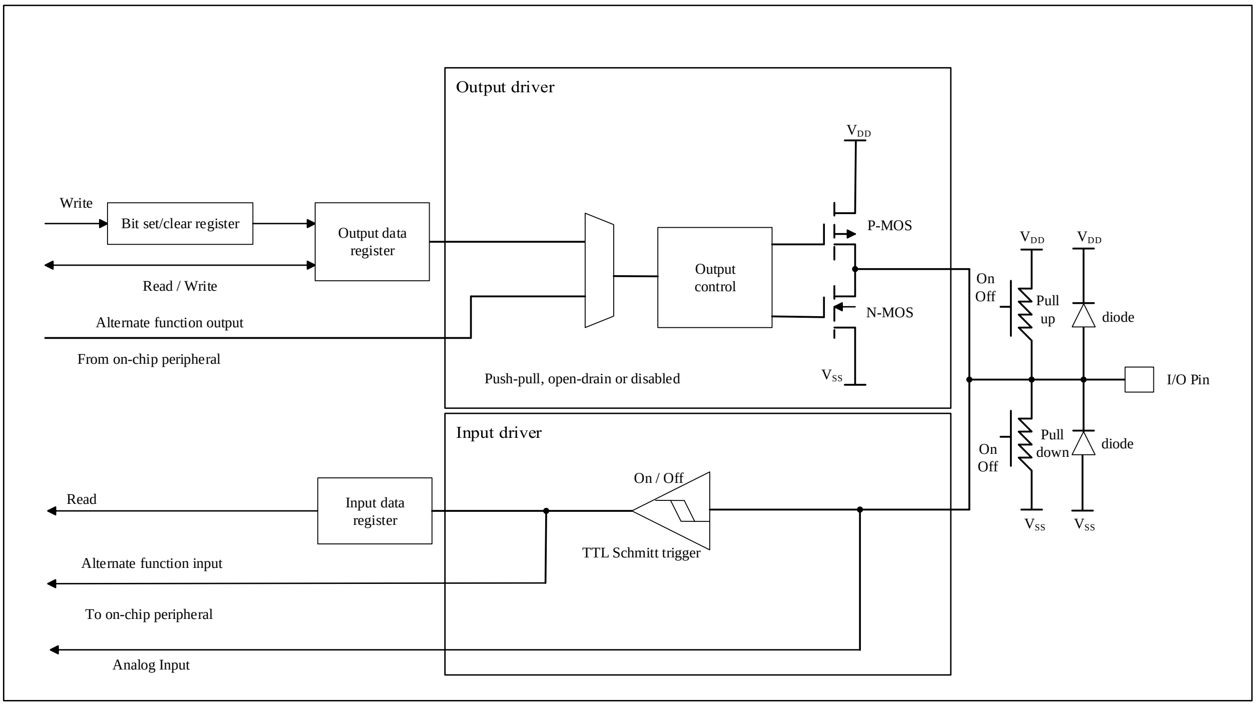
Figure 6-1 Basic Structure of I/O Ports (Fail-safe Not Supported)



6.2 Function Description

6.2.1 IO Mode Configuration

The mode control of I/O is set by configuration registers GPIOx_PMODE, GPIOx_POTYPE, and GPIOx_PUPD (x=A, B, F). The configurations for different operating modes are shown in the table below:

Table 6-1 I/O Relationship Between Mode and Configuration

PMODE[1:0]	POTYPE	PUPD[1:0]		I/O Configuration
01	0	0	0	General Output Push-Pull
	0	0	1	General Output Push-Pull + Pull-Up
	0	1	0	General Output Push-Pull + Pull-Down
	0	1	1	Reserved
	1	x	x	Reserved
10	0	0	0	Push-Pull alternate function
	0	0	1	Push-Pull alternate function + Pull-Up
	0	1	0	Push-Pull alternate function + Pull-Down
	0	1	1	Reserved
	1	0	0	Open-Drain alternate function
	1	0	1	Open-Drain alternate function + Pull-Up
	1	1	0	Open-Drain alternate function + Pull-Down
	1	1	1	Reserved
00	x	0	0	Input Floating
	x	0	1	Input Pull-up

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PMODE[1:0]	POTYPE	PUPD[1:0]		I/O Configuration
	x	1	0	Input Pull-down
	x	1	1	Reserved
11	x	0	0	Analog mode
	x	0	1	Reserved
	x	1	0	
	x	1	1	

Additionally, the GPIOx_DS.DSy bit can be used to configure high/low drive strength, and the GPIOx_SR.SRy bit can be used to configure high/low slew rate.

The characteristics of I/O under different configurations are shown in the table below:

Table 6-2 Input/Output Characteristics Under Different Configurations

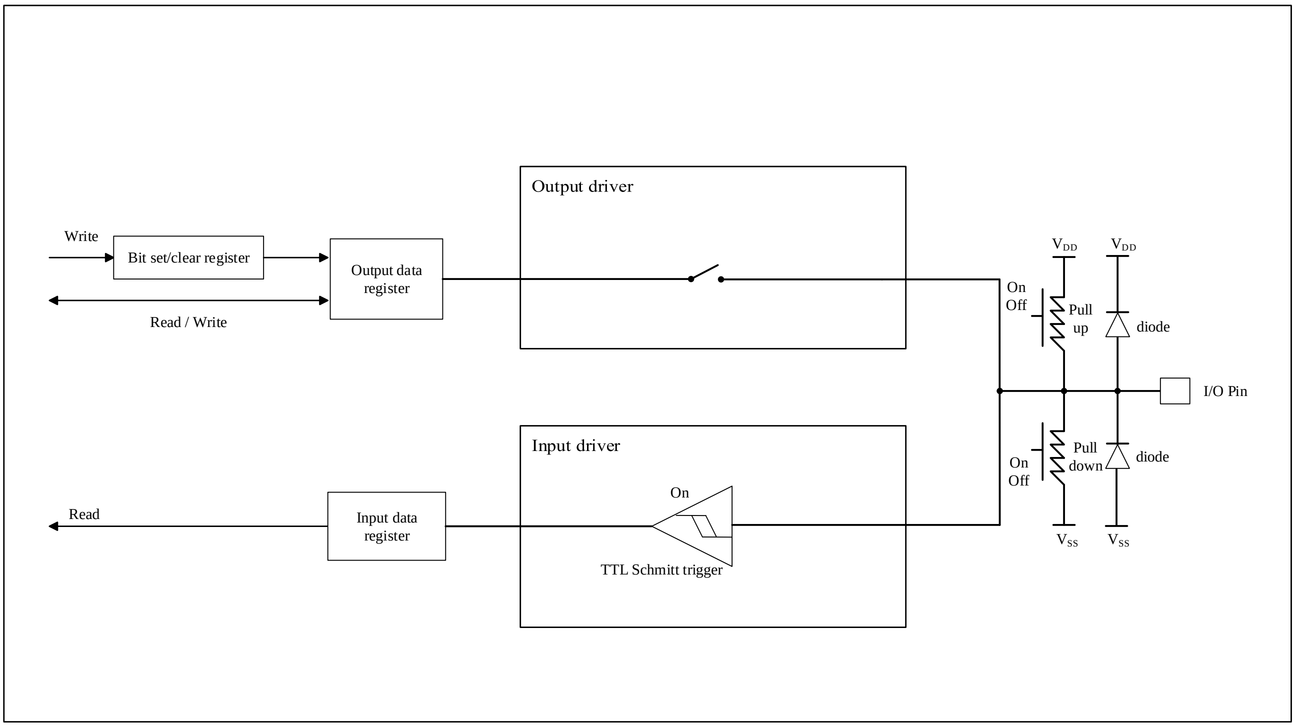
Characteristics	GPIO Input	GPIO Output	Analog	Peripheral alternate function
Output buffer	Disable	Enable	Disable	Configured according to the peripheral function
Schmitt trigger	Enable	Enable	Disable Output is 0	Enable
Pull-up/Pull-down	Configurable	Configurable	Disable	Configured according to the peripheral function
Open-drain	Disable	Configurable, When the output data is "0", the GPIO outputs 0, and when it is "1", the GPIO is in high-Z state.	Disable	Configurable, When the output data is "0", the GPIO outputs 0, and when it is "1", the GPIO is in high-Z state.
Push-pull	Disable	Configurable, When the output data is "0", the GPIO outputs 0, and when it is "1", the GPIO outputs 1.	Disable	Configurable, When the output data is "0", the GPIO outputs 0, and when it is "1", the GPIO outputs 1.
Input Data Register(IO Status)	RO	RO	Read Only 0	Readable
Output Data Register (Output Value)	Invalid	RW	Invalid	Readable

6.2.1.1 Input mode

When the I/O port is configured in input mode:

- Output buffer is disabled
- Schmitt trigger input is activated
- Whether the pull-up and pull-down resistors are connected depends on the configuration of the GPIOx_PUPD register.
- The data present on the I/O pin is sampled into the input data register at each AHB clock.
- Reading from the input data register retrieves the I/O status.

Figure 6-2 Input Floating/Pull-Up/Pull-Down Mode (Fail-safe Not Supported)



6.2.1.2 Output mode

When the I/O port is configured in output mode:

- Schmitt trigger input is activated
- Whether the pull-up and pull-down resistors are connected depends on the configuration of the GPIOx_PUPD register
- Output buffer is activated
  - Open-drain mode(I2C only supported)：

    '0' in the output data register activates the N-MOS, causing the pin to output a low level

    '1' in the output data register puts the port in a high-impedance state (P-MOS is never activated)
  - Push-pull mode：

    '0' in the output data register activates the N-MOS, causing the pin to output a low level

    '1' in the output data register activates the P-MOS, causing the pin to output a high level
- The data present on the I/O pin is sampled into the input data register at each AHB clock
- Reading from the input data register retrieves the I/O status
- Reading from the output data register retrieves the last written value

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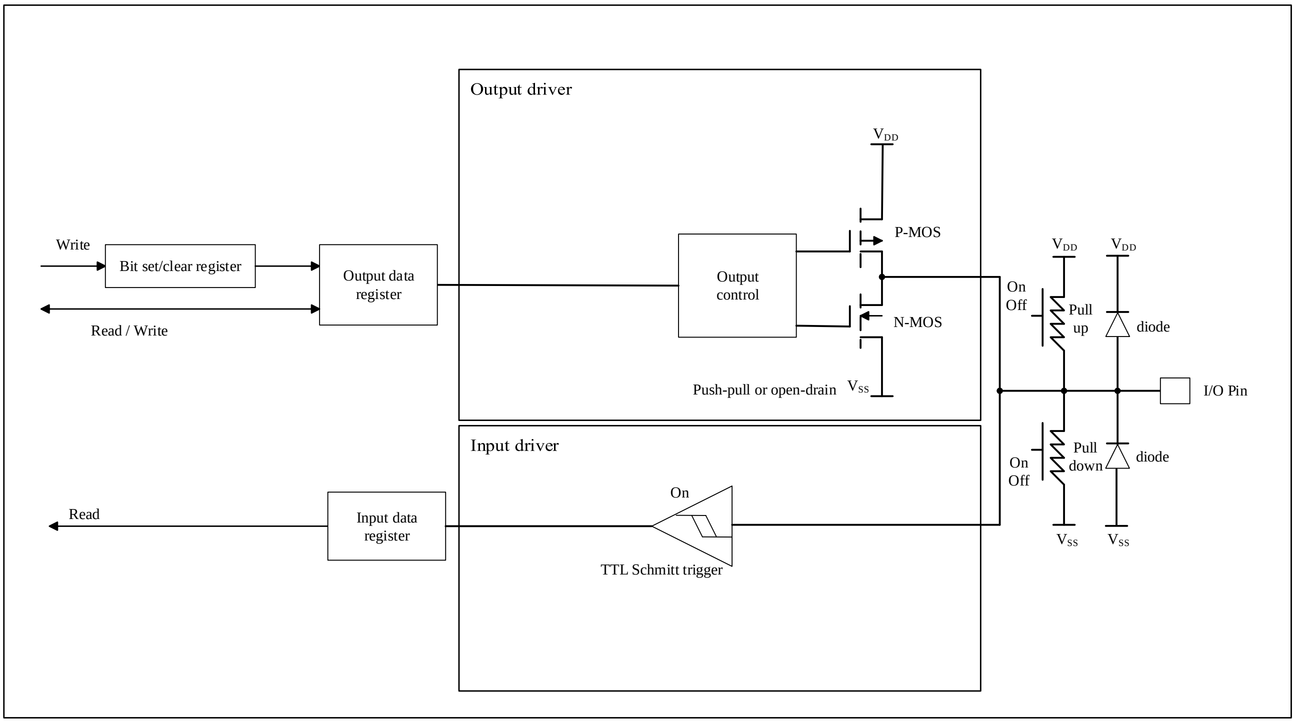
Figure 6-3 Output Mode (Fail-safe Not Supported)



6.2.1.3 Alternate function mode

When the I/O port is configured in alternate function mode:

- Schmitt trigger input is activated
- Whether the pull-up and pull-down resistors are connected depends on the configuration of the GPIOx_PUPD register
- In open-drain or push-pull configurations, the output buffer is controlled by the peripheral
- Built-in peripheral signals drive the output buffer
- At each AHB clock cycle, the data present on the I/O pins are sampled into the input data register
- Reading from the input data register retrieves the I/O status
- Reading from the output data register retrieves the last written value

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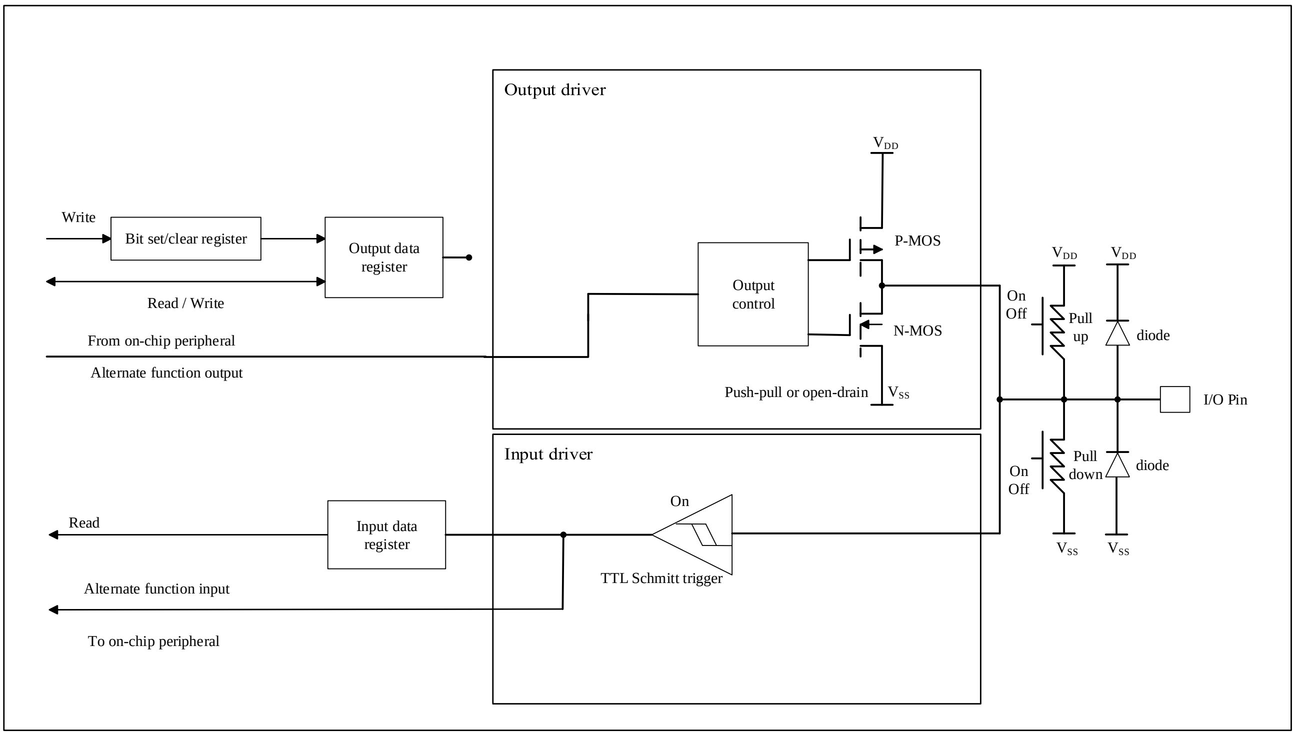
Figure 6-4 Alternate Function Mode (Fail-safe Not Supported)



6.2.1.4 Analog function mode

When the I/O port is configured in analog function mode:

- Pull-up and pull-down resistors are disabled
- Reading the input data register yields a value of '0'
- The output buffer is disabled
- Schmitt trigger input is disabled, and the output value is forced to '0' (achieving zero consumption on each analog I/O pin)

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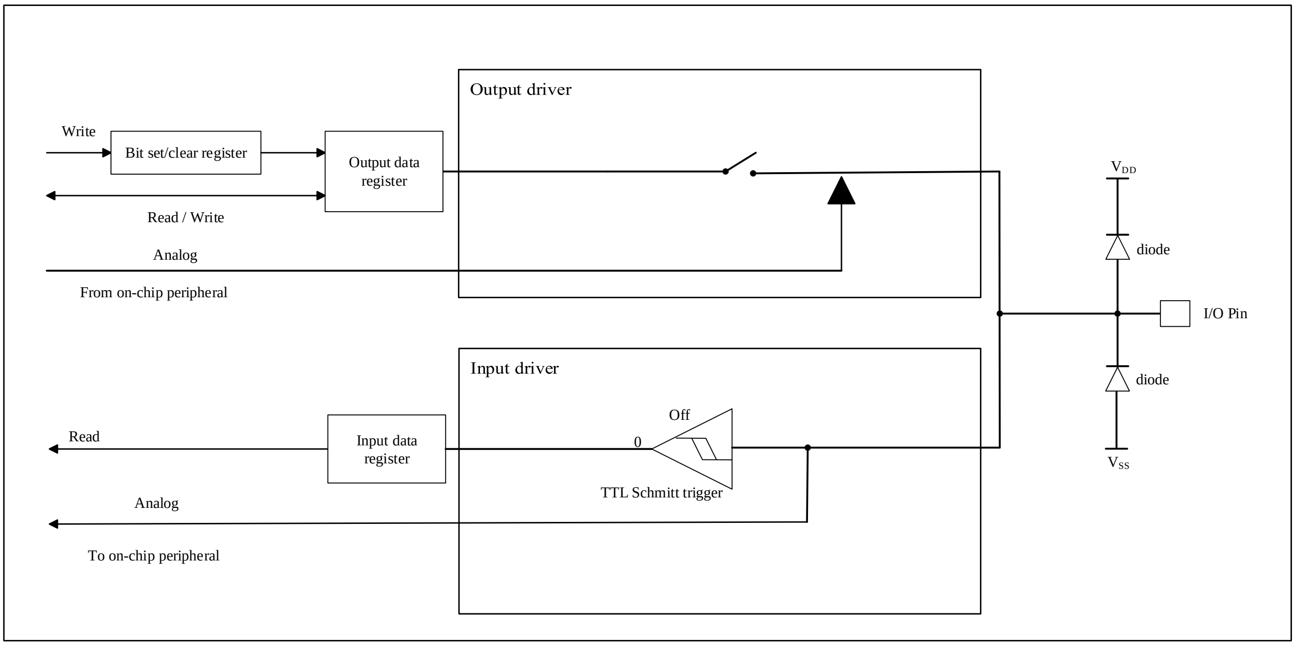
Figure 6-5 High-impedance Analog Function Mode (Fail-safe Not Supported)



6.2.2 Status After Reset

During and immediately after reset, the alternate function is not enabled, and the I/O port is configured in analog function mode(GPIOx_PMODE.PMODEx[1:0]=2’b11). But there are a few exceptions:

- NRST(PF3):
  - FLASH_OB.NRST_PF3=1 (default value): Pull up as NRST input
  - FLASH_OB.NRST_PF3=0:As a regular GPIO, it cannot be connected to a low level during power on when used as an input (otherwise the chip will remain in a reset state)
- After reset, the pins related to the debug system are configured by default as SWD interface I/O configuration:
  - PA14: SWCLK is set to input pull-down mode
  - PA13: SWDIO is set to input pull-up mode
- PF2/BOOT0:
  - During chip startup, PF2 functions as BOOT0 by default in pull-down input mode. After chip initialization, it is used as a general GPIO and configured in analog function mode.

6.2.3 Individual Bit Set and Clear

Individual bits in the data register (GPIOx_POD) can be manipulated by writing '1' to the desired bits in the bit set/clear register (GPIOx_PBSC) and bit clear register (GPIOx_PBC). This allows for individual bit operations on one or multiple bits. The bits written as '1' will be set or cleared accordingly, while the bits not written as '1' will remain unchanged. Software does not need to disable interrupts and the operation can be completed in a single AHB write operation.

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6.2.4 External Interrupt/Wake-up Lines

All ports have external interrupt capability, which can be configured in the EXTI module as follows:

- Ports must be configured in input mode
- All ports can be configured for wake-up in STOP mode, supporting configurable rising or falling edges
- General I/O ports are connected to 7 external interrupt/event lines in the manner shown in Figure 5-2, configured by the AFIO_EXTI_CFGx register.

6.2.5 Alternate Function

When the I/O port is configured in alternate function mode, the port bit configuration registers (GPIOx_AFL/GPIOx_AFH, GPIOx_PMODE, GPIOx_POTYPE, and GPIOx_PUPD) must be configured before use. The determination of whether the alternate function is used for input or output is determined by the peripheral.

Table 6-3 External Interrupt Universal I/O Image

EXTI line 0 is connected to:	PA0、PA1、PA2、PA3
EXTI line 1 is connected to:	PA4、PA5、PA6、PA7
EXTI line 2 is connected to:	PA8、PA9、PA10、PA11
EXTI line 3 is connected to:	PA12、PA13、PA14、PA15
EXTI line 4 is connected to:	PB0、PB1、PB2、PB3
EXTI line 5 is connected to:	PB4、PB5、PB6、PB7、PB8
EXTI line 6 is connected to:	PF0、PF1、PF2、PF3

6.2.5.1 Software remapping I/O alternate function

To enhance the flexibility of multiplexed peripheral functions across different device packages, it is possible to Remapping some peripheral functions to other pins. Each I/O has up to 16 multiplexed functions (AF0~ AF15). After reset, except for PA13 and PA14, AFSELy defaults to AF15. The multiplexed I/O functions can be Remappingped by software configuration of the corresponding registers (GPIOx_AFL/AFH).

At this point, the alternate functions are no longer mapped to their original pins. For the IO Remappingping feature of peripherals, if Remappingped to a different pin, the input is multiplexed to the Remappingped pin, and the output is connected to the Remappingped location, disconnecting the original location.

6.2.5.2 SWD alternate function I/O remapping

Table 6-4 SWD Alternate Function I/O Remapping

Alternate Function	I/O	Remapping
SWDIO	PA13	AF0
SWCLK	PA14	AF0

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6.2.5.3 TIMx alternate function I/O remapping

6.2.5.3.1 TIM1 alternate function I/O remapping

Table 6-5 TIM1 Alternate Function I/O Remapping

Alternate Function	I/O	Remapping
TIM1_ETR	PA12	AF3
TIM1_BKIN1	PA2	AF2
TIM1_BKIN2	PA6	AF3
TIM1_BKIN3	PA11	AF1
TIM1_BKIN4	PA12	AF1
TIM1_CH1	PA15	AF1
	PA4	AF3
	PA8	AF3
	PB3	AF1
	PB4	AF1
	PB5	AF1
	PB6	AF1
	PB7	AF1
	PB8	AF1
	PF2	AF1
TIM1_CH2	PA3	AF3
	PA9	AF3
	PA15	AF7
	PB3	AF7
	PB4	AF7
	PB5	AF7
	PB6	AF7
	PB7	AF7
	PB8	AF7
	PF2	AF7
TIM1_CH3	PA5	AF3
	PA10	AF3
	PA15	AF9
	PB3	AF9
	PB4	AF9
	PB5	AF9
	PB6	AF9
	PB7	AF9
	PB8	AF9
	PF2	AF9
TIM1_CH4	PA11	AF3
	PA15	AF11
	PB3	AF11

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	PB4	AF11
	PB5	AF11
	PB6	AF11
	PB7	AF11
	PB8	AF11
	PF2	AF11
TIM1_CH5	PA0	AF3
TIM1_CH6	PA1	AF3
TIM1_CH7	PA2	AF3
TIM1_CH1N	PA7	AF3
	PA15	AF5
	PB3	AF5
	PB4	AF5
	PB5	AF5
	PB6	AF5
	PB7	AF5
	PB8	AF5
	PF2	AF5
TIM1_CH2N	PA5	AF1
	PA15	AF8
	PB0	AF1
	PB3	AF8
	PB4	AF8
	PB5	AF8
	PB6	AF8
	PB7	AF8
	PB8	AF8
	PF2	AF8
TIM1_CH3N	PA15	AF10
	PB1	AF1
	PB3	AF10
	PB4	AF10
	PB5	AF10
	PB6	AF10
	PB7	AF10
	PB8	AF10
	PF2	AF10
TIM1_CH4N	PA15	AF12
	PB3	AF12
	PB4	AF12
	PB5	AF12
	PB6	AF12
	PB7	AF12

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	PB8	AF12
	PF2	AF12

6.2.5.3.2 TIM3 alternate function I/O remapping

Table 6-6 TIM3 Alternate Function I/O Remapping

Alternate Function	IO	Remapping
TIM3_ETR	PB3	AF2
	PF0	AF11
	PA1	AF10
TIM3_CH1	PA0	AF11
	PA4	AF11
	PA6	AF11
	PA14	AF11
	PB4	AF2
	PF0	AF0
TIM3_CH2	PA1	AF11
	PA7	AF11
	PA13	AF11
	PB5	AF2
	PF1	AF0
TIM3_CH3	PA2	AF11
	PB6	AF2
	PB1	AF10
	PB0	AF11
	PF3	AF0
TIM3_CH4	PB7	AF2
	PB8	AF2
	PB2	AF10
	PB1	AF11

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6.2.5.3.3 TIM4 alternate function I/O remapping

Table 6-7 TIM4 Alternate Function I/O Remapping

Alternate Function	IO	Remapping
TIM4_ETR	PF1	AF12
	PF3	AF12
TIM4_CH1	PA15	AF6
	PA0	AF12
	PA14	AF12
TIM4_CH2	PA1	AF12
	PA13	AF12
	PB3	AF6
TIM4_CH3	PA2	AF12

6.2.5.4 UARTx alternate function I/O remapping

6.2.5.4.1 UART1 alternate function I/O remapping

Table 6-8 UART1 Alternate Function I/O Remapping

Alternate Function	I/O	Remapping
UART1_TX	PA1	AF1
	PA2	AF1
	PA9	AF4
	PA14	AF4
	PB6	AF4
	PF0	AF2
UART1_RX	PA0	AF1
	PA3	AF1
	PA10	AF4
	PA13	AF4
	PA15	AF4
	PB7	AF4
	PF1	AF2
UART1_DE	PA4	AF1
	PA8	AF4
	PF3	AF2

6.2.5.4.2 UART2 alternate function I/O remapping

Table 6-9 UART2 Alternate Function I/O Remapping

Alternate Function	I/O	Remapping
UART2_TX	PA14	AF1
	PA1	AF4

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Alternate Function	I/O	Remapping
	PA2	AF4
	PA9	AF10
	PF0	AF3
UART2_RX	PA13	AF1
	PA15	AF3
	PA0	AF4
	PA3	AF4
	PA10	AF10
	PF1	AF3
UART2_DE	PA4	AF4
	PA8	AF10
	PF3	AF3

6.2.5.4.3 UART3 alternate function I/O remapping

Table 6-10 UART3 Alternate Function I/O Remapping

Alternate Function	I/O	Remapping
UART3_TX	PA1	AF6
	PA2	AF6
	PA4	AF6
	PA6	AF6
	PA14	AF6
	PB3	AF4
	PB5	AF4
	PF0	AF4
UART3_RX	PA0	AF6
	PA3	AF6
	PA7	AF6
	PA13	AF6
	PB7	AF3
	PB4	AF4
	PF1	AF4
UART3_DE	PF3	AF4

6.2.5.5 I2Cx alternate function I/O remapping

6.2.5.5.1 I^{2}C1 alternate function I/O remapping

Table 6-11 I^{2}C1 Alternate Function I/O Remapping

Alternate Function	I/O	Remapping
I2C1_SCL	PA9	AF6
	PA4	AF7

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	PB6	AF6
	PB8	AF6
	PF1	AF1
I2C1_SDA	PA10	AF6
	PA5	AF7
	PA13	AF7
	PB7	AF6
	PF0	AF1
I2C1_SMBA	PA1	AF7
	PA14	AF7
	PB2	AF6
	PB5	AF6

6.2.5.5.2 I^2C2 alternate function I/O remapping

Table 6-12 I^2C2 Alternate Function I/O Remapping

Alternate Function	I/O	Remapping
I2C2_SCL	PA6	AF7
	PA9	AF7
	PA11	AF7
I2C2_SDA	PA7	AF7
	PA10	AF7
	PA12	AF7
I2C2_SMBA	PB2	AF7

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6.2.5.6 SPIx alternate function I/O remapping

6.2.5.6.1 SPI1 alternate function I/O remapping

Table 6-13 SPI1 Alternate Function I/O Remapping

Alternate Function	I/O	Remapping
SPI1_NSS	PA1	AF0
	PA4	AF0
	PA15	AF0
SPI1_SCK	PA0	AF0
	PA5	AF0
	PA13	AF5
	PB3	AF0
SPI1_MISO	PA3	AF0
	PA6	AF0
	PA1	AF5
	PA4	AF5
	PA14	AF5
	PB4	AF0
SPI1_MOSI	PA2	AF0
	PA7	AF0
	PA5	AF5
	PB1	AF0
	PB5	AF0

6.2.5.6.2 SPI2 alternate function I/O remapping

Table 6-14 SPI2 Alternate Function I/O Remapping

Alternate Function	I/O	Remapping
SPI2_NSS	PA8	AF0
	PA7	AF5
SPI2_SCK	PA9	AF0
	PB0	AF0
SPI2_MISO	PA10	AF0
	PA12	AF0
SPI2_MOSI	PA11	AF0
	PB1	AF5

6.2.5.7 COMPx alternate function I/O remapping

Table 6-15 COMP Alternate Function I/O Remapping

Alternate Function	I/O	Remapping
COMP_OUT	PA0	AF8

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Alternate Function	I/O	Remapping
	PA6	AF8
	PA11	AF8
	PA12	AF8

6.2.5.8 EVENT_OUT alternate function I/O remapping

Table 6-16 EVENTOUT Alternate Function I/O Remapping

Alternate Function	I/O	Remapping
EVENT_OUT	PA1	AF9
	PA6	AF9
	PA12	AF9
	PB4	AF3

6.2.5.9 MCO alternate function I/O remapping

Table 6-17 RCC Alternate Function I/O Remapping

Alternate Function	I/O	Remapping
MCO	PA8	AF5
	PA9	AF5

6.2.5.10 ADC alternate function I/O remapping

External trigger sources for ADC regular conversions support all GPIOs.

6.2.6 I/O Configuration of Peripherals

Table 6-18 ADC

ADC	GPIO Configuration
ADC	Analog function mode

Table 6-19 TIM1/3/4

TIM1 Pins	Configuration	GPIO Configuration
TIM1_CHx	Input capture channel x	Push-pull alternate function
	Output compare channel x	Push-pull alternate function
TIM1_CHxN	Complementary output channel x	Push-pull alternate function
TIM1_BKIN	Brake input	Input mode + alternate function
TIM1_ETR	External trigger clock input	Input mode + alternate function

Table 6-20 UART

UART Pins	Configuration	GPIO Configuration
UARTx_TX	Full-duplex mode	Push-pull alternate function
	Half-duplex mode	Push-pull alternate function + pull up
UARTx_RX	Full-duplex mode	Push-pull alternate function

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UART Pins	Configuration	GPIO Configuration
	Half-duplex mode	Not used, can be used as general I/O
UARTx_DE	Full-duplex mode	Push-pull alternate function
	Half-duplex mode	Push-pull alternate function + pull up

Table 6-21 I^2C

I^2C Pins	Configuration	GPIO Configuration
I2Cx_SCL	I^2C clock	Open-drain alternate function
I2Cx_SDA	I^2C data	Open-drain alternate function

Table 6-22 SPI

SPI Pins	Configuration	GPIO Configuration
SPIx_SCK	Master mode	Push-pull alternate function
	Slave mode	Push-pull alternate function
SPIx_MOSI	Full-duplex mode / master mode	Push-pull alternate function
	Full-duplex mode / slave mode	Push-pull alternate function
	Single-wire bidirectional data line / master mode	Push-pull alternate function
	Single-wire bidirectional data line / slave mode	Not used, can be used as general I/O
SPIx_MISO	Full-duplex mode / master mode	Push-pull alternate function
	Full-duplex mode / slave mode	Push-pull alternate function
	Single-wire bidirectional data line / master mode	Not used, can be used as general I/O
	Single-wire bidirectional data line / slave mode	Push-pull alternate function
SPIx_NSS	Hardware master/slave mode	Push-pull alternate function
	Software mode	Not used, can be used as general I/O

Table 6-23 COMP

COMPx Pins	Configuration	GPIO Configuration
COMPx_OUT	COMP output	Push-pull alternate function
COMPx_INM	COMP negative input.	Analog mode
COMPx_INP	COMP positive input	Analog mode

Table 6-24 Others

Pins	Configuration	GPIO Configuration
MCO	Clock output	Push-pull alternate function
EXTI lines	External interrupt input	Floating input + pull-up/pull-down

6.2.7 GPIO Locking Mechanism

The locking mechanism is used to freeze the IO configuration to prevent accidental changes. When a lock (LOCK) operation is performed on a port bit, the configuration of the port cannot be changed until the next reset, referring to the port configuration locking register GPIOx_PLOCK.

- GPIOx_PLOCK.PLOCKK bit will only become 1 after the correct sequence of operations w1->w0->w1->r0 (here r0 must be included); thereafter, it will only become 0 after a system reset.
- GPIOx_PLOCK.PLOCKK must be 0, indicating unlocked, in order to modify GPIOx_PLOCK.PLOCK[15:0].

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- GPIOx_PLOCK.PLOCK will only be effective when writing simultaneously with a non-zero value to GPIOx_PLOCK.PLOCK[15:0] in the sequence w1->w0->w1->r0; during the sequence write, GPIOx_PLOCK.PLOCK[15:0] must not change.
- As long as GPIOx_PLOCK.PLOCKK = 0, the bits of GPIOx_PMODE / GPIOx_POTYPE / GPIOx_PUPD / GPIOx_AFL / GPIOx_AFH can be modified, unaffected by the configuration of GPIOx_PLOCK.PLOCK[15:0].
- When GPIOx_PLOCK.PLOCKK = 1, GPIOx_PMODE / GPIOx_POTYPE / GPIOx_PUPD / GPIOx_AFL / GPIOx_AFH are controlled by GPIOx_PLOCK.PLOCK[15:0]. When GPIOx_PLOCK.PLOCKy (y = 0…15) = 1, the configuration is locked and cannot be modified; when PLOCKy = 0, it can be modified.
- If the sequence operation is incorrect, the lock operation must be re-initiated with w1->w0->w1->r0.

6.3 GPIO Registers

These peripheral registers must be accessed in 32-bit words.

6.3.1 GPIO Register Overview

GPIO Base Address：0x4002 3000

Table 6-25 GPIO Register Overvie

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x00	GPIOA_PMODE	PMODE15		PMODE14		PMODE13		PMODE12		PMODE11		PMODE10		PMODE9		PMODE8		PMODE7		PMODE6		PMODE5		PMODE4		PMODE3		PMODE2		PMODE1		PMODE0	
0x100	GPIOB_PMODE	Reserved														PMODE8		PMODE7		PMODE6		PMODE5		PMODE4		PMODE3		PMODE2		PMODE1		PMODE0	
0x200	GPIOF_PMODE	Reserved																								PMODE3		PMODE2		PMODE1		PMODE0	
0x04	GPIOA_POTYPE	Reserved																	POT14	POT13	POT12	POT11	POT10	POT9	Reserved	POT7	POT6	POT5	POT4	Reserved		POT1	Reserved
0x104	GPIOB_POTYPE	Reserved																							POT8	POT7	POT6	POT5	Reserved		POT2	Reserved	
0x204	GPIOF_POTYPE	Reserved																														POT1	POT0
0x0C	GPIOA_PUPD	PUPD15		PUPD14		PUPD13		PUPD12		PUPD11		PUPD10		PUPD9		PUPD8		PUPD7		PUPD6		PUPD5		PUPD4		PUPD3		PUPD2		PUPD1		PUPD0	
0x10C	GPIOB_PUPD	Reserved														PUPD8		PUPD7		PUPD6		PUPD5		PUPD4		PUPD3		PUPD2		PUPD1		PUPD0	
0x20C	GPIOF_PUPD	Reserved																								PUPD3		PUPD2		PUPD1		PUPD0	
0x10	GPIOA_PID	Reserved																PID15	PID14	PID13	PID12	PID11	PID10	PID9	PID8	PID7	PID6	PID5	PID4	PID3	PID2	PID1	PID0
0x110	GPIOB_PID	Reserved																							PID8	PID7	PID6	PID5	PID4	PID3	PID2	PID1	PID0
0x210	GPIOF_PID	Reserved																												PID3	PID2	PID1	PID0
0x14	GPIOA_POD	Reserved																POD1	POD1	POD1	POD1	POD1	POD1	POD9	POD8	POD7	POD6	POD5	POD4	POD3	POD2	POD1	POD0
0x114	GPIOB_POD	Reserved																							POD	POD	POD	POD	POD	POD	POD	POD	POD
0x214	GPIOF_POD	Reserved																												POD	POD	POD	POD

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<table>
<tr><td>0x18</td><td>GPIOA_PBSC</td><td>PBC1</td><td>PBC1</td><td>PBC1</td><td>PBC1</td><td>PBC1</td><td>PBC1</td><td>PBC9</td><td>PBC8</td><td>PBC7</td><td>PBC6</td><td>PBC5</td><td>PBC4</td><td>PBC3</td><td>PBC2</td><td>PBC1</td><td>PBC0</td><td>PBS15</td><td>PBS14</td><td>PBS13</td><td>PBS12</td><td>PBS11</td><td>PBS10</td><td>PBS9</td><td>PBS8</td><td>PBS7</td><td>PBS6</td><td>PBS5</td><td>PBS4</td><td>PBS3</td><td>PBS2</td><td>PBS1</td><td>PBS0</td></tr>
<tr><td>0x118</td><td>GPIOB_PBSC</td><td colspan="7">Reserved</td><td>PBC</td><td>PBC</td><td>PBC</td><td>PBC</td><td>PBC</td><td>PBC</td><td>PBC</td><td>PBC</td><td>PBC</td><td colspan="7">Reserved</td><td>PBS8</td><td>PBS7</td><td>PBS6</td><td>PBS5</td><td>PBS4</td><td>PBS3</td><td>PBS2</td><td>PBS1</td><td>PBS0</td></tr>
<tr><td>0x218</td><td>GPIOF_PBSC</td><td colspan="12">Reserved</td><td>PBC</td><td>PBC</td><td>PBC</td><td>PBC</td><td colspan="12">Reserved</td><td>PBS3</td><td>PBS2</td><td>PBS1</td><td>PBS0</td></tr>
<tr><td>0x1C</td><td>GPIOA_PLOCK</td><td colspan="15">Reserved</td><td>PLOCK</td><td>PLOCK1</td><td>PLOCK1</td><td>PLOCK1</td><td>PLOCK1</td><td>PLOCK1</td><td>PLOCK1</td><td>PLOCK9</td><td>PLOCK8</td><td>PLOCK7</td><td>PLOCK6</td><td>PLOCK5</td><td>PLOCK4</td><td>PLOCK3</td><td>PLOCK2</td><td>PLOCK1</td><td>PLOCK0</td></tr>
<tr><td>0x11C</td><td>GPIOB_PLOCK</td><td colspan="15">Reserved</td><td>PLOCK</td><td colspan="7">Reserved</td><td>PLOCK</td><td>PLOCK</td><td>PLOCK</td><td>PLOCK</td><td>PLOCK</td><td>PLOCK</td><td>PLOCK</td><td>PLOCK</td><td>PLOCK</td></tr>
<tr><td>0x21C</td><td>GPIOF_PLOCK</td><td colspan="15">Reserved</td><td>PLOCK</td><td colspan="12">Reserved</td><td>PLOCK</td><td>PLOCK</td><td>PLOCK</td><td>PLOCK</td></tr>
<tr><td>0x20</td><td>GPIOA_AFL</td><td colspan="4">AFSEL7</td><td colspan="4">AFSEL6</td><td colspan="4">AFSEL5</td><td colspan="4">AFSEL4</td><td colspan="4">AFSEL3</td><td colspan="4">AFSEL2</td><td colspan="4">AFSEL1</td><td colspan="4">AFSEL0</td></tr>
<tr><td>0x120</td><td>GPIOB_AFL</td><td colspan="4">AFSEL7</td><td colspan="4">AFSEL6</td><td colspan="4">AFSEL5</td><td colspan="4">AFSEL4</td><td colspan="4">AFSEL3</td><td colspan="4">AFSEL2</td><td colspan="4">AFSEL1</td><td colspan="4">AFSEL0</td></tr>
<tr><td>0x220</td><td>GPIOF_AFL</td><td colspan="16">Reserved</td><td colspan="4">AFSEL3</td><td colspan="4">AFSEL2</td><td colspan="4">AFSEL1</td><td colspan="4">AFSEL0</td></tr>
<tr><td>0x24</td><td>GPIOA_AFH</td><td colspan="4">AFSEL15</td><td colspan="4">AFSEL14</td><td colspan="4">AFSEL13</td><td colspan="4">AFSEL12</td><td colspan="4">AFSEL11</td><td colspan="4">AFSEL10</td><td colspan="4">AFSEL9</td><td colspan="4">AFSEL8</td></tr>
<tr><td>0x124</td><td>GPIOA_AFH</td><td colspan="28">Reserved</td><td colspan="4">AFSEL8</td></tr>
<tr><td>0x28</td><td>GPIOA_PBC</td><td colspan="16">Reserved</td><td>PBC1</td><td>PBC1</td><td>PBC1</td><td>PBC1</td><td>PBC1</td><td>PBC1</td><td>PBC9</td><td>PBC8</td><td>PBC7</td><td>PBC6</td><td>PBC5</td><td>PBC4</td><td>PBC3</td><td>PBC2</td><td>PBC1</td><td>PBC0</td></tr>
<tr><td>0x128</td><td>GPIOB_PBC</td><td colspan="16">Reserved</td><td colspan="7">Reserved</td><td>PBC</td><td>PBC</td><td>PBC</td><td>PBC</td><td>PBC</td><td>PBC</td><td>PBC</td><td>PBC</td><td>PBC</td></tr>
<tr><td>0x228</td><td>GPIOF_PBC</td><td colspan="16">Reserved</td><td colspan="12">Reserved</td><td>PBC</td><td>PBC</td><td>PBC</td><td>PBC</td></tr>
<tr><td>0x012C</td><td>GPIOB_DS</td><td colspan="21">Reserved</td><td>SR5</td><td>SR4</td><td>SR3</td><td colspan="2">Reserved</td><td>DSR5</td><td>DSR4</td><td>DSR3</td><td colspan="3">Reserved</td></tr>
</table>

6.3.2 GPIO Port Mode Register (GPIOx_PMODE)

Offset Address: 0x0000 (x=A)；0x0100 (x=B)；0x0200 (x=F)

Reset Value: 0xCBFF FFFF（x=A）；0x3 FFFF（x=B）；0xFF（x=F）

31-30	29-28	27-26	25-24	23-22	21-20	19-18	17-16
PMODE15[1:0]	PMODE14[1:0]	PMODE13[1:0]	PMODE12[1:0]	PMODE11[1:0]	PMODE10[1:0]	PMODE9[1:0]	PMODE8[1:0]
rw	rw	rw	rw	rw	rw	rw	rw

15-14	13-12	11-10	9-8	7-6	5-4	3-2	1-0
PMODE7[1:0]	PMODE6[1:0]	PMODE5[1:0]	PMODE4[1:0]	PMODE3[1:0]	PMODE2[1:0]	PMODE1[1:0]	PMODE0[1:0]
rw	rw	rw	rw	rw	rw	rw	rw

Bit Field	Name	Description
31:30 29:28 27:26 25:24 23:22 21:20 19:18 17:16	PMODEy[1:0]	GPIOx (x = A, B, F) PINy Mode: 00: Input Mode 01: General Output Mode 10: Alternate Function Mode 11: Analog Mode *Note:* *When x=A, y = 0…15；* *When x=B, y = 0…8；*

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Bit Field	Name	Description
15:14 13:12 11:10 9:8 7:6 5:4 3:2 1:0		*When x=F, y = 0...3；* *The remaining bits are reserved, and the reserved bits are read-only;*

6.3.3 GPIO Port Output Type Register (GPIOx_POTYPE)

Offset address : 0x0004 (x=A)；0x0104 (x=B)；0x0204 (x=F)

Reset value : 0x0000 0000（x=A,B,F）

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
POT15	POT14	POT13	POT12	POT11	POT10	POT9	POT8	POT7	POT6	POT5	POT4	POT3	POT2	POT1	POT0
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Bit Field	Name	Description
31:16	Reserved	Reserved, must be maintained at reset value.
15:0	POTy	Output type of port GPIOx (x = A, B, F) pin PINy: 0: Push-pull output mode (post-reset state) 1: Open-drain output mode (Open drain mode can be configured only for I2C multiplexing function) *Note: When x=A, y = 1,4,5,6,7,9,10,11,12,13,14；* *When x=B, y = 2,5,6,7,8；* *When x=F, y = 0,1；* *The remaining bits are reserved, and the reserved bits are read-only.*

6.3.4 GPIO Port Pull-up/Pull-down Register (GPIOx_PUPD)

Offset address : 0x000C (x=A)；0x010C (x=B)；0x020C (x=F)

Reset value : 0x2400 0000 (x=A); 0x0000 0000 (x=B,F)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PUPD15[1:0]		PUPD14[1:0]		PUPD13[1:0]		PUPD12[1:0]		PUPD11[1:0]		PUPD10[1:0]		PUPD9[1:0]		PUPD8[1:0]	
rw		rw		rw		rw		rw		rw		rw		rw	

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15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PUPD7[1:0]		PUPD6[1:0]		PUPD5[1:0]		PUPD4[1:0]		PUPD3[1:0]		PUPD2[1:0]		PUPD1[1:0]		PUPD0[1:0]	
rw		rw		rw		rw		rw		rw		rw		rw	

Bit Field	Name	Description
31:30 29:28 27:26 25:24 23:22 21:20 19:18 17:16 15:14 13:12 11:10 9:8 7:6 5:4 3:2 1:0	PUPDy[1:0]	Pull-up/Pull-down mode of port GPIOx (x = A, B, F) pin PINy: 00: No pull-up/pull-down 01: Pull-up 10: Pull-down 11: Reserved *Note: When x=A, y = 0…15；* *When x=B, y = 0…8；* *When x=F, y = 0…3；* *The remaining bits are reserved, and the reserved bits are read-only;*

6.3.5 GPIO Port Input Data Register (GPIOx_PID)

Offset address : 0x0010 (x=A)；0x0110 (x=B)；0x0210 (x=F)

Reset value : 0x0000 0000 (x=A, B, F)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PID15	PID14	PID13	PID12	PID11	PID10	PID9	PID8	PID7	PID6	PID5	PID4	PID3	PID2	PID1	PID0
r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r

Bit Field	Name	Description
31:16	Reserved	Reserved, must be maintained at reset value.
15:0	PIDy	Input data of port GPIOx (x = A, B, F) pin PINy. These bits are read-only, and the read value corresponds to the status of the respective I/O port. *Note: When x=A, y = 0…15；*

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Bit Field	Name	Description
		When x=B, y = 0...8; *When x=F, y = 0...3;* *The remaining bits are reserved, and the reserved bits are read-only;*

6.3.6 GPIO Port Output Data Register (GPIOx_POD)

Offset address : 0x0014 (x=A); 0x0114 (x=B); 0x0214 (x=F)

Reset value : 0x0000 0000 (x=A, B, F)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
POD15	POD14	POD13	POD12	POD11	POD10	POD9	POD8	POD7	POD6	POD5	POD4	POD3	POD2	POD1	POD0
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Bit Field	Name	Description
31:16	Reserved	Reserved, must be maintained at reset value.
15:0	PODy	Output data of port GPIOx (x = A, B, F) pin PINy These bits can be read or written by software, allowing independent configuration/clearing of the corresponding POD bits. *Note: When x=A, y = 0...15;* *When x=B, y = 0...8;* *When x=F, y = 0...3;* *The remaining bits are reserved, and the reserved bits are read-only;*

6.3.7 GPIO Port Bit Set/Clear Register (GPIOx_PBSC)

Offset address : 0x0018 (x=A); 0x0118 (x=B); 0x0218 (x=F)

Reset value : 0x0000 0000 (x=A, B, F)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PBC15	PBC14	PBC13	PBC12	PBC11	PBC10	PBC9	PBC8	PBC7	PBC6	PBC5	PBC4	PBC3	PBC2	PBC1	PBC0
w	w	w	w	w	w	w	w	w	w	w	w	w	w	w	w

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PBS15	PBS14	PBS13	PBS12	PBS11	PBS10	PBS9	PBS8	PBS7	PBS6	PBS5	PBS4	PBS3	PBS2	PBS1	PBS0
w	w	w	w	w	w	w	w	w	w	w	w	w	w	w	w

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Bit Field	Name	Description
31:16	PBCy	Clear bit y of port GPIOx (x = A, B, F). These bits can only be written. 0: No effect on the corresponding PODy bit. 1: Clear the corresponding PODy bit to 0. *Note:* *If both PBCy and the corresponding bit of PBCy are set simultaneously, the PBCy bit takes effect.* *Note:* *When x=A, y = 0...15;* *When x=B, y = 0...8;* *When x=F, y = 0...3;* *The remaining bits are reserved, and the reserved bits are read-only;*
15:0	PBSy	Set bit y of port GPIOx (x = A, B, F) These bits can only be written. 0: No effect on the corresponding PODy bit. 1: Set the corresponding PODy bit to 1. *Note:* *When x=A, y = 0...15;* *When x=B, y = 0...8;* *When x=F, y = 0...3;* *The remaining bits are reserved, and the reserved bits are read-only;*

6.3.8 GPIO Port Locking Configuration Register (GPIOx_ PLOCK)

Offset address : 0x001C (x=A); 0x011C (x=B); 0x021C (x=F)

Reset value : 0x0000 0000 (x=A, B, F)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															PLOCKK
															rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PLOCK15	PLOCK14	PLOCK13	PLOCK12	PLOCK11	PLOCK10	PLOCK9	PLOCK8	PLOCK7	PLOCK6	PLOCK5	PLOCK4	PLOCK3	PLOCK2	PLOCK1	PLOCK0
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Bit Field	Name	Description
31:17	Reserved	Reserved, must be maintained at reset value.
16	PLOCKK	Lock bit This bit can be read at any time, and it can only be modified through a write sequence with a lock key. 0: Port configuration lock key bit is not activated 1: Port configuration lock key bit is activated, GPIOx_PLOCK register will be locked

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Bit Field	Name	Description
		until the next system reset. Lock key write sequence: Write 1 -> Write 0 -> Write 1 -> Read 0 -> (Read 1) The last read of 1 can be omitted, but can be used to confirm that the lock key has been activated. *Note: When performing the lock key write sequence, the value of PLOCK[15:0] cannot be changed. Any errors in the lock key write sequence will prevent the lock key from being activated.*
15:0	PLOCKy	Port GPIOx (x = A, B, C, D) pin PINy configuration lock bit. These bits can be read and written, but can only be written when PLOCKK bit is 0. 0: Configuration of the port is not locked. 1: Configuration of the port is locked. *Note:* *When x=A, y = 0…15；* *When x=B, y = 0…8；* *When x=F, y = 0…3；* *The remaining bits are reserved, and the reserved bits are read-only;*

6.3.9 GPIO Alternate Function Low Configuration Register (GPIOx_AFL)

Offset address : 0x0020 (x=A)；0x0120 (x=B)；0x0220 (x=F)

Reset value : 0xFFFF FFFF（x= A,B）, 0x FFFF（x= F）

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
AFSEL7[3:0]				AFSEL6[3:0]				AFSEL5[3:0]				AFSEL4[3:0]			
rw				rw				rw				rw			

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
AFSEL3[3:0]				AFSEL2[3:0]				AFSEL1[3:0]				AFSEL0[3:0]			
rw				rw				rw				rw			

Bit Field	Name	Description
31:28 27:24 23:20 19:16 15:12 11:8 7:4 3:0	AFSELy[3:0]	GPIOx（x = A, B, F）port PINy（y = 0…7）alternate function configuration bit 0000: AF0 0001: AF1 0010: AF2 0011: AF3 0100: AF4 0101: AF5 0110: AF6 0111: AF7 1000: AF8 1001: AF9

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Bit Field	Name	Description
		1010: AF10 1011: AF11 1100: AF12 1101: AF13 1110: AF14 1111: AF15 *Note: When x=A, y = 0…7;* *When x=B, y = 0…7;* *When x=F, y = 0…3;* *The remaining bits are reserved, and the reserved bits are read-only;* *Note: AF15 is GPIO without* alternate function.

6.3.10 GPIO Alternate Function High Configuration Register (GPIOx_AFH)

Offset address : 0x0024 (x=A); 0x0124 (x=B)

Reset value : 0xF00F FFFF (x = A); 0xF（x= B）

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
AFSEL15[3:0]				AFSEL14[3:0]				AFSEL13[3:0]				AFSEL12[3:0]			
rw				rw				rw				rw			

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
AFSEL11[3:0]				AFSEL10[3:0]				AFSEL9[3:0]				AFSEL8[3:0]			
rw				rw				rw				rw			

Bit Field	Name	Description
31:28 27:24 23:20 19:16 15:12 11:8 7:4 3:0	AFSELy[3:0]	GPIOx（x = A, B）port PINy（y = 8…15）alternate function configuration bit 0000: AF0 0001: AF1 0010: AF2 0011: AF3 0100: AF4 0101: AF5 0110: AF6 0111: AF7 1000: AF8 1001: AF9 1010: AF10 1011: AF11 1100: AF12 1101: AF13 1110: AF14

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Bit Field	Name	Description
		1111: AF15 Note: When x=A, y = 8…15； When x=B, y = 8； The remaining bits are reserved, and the reserved bits are read-only; *Note: AF15 is GPIO without* alternate function.

6.3.11 GPIO Port Bit Clear Register (GPIOx_PBC)

Offset address : 0x0028 (x=A)；0x0128 (x=B)；0x0228 (x=F)

Reset value : 0x0000 0000 (x=A, B, F)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PBC15	PBC14	PBC13	PBC12	PBC11	PBC10	PBC9	PBC8	PBC7	PBC6	PBC5	PBC4	PBC3	PBC2	PBC1	PBC0
w	w	w	w	w	w	w	w	w	w	w	w	w	w	w	w

Bit Field	Name	Description
31:16	Reserved	Reserved, must be maintained at reset value.
15:0	PBCy	Clear the bit y of port GPOx (y=0... 15) These bits can only be written. 0: No effect on the corresponding PODy bit. 1: Clear the corresponding PODy bit to 0. *Note:* *When x=A, y = 0…15；* *When x=B, y = 0…8；* *When x=F, y = 0…3；* *The remaining bits are reserved, and the reserved bits are read-only;*

6.3.12 GPIOB Driver Strength Configuration Register (GPIOB_ DS)

Offset address : 0x12C

Reset value : 0x0000 0738

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved					SR5	SR4	SR3	Reserved		DS5	DS4	DS3	Reserved		

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rw rw rw rw rw rw

Bit Field	Name	Description
31:11	Reserved	Reserved, must be maintained at reset value.
10:8	SRy	Slew rate configuration bit for port GPOB pin PINy (y=3... 5) 0: Quick Flip 1: Slow Flip *Note: y=3,4,5;*
7:6	Reserved	Reserved, must be maintained at reset value.
5:3	DSy	Driver capability configuration bit for port GPOB pin PINy (y=3... 5) 0: High driving capability (16mA (5V)/8mA (3.3V)/4mA (2.0V)) 1: Low driving capability (8mA (5V)/4mA (3.3V)/2mA (2.0V)) *Note: y=3,4,5;* *Note: For other GPIO, VDD=5/3.3/2V corresponds to a driving capability of 12/6/3mA*
2:0	Reserved	Reserved, must be maintained at reset value.

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6.4 AFIO Registers

6.4.1 AFIO Register Overview

AFIO Base Address：0x4002 3000

Table 6-26 AFIO Register Overview

<table>
<tr><th>Offset</th><th>Register</th><th>31</th><th>30</th><th>29</th><th>28</th><th>27</th><th>26</th><th>25</th><th>24</th><th>23</th><th>22</th><th>21</th><th>20</th><th>19</th><th>18</th><th>17</th><th>16</th><th>15</th><th>14</th><th>13</th><th>12</th><th>11</th><th>10</th><th>9</th><th>8</th><th>7</th><th>6</th><th>5</th><th>4</th><th>3</th><th>2</th><th>1</th><th>0</th></tr>
<tr><td>0x0300</td><td>AFIO_CFG</td><td colspan="8">Reserved</td><td>SPI2_NSS</td><td>SPI1_NSS</td><td colspan="8">Reserved</td><td colspan="3">EXTI_ETRR</td><td colspan="7">Reserved</td><td>EXTIFLITEN</td><td colspan="3">IOFLITCFG</td></tr>
<tr><td>0x0308</td><td>AFIO_EXTI_CFG1</td><td colspan="17">Reserved</td><td colspan="3">EXTI3_CFG</td><td>Reserved</td><td colspan="3">EXTI2_CFG</td><td>Reserved</td><td colspan="3">EXTI1_CFG</td><td>Reserved</td><td colspan="3">EXTI0_CFG</td></tr>
<tr><td>0x030c</td><td>AFIO_EXTI_CFG2</td><td colspan="21">Reserved</td><td colspan="3">EXTI6_CFG</td><td>Reserved</td><td colspan="3">EXTI5_CFG</td><td>Reserved</td><td colspan="3">EXTI4_CFG</td></tr>
<tr><td>0x0310</td><td>AFIO_DIGEFT_CFG1</td><td colspan="16">Reserved</td><td colspan="16">PAyDIGEFTEN</td></tr>
<tr><td>0x0314</td><td>AFIO_DIGEFT_CFG2</td><td colspan="23">Reserved</td><td colspan="9">PByDIGEFTEN</td></tr>
<tr><td>0x0318</td><td>AFIO_DIGEFT_CFG3</td><td colspan="28">Reserved</td><td colspan="4">PFyDIGEFTEN</td></tr>
</table>

6.4.2 AFIO Configuration Register (AFIO_CFG)

Offset address : 0x0300

Reset value : 0x0000 3800

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">Reserved</td><td>SPI2_NSS</td><td>SPI1_NSS</td><td colspan="6">Reserved</td></tr>
<tr><td colspan="8"></td><td>rw</td><td>rw</td><td colspan="6"></td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">Reserved</td><td colspan="3">EXTI_ETRR[2:0]</td><td colspan="7">Reserved</td><td>EXTIFLITEN</td><td colspan="3">IOFILTCFG[2:0]</td></tr>
<tr><td colspan="2"></td><td colspan="3">rw</td><td colspan="7"></td><td>rw</td><td colspan="3">rw</td></tr>
</table>

Bit Field	**Name**	**Description**
31:24	Reserved	Reserved, must be maintained at reset value.
23	SPI2_NSS	SPI2 NSS mode selection bit (NSS configured as AFIO push-pull mode). 0: NSS is high impedance when idle 1: NSS is high level when idle
22	SPI1_NSS	SPI1 NSS mode selection bit (NSS configured as AFIO push-pull mode). 0: NSS is high impedance when idle

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Bit Field	Name	Description
		1: NSS is high level when idle
21:14	Reserved	Reserved, must be maintained at reset value.
13:11	EXTI_ETRR[2:0]	Select interrupt line remapping for external trigger remapping. 000: Select EXTI0 rule for external trigger remapping 001: Select EXTI1 rule for external trigger remapping ... 110: Select EXTI6 rule for external trigger remapping
10:4	Reserved	Reserved, must be maintained at reset value.
3	EXTIFLITEN	EXTI interrupt line filtering enabled 0: Disable 1: Enable *Note: After enabling the filtering, fix the filtering of 2 LSI CLK*
2:0	IOFILTCFG[2:0]	IO filter control. 000: Bypass filter 001: IO filter time is 1 HCLK clock cycle 010: IO filter time is 2 HCLK clock cycles ... 110: IO filter time is 7 HCLK clock cycles

6.4.3 AFIO External Interrupt Configuration Register 1 (AFIO_EXTI_CFG1)

Offset address : 0x0308

Reset value : 0x0000 7777

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EXTI3_CFG[3:0]				EXTI2_CFG[3:0]				EXTI1_CFG[3:0]				EXTI0_CFG[3:0]			
rw				rw				rw				rw			

Bit Field	Name	Description
31:16	Reserved	Reserved, must be maintained at reset value.
15:12	EXTI3_CFG	EXTI3 configuration These bits can be read and written by software and are used to select the input source for external interrupts of EXTI3. 0000b: PA12 pin 0001b: PA13 pin 0010b: PA14 pin 0011b: PA15 pin Other: Reserved

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Bit Field	Name	Description
11:8	EXTI2_CFG	EXTI2 configuration These bits can be read and written by software and are used to select the input source for external interrupts of EXTI2. 0000b: PA8 pin 0001b: PA9 pin 0010b: PA10 pin 0011b: PA11 pin Other: Reserved
7:4	EXTI1_CFG	EXTI1 configuration These bits can be read and written by software and are used to select the input source for external interrupts of EXTI1. 0000b: PA4 pin 0001b: PA5 pin 0010b: PA6 pin 0011b: PA7 pin Other: Reserved
3:0	EXTI0_CFG	EXTI0 configuration These bits can be read and written by software and are used to select the input source for EXTI0 external interrupts. 0000b: PA0 pin 0001b: PA1 pin 0010b: PA2 pin 0011b: PA3 pin Other: Reserved

6.4.4 AFIO External Interrupt Configuration Register 2 (AFIO_EXTI_CFG2)

Offset address : 0x030C

Reset value : 0x0000 0777

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EXTI7_CFG[3:0]				EXTI6_CFG[3:0]				EXTI5_CFG[3:0]				EXTI4_CFG[3:0]			
rw				rw				rw				rw			

Bit Field	Name	Description
31:12	Reserved	Reserved, must be maintained at reset value.
11:8	EXTI6	EXTI6 configuration These bits can be read and written by software and are used to select the input

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Bit Field	Name	Description
		source for external interrupts in EXTI6. 0000b: PF0 pin 0001b: PF1 pin 0010b: PF2 pin 0011b: PF3 pin Other: Reserved
7:4	EXTI5	EXTI5 configuration These bits can be read and written by software and are used to select the input source for external interrupts of EXTI5. 0000b: PB4 pin 0001b: PB5 pin 0010b: PB6 pin 0011b: PB7 pin 0100b: PB8 pin Other: Reserved
3:0	EXTI4	EXTI4 configuration These bits can be read and written by software and are used to select the input source for external interrupts in EXTI4. 0000b: PB0 pin 0001b: PB1 pin 0010b: PB2 pin 0011b: PB3 pin Other: Reserved

6.4.5 Digital Glitch Filter Configuration Register 1 (AFIO_DIGEFT_CFG1)

Offset address : 0x0310

Reset value : 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PA15DIGEFTEN	PA14DIGEFTEN	PA13DIGEFTEN	PA12DIGEFTEN	PA11DIGEFTEN	PA10DIGEFTEN	PA9DIGEFTEN	PA8DIGEFTEN	PA7DIGEFTEN	PA6DIGEFTEN	PA5DIGEFTEN	PA4DIGEFTEN	PA3DIGEFTEN	PA2DIGEFTEN	PA1DIGEFTEN	PA0DIGEFTEN
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Bit Field	Name	Description
31:16	Reserved	Reserved, must be maintained at reset value.
15:0	PAyDIGEFTEN	Digital filter enable bit for pin PAy (y=0...15) 0: Disable digital filter 1: Enable digital filter

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6.4.6 Digital Glitch Filter Configuration Register 2 (AFIO_DIGEFT_CFG2)

Offset address : 0x0314

Reset value : 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved							PB8DIG EFTEN	PB7DIG EFTEN	PB6DIG EFTEN	PB5DIG EFTEN	PB4DIG EFTEN	PB3DIG EFTEN	PB2DIG EFTEN	PB1DIG EFTEN	PB0DIG EFTEN
							rw	rw	rw	rw	rw	rw	rw	rw	rw

Bit Field	Name	Description
31:9	Reserved	Reserved, must be maintained at reset value.
8:0	PByDIGEFTEN	Digital filter enable bit for pin PBy (y=0...8) 0: Disable digital filter 1: Enable digital filter

6.4.7 Digital Glitch Filter Configuration Register 3 (AFIO_DIGEFT_CFG3)

Offset address : 0x0318

Reset value : 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved												PF3DIG EFTEN	PF2DIG EFTEN	PF1DIG EFTEN	PF0DIG EFTEN
												rw	rw	rw	rw

Bit Field	Name	Description
31:16	Reserved	Reserved, must be maintained at reset value.
15:0	PFyDIGEFTEN	Digital filter enable bit for pin PFy (y=0...3) 0: Disable digital filter 1: Enable digital filter

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7 DMA Controller

7.1 Introduction

The DMA controller can access totally 3 AHB slaves: Flash, SRAM, APB. DMA Controller is controlled by CPU to perform fast data transfer from source to destination. After configuration, data can be transferred without CPU intervention. Thus, CPU can be released for other computation/control tasks or save overall system power consumption.

The main architecture of the MCU is a multi-layer AHB-Lite bus structure with round-robin arbitration scheme. DMA and CPU can access different slaves in parallel or same slaves sequentially.

DMA controller has 3 logic channels. Each logic channel is used to serve memory access requests from single or multiple peripherals. The priorities of different DMA channels are controlled by the internal arbiter.

Support user-configurable peripheral request channels.

7.2 Main Features

DMA main features:

- 3 DMA channels which can be configured independently.
- Each DMA channel supports hardware requests and software triggers to initiate transfer which is configured by software.
- Each DMA channel has dedicated software priority level (DMA_CHCFGx.PRIOLVL [1:0] bits, corresponding to 4 levels of priority) which can be configured individually. Channels with the same software priority level will further compare hardware index (channel number) to decide final priority (lower index number channel will has higher priority).
- Configurable source and destination size. Address setting should correspond to data size.
- Configurable circular transfer mode for each channel.
- Each channel has 3 independent event flags and interrupts (Transfer complete, Half transfer, Transfer error), and a global interrupt flag (set by logical or of 3 events).
- Support three transfer types which are Memory-to-Memory, Memory-to-Peripheral and Peripheral-to-Memory.

  Note: Transfer of peripheral SPI to peripheral DAC can also be supported (mode configuration is peripheral to memory mode).
- Access totally 3 AHB slaves: Flash, SRAM, APB.
- Configurable data transmit number (0~65535).

Note: It is not recommended to use DMA for programming FLASH to avoid timing errors.

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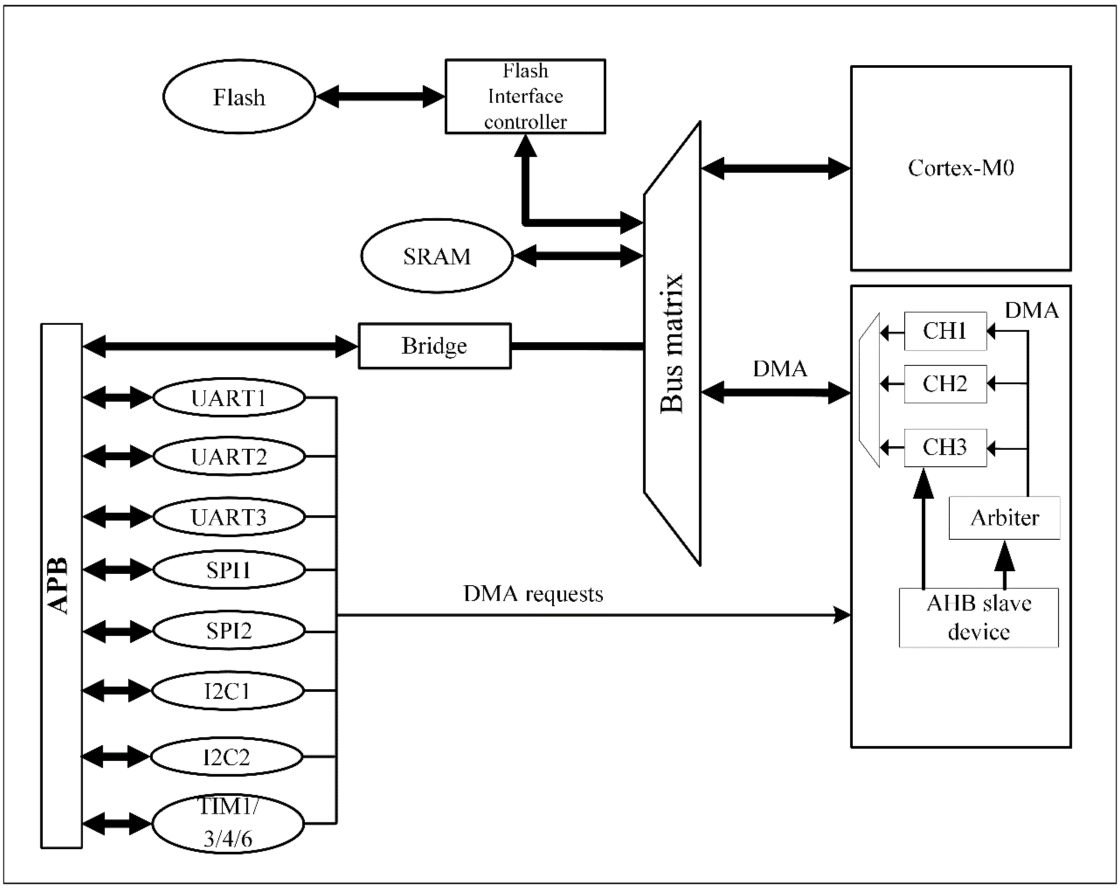
7.3 Block Diagram

Figure 7-1 DMA Block Diagram



7.4 Function Description

DMA controller and Cortex®-M0 core share the same system data bus. When CPU and DMA access the same destination (RAM or peripheral) at the same time, DMA request will suspend CPU from accessing the system bus for several cycles, and the bus arbiter will perform round-robin scheduling. This allows the CPU to get at least half of the system bus (memory or peripheral) bandwidth.

7.4.1 DMA Operation

A DMA request can be triggered by hardware peripherals or software, and the DMA controller processes the request according to the priority level of the channel. The data is read from the source address according to the configured transfer address and bit width, and then the read data is stored in the destination address space. After one operation, the controller calculates the number of remaining transfers and updates the source address and the destination address for the next transfer.

Each DMA data transfer consists of three operations:

- Data access: determine the source address (DMA_PADDRx or DMA_MADDRx) according to the transfer direction and read data from the source address.
- Data storage: determine the destination address (DMA_PADDRx or DMA_MADDRx) according to the transfer direction and store the read data into the destination address space.

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- Calculate the number of unfinished operations, perform a decrement operation on the DMA_TXNUMx register, and update the source and destination addresses for the next operation.

7.4.2 Channel Priority and Arbitration

The DMA uses arbitration to handle multiple requests from different channels. The priority of each channel is programmable in the channel control register (DMA_CHCFGx).

4 levels of priority:

- Very high priority
- High priority
- Medium priority
- Low priority

By default, channel with lower index has higher priority if the programmed priority is the same.

For memory to memory transfer, re-arbitration is performed after 4 transfer operations.

For transfer related to periphery, re-arbitration is performed after each transfer operation.

7.4.3 DMA Channels and Number of Transfers

Each channel can perform DMA transfer between the specified peripheral registers and memory addresses. The number of data transferred by DMA is programmable, and the maximum supported value is 65535. The DMA_TXNUM register is decremented after each transfer.

7.4.4 Programmable Data Bit Width

Peripheral and memory transfer data width supports byte, half-word and word, which can be programmed through DMA_CHCFGx.PSIZE and DMA_CHCFGx.MSIZE.

When DMA_CHCFGx.PSIZE and DMA_CHCFGx.MSIZE are different, the DMA module aligns the data according to the below.

Table 7-1 Programmable Data Width and Endian Operation (When PINC = MINC = 1)

Source width (bit)	Destination width (bit)	Number of transfer (Byte)	Source: Address / data	Transfer operations (R: Read, W: Write)	Destination: Address / data
8	8	4	0x0 / B0 0x1 / B1 0x2 / B2 0x3 / B3	1: R B0 [7:0] @0x0, W B0 [7:0] @0x0 2: R B1 [7:0] @0x1, W B1 [7:0] @0x1 3: R B2 [7:0] @0x2, W B2 [7:0] @0x2 4: R B3 [7:0] @0x3, W B3 [7:0] @0x3	0x0 / B0 0x1 / B1 0x2 / B2 0x3 / B3
8	16	4	0x0 / B0 0x1 / B1 0x2 / B2 0x3 / B3	1: R B0 [7:0] @0x0, W 00B0 [15:0] @0x0 2: R B1 [7:0] @0x1, W 00B1 [15:0] @0x2 3: R B2 [7:0] @0x2, W 00B2 [15:0] @0x4 4: R B3 [7:0] @0x3, W 00B3 [15:0] @0x6	0x0 / 00B0 0x2 / 00B1 0x4 / 00B2 0x6 / 00B3

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Source width (bit)	Destination width (bit)	Number of transfer (Byte)	Source: Address / data	Transfer operations (R: Read, W: Write)	Destination: Address / data
8	32	4	0x0 / B0 0x1 / B1 0x2 / B2 0x3 / B3	1: R B0 [7:0] @0x0, W 000000B0 [31:0] @0x0 2: R B1 [7:0] @0x1, W 000000B1 [31:0] @0x4 3: R B2 [7:0] @0x2, W 000000B2 [31:0] @0x8 4: R B3 [7:0] @0x3, W 000000B3 [31:0] @0xC	0x0 / 000000B0 0x4 / 000000B1 0x8 / 000000B2 0xC / 000000B3
16	8	4	0x0 / B1B0 0x2 / B3B2 0x4 / B5B4 0x6 / B7B6	1: R B1B0 [15:0] @0x0, W B0 [7:0] @0x0 2: R B3B2 [15:0] @0x2, W B2 [7:0] @0x1 3: R B5B4 [15:0] @0x4, W B4 [7:0] @0x2 4: R B7B6 [15:0] @0x6, W B6 [7:0] @0x3	0x0 / B0 0x1 / B2 0x2 / B4 0x3 / B6
16	16	4	0x0 / B1B0 0x2 / B3B2 0x4 / B5B4 0x6 / B7B6	1: R B1B0 [15:0] @0x0, W B1B0 [15:0] @0x0 2: R B3B2 [15:0] @0x2, W B3B2 [15:0] @0x2 3: R B5B4 [15:0] @0x4, W B5B4 [15:0] @0x4 4: R B7B6 [15:0] @0x6, W B7B6 [15:0] @0x6	0x0 / B1B0 0x2 / B3B2 0x4 / B5B4 0x6 / B7B6
16	32	4	0x0 / B1B0 0x2 / B3B2 0x4 / B5B4 0x6 / B7B6	1: R B1B0 [15:0] @0x0, W 0000B1B0 [31:0] @0x0 2: R B3B2 [15:0] @0x2, W 0000B3B2 [31:0] @0x4 3: R B5B4 [15:0] @0x4, W 0000B5B4 [31:0] @0x8 4: R B7B6 [15:0] @0x6, W 0000B7B6 [31:0] @0xC	0x0 / 0000B1B0 0x4 / 0000B3B2 0x8 / 0000B5B4 0xC / 0000B7B6
32	8	4	0x0 / B3B2B1B0 0x4 / B7B6B5B4 0x8 / BBBAB9B8 0xC / BFBEBDBC	1: R B3B2B1B0 [31:0] @0x0, W B0 [7:0] @0x0 2: R B7B6B5B4 [31:0] @0x4, W B4 [7:0] @0x1 3: R BBBAB9B8 [31:0] @0x8, W B8 [7:0] @0x2 4: R BFBEBDBC [31:0] @0xC, W BC [7:0] @0x3	0x0 / B0 0x1 / B4 0x2 / B8 0x3 / BC
32	16	4	0x0 / B3B2B1B0 0x4 / B7B6B5B4 0x8 / BBBAB9B8 0xC / BFBEBDBC	1: R B3B2B1B0 [31:0] @0x0, W B1B0 [15:0] @0x0 2: R B7B6B5B4 [31:0] @0x4, W B5B4 [15:0] @0x2 3: R BBBAB9B8 [31:0] @0x8, W B9B8 [15:0] @0x4 4: R BFBEBDBC [31:0] @0xC, W BDBC [15:0] @0x6	0x0 / B1B0 0x2 / B5B4 0x4 / B9B8 0x6 / BDBC
32	32	4	0x0 / B3B2B1B0 0x4 / B7B6B5B4 0x8 / BBBAB9B8 0xC / BFBEBDBC	1: R B3B2B1B0 [31:0] @0x0, W B3B2B1B0 [31:0] @0x0 2: R B7B6B5B4 [31:0] @0x4, W B7B6B5B4 [31:0] @0x4 3: R BBBAB9B8 [31:0] @0x8, W BBBAB9B8 [31:0] @0x8 4: R BFBEBDBC [31:0] @0xC, W BFBEBDBC [31:0] @0xC	0x0 / B3B2B1B0 0x4 / B7B6B5B4 0x8 / BBBAB9B8 0xC / BFBEBDBC

Note:

DMA always provide full 32-bits data to HWDATA[31:0] no matter what destination size it is (HSIZE still follows destination size setting for device supports byte/half-word operation). The HWDATA[31:0] follows the following rules:

- When source size is smaller than destination size, DMA fills the MSB with 0 until their sizes match and duplicates it to be 32 bits. E.g., source is 8 bits data 0x55 and destination size is 16 bits. DMA fills the source data with 0 to make it 16 bits and become 0x0055, then duplicate it to 32-bit data 0x0055_0055 and provide to HWDATA[31:0]; (if destination size is 32-bit then DMA will only pad source data with 0).
- When source size is larger or equal to destination size and smaller than 32 bits, DMA duplicates source data to 32 bits data. E.g., source data is 8 bits data 0x1F, HWDATA[31:0] =0x1F1F_1F1F. if source data is 16 bits data 0x2345, then

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HWDATA[31:0] = 0x2345_2345.

This ensures peripherals that only support word operation won't generate bus error and the desired data can still move to the place we want with extra bits i.e. 0 padding. If user wants to configure an 8-bit register but is aligned to a 32-bit address boundary, the source size should be set to 8 bits and destination to 32 bits so extra bits will be padded with 0.

7.4.5 Peripheral/Memory Address Incrementation

DMA_CHCFGx.PINC and DMA_CHCFGx.MINC respectively control whether the peripheral address and memory address are enabled in auto-increment mode. The software cannot write (can read) the address register during transfer.

- In auto-increment mode, the next address to be transferred is automatically increased according to the data width (1, 2 or 4) after each transfer. The address of the first transfer is stored in DMA_PADDRx or DMA_MADDRx register.
- In fixed mode, the address is always fixed to the initial address.

At the end of transfer (i.e. the transfer count changes to 0), different processes will be carried out according to whether the current operation is under circular mode or not.

- In non-circular mode, DMA stops after the transfer is completed. To start a new DMA transfer, need to rewrite the transfer number in the DMA_TXNUMx register with the DMA channel disabled.
- In circular mode, at the end of the transfer, the content of the DMA_TXNUMx register will be automatically reloaded to its initial value, and the current internal peripheral or memory address register will also be reloaded to the initial base address set by the DMA_PADDRx or DMA_MADDRx register.

7.4.6 Channel Configuration Process

The detail configuration process is as below:

1. Configure interrupt mask bits, 1: enable interrupts, 0 disable interrupts.
2. Configure channel peripheral address, memory address and transfer direction.
3. Configure channel priority, 0: lowest, 3: highest.
4. Configure peripheral and memory address increment.
5. Configure channel transfer data width and the number of transfer
6. If necessary, configure circular mode.
7. If it is memory to memory, configure MEM2MEM mode (Note: configure DMA to operation in M2M mode, user needs to set corresponding channel select value to reserved value, e.g., 47).
8. Repeat steps 1 to 3 on channels 1 to 8.
9. Finally, enable the corresponding channel.

If software is used to serve interrupt, the software must enquire interrupt status register to check which interrupt occurred (software needs to write 1 to interrupt flag clear bit to clear the corresponding interrupt). Before enable channel, all interrupts corresponding to the channel should be cleared.

If the interrupt is transfer complete interrupt, software can configure the next transfer, or report to user this channel transfer is complete.

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7.4.7 Flow Control

Three major flow controls are supported:

- Memory to memory
- Memory to peripheral
- Peripheral to memory

Flow control is controlled by two register bits in each DMA channel configuration register. Flow control is used to control source/destination and direction of DMA channel.

Table 7-2 Flow Control Table

DMA_CHCFGx.MEM2MEM	DMA_CHCFGx.DIR	Source	Destination	Transfer
1	x	Memory	Memory	AHB read to AHB write, can do back2back transfer
0	1	Memory	AHB Peripheral	AHB read to AHB write, single transfer
0	1	Memory	APB Peripheral	AHB read to APB write, single transfer
0	0	AHB Peripheral	Memory	AHB read to AHB write, single transfer
0	0	APB Peripheral	Memory	APB read to AHB write, single transfer

7.4.8 Circular Mode

The circular mode is used to process circular buffers and continuous data transmission. The DMA_CHCFGx.CIRC is used to enable this function. When the circular mode is activated, if the number of data to be transferred becomes 0, it will automatically be restored to the initial value when configuring the channel, and the DMA operation will continue.

If the user wants to turn off the circular mode, the user needs to write 0 to DMA_CHCFGx.CHEN to disable the DMA channel, and then write 0 to DMA_CHCFGx.CIRC (when DMA_CHCFGx.CHEN is 1, other bits in the DMA_CHCFGx register cannot be rewritten).

7.4.9 Error Management

DMA access to reserved address space will cause DMA transfer error. When an error occurs, the transfer error flag is set, and the hardware automatically clears the current DMA channel enable bit (DMA_CHCFGx.CHEN), and the channel operation is stopped. If the transfer error interrupt enable bit is set in the DMA_CHCFGx register, an interrupt will be generated.

7.4.10 Interrupt

- Transfer complete interrupt:

  An interrupt is generated when channel data transfer is completed. Interrupt is a level signal. Each channel has its

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dedicated interrupt, interrupt mask control and interrupt status bit. Interrupt status bit is cleared when interrupt flag clear bit is set.

- Half transfer interrupt:

  An interrupt is generated when half of the channel data is transferred. Interrupt is a level signal. Each channel has its dedicated interrupt, interrupt mask control and interrupt status bit. Interrupt status bit is cleared when interrupt flag clear bit is set.

- Transfer error interrupt:

  An interrupt is generated when bus returned error. Interrupt is a level signal. Each channel has its dedicated interrupt, interrupt mask control and interrupt status bit. Interrupt status bit is cleared when interrupt flag clear bit is set.

Table 7-3 DMA Interrupt Request

Interrupt Event	Event Flag Bit	Enable Control Bit
Half transfer	HTXF	HTXIE
Transfer complete	TXCF	TXCIE
Transfer error	ERRF	ERRIE

7.4.11 DMA Request Mapping

Totally there are 33 DMA requests from all the peripherals. To have better support with full flexibility, register bits can be used to select which DMA request is mapped to which DMA channel. The table blow show the mapping scheme of peripherals' DMA request to DMA controller's DMA channels.

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Table 7-4 DMA Request Mapping

DMA request source select	Peripheral DMA request	DMA request source select	Peripheral DMA request
sel = 0	UART1_TX	sel = 21	TIM3_CH1
sel = 1	UART1_RX	sel = 22	TIM3_CH2
sel = 2	UART2_TX	sel = 23	TIM3_CH3
sel = 3	UART2_RX	sel = 24	TIM3_CH4
sel = 4	UART3_TX	sel = 25	TIM3_UP
sel = 5	UART3_RX	sel = 26	TIM3_TRIG
sel = 6	SPI1_TX	sel = 27	TIM4_CH1
sel = 7	SPI1_RX	sel = 28	TIM4_CH2
sel = 8	SPI2_TX	sel = 29	TIM4_CH3
sel = 9	SPI2_RX	sel = 30	TIM4_UP
sel = 10	I2C1_TX	sel = 31	TIM4_TRIG
sel = 11	I2C1_RX	sel = 32	TIM6_UP
sel = 12	I2C2_TX		
sel = 13	I2C2_RX		
sel = 14	TIM1_CH1		
sel = 15	TIM1_CH2		
sel = 16	TIM1_CH3		
sel = 17	TIM1_CH4		
sel = 18	TIM1_COM		
sel = 19	TIM1_UP		
sel = 20	TIM1_TRIG		

Note: Different DMA channels cannot use the same request source, otherwise only high priority channels will be triggered if multiple channels are enabled.

7.5 DMA Registers

7.5.1 DMA Register Overview

Table 7-5 DMA Register Overview

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
000h	DMA_INTSTS	Reserved																				ERRF3	HTXF3	TXCF3	GLBF3	ERRF2	HTXF2	TXCF2	GLBF2	ERRF1	HTXF1	TXCF1	GLBF1
	Reset Value																					0	0	0	0	0	0	0	0	0	0	0	0
004h	DMA_INTCLR	Reserved																				CERRF3	CHTXF3	CTXCF3	CGLBF3	CERRF2	CHTXF2	CTXCF2	CGLBF2	CERRF1	CHTXF1	CTXCF1	CGLBF1
	Reset Value																					0	0	0	0	0	0	0	0	0	0	0	0
008h	DMA_CHCFG1	Reserved																	MEM2MEM	PRIOLVL[1:0]		MSIZE[1:0]		PSIZE[1:0]		MINC	PINC	CIRC	DIR	ERRIE	HTXIE	TXCIE	CHEN
	Reset Value																		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
00Ch	DMA_TXNUM1	Reserved																NDTX[15:0]															
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
010h	DMA_PADDR1	ADDR[31:0]																															
	Reset Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
014h	DMA_MADDR1	ADDR[31:0]																															
	Reset Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
018h	DMA_CHSEL1	Reserved																										CH_SEL[5:0]					
	Reset Value																											0	0	0	0	0	0

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Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
01Ch	DMA_CHCFG2	Reserved																	MEM2MEM	PRIOLVL[1:0]		MSIZE[1:0]		PSIZE[1:0]		MINC	PINC	CIRC	DIR	ERRIE	HTXIE	TXCIE	CHEN
	Reset Value																		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
020h	DMA_TXNUM2	Reserved																NDTX[15:0]															
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
024h	DMA_PADDR2	ADDR[31:0]																															
	Reset Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
028h	DMA_MADDR2	ADDR[31:0]																															
	Reset Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
02Ch	DMA_CHSEL2	Reserved																										CH_SEL[5:0]					
	Reset Value																											0	0	0	0	0	0
030h	DMA_CHCFG3	Reserved																	MEM2MEM	PRIOLVL[1:0]		MSIZE[1:0]		PSIZE[1:0]		MINC	PINC	CIRC	DIR	ERRIE	HTXIE	TXCIE	CHEN
	Reset Value																		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
034h	DMA_TXNUM3	Reserved																NDTX[15:0]															
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
038h	DMA_PADDR3	ADDR[31:0]																															
	Reset Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
03Ch	DMA_MADDR3	ADDR[31:0]																															
	Reset Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
040h	DMA_CHSEL3	Reserved																										CH_SEL[5:0]					
	Reset Value																											0	0	0	0	0	0

7.5.2 DMA Interrupt Status Register (DMA_INTSTS)

Address offset: 0x00

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
												r	r	r	r

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved				ERRF3	HTXF3	TXCF3	GLBF3	ERRF2	HTXF2	TXCF2	GLBF2	ERRF1	HTXF1	TXCF1	GLBF1
r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r

Bit Field	Name	Description
31:12	Reserved	Reserved, the reset value must be maintained.
11/7/3	ERRFx	Transfer error flag for channel x (x=1…3). Hardware sets this bit when transfer error happen. This bit is cleared by software by writing ‘1’ to DMA_INTCLR.CERRFx bit. 0: Transfer error no happened on channel x. 1: Transfer error happened on channel x.
10/6/2	HTXFx	Half transfer flag for channel x (x=1…3). Hardware sets this bit when half transfer is done. This bit is cleared by software by writing ‘1’ to DMA_INTCLR.CHTXFx bit. 0: Half transfer not yet done on channel x. 1: Half transfer was done on channel x.
9/5/1	TXCFx	Transfer complete flag for channel x (x=1…3). Hardware sets this bit when transfer is done. This bit is cleared by software by writing ‘1’ to DMA_INTCLR.CTXCFx bit.

Bit Field	Name	Description
		0: Transfer not yet done on channel x. 1: Transfer was done on channel x.
8/4/0	GLBFx	Global flag for channel x (x=1…3). Hardware sets this bit when any interrupt events happen in this channel. This bit is cleared by software by writing '1' to DMA_INTCLR.CGLBFx bit. 0: No transfer error, half transfer or transfer done event happen on channel x. 1: One of transfer error, half transfer or transfer done event happen on channel x.

7.5.3 DMA Interrupt Flag Clear Register (DMA_INTCLR)

Address offset: 0x04

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
												w	w	w	w

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved				CERRF3	CHTXF3	CTXCF3	CGLBF3	CERRF2	CHTXF2	CTXCF2	CGLBF2	CERRF1	CHTXF1	CTXCF1	CGLBF1
w	w	w	w	w	w	w	w	w	w	w	w	w	w	w	w

Bit Field	Name	Description
31:12	Reserved	**Reserved, the reset value must be maintained.**
11/7/3	CERRFx	Clear transfer error flag for channel x (x=1…3). Software can set this bit to clear ERRF of corresponding channel. 0: No action. 1: Reset DMA_INTSTS.ERRF bit of corresponding channel.
10/6/2	CHTXFx	Clear half transfer flag for channel x (x=1…3). Software can set this bit to clear HTXF of corresponding channel. 0: No action. 1: Reset DMA_INTSTS.HTXF bit of corresponding channel.
9/5/1	CTXCFx	Clear transfer complete flag for channel x (x=1…3). Software can set this bit to clear TXCF of corresponding channel. 0: No action. 1: Reset DMA_INTSTS.TXCF bit of corresponding channel.
8/4/0	CGLBFx	Clear global event flag for channel x (x=1…3). Software can set this bit to clear GLBF of corresponding channel. 0: No action. 1: Reset DMA_INTSTS.GLBF bit of corresponding channel.

7.5.4 DMA Channel x Configuration Register (DMA_CHCFGx)

Note: The x is channel number, x = 1…3

Address offset: 0x08+20 * (x–1)

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Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved	MEM2 MEM	PRIOLVL[1:0]		MSIZE[1:0]		PSIZE[1:0]		MINC	PINC	CIRC	DIR	ERRIE	HTXIE	TXCIE	CHEN
	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Bit Field	Name	Description
31:15	Reserved	Reserved, the reset value must be maintained.
14	MEM2MEM	Memory to memory mode. Software can configure this channel to memory to memory transfer when it is not enabled. 0: Channel transfer between memory and peripheral. 1: Channel set to memory to memory transfer.
13:12	PRIOLVL[1:0]	Channel priority. Software can program channel priority when channel is not enable. 00: Low 01: Medium 10: High 11: Very high
11:10	MSIZE[1:0]	Memory data size. Software can configure data size read/write from/to memory address. 00: 8-bits 01: 16-bits 10: 32-bits 11: Reserved
9:8	PSIZE[1:0]	Peripheral data size. Software can configure data size read/write from/to peripheral address. 00: 8-bits 01: 16-bits 10: 32-bits 11: Reserved
7	MINC	Memory increment mode. Software can enable/disable memory address increment mode. 0: Memory address won't increase with each transfer. 1: Memory address increase with each transfer.
6	PINC	Peripheral increment mode. Software can enable/disable peripheral address increment mode. 0: Peripheral address won't increase with each transfer. 1: Peripheral address increase with each transfer.

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Bit Field	Name	Description
5	CIRC	Circular mode. Software can set/clear this bit. 0: Channel will stop after one round of transfer. 1: Channel configure as circular mode.
4	DIR	Data transfer direction Software can set/clear this bit. 0: Data transfer from Peripheral to Memory 1: Data transfer from Memory to Peripheral.
3	ERRIE	Transfer error interrupt enable. Software can enable/disable transfer error interrupt. 0: Disable transfer error interrupt of channel x. 1: Enable transfer error interrupt of channel x.
2	HTXIE	Half transfer interrupt enable. Software can enable/disable half transfer interrupt. 0: Disable half transfer interrupt of channel x. 1: Enable half transfer interrupt of channel x.
1	TXCIE	Transfer complete interrupt enable. Software can enable/disable transfer complete interrupt. 0: Disable transfer complete interrupt of channel x. 1: Enable transfer complete interrupt of channel x.
0	CHEN	Channel enable. Software can set/reset this bit. 0: Disable channel. 1: Enable channel.

7.5.5 DMA Channel x Transfer Number Register (DMA_TXNUMx)

Note: The x is channel number, x = 1…3

Address offset: 0x0C+20 * (x–1)

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NDTX[15:0]															
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Bit Field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained.
15:0	NDTX	Number of data to transfer. Number of data to be transferred (0～65535). Software can read/write the number of

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Bit Field	Name	Description
		transfers when channel is disable and it will be read only after channel enable. Every successful transfer of corresponding DMA channel will decrease this register by 1. If circular mode is enable, it will automatically reload pre-set value when it reach zero. Otherwise it will keep at zero and reset channel enable.

7.5.6 DMA Channel x Peripheral Address Register (DMA_PADDRx)

Note: The x is channel number, x = 1…3

Address offset: 0x10+20 * (x–1)

Reset value: 0x0000 0000

This register can only be written if the channel is disabled (DMA_CHCFGx.CHEN = 0).

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR[31:16]															
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR[15:0]															
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Bit Field	Name	Description
31:0	ADDR	Peripheral address. Peripheral starting address for DMA to read/write from/to. Increment of address will be decided by DMA_CHCFGx.PSIZE. With DMA_CHCFGx.PSIZE equal to 01, DMA ignores bit 0 of PADDR and if DMA_CHCFGx.PSIZE equal to 10 DMA will ignore bit [1:0] of PADDR.

7.5.7 DMA Channel x Memory Address Register (DMA_MADDRx)

Note: The x is channel number, x = 1…3

Address offset: 0x14+20 * (x–1)

Reset value: 0x0000 0000

This register can only be written if the channel is disabled (DMA_CHCFGx.CHEN = 0).

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR[31:16]															
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR[15:0]															
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

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Bit Field	Name	Description
31:0	ADDR	ADDR Memory address. Memory starting address for DMA to read/write from/to. Increment of address will be decided by DMA_CHCFGx.MSIZE. With DMA_CHCFGx.MSIZE equal to 01, DMA ignores bit 0 of MADDR and if DMA_CHCFGx.MSIZE equal to 10 DMA will ignore bit [1:0] of MADDR.

7.5.8 DMA Channel x Channel Request Select Register (DMA_CHSELx)

Note: The x is channel number, x = 1…3

Address offset: 0x18+20 * (x–1)

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved										CH_SEL[5:0]					
										rw	rw	rw	rw	rw	rw

Bit Field	Name	Description
31:6	Reserved	Reserved, the reset value must be maintained.
5:0	CH_SEL[5:0]	DMA channel request source selection 0x00：UART1_TX …… 0x20：TIM6_UP For the mapping of peripheral DMA requests to DMA input request channel numbers, please refer to Table 7-4

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8 Internal Integrated Circuit Bus (I2C)

8.1 Introduction

The I^2C (Inter-Integrated Circuit) bus is a widely used bus structure that consists of only two bidirectional lines, namely the data line SDA and the clock line SCL. Through these two lines, all devices compatible with the I^2C bus can communicate directly with each other via the I^2C bus.

I2C interface connects the microcontroller and the serial I2C bus, which can be used for communication between the MCU and external I2C devices. The I2C interface module implements standard speed and fast mode of the I2C protocol, with CRC calculation and verification functions, supporting SMBus (System Management Bus) and PMBus (Power Management Bus). Additionally, it provides multi-master functionality, controlling all I2C bus-specific timing, protocol, and arbitration. The I2C interface module also supports DMA mode, effectively reducing the burden on the CPU.

8.2 Main Features

- Can implement both master and slave functions on the same interface
- Acts as a converter from parallel bus to I^2C bus protocol
- Supports 7-bit and 10-bit address modes and broadcast addressing
- As an I^2C master device, can generate clock, start, and stop signals
- As an I^2C slave device, has programmable I^2C address detection and stop bit detection functions
- Supports standard speed (up to 100kHz), fast speed (up to 400kHz), and fast mode+ (up to 1MHz) modes
- Supports interrupt vectors, byte transfer success interrupts, and error event interrupts
- Optional clock stretching function
- Supports DMA mode
- Optional PEC (Packet Error Checking) generation and verification
- Compatible with SMBus 2.0 and PMBus
- Programmable Analog and Digital Filtering

Note: Not all products include all the features mentioned above. Please refer to the relevant datasheet to confirm the I^2C functionalities supported by the product.

8.3 Function Description

The I^2C interface is connected to I^2C bus through data pin (SDA) and clock pin (SCL) to communicate with external devices. It can be connected to standard (up to 100kHz) or fast (up to 400kHz) or fast$^+$ (up to 1MHz) I^2C bus. I^2C module converts data from serial to parallel when receiving, and converts data from parallel to serial when transmitting. It supports interrupt mode, users can enable or disable interrupt according to their needs.

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8.3.1 SDA and SCL Control

I^2C module has two interface lines: serial data line (SDA) and serial clock line (SCL). Devices connected to the bus and exchange information through these two wires. Both SDA and SCL are bidirectional lines, connected to positive power supply with a pull-up resistor. When the bus is idle, both lines are high level. The output of device which is connected to the bus must have open drain or open collector to provide wired-AND functionality. The data on I^2C bus can reach 100 kbit/s in standard mode and 1000 kbit/s in fast mode. Since devices of different processors may be connected to the I2C bus, the levels of logic '0' and logic '1' are not fixed and depend on the actual level of V_{DD}.

If the clock stretchingis allowed, the SCL line is pulled down which can be avoided the overload error during receiving and the under load error during transmission.

For example, when in the transmission mode, if the transmit data register is empty and the byte transmit end bit is set (I2C_STS1.TXDATE = 1, I2C_STS1.BSF = 1), the I^2C interface keeps the clock line low before transmission to wait for the software to read STS1 and write the data into the data register (both buffer and shift register are empty); when In the receive mode, if the data register is not empty and the byte sending end bit is set (I2C_STS1.RXDATNE = 1, I2C_STS1.BSF = 1), the I^2C interface keeps the clock line low after receiving the data byte, waiting for the software to read STS1, and then read the data register(buffer and shift register are full).

If clock stretchingis disable in slave mode, if the receive data register is not empty (I2C_STS1.RXDATNE = 1) in the receive mode, and the data has not been read before receiving the next byte, an overrun error will issue and the last word byte will be discarded. In transmit mode, if the transmit data register is empty (I2C_STS1.TXDATE = 1), no new data is written into the data register before the next byte must be sent, an underrun error will issue. The same byte will be send repeatedly. In this case, duplicate write conflicts are not controlled.

8.3.2 Software Communication Process

The data transmission of I^2C device is divided into master and slave. Master is the device responsible for initializing the transmission of data on the bus and generating clock signal. At this time, any addressed device is a slave. Whether the I^2C device is a master or a slave, it can send or receive data. Therefore, the I2C interface supports four operation modes:

- Slave transmitter mode
- Slave receiver mode
- Master transmitter mode
- Master receiver mode

After system reset, I^2C works in slave mode by default. The I^2C interface is configured by software to send a start bit on the bus, and then the interface automatically switches from the slave mode to the master mode. When arbitration is lost or a stop signal is generated, the interface will switched to the slave mode from the master mode.

The block diagram of I^2C interface is shown in the figure below.

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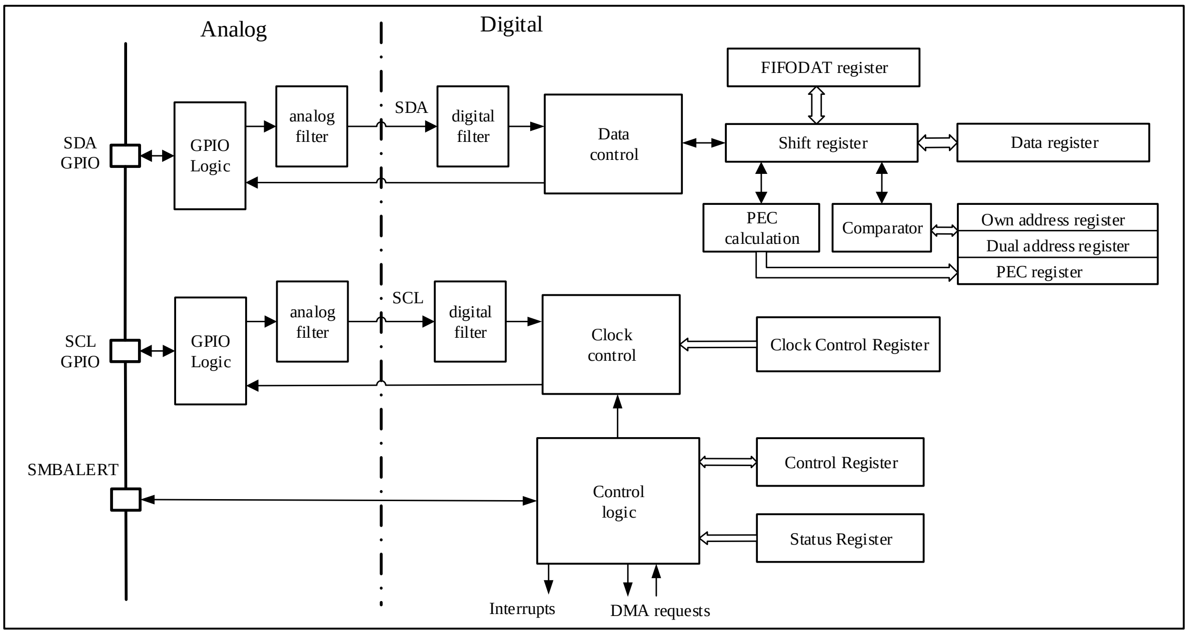
Figure 8-1 I2C Functional Block Diagram

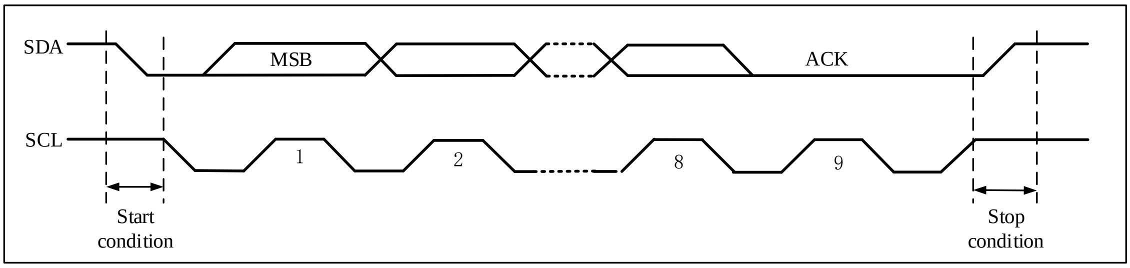


Note: in SMBus mode, SMBALERT is an optional signal. If SMBus is disabled, the signal cannot be used.

8.3.2.1 Start and stop conditions

All data transfers always start with the start bit and end with the stop bit. The start and stop conditions are generated by software in the master mode. Start bit is a level conversion from high to low on SDA line when SCL is high. Stop bit is a level transition from low to high on SDA line when SCL is high. as shown in the figure below.

Figure 8-2 I2C Bus Protocol



8.3.2.2 Clock synchronization and arbitration

The I^{2}C module supports multi-master arbitration, which means two masters can initiate an I^{2}C start operation concurrently when the bus is inactive. So some mechanisms are needed to grant a master the access to the bus. This process is generally named Clock Synchronization and Arbitration.

I^{2}C module has two key features:

- SDA and SCL are open-drain circuit structures, and the signal 'wire-AND' logic is realized through an external pull-up resistor.
- SDA and SCL pins will also detect the level on the pin while outputting the signal to check whether the output is consistent with the previous output. This provides the hardware basis for "Clock Synchronization" and "Bus Arbitration".

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The I^2C device on the bus is to output logic 0 by grounding the line. Based on the characteristics of the I^2C bus, if one device sends logic 0 and the other sends logic 1, then the line sees only logic 0, so there is no possibility of level conflicts on the line.

The physical connection of the bus allows the master to read data while writing data to the bus. In this way, when two masters are competing for the bus, the one that sends logic 0 does not know the occurrence of the competition. Only the one that sends logic 1 will find the conflict (when writing a logic 1, but read 0) and exit the competition.

Clock synchronization

Multiple hosts can simultaneously generate clock signals on an idle bus.The high-to-low switching of the SCL line causes the devices to begin counting their low-level periods, and once the device's clock goes low, it keeps the SCL line in this state until the high-level of the clock is reached. However, if another clock is still in the low period, the low-to-high switch of this clock will not change the state of the SCL line. Therefore, the SCL line is kept low by the device with the longest low-level period. A device with a short low-level period will enter a high-level wait state.

When all related devices have counted their low-level periods, the clock line is released and goes high-level, after which there is no difference in the state of the device clock and SCL lines, and all devices will begin counting their high-level periods, the device that completes the high-level period first will pull the SCL line low again.

In this way, the low-level period of the generated synchronous SCL clock is determined by the device with the longest low-level clock period, and the high-level period is determined by the device with the shortest high-level clock period.

Arbitration:

Arbitration, like synchronization, is to resolve bus control conflicts in the case of multiple masters. The arbitration process has nothing to do with the slave. When the two masters both produce a valid start bit when the bus is idle, in this case, it is necessary to decide which master will complete the data transmission. This is the process of arbitration.

Each master controller does not have the priority level of controlling the bus, which is all determined by arbitration. The bus control is determined and carried out bit by bit. They follow the principle of "low level first", that is, whoever sends the low level first will control the bus. During the arbitration of each bit, when SCL is high, each host checks whether its own SDA level is the same as that sent by itself. In theory, if the content transmitted by two hosts is exactly the same, then they can successfully transmit without errors. If a host sends a high level but detects that the SDA line is low, it considers that it has lost arbitration and shuts down its SDA output driver, while the other host continues to complete its own transmission.

8.3.2.3 I2C data communication process

Each I^2C device is identified by a unique address. According to the device function, they can be either a transmitter or a receiver.

The I^2C host is responsible for generating the start bit and the end bit in order to start and end a transmission. And is responsible for generating the SCL clock.

The I^2C module supports 7-bit and 10-bit addresses, and the user can configure the address of the I^2C slave through software. After the I^2C slave detects the start bit on the I^2C bus, it starts to receive the address from the bus, and compares the received address with its own address. Once the two addresses are matched, the I^2C slave will send an acknowledgement (ACK) and respond to subsequent commands on the bus: transmit or receive the requested data. In addition, if the software opens a broadcast call, the I^2C slave always sends a confirmation response to a broadcast address (0x00).

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Data and address are transmitted in 8-bit width, with the most significant bit first. The 1 or 2 bytes following the start condition is the address (1 byte in 7-bit mode, 2 bytes in 10-bit mode). The address is only sent in master mode. During the 9th clock period after 8 clocks of a byte transmission, the receiver must send back an acknowledge bit (ACK) to the transmitter, as shown in the Figure 8-2 I2C I^2C bus protocol.

Software can enable or disable acknowledgement (ACK), and can set the I^2C interface address (7-bit, 10-bit address or general call address).

8.3.2.4 I2C slave transmission mode

In slave mode, the transmission reception flag bit (I2C_STS2.TRF) indicates whether it is currently in receiver mode or transmission mode. When sending data to I^2C bus in transmission mode, the software should follow the following steps:

1. First, enable I^2C peripheral clock and configure the clock related register in I2C_CTRL1, ensuring the correct I^2C timing. After these two steps are completed, I^2C runs in slave mode, waiting for receiving start bit and address.
2. I^2C slave receives a start bit first, and then receives a matching 7-bit or 10-bit address. I^2C hardware will set the I2C_STS1.ADDRF(received address and matched its own address). The software should monitor this bit regularly or have an interrupt to monitor this bit. After this bit is set, the software reads I2C_STS1 register and then read I2C_STS2 register to clear the I2C_STS1.ADDRF bit. If the address is in 10 bit format, the I^2C master should then generate a START and send an address header to the I^2C bus. After detecting START and the following address header, the slave will continue to set I2C_STS1.ADDRF bit. The software continues to read I2C_STS1 register and read I2C_STS2 register to clear the I2C_STS1.ADDRF bit a second time.
3. I^2C enters the data sending state, and now shift register and data register I2C_DAT are all empty, so the hardware will set the I2C_STS1.TXDATE(send data empty). At this time, the software can write the first byte data to I2C_DAT register, however, because the byte of the I2C_DAT register is immediately moved into the internal shift register, the I2C_STS1.TXDATE bit is not cleared to zero. When the shift register is not empty, I2C starts to send data to I^2C bus.
4. During the transmission of the first byte, the software writes the second byte to I2C_DAT, neither the I2C_DAT register nor the shift register is empty. The I2C_STS1.TXDATE bit is cleared to 0.
5. After the first byte is sent, I2C_STS1.TXDATE is set again, and the software writes the third byte to I2C_DAT, the same time, the I2C_STS1.TXDATE bit is cleared.After that, as long as there is still data to be sent and I2C_STS1.TXDATE is set to 1, the software can write a byte to I2C_DAT register.
6. During the sending of the second last byte, the software writes the last data to the I2C_DAT register to clear the I2C_STS1.TXDATE flag bit, and then the I2C_STS1.TXDATE status is no longer concerned. I2C_STS1.TXDATE bit is set after the second last byte is sent until the stop end bit is detected.
7. According to the I^2C protocol, the I^2C master will not send a ACK to the last byte received. Therefore, after the last byte is sent, the I2C_STS1.ACKFAIL bit (acknowledge fail) of the I^2C slave will be set to notify the software of the end of sending. The software writes 0 to the I2C_STS1.ACKFAIL bit to clear this bit.

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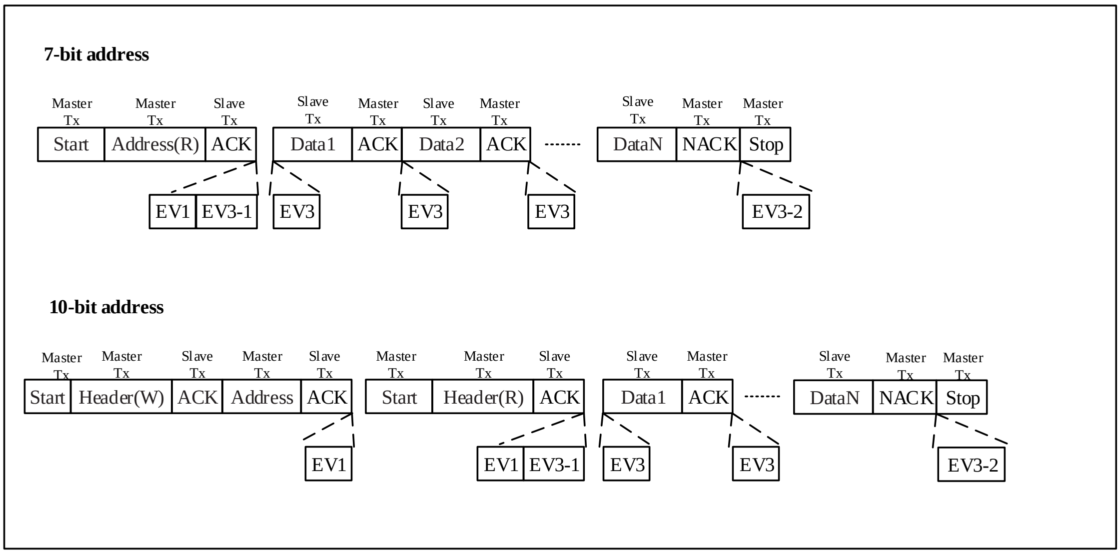
Figure 8-3 Slave Transmitter Transfer Sequence Diagram



Instructions：

1. EV1: I2C_STS1.ADDRF = 1, reading STS1 and then STS2 will clear this event.
2. EV3-1: I2C_STS1.TXDATE=1, shift register empty, data register empty, write DAT.
3. EV3: I2C_STS1.TXDATE=1, shift register not empty, data register empty, writing DAT will clear this event.
4. EV3-2: I2C_STS1.ACKFAIL=1, writing '0' to the ACKFAIL bit in STS1 will clear this event.

Notes:

(1) EV1 and EV3_1 event prolongs the low SCL time until the end of the corresponding software sequence.

(2) The software sequence of EV3 must be completed before the end of the current byte transfer.

8.3.2.5 I2C slave receiving mode

When receiving data in slave mode, the software should follow these steps:

1. First, enable the I^2C peripheral clock and configure the clock-related registers in I2C_CTRL1 to ensure correct I^2C timing. Once these steps are completed, the I^2C operates in slave mode, waiting to receive the start bit and address.
2. After receiving the START condition and a matching 7-bit or 10-bit address, the I^2C hardware sets the I2C_STS1.ADDRF bit (indicating the address received matches its own address) to 1. This bit should be detected by software through polling or interrupts. Once detected, the software clears the I2C_STS1.ADDRF bit by first reading the I2C_STS1 register and then the I2C_STS2 register. Once the I2C_STS1.ADDRF bit is cleared, the I2C slave begins receiving data from the I^2C bus.
3. Upon receiving the first byte, the I2C_STS1.RXDATNE bit (receive data not empty) is set to 1 by the hardware. If the I2C_CTRL2.EVTINTEN and I2C_CTRL2.BUFINTEN bits are set, an interrupt is generated. The software should detect this bit through polling or interrupts. Once detected, the software can read the first byte from the I2C_DAT register, and the I2C_STS1.RXDATNE bit is cleared. Note that if the I2C_CTRL1.ACKEN

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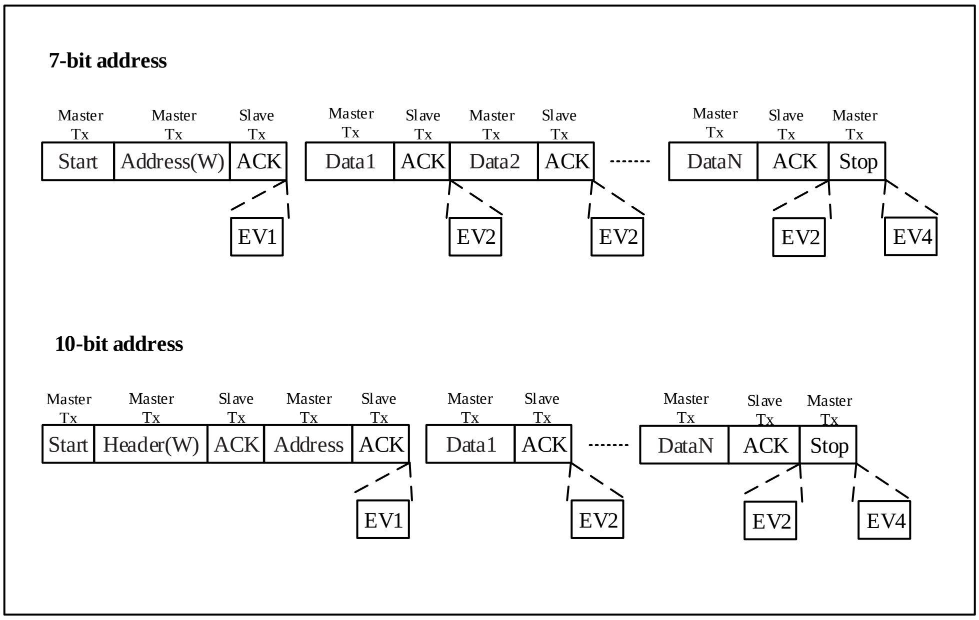
bit is set, the slave should generate an acknowledgment pulse after receiving a byte.

4. At any time the I2C_STS1.RXDATNE bit is set to 1, the software can read a byte from the I2C_DAT register. When the last byte is received, the I2C_STS1.RXDATNE is set to 1, and the software reads the last byte.

5. When the slave detects a stop condition (STOP) on the I^2C bus, the I2C_STS1.STOPF bit is set to 1. If the I2C_CTRL2.EVTINTEN bit is set, an interrupt is generated. The software clears the I2C_STS1.STOPF bit by reading the I2C_STS1 register and then writing to the I2C_CTRL1 register (see EV4 in the diagram below).

Figure 8-4 Slave receiver transmitting sequence



Instructions:

1. EV1: I2C_STS1.ADDRF = 1, reading STS1 and then STS2 to clear the event.

2. EV2: I2C_STS1.RXDATNE =1, reading DAT will clear this event.

3. EV4: I2C_STS1.STOPF=1, reading STS1 and then writing the CTRL1 register will clear this event.

Notes:

(1) EV1 event prolongs the time when SCL is low until the end of the corresponding software sequence.

(2) The software sequence of EV2 must be completed before the end of the current byte transmission.

8.3.2.6 I2C master transmission mode

In the master mode, the I^2C interface starts data transmission and generates a clock signal. Serial data transmission always starts with a start condition and ends with a stop condition. When the START condition is generated on the bus through the start bit, the device enters the master mode.

When sending data to I^2C bus in master mode, the software should operate as follows:

1. First, enable the I^2C peripheral clock, and configure the clock-related registers in I2C_CTRL1 to ensure the correct I^2C timing. When these two steps are completed, I^2C runs in the slave mode by default, waiting for receiving the start bit and address.

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2. When BUSY=0, I2C_CTRL1.STARTGEN bit set to 1, and the I^2C interface will generate a start condition and switch to the master mode (I2C_STS2.MSMODE bit set to “1”).

3. Once the start condition is issued, I^2C hardware will set I2C_STS1.STARTBF bit(START bit flag) and then enters the master mode. If the I2C_CTRL2.EVTINTEN bit is set, an interrupt will be generated. Then the software reads the I2C_STS1 register and then writes a 7-bit address bit or a 10-bit address bit with an address header to the I2C_DAT register to clear the I2C_STS1.STARTBF bit. After the I2C_STS1.STARTBF bit is cleared to 0, I^2C starts sending addresses or address headers to I^2C bus.

   In 10-bit address mode, sending a header sequence will generate the following events:

   - I2C_STS1.ADDR10F bit is set by hardware, and if I2C_CTRL2.EVTINTEN bit is set, an interrupt is generated. Then the master reads the STS1 register, and then writes the second address byte into the DAT register.
   - I2C_STS1.ADDRF bit is set by hardware, and if I2C_CTRL2.EVTINTEN bit is set, an interrupt is generated. Then the master reads the STS1 register, followed by the STS2 register.

   Note: In the transmitter mode, the master device first transmits the header byte (11110xx0) and then transmits the lower 8 bits of the slave address. (where xx represents the highest 2 bits of the 10-bit address).

   In the 7-bit address mode, only one address byte needs to be sent out. Once the address byte is sent out:

   - I2C_STS1.ADDRF bit is set by hardware, and if I2C_CTRL2.EVTINTEN bit is set, an interrupt is generated. Then the master device waits for reading the STS1 register once, followed by reading the STS2 register.

   Note: in the transmitter mode, when the master transmits the slave address, set the lowest bit to "0".

   Note: When the master transmission and in 7-bit address mode, the slave address cannot be configured as 0xF0, 0xF2, 0xF4, or 0xF6.

4. After the 7-bit or 10-bit address bit is sent, the I2C hardware sets the I2C_STS1.ADDRF bit (address has been sent) to 1, if the I2C_CTRL2.EVTINTEN bit is set, an interrupt is generated, and the software is cleared by reading the I2C_STS1 register and then the I2C_STS2 register I2C_STS1.ADDRF.

5. I^2C enters the data transmission state. Because the shift register and the data register (I2C_DAT) are empty, the hardware sets the I2C_STS1.TXDATE bit (transmission data empty) to 1, and then the software writes the first byte of data to the I2C_DAT register, but because the byte written into the I2C_DAT register is immediately moved into the internal shift register, the I2C_STS1.TXDATE bit will not be cleared at this time. Once the shift register is not empty, I^2C starts transmitting data to the bus.

6. During the transmission of the first byte, the software writes the second byte to I2C_DAT, and I2C_STS1.TXDATE is cleared at this time. At any time, as long as there is data waiting to be sent and the I2C_STS1.TXDATE bit is set to 1, the software can write a byte to the I2C_DAT register.

7. In the process of sending the penultimate byte, the software writes the last byte of data to I2C_DAT to clear the I2C_STS1.TXDATE flag bit. After that, there is no need to care about the status of the I2C_STS1.TXDATE bit. The I2C_STS1.TXDATE bit will be set after the penultimate byte is sent, and will be cleared when the stop bit (STOP) is sent.

8. After the last byte is sent, because the shift register and the I2C_DAT register are empty at this time, the I^2C host sets the I2C_STS1.BSF bit (byte transmission end), and the I2C interface will keep SCL low before clearing

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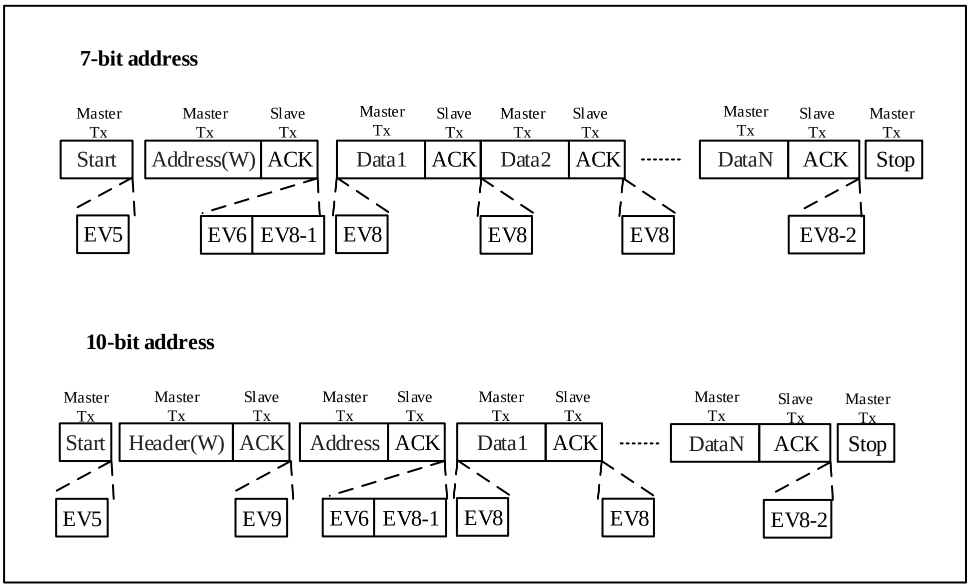
the I2C_STS1.BSF bit. After reading I2C_STS1, writing to the I2C_DAT register will clear the I2C_STS1.BSF bit. The software sets the I2C_CTRL1.STOPGEN bit at this time to generate a stop condition, and then the I2C interface will automatically return to the slave mode (I2C_STS2.MSMODE bit is cleared).

Figure 8-5 Master Transmitter Transfer Sequence Diagram



Instructions：

1. EV5: I2C_STS1.STARTBF = 1, reading STS1 and writing the address to the DAT register will clear the event.
2. EV6: I2C_STS1.ADDRF = 1, read STS1 and then STS2 to clear the event.
3. EV8_1: I2C_STS1.TXDATE = 1, shift register is empty, data register is empty, write DAT register.
4. EV8: I2C_STS1.TXDATE = 1, shift register is not empty, data register is empty, write to DAT register will clear the event.
5. EV8_2: I2C_STS1.TXDATE = 1, I2C_STS1.BSF = 1, request to set stop bit. These two events are cleared by the hardware when a stop condition is generated.
6. EV9: I2C_STS1.ADDR10F = 1, read STS1 and then write to DAT register to clear the event.

Notes:

a) *EV5, EV6, EV9, EV8_1 and EV8_2 event prolonged the low SCL time until the end of the corresponding software sequence.*

b) *The software sequence of EV8 must be completed before the end of the current byte transfer.*

c) *When I2C_STS1.TXDATE or I2C_STS1.BSF bit is set, stop condition should be arranged when EV8_2 occurs.*

8.3.2.7 I2C master receiving mode

In master mode, software receiving data from I^2C bus should follow the following steps:

1. First, enable the I^2C peripheral clock and configure the clock-related registers in I2C_CTRL1, in order to ensure that the correct I^2C timing is output. After enabling and configuring, I_2C runs in slave mode by default, waiting

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to receive the start bit and address.

2. When BUSY=0, set the I2C_CTRL.STARTGEN bit, and the I^{2}C interface will generate a start condition and switch to the master mode (I2C_STS2.MSMODE bit is set to 1).

3. Once the start condition is issued, the I^{2}C hardware sets I2C_STS1.STARTBF(start bit flag) and enters the host mode. If the I2C_CTRL2.EVTINTEN bit is set to 1, an interrupt will be generated. Then the software reads the I2C_STS1 register and then writes a 7-bits address or a 10-bits address with an address header to the I2C_DAT register, in order to clear the I2C_STS1.STARTBF bit. After the I2C_STS1.STARTBF bit is cleared to 0, I^{2}C begins to send the address or address header to the I^{2}C bus.
In 10-bits address mode, sending a header sequence will generate the following events:

   - The I2C_STS1.ADDR10F bit is set to 1 by hardware, and if the I2C_CTRL2.EVTINTEN bit is set to 1, an interrupt will be generated. Then the master device reads the STS1 register, and then writes the second byte of address into the DAT register.

   - The I2C_STS1.ADDRF bit is set to 1 by hardware, and if the I2C_CTRL2.EVTINTEN bit is set to 1, an interrupt will be generated. Then the master device reads the STS1 register and the STS2 register in sequence.

   Note: In the receiver mode, the master device sends the header byte (11110xx0) firstly, then sends the lower 8 bits of the slave address, and then resends a start condition followed by the header byte (11110xx1) (where xx represents the highest 2 digits of the 10-bits address).

   In the 7-bits address mode, only one address byte needs to be sent, once the address byte is sent:

   - The I2C_STS1.ADDRF bit is set to 1 by hardware, and if the I2C_CTRL2.EVTINTEN bit is set to 1, an interrupt will be generated. Then the master device waits to read the STS1 register once, and then reads the STS2 register.

   Note: In the receiving mode, the master device sets the lowest bit as '1' when sending the slave address.

4. After the 7-bits or 10-bits address is sent, the I^{2}C hardware sets the I2C_STS1.ADDRF bit (address has been sent) to 1. If the I2C_CTRL2.EVTINTEN bit is set to 1, an interrupt will be generated. The software clears the I2C_STS1.ADDRF bit by reading the I2C_STS1 register and the I2C_STS2 register in sequence. If in the 10-bit address mode, software should set the I2C_CTRL1.STARTGEN bit again to regenerate a START. After the START is generated, the I2C_STS1.STARTBF bit will be set. The software should clear the I2C_STS1.STARTBF bit by reading I2C_STS1 firstly and then writing the address header to I2C_DAT, and then the address header is sent to the I^{2}C bus, I2C_STS1.ADDRF is set to 1 again. The software should clear the I2C_STS1.ADDRF bit again by reading I2C_STS1 and I2C_STS2 in sequence.
5. After sending the address and clearing the I2C_STS1.ADDRF bit, the I^{2}C interface enters the host receiving mode. In this mode, the I^{2}C interface receives data bytes from the SDA line and sends them to the DAT register through the internal shift register. Once the first byte is received, the hardware will set the I2C_STS1.RXDATNE bit (not empty flag bit of received data) to 1, and if the I2C_CTRL1.ACKEN bit is set to 1, an acknowledge pulse will be sent. At this time, the software can read the first byte from the I2C_DAT register, and then the I2C_STS1.RXDATNE bit is cleared to 0. After that, as long as I2C_STS1.RXDATNE is set to 1, the software can read a byte from the I2C_DAT register.
6. The master device sends a NACK after receiving the last byte from the slave device. After receiving the NACK, the slave device releases the control of SCL and SDA lines; the master device can send a stop/restart condition. In order to generate a NACK pulse after receiving the last byte, the software should clear the

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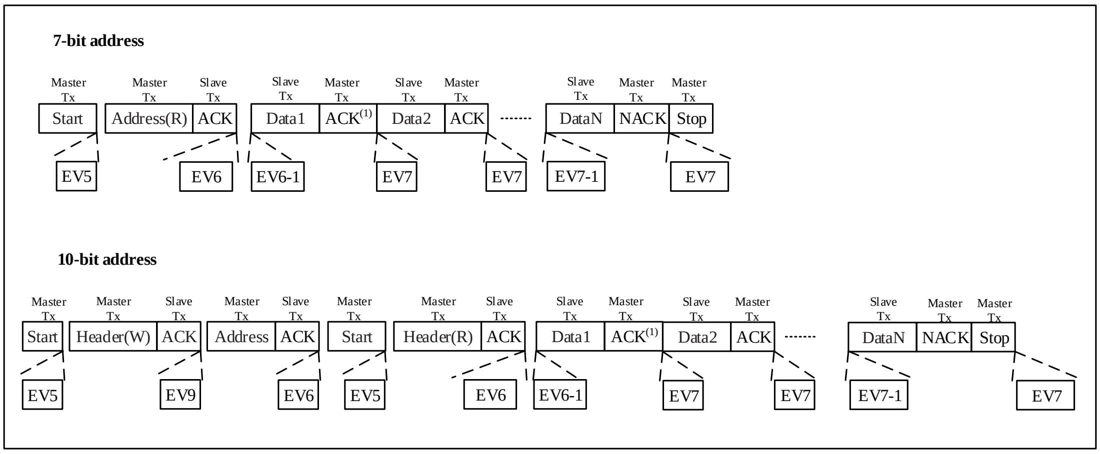
I2C_CTRL1.ACKEN bit immediately after receiving the penultimate byte (N-1). In order to generate a stop/restart condition, the software must set the I2C_CTRL1.STOPGEN bit or I2C_CTRL1.STARTGEN to 1 after reading the penultimate data byte. This process needs to be completed before the last byte is received to ensure that the NACK is sent for the last byte.

7. After the last byte is received, the I2C_STS1.RXDATNE bit is set to 1, and the software can read the last byte. Since I2C_CTRL1.ACKEN has been cleared to 0 in the previous step, I^2C no longer sends ACK for the last byte, and generates a STOP bit after the last byte is sent.

Note: The above steps require the number of bytes N>1. If N=1, step 6 should be executed after step 4, and it needs to be completed before the reception of byte is completed.

Figure 8-6 Master receiver transmission sequence diagram



Instructions:

1. EV5: I2C_STS1.STARTBF=1, Reading STS1 and then writing the address into the DAT register will clear this event.
2. EV6: I2C_STS1.ADDRF=1, Reading STS1 and then reading STS2 will clear this event. In 10-bit master receive mode, after this event, STARTGEN=1 should be set in CTRL1.
3. EV6_1: There is no corresponding event flag, suitable for receiving one byte. Right after EV6 (i.e., after clearing ADDRF), the generation bits for acknowledgment and stop condition need to be cleared.)
4. EV7: I2C_STS1.RXDATNE=1, Reading the DAT register clears this event.
5. EV7_1: I2C_STS1.RXDATNE =1, Reading the DAT register clears this event. Set I2C_CTRL1.ACKEN=0 and I2C_CTRL1.STOPGEN=1.
6. EV9: I2C_STS1.ADDR10F=1, Reading STS1 and then writing to the DAT register will clear this event.

Notes:

a) If a single byte is received, it is NA.

b) EV5, EV6, and EV9 events extend the low level of SCL until the corresponding software sequence ends.

c) The EV7 software sequence shall be completed before the end of the current byte transmission.

d) The software sequence of EV6_1 or EV7_1 shall be completed before the ACK pulse of the current transmission

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byte.

8.3.3 Error Conditions

I^{2}C errors mainly include bus error, acknowledge error, arbitration loss, overload\ underload error. These errors may cause communication failure.

8.3.3.1 Acknowledge failure (ACKFAIL)

The interface have a acknowledge bit is detected that does not match the expectation, it will occurs acknowledge fail error, I2C_STS1.ACKFAIL bit is set. An interrupt occurs, when I2C_CTRL2.ERRINTEN bit is set to 1.

When transmitter receives a NACK, The communication must be reset: Device in slave mode, hardware release the bus; Device in master mode, it must generate a stop condition from software.

8.3.3.2 Bus error (BUSERR)

when address or data is transmissing, I^{2}C interface receive external stop or start condition,it will happen a bus error, I2C_STS1.BUSERR bit is set. An interrupt occurs, when I2C_CTRL2.ERRINTEN bit is set to 1.

I^{2}C device as master, the hardware does not release bus, as the same time it done not affect the current status of transfer, The current transfer will determined by software whether suspend.

I^{2}C device as slave, when data is discarded in transmission and the bus releases by hardware, it will have two situation: If an error start condition is detected, the slave device considers a restart condition and waits for an address or a stop condition. If an error stop condition is detected, the slave device operates as a normal stop condition and the hardware releases the bus.

8.3.3.3 Arbitration lost (ARLOST)

The interface have arbitration lost is detected, hardware release the bus, it will occurs arbitration lost error, I2C_STS1.ARLOST bit is set. An interrupt occurs, when I2C_CTRL2.ERRINTEN bit is set to 1.

I^{2}C interface will go to slave mode automatically (I2C_STS2.MSMODE bit is cleared). When the I^{2}C interface lost the arbitration, in the same communication, it can not respond to its slave address, but it can respond when master win the bus retransmits a start signal. Hardware release the bus.

8.3.3.4 Overrun/underrun error (OVERRUN)

In slave mode, Overrun/Underrun error can easily occur if clock stretching is disable.

When I^{2}C interface is receiving data (I2C_STS1.RXDATNE=1, data have received in register), and I2C_DAT register still has previous byte which has not been read, it will occurs an overrun error. In this situation, the last received data is discarded. And software should clear I2C_STS1.RXDATNE bit, transmitter retransmit last byte.

When I2C interface is sending data (I2C_STS1.TXDATE=1, new data has not sent to register), and I2C_DAT register still empty, it will occur an underrun error. In this situation, the previous byte in the I2C_DAT register is sent repeatedly. And user makes sure that in the event of an underrun error, the receiver discard repeatedly byte, and transmitter should update the I2C_DAT register at the specified time according to the I2C bus standard.

In sending the first byte, I2C_DAT register must be written after I2C_STS1.ADDRF bit is cleared and the before the first SCL rising edge. If cannot make sure do that, the first byte should be discard by receiver.

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8.3.4 DMA Application

DMA can generate a requests when transfer data register empty or full. DMA can write data to I^2C or read data from I^2C reduce the CPU overload.

Before the current byte transfers end, DMA requests must be responded. If set the DMA channel transfer data is done, DMA will send EOT(End Of Transmission) to I^2C, and ocurr a interrupt when enable interrupt bit.

In the master transfer mode, in EOT interrupt handler DMA request need to be disbale, and set stop condition after waiting for I2C_STS1.BSF event.

In the master receive mode, the data of received is great than or equal to 2, DMA will send a hardware signal EOT_1 in DMA transmission(byte number-1). If set I2C_CTRL2.DMALAST bit, when hardware has sent the EOT_1 next byte it will send a NACK automatically. The user can set a stop condition in the interrupt handler after the DMA transfer is completed if interrupt enable.

8.3.4.1 Transmit process

DMA mode can be enabled by setting the I2C_CTRL2.DMAEN bit. When I2C_STS1.TXDATE bit is set, the data will send to I2C_DAT from storage area by the DMA. DMA assigns a channle for I2C transmission, (x is the channel number) the following step must be opreate:

1. In the DMA_PADDRx register set the I2C_DAT register address. Data will be send to address in every I2C_STS1.TXDATE event.
2. In the DMA_MADDRx register set the memory address. Data will send to I2C_DAT address in every I2C_STS1.TXDATE event.
3. In the DMA_TXNUMx register set the number of need to be transferred.In every I2C_STS1.TXDATE event this number-1 until 0.
4. In the DMA_CHCFGx register set PRIOLVL[1:0] bit to configure the priority of channel.
5. In the DMA_CHCFGx register set DIR bit to configure when ocurrs an interrupt whether send a half data or all completed.
6. In the DMA_CHCFGx register set CHEN bit to enable transfer channel.
7. When DMA transfer data is done, DMA need send a EOT/EOT_1 signal to I2C indicate this transfer is done. If interrupt is enable, DMA ocurrs a interrrupt.

Note: If DMA is used for transmission, do not set I2C_CTRL2.BUFINTEN bit

8.3.4.2 Receive process

DMA mode can be enabled by setting I2C_CTRL2.DMAEN bit. When data byte is received, DMA will send I^2C data to storage area. To set DMA channel for I^2C reception, the following steps must be opreate:

1. In DMA_PADDRx register set the address of the I2C_DAT register. In every I2C_STS1.RXDATEN event, data will send from address to storage area.
2. In DMA_MADDRx register set the memory area address. In every I2C_STS1.RXDATEN event,data will send from I2C_DAT register to storage area.
3. In DMA_TXNUMx register set the number of need to be transferred. In every I2C_STS1.RXDATEN event the

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number-1 until 0.

4. In DMA_CHCFGx register set PRIOLVL[1:0] to configure the priority of channel.
5. In DMA_CHCFGx register clear DIR to configure when ocurrs a interrupt request whether received half data or all data is received.
6. In the DMA_CHCFGx register set CHEN bit to activate the channle.
7. When DMA tansfer data is done, DMA need to send EOT/EOT_1 signal to I2C indicate this transfer is done, if interrupt is enbale, DMA ocurrs a interrupt.

Note: If DMA is used for receiving, do not set I2C_CTRL2.BUFINTEN bit.

8.3.5 Packet Error Check (PEC)

Setting the I2C_CTRL1.PECEN bit to 1 enable the PEC function. PEC uses CRC-8 algorithm to calculate all information bytes including address and read/write bits. It can improve the reliability of communication. The CRC-8 polynomial uses by the PEC calculator is $C(x) = x^8 + x^2 + x + 1$.

In transmitting mode, software sets I2C_CTRL1.PEC transfer bit in the last I2C_STS1.TXDATE event, and then PEC will be transferred in the last byte. In receiving mode, software sets I2C_CTRL1.PEC transfer bit after the last I2C_STS1.RXDATNE event, and then receives the PEC byte and compares the received PEC byte to the internally calculated PEC value. If it is not equal to the internally calculated PEC value, the receiver needs to send a NACK. If it is host receiver mode, NACK will be sent after PEC regardless of the calculated result. It should pay attention that I2C_CTRL1.PEC bit has to be set before receiving.

If both DMA and PEC calculator are activated, I^2C will automatically send or check the PEC value.

In transmitting mode, when I^2C interface receives EOT signal from DMA controller, it will automatically send PEC following the last byte. In receiving mode, when I^2C interface receives an EOT_1 signal from DMA, it will automatically consider the next byte as PEC and compare it with the internally calculated PEC. It will happen a DMA request after receiving PEC.

In order to allow intermediate PEC transfer, I2C_CTRL2.DMALAST bit is used to determine whether it is the last DMA transfer. And if it does the last DMA request of the master receiver, NACK will be sent automatically after receiving the last byte.

When arbitration is lost, PEC calculation is invalid.

8.3.6 Timeout Error

The SMBus features a timeout mechanism: if a communication process takes too long, it will automatically reset the device. This is why SMBus requires a minimum data transfer rate — to prevent the bus from remaining locked up for an extended period after a timeout occurs. The I2C bus supports "clock stretching," a mechanism allowing a busy slave device to halt communication by holding the clock line low, forcing the master to wait until the slave is ready to proceed.

The N32G033 series chips support configurable timeout periods in both I2C mode and SMBUS mode, including SCL low timeout detection, SCL high timeout detection, and SDA low timeout detection:

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SCL Low Timeout: The timeout threshold is configured via I2C_CTRL1.LTOSEL, and the timeout detection is enabled by I2C_CTRL2.LTOEN. If SCL remains low longer than the set threshold, I2C_STS1.SCLLTO is set to 1. An interrupt is generated if I2C_CTRL2.SCLLTOINTEN is set to 1.

SCL High Timeout: The timeout threshold is configured via I2C_CTRL1.HTOSEL, and the timeout detection is enabled by I2C_CTRL2.HTOEN. If SCL remains high longer than the set threshold, I2C_STS1.SCLHTO is set to 1. An interrupt is generated if I2C_CTRL2.SCLHTOINTEN is set to 1.

SDA Low Timeout: The timeout threshold is configured via I2C_CTRL1.LTOSEL, and the timeout detection is enabled by I2C_CTRL2.LTOEN. If SDA remains low longer than the set threshold, I2C_STS1.SDALTO is set to 1. An interrupt is generated if I2C_CTRL2.SDALTOINTEN is set to 1.

Additionally, in SMBUS mode, the cumulative SCL low timeout feature is automatically enabled. The timeout threshold is fixed at 10 ms for the master and 25 ms for the slave. If the cumulative time SCL remains low exceeds the threshold, I2C_STS1.SCLHTO is set to 1. An interrupt is generated if I2C_CTRL2.SCLHTOINTEN is set to 1.

Slave Mode Timeout: The slave device resets the communication and the hardware releases the bus.

Master Mode Timeout: The hardware issues a STOP condition.

8.3.7 SMBus

8.3.7.1 Introduction

The System Management Bus(SMBus or SMB) is a simple single-ended two-wire bus structure. Using SMBus can communicate with other device or other parts of the system, it able to commnicate with multiple devices without other independent control wire. SMBus is a derivate of the I^2C bus and provides a control bus for system and power management related tasks. If you want browse more information, please refer to the SMBus specification V2.0 (http://smbus.org/specs/).

SMBus have three types of device standard.

- Master: device send command, generate clocks and stop transmmissions;
- Slave: device receive, respond to commands;
- Host: system have only one host. A device provides a master to system CPU. Host have functions of master and slave, it supports SMBus alert protocol.

SMBus is a subset of the data transmission format of the I^2C specification.

Similarities between SMBus and I^2C:

- Both bus protocols contain of 2 wires (a clock wire SCL and a data wire SDA), with an optional SMBus alert wire.
- The data format is similar. SMBus data format is similar to 7-bit address format of I2C(See Figure 8-2).
- Both are master-slave communication modes, and the master device provides the clock.
- Both support multi master.

Differences between SMBus and I^2C:

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Table 8-1 Comparison Between SMBus And I2C

SMBus	I^2C
Maximum transmission speed 100kHz	Maximum transmission speed 1MHz
Minimum transmission speed 10kHz	No minimum transmission speed
Low clock timeout 35ms	No clock timeout
Fixed logic level	V_{DD} determined logic level
Different address types (reserved, dynamic, etc.)	7-bit, 10-bit, and broadcast call slave address types
Different bus protocols (quick command, call handling, etc.)	No bus protocol

8.3.7.2 Purpose of SMBus

SMBus uses the system management bus to meet lightweight communication requirements. In general, SMBus is commonly used on the computer motherboard. It is mainly used to transmit ON/OFF instructions for power unit and provide a control bus for system and power management-related tasks.

8.3.7.3 Device identification

In SMBus, any device acting as a slave device has an address called the slave address.

In order to distribute addres for each devices, it must have a unique device identifier(UDID) to distinguish devices.

8.3.7.4 Bus protocol

SMBus specification includes eight bus protocols. If user wants browse the details on protocols or SMBus address types,it can refer to the SMBus specification v2.0(http://smbus.org/specs/). User's software can device what protocols are implemented.

Every packet through the SMBus complies with the SMBus protocol predefined format. SMBus is a subset of the data transfer format of I^2C specification. As long as an I^2C device can be accessed through one of the SMBus protocols, it is considered to be SMBus compliant.

Note: SMBus does not support Quick command protocol.

8.3.7.5 Address resolution protocol (ARP)

The SMBus resolves address conflicts by dynamically assigning a new unique address to each slave device. This is the address resolution protocol(ARP) .

Any master device can connected bus to access all devices.

SMBus physical layer arbitration enable to distribute addresses.When device powers on, the device's distribute address is not change, the protocol allows address retain when device power off.

When address is distributed, there is no extra SMBus packaging cost (the cost time that access distribute address device and access fixed address device is same).

8.3.7.6 SMBus alter mode

SMBus offers a optional interrupt signal SMBALERT(like SCL and SDA, is a wire-AND signal) that devices use to extend their control capabilities at expense of a pin. SMBus broadcast call address often combine with SMBALERT. There are 2 bytes message about SMBus.

A device which only has slave function can set I2C_CTRL1.SMBALERT bit to indicate it want to communicate with

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host. The host handles the interrupt and accesses all SMBALERT devices through the ARA (Alert Response Address, address value 0001100x). Only those devices that pull SMBALERT low can respond to ARA. This state is identified by the I2C_STS1.SMBALERT. The 7-bit device address provided from the sending device is placed on the 7 most significant bits of the byte, the eighth bit can be either '0' or '1'.

When more than one device's SMBALERT is low, the highest priority(The smaller the address, the higher the priority) can win bus communication through the standard arbitration during address transmission. If confirming the slave address, device's SMBALERT is no longer pulled low. If message transmitted completely, device's SMBALERT still is low, it means host will read ARA again. The host can periodically access the ARA when the SMBALERT signal is not used.

8.3.7.7 SMBus communication process

The communication process on SMBus is similar to that on I^2C. To use the SMBus mode, you need to configure SMBus specific registers in the program, respond and process SMBus specific flag, and implement the upper-layer protocols described in the SMBus manual.

1. At first, set I2C_CTRL1.SMBMODE bit, and configure I2C_CTRL1.SMBTYPE bit and I2C_CTRL1.ARPEN bit according to the application requirements. If I2C_CTRL1.ARPEN=1 and I2C_CTRL1.SMBTYPE=0, use the default address of the SMB device. If I2C_CTRL1.ARPEN=1 and I2C_CTRL1.SMBTYPE=1, use the SMB master header field.
2. In order to support ARP (I2C_CTRL1.ARPEN=1), in SMBus host mode (I2C_CTRL1.SMBTYPE=1), software needs to respond to the I2C_STS2.SMBHADDR bit (in SMBus slave mode, respond to I2C_STS2.SMBDADDR bit) and implement the functions according to the ARP protocol.
3. To support the SMBus warning mode, software should respond to the I2C_STS1.SMBALERT bit and implement the corresponding functions.

8.3.8 Noise Filtering

The I^2C interface standard requires the ability to filter spikes on the SCL/SDA lines with a duration of 50ns, hence analog and digital filters are designed. The analog filter is enabled by default and can also be disabled by setting the I2C_GFLTRCTRL.SCLAFENN/SDAAFENN bits. The analog filter sets the spike filter width to 5ns, 15ns, 25ns, 35ns by configuring the I2C_GFLTRCTRL.SCLAFE/SDAAFW.

The digital filter is enabled by setting I2C_GFLTRCTRL.SCLDFW/SDADFW to a non-zero value. The maximum filter width is (I2C_GFLTRCTRL.SCLDFW[3:0] or I2C_GFLTRCTRL.SDADFW[3:0]) * TPCLK. Enabling the digital filter will increase the hold time of the SDA line by an amount of (SDADFW[3:0]+1) * TPCLK.

8.4 Debug Mode

When the microcontroller enters debug mode (with the Cortex®-M0 core halted), the SMBus timeout control either continues to function normally or can be stopped according to the configuration bits DBG_CTRL.I2C1TIMOUT and DBG_CTRL.I2C2TIMOUT in the PWR module. For details, refer to Section 3.3.1.

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8.5 Interrupt Request

All I²C interrupt requests are listed in the following table.

Table 8-2 I2C Interrupt Request

Interrupt Function	Interrupt Event	Event Flag	Set Control Bit
I2C event interrupt	Start bit sent (master)	STARTBF	EVTINTEN
	Address sent (master) or address matched (slave)	ADDRF	
	10-bit header sent (master)	ADDR10F	
	Received stop (slave)	STOPF	
	Data byte transfer completed.	BSF	
	Receive buffer is not empty.	RXDATNE	EVTINTEN and BUFINTEN
	Send buffer is empty.	TXDATE	
I2C error interrupt	Bus error	BUSERR	ERRINTEN
	Lost arbitration (master)	ARLOST	
	Acknowledge fail	ACKFAIL	
	Overrun/underrun	OVERRUN	
	PEC error	PECERR	
	SMBus Alert	SMBALERT	
	SCL Low Timeout	SCLLTO	SCLLTOINTEN
	SCL High Timeout	SCLHTO	SCLHTOINTEN
	SDA Low Timeout	SDALTO	SDALTOINTEN

8.6 I2C Registers

These peripheral registers can be operated by half word (16 bits) or word (32 bits)

8.6.1 I²C Register Overview

Table 8-3 Register Overview

Offset	Register	32	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
000h	I2C_CTRL1	Reserved	LTOSEL		HTOSEL		Reserved											Reserved		SWRESET	SMBALERT	PEC	ACKPOS	ACKEN	STOPGEN	STARTGEN	NOEXTEND	GCEN	PECEN	ARPEN	SMBTYPE	SMBMODE	EN
004h	I2C_CTRL2	Reserved	LTOEN	HTOEN	SCLLTOINTEN	SCLHTOINTEN	SDALTOINTEN	Reserved										DMAEN	ERRINTEN	EVTINTEN	BUFINTEN	Reserved			DMALAST	Reserved	CLKFREQ[6:0]						
008h	I2C_OADDR1	Reserved																ADDRMODE	Reserved					ADDR[9:8]		ADDR[7:1]							ADDR0

00Ch	I2C_OADDR2	Reserved	Reserved	ADDR2[7:1]	DUALE																	
010h	I2C_DAT	Reserved	Reserved	DATA[7:0]																		
014h	I2C_STS1	Reserved	SCLLTO	SCLHTO	SDALTO	Reserved	Reserved	SMBALERT	TIMEOUT	PECERR	OVERRUN	BUSERR	ARLOST	ACKFAIL	Reserved	ADDR10F	TXDATE	RXDATNE	STOPF	BSF	ADDRF	STARTBF
018h	I2C_STS2	Reserved	PECVAL[7:0]	SMBHADDR	SMBDADDR	DUALFLAG	GCALLADDR	Reserved	TRF	MSMODE	BUSY											
01Ch	I2C_CLKCTRL	Reserved	DUTY	FSMODE	Reserved	CLKCTRL[11:0]																
020h	I2C_TMRISE	Reserved	Reserved	TMRISE[5:0]																		
028h	I2C_GFLTRCTRL	Reserved	SCLAFENN	Reserved	SCLAFW[1:0]	SDAAFENN	Reserved	SDAAFW[1:0]	SCLDFW[3:0]	SDADFW[3:0]												

8.6.2 I2C Control Register 1 (I2C_CTRL1)

Address offset: 0x00

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved	LTOSEL		HTOSEL		Reserved										
	rw		rw												

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved		SW RESET	SMB ALERT	PEC	ACKPOS	ACKEN	STOP GEN	START GEN	NO EXTEND	GCEN	PECEN	ARPEN	SMB TYPE	SMB MODE	EN
		rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Bit Field	**Name**	**Description**
31	Reserved	Reserved, the reset value must be maintained.
30:29	LTOSEL	Low Timeout Threshold Selection 00:25ms; 01:100ms; 10:1s; 11:4s. *Note: Only used for I2C mode.*
28:27	LTOSEL	High Timeout Threshold Selection 00:256us; 01:512us; 10:1000us;

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Bit Field	Name	Description
		11:128us. *Note: Only used for I2C mode.*
26:14	Reserved	Reserved, the reset value must be maintained.
13	SWRESET	Software reset Make sure the I2C bus is idle before resetting this bit. 0:I2C not reset; 1:I2C reset. *Note: This bit can be used when the I2C_STS2.BUSY bit is set to 1 and no stop condition is detected on the bus.*
12	SMBALERT	SMBus alert It can be set or cleared by software. When I2C_CTRL1.EN=0, it will be cleared by hardware. 0: SMBAlert pin go high. The response address header is followed by the NACK signal; 1: SMBAlert pin go low. The response address header is followed by the ACK signal.
11	PEC	Packet error checking It can be set or cleared by software. It will be cleared by hardware when PEC has been transferred, or by start or stop condition, or when I2C_CTRL1.EN=0. 0: No PEC transfer; 1: PEC transfer. *Note: When arbitration is lost, the calculation of PEC is invalid.*
10	ACKPOS	Acknowledge/PEC Position (for data reception) It can be set or cleared by software. Or when I2C_CTRL1.EN=0, it will be cleared by hardware. 0: I2C_CTRL1.ACKEN bit determines whether to send an ACK to the byte currently being received; I2C_CTRL1.PEC bit indicates that the byte in the current shift register is PEC; 1: I2C_CTRL1.ACKEN bit etermines whether to send an ACK to the next received byte. I2C_CTRL1.PEC bit indicates that the next byte received in the shift register is PEC. *Note：* *ACKPOS bit can only be used in 2-byte receiving configuration and must be configured before receiving data.* *For the second byte of NACK, the I2C_CTRL1.ACKEN bit must be cleared after the I2C_STS1.ADDRF bit is cleared.* *To detect the PEC of the second byte, the I2C_CTRL1.PEC bit must be set after the ACKPOS bit is configured and when the ADDR event is extended.*
9	ACKEN	Acknowledge enable It can be set or cleared by software. Or when I2C_CTRL1.EN equals to 0, it will be cleared by hardware. 0: No acknowledge send; 1: Send an acknowledge after receiving a byte.
8	STOPGEN	Stop generation It can be set or cleared by software. Or it will be cleared by hardware when a stop condition is detected. Or it will be set by hardware when SMBus timeout error is detected,. In the master mode: 0: No stop condition generates;

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Bit Field	Name	Description
		1: A stop condition is issued after either the current byte transfer or the current start condition. In the slave mode: 0: No stop condition generates; 1: During the current byte transmission or release of the SCL and SDA lines. *Note：When the STOPGEN, STARTGEN or PEC bit is set, the software should not take any write operation to I2C_CTRL1 until this bit is cleared by hardware. Otherwise, the STOPGEN, STARTGEN or PEC bits may be set twice.*
7	STARTGEN	Start generation It can be set or cleared by software. Or it will be cleared by hardware when the start condition is transferred or I2C_CTRL1.EN=0. 0: No start condition generates; 1: Generate a start conditions.
6	NOEXTEND	Clock extending disable (Slave mode) This bit determines whether to pull SCL low when the data is not ready(I2C_STS1.ADDRF or I2C_STS1.BSF flag is set) in slave mode, and is cleared by software reset 0: Enable Clock extending; 1: Disable Clock extending.
5	GCEN	General call enable 0: Disable General call. not respond(NACK) to the address 00h; 1: Enable General call. respond(ACK) the address 00h.
4	PECEN	PEC enable 0: Disable PEC module; 1: Enable PEC module.
3	ARPEN	ARP enable 0: Disable ARP; 1: Enable ARP. If I2C_CTRL1.SMBTYPE=0, the default address of SMBus device is used. If I2C_CTRL1.SMBTYPE=1, the host address of SMBus is used.
2	SMBTYPE	SMBus type 0: Device; 1: Host.
1	SMBMODE	SMBus mode 0: I2C mode; 1: SMBus mode.
0	EN	I2C Peripheral enable 0: Disable I2C module; 1: Enable I2C module. *Note: If communication is in progress when this bit is cleared, the I2C module will be disabled and return to the idle state upon completion of the current communication. Since EN=0 occurs after the communication ends, all bits are cleared.*

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8.6.3 I2C Control Register 2 (I2C_CTRL2)

Address offset: 0x04

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved	LTOEN	HTOEN	SCLLTO INTEN	SCLHTO INTEN	SDALTO INTEN	Reserved									
	rw	rw	rw	rw	rw										

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DMAEN	ERRINT EN	EVTINT EN	BUFINT EN	Reserved			DMA LAST	Reserved	CLKFREQ[6:0]						
rw	rw	rw	rw				rw		rw						

Bit Field	Name	Description
31	Reserved	Reserved, the reset value must be maintained.
30	LTOEN	Low Timeout function Enable 0: Disable; 1: Enable. *Note: In I2C mode, this bit can be disabled when timeout error reporting is not required.*
29	HTOEN	High Timeout Enable 0: Disable; 1: Enable. *Note: In I2C mode, this bit can be disabled when timeout error reporting is not required.*
28	SCLLTOINTEN	SCL Low Timeout Interrupt Enable 0: When I2C_STS1.SCLLTO = 1, no interrupt is generated; 1: When I2C_STS1.SCLLTO = 1, an interrupt is generated.
27	SCLHTOINTEN	SCL High Timeout Error Interrupt Enable This bit is cleared by software writing '0', or cleared by hardware when I2C_CTRL1.EN = 0. 0: No interrupt is generated when I2C_STS1.SCLHTO = 1; 1: An interrupt is generated when I2C_STS1.SCLHTO = 1. *Note: In SMBUS mode, this bit also serves as the interrupt enable for cumulative SCL low timeout.*
26	SDALTOINTEN	SDA Low Timeout Error Interrupt Enable This bit is cleared by software writing '0', or cleared by hardware when I2C_CTRL1.EN = 0. 0: No interrupt is generated when I2C_STS1.SDALTO = 1; 1: An interrupt is generated when I2C_STS1.SDALTO = 1.

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Bit Field	Name	Description
25:16	Reserved	Reserved, the reset value must be maintained.
15	DMAEN	DMA requests enable 0: Disable DMA request; 1: Enable DMA request.
14	ERRINTEN	0: Disable error interrupt. 1: Enable error interrupt. This interrupt is generated under the following conditions: I2C_STS1.BUSERR = 1 I2C_STS1.ARLOST = 1 I2C_STS1.ACKFAIL = 1 I2C_STS1.OVERRUN = 1 I2C_STS1.PECERR = 1 I2C_STS1.SMBALERT = 1
13	EVTINTEN	Event interrupt enable nterrupt Enable Setting: 0: Event interrupt disabled; 1: Event interrupt enabled. This interrupt will be generated under the following conditions: I2C_STS1.STARTBF = 1 (Master mode) I2C_STS1.ADDRF = 1 (Master/Slave mode) I2C_STS1.ADD10F = 1 (Master mode) I2C_STS1.STOPF = 1 (Slave mode) I2C_STS1.BSF = 1, but without an I2C_STS1.TXDATE or I2C_STS1.RXDATNE event If I2C_STS1.BUFINTEN = 1, and the I2C_STS1.TXDATE flag is 1 If I2C_STS1.BUFINTEN = 1, and the I2C_STS1.RXDATNE flag is 1
12	BUFINTEN	Buffer interrupt enable 0: No interrupt is generated when I2C_STS1.TXDATE=1 or I2C_STS1.RXDATNE=1; 1: An event interrupt is generated when I2C_STS1.TXDATE=1 or I2C_STS1.RXDATNE=1. (provided I2C_CTRL2.EVTINTEN=1), regardless of the state of DMAEN.
11:9	Reserved	Reserved, the reset value must be maintained.
8	DMALAST	DMA last transfer 0: The next DMA EOT is not the last transfer; 1: The next DMA EOT is the last transfer. *Note: This bit is used in Master Receiver mode to enable generating a NACK upon receiving the last data byte.*
7	Reserved	Reserved, the reset value must be maintained.
6:0	CLKFREQ[6:0]	I2C peripheral clock frequency

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Bit Field	Name	Description
		CLKFREQ[6:0] should be set according to the APB clock frequency to ensure correct timing: 0000000: Disabled 0000001: Disabled 0000010: 2 MHz 0000011: 3 MHz ... 1000000: 64 MHz 1000001~1111111: Disabled

8.6.4 I2C Own Address Register 1 (I2C_OADDR1)

Address offset: 0x08

Reset value: 0x0000

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR MODE	Reserved	Reserved				ADDR [9:8]		ADDR[7:1]							ADDR0
rw						rw		rw							rw

Bit Field	Name	Description
15	ADDRMODE	Addressing mode (slave mode) 0: 7-bit slave address(does not respond to 10-bit address); 1: 10-bit slave address (does not respond to 7-bit address).
14	Reserved	Reserved, the reset value must be maintained.
13:10	Reserved	Reserved, the reset value must be maintained.
9:8	ADDR[9:8]	Interface address 9~8 bit of the address. *Note: don't care these bits in 7-bit address mode.*
7:1	ADDR[7:1]	Interface address 7~1 bits of the address.
0	ADDR0	Interface address 0 bit of the address. *Note: don't care these bits in 7-bit address mode.*

8.6.5 I2C Own Address Register 2 (I2C_OADDR2)

Address offset: 0x0C

Reset value: 0x0000 0000

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15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								ADDR2[7:1]							DUALEN
											rw				rw

Bit Field	Name	Description
31:8	Reserved	Reserved, the reset value must be maintained.
7:1	ADDR2[7:1]	Interface address 7~1 bits of address in dual address mode.
0	DUALEN	Dual addressing mode enable 0: Disable dual address mode, only OADDR1 is recognized; 1: Enable dual address mode, both OADDR1 and OADDR2 are recognized. *Note: Valid only for 7-bit address mode.*

8.6.6 I2C Data Register (I2C_DAT)

Address offset: 0x10

Reset value: 0x0000 0000

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								DATA[7:0]							
											rw				

Bit Field	Name	Description
31:8	Reserved	Reserved, the reset value must be maintained.
7:0	DATA[7:0]	8-bit data register Send or receive data buffer. *Note: In the slave mode, the address will not be copied into the data register;* *Note: if I2C_STS1.TXDATE =0, data can still be written into the data register;* *Note: If the ARLOST event occurs when processing the ACK pulse, the received byte will not be copied into the data register, so it cannot be read.*

8.6.7 I2C Status Register 1 (I2C_STS1)

Address offset: 0x14

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved						SCLLTO	SCLHTO	SDALTO	Reserved						
						rc_w0	rc_w0	rc_w0							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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Reserved	SMB ALERT	TIMEOUT	PECERR	OVER RUN	BUSERR	ARLOST	ACKFAIL	Reserved	ADDR10F	TXDATE	RXDAT NE	STOPF	BSF	ADDRF	STARTBF
	rc_w0	rc_w0	rc_w0	rc_w0	rc_w0	rc_w0	rc_w0		r	r	r	r	r	r	r

Bit Field	Name	Description
31:26	Reserved	Reserved, the reset value must be maintained.
25	SCLLTO	SCL Low Timeout Error This bit is cleared by software writing '0', or cleared by hardware when I2C_CTRL1.EN = 0. 0: No SCL low timeout error occurred; 1: SCL low timeout error occurred.
24	SCLHTO	SCL High Timeout Error This bit is cleared by software writing '0', or cleared by hardware when I2C_CTRL1.EN = 0. 0: No timeout error occurred; 1: A timeout error has occurred. Note: In SMBUS mode, this bit also functions as the SCL cumulative low timeout flag.
23	SDALTO	SDA Low Timeout Error This bit is cleared by software writing '0', or cleared by hardware when I2C_CTRL1.EN = 0. 0: No timeout error occurred; 1: A timeout error has occurred.
22:15	Reserved	Reserved, the reset value must be maintained.
14	SMBALERT	SMBus alert Writing '0' to this bit by software can clear it, or it is cleared by hardware when I2C_CTRL1.EN=0. 0: No SMBus alert(host mode) or no SMB alert response address header sequence(slave mode); 1: SMBus alert event is generated on the pin(host mode) or receive SMBAlert response address(slave mode).
13	TIMEOUT	Timeout Flag This bit is set to 1 upon the occurrence of any timeout. It is cleared by software writing '0' to it, or cleared by hardware when I2C_CTRL1.EN = 0. 0: No timeout error; 1: A timeout error has occurred.
12	PECERR	PEC Error in reception This bit is cleared by software writing '0', or cleared by hardware when I2C_CTRL1.EN = 0.

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Bit Field	Name	Description
		0: No PEC error - Receiver returns ACK after receiving PEC (if I2C_CTRL1.ACKEN = 1); 1: PEC error - Receiver returns NACK after receiving PEC (regardless of whether I2C_CTRL1.ACKEN is set).
11	OVERRUN	Overrun/Underrun Writing ‘0’ to this bit by software can clear it, or it is cleared by hardware when I2C_CTRL1.EN=0. 0: No Overrun/Underrun; 1: Overrun/Underrun. Set by hardware in slave mode when I2C_CTRL1.NOEXTEND=1, and when receiving a new byte in receiving mode, if the data within DAT register has not been read yet, over-run occurs,the new received byte will be lost.When transferring a new byte in transfer mode, but there is not new data that has not been written in DAT register, under-run occurs which leads that the same byte will be send twice.
10	BUSERR	Bus error Writing ‘0’ to this bit by software can clear it, or it is cleared by hardware when I2C_CTRL1.EN=0. 0: No start or stop condition error; 1: Start or stop condition error.
9	ARLOST	Arbitration lost (master mode) Writing ‘0’ to this bit by software can clear it, or it is cleared by hardware when I2C_CTRL1.EN=0. 0: No arbitration lost; 1: Arbitration lost. When the interface loses control of the bus to another host, the hardware will set this bit to '1', and the I2C interface will automatically switch back to slave mode (I2C_STS2.MSMODE=0). *Note: In SMBUS mode, the arbitration of data in slave mode only occurs in the data stage or the acknowledge transfer interval (excluding the address acknowledge).*
8	ACKFAIL	Acknowledge failure Writing ‘0’ to this bit by software can clear it, or it is cleared by hardware when I2C_CTRL1.EN=0. 0: No acknowledge failed; 1: Acknowledge failed.
7	Reserved	Reserved, the reset value must be maintained.
6	ADDR10F	10-bit header sent (Master mode) After the software reads the STS1 register, the operation of writing to the CTRL1 register will clear this bit, or when I2C_CTRL1.EN=0, the hardware will clear this bit. 0: No ADD10F event; 1: Master has sent the first address byte. In 10-bit address mode, when the master device has sent the first byte, the hardware sets this bit to' 1'. *Note: After receiving a NACK, the I2C_STS1.ADDR10F bit is not set.*

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Bit Field	Name	Description
5	TXDATE	Data register empty (transmitters) Writing data to DAT register by software can clear this bit; Or after a start or stop condition occurs, automatically cleared by hardware when I2C_CTRL1.EN=0. 0: Data register is not empty; 1: Data register is empty. When sending data, this bit is set to' 1' when the data register is empty, and it is not set at the address sending stage. If a NACK is received, or the next byte to be sent is PEC(I2C_CTRL1.PEC=1), this bit will not be set. *Note: After the first data to be sent is written, or data is written when BSF is set, the TXDATE bit cannot be cleared, because the data register is still empty.*
4	RXDATNE	Data register not empty(receivers) This bit is cleared by software reading and writing to the data register, or cleared by hardware when I2C_CTRL1.EN=0. 0: Data register is empty; 1: Data register is not empty. During receiving data, this bit is set to' 1' when the data register is not empty, and it is not set at the address receiving stage. RXDATNE is not set when the ARLOST event occurs. *Note: When BSF is set, the RXDATNE bit cannot be cleared when reading data, because the data register is still full.*
3	STOPF	Stop detection (slave mode) After the software reads the STS1 register, the operation of writing to the CTRL1 register will clear this bit, or when I2C_CTRL1.EN=0, the hardware will clear this bit. 0: No stop condition is detected; 1: Stop condition is detected. After a ACK, the hardware sets this bit to' 1' when the slave device detects a stop condition on the bus. *Note: I2C_STS1.STOPF bit is not set after receiving NACK.*
2	BSF	Byte transfer finished After the software reads the STS1 register, reading or writing the data register will clear this bit; Or after sending a start or stop condition in sending mode, or when I2C_CTRL1.EN=0, this bit is cleared by hardware. 0: Byte transfer does not finish; 1: Byte transfer finished. When I2C_CTRL1.NOEXTEND =0, the hardware sets this bit to' 1' in the following cases: In receiving mode, when a new byte (including ACK pulse) is received and the data register has not been read (I2C_STS1.RXDATNE=1).In sending mode, when a new data is to be transmitted and the data register has not been written with the new data (I2C_STS1.TXDATE=1). *Note: After receiving a NACK, the BSF bit will not be set.* *If the next byte to be transferred is PEC (I2C _STS2.TRF is' 1' and I2C_CTRL1.PEC is'*

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Bit Field	Name	Description
		1'), the BSF bit will not be set.
1	ADDRF	Address sent (master mode) / matched (slave mode) After the STS1 register is read by software, reading the STS2 register will clear this bit, or when I2C_CTRL1.EN=0, it will be cleared by hardware. 0: Address mismatch or no address received(slave mode) or Address sending did not end(master mode); 1: Received addresses matched(slave mode) or Address sending ends(master mode) In master mode. In 7-bit address mode, this bit is set to' 1' after receiving the ACK of the address.In 10-bit address mode, this bit is set to' 1' after receiving the ACK of the second byte of the address. In slave mode: Hardware sets this bit to' 1' (when the corresponding setting is enabled) when the received slave address matches the content in the OADDR register, or a general call or SMBus device default address or SMBus host or SMBus alter is recognized. *Note: After receiving NACK, the I2C_STS1.ADDRF bit will not be set.*
0	STARTBF	Start bit (Master mode) After the STS1 register is read by software, writing to the data register will clear this bit, or when I2C_CTRL1.EN=0, the hardware will clear this bit. 0: Start condition was not sent; 1: Start condition has been sent. This bit is set to' 1' when the start condition is sent.

8.6.8 I2C Status Register 2 (I2C_STS2)

Address offset: 0x18

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PECVAL[7:0]								SMBH ADDR	SMBD ADDR	DUAL FLAG	GCALL ADDR	Reserved	TRF	MSMODE	BUSY
r								r	r	r	r		r	r	r

Bit Field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained.
15:8	PECVAL[7:0]	Packet error checking register Stores the internal PEC value When I2C_CTRL1.PECEN =1.
7	SMBHADDR	SMBus host header (Slave mode)

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Bit Field	Name	Description
		Hardware clears this bit when a stop condition or a repeated start condition is generated, or when I2C_CTRL1.EN=0. 0: SMBus host address was not received; 1: when I2C_CTRL1.SMBTYPE=1 and I2C_CTRL1.ARPEN=1, SMBus host address is received.
6	SMBDADDR	SMBus device default address (Slave mode) Hardware clears this bit when a stop condition or a repeated start condition is generated, or when I2C_CTRL1.EN=0. 0: The default address of SMBus device has not been received; 1: when I2C_CTRL1.ARPEN=1, the default address of SMBus device is received.
5	DUALFLAG	Dual flag(Slave mode) Hardware clears this bit when a stop condition or a repeated start condition is generated, or when I2C_CTRL1.EN=0. 0: Received address matches the content in OADDR1; 1: Received address matches the content in OADDR2.
4	GCALLADDR	General call address(Slave mode) Hardware clears this bit when a stop condition or a repeated start condition is generated, or when I2C_CTRL1.EN=0. 0: No general call address was received; 1: when I2C_CTRL1.GCEN=1, general call address was received.
3	Reserved	Reserved, the reset value must be maintained.
2	TRF	Transmitter/receiver After detecting the stop condition (I2C_STS1.STOPF=1), repeated start condition or bus arbitration loss (I2C_STS1.ARLOST=1), or when I2C_CTRL1.EN=0, the hardware clears it. 0: Data receiving mode; 1: Data transmission mode. At the end of the whole address transmission stage, this bit is set according to the R/W bit of the address byte.
1	MSMODE	Master/slave mode Hardware clears this bit when a stop condition is detected on the bus, arbitration is lost (I2C_STS1.ARLOST=1), or when I2C_CTRL1.EN=0. 0: In slave mode; 1: In master mode. When the interface is in the master mode (I2C_STS1.STARTBF=1), the hardware sets this bit;
0	BUSY	Bus busy Hardware clears this bit when a stop condition is detected. 0: No data communication on the bus; 1: Data communication on the bus. When detecting that SDA or SCL is low level, the hardware sets this bit to' 1'; *Note:This bit indicates the bus communication currently in progress, and this information is still updated when the interface is disabled (I2C_CTRL1.EN=0).*

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8.6.9 I2C Clock Control Register (I2C_CLKCTRL)

Address offset: 0x1C

Reset value: 0x0000 0000

Note:

The CLKCTRL register can only be configured when the I2C is disabled (I2C_CTRL1.EN = 0).

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DUTY	FSMODE	Reserved		CLKCTRL[11:0]											
rw	rw			rw											

Bit Field	Name	Description
15	DUTY	Duty cycle in fast mode 0: Tlow/Thigh = 2; 1: Tlow/Thigh = 16/9.
14	FSMODE	I2C master mode selection 0: I2C in standard mode(duty cycle defaults to 1/1); 1: I2C in fast mode(duty cycle can be configured).
13:12	Reserved	Reserved, the reset value must be maintained.
11:0	CLKCTRL[11:0]	Clock control register in Fast/Standard mode (Master mode) This division factor is used to set the SCL clock in the master mode. ■ If duty cycle = Tlow/Thigh = 1/1: CLKCTRL = f_{PCLK1}(Hz)/100000/2 Tlow = CLKCTRL ×T_{PCLK1} Thigh = CLKCTRL ×T_{PCLK1} ■ If duty cycle = Tlow/Thigh = 2/1: CLKCTRL = f_{PCLK1}(Hz)/100000/3 Tlow = 2 ×CLKCTRL ×TPCLK1 Thigh = CLKCTRL ×T_{PCLK1} ■ If duty cycle = Tlow/Thigh = 16/9: CLKCTRL = f_{PCLK1}(Hz)/100000/25 Tlow = 16 ×CLKCTRL ×T_{PCLK1} Thigh = 9 ×CLKCTRL ×T_{PCLK1} For example, if f_{PCLK1}(Hz) = 8MHz, duty cycle = 1/1, CLKCTRL = 8000000/100000/2 = 0x28. *Note: 1. The minimum setting value is 0x04 in standard mode and 0x01 in fast mode;* *2. T_{high}= $T_{r(SCL)}$+$T_{w(SCLH)}$. See the definitions of these parameters in the data sheet for details.* *3. T_{low}= $T_{f(SCL)}$+$T_{w(SCLL)}$, see the definitions of these parameters in the data sheet for details;* *4. These delays have no filters;*

8.6.10 I2C Rise Time Register (I2C_TMRISE)

Address offset: 0x20

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Reset value: 0x0000 0002

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved										TMRISE[5:0]					
										rw					

Bit Field	Name	Description
31:8	Reserved	Reserved, the reset value must be maintained.
7:0	TMRISE[5:0]	Maximum Rise Time in Fast/Standard Mode (Master Mode) These bits must be set to the maximum SCL rise time specified in the I2C bus specification, with an increment of 1. For example, the maximum allowed SCL rise time in Standard Mode is 1000ns. If the value in I2C_CTRL2.CLKFREQ[5:0] is 0x08(8MHZ)and T_{PCLK1}=125ns, then 09h must be written to TMRISE[5:0] (1000ns/128 ns + 1). If the result is not an integer, write the integer part to TMRISE[5:0] to ensure the tHIGH parameter.

8.6.11 I2C Digital Filter Control Register (I2C_GFLTRCTRL)

Address offset: 0x28

Reset value: 0x0000

Note: The GFLTRCTRL register can only be configured when the I2C is disabled (I2C_CTRL1.EN = 0).

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SCLAFENN	Reserved	SCLAFW[1:0]		SDAAFENN	Reserved	SDAAFW[1:0]		SCLDFW[3:0]				SDADFW[3:0]			
rw		rw		rw		rw		rw				rw			

Bit Field	Name	Description
15	SCLAFENN	SCL Analog Filter Enable. 0: Enable; 1: Disable.
14	Reserved	Reserved, the reset value must be maintained.
13:12	SCLAFW[1:0]	SCL Analog Filter Width Selection. 00: 5ns; 01: 15ns; 10: 25ns; 11: 35ns.
11	SDAAFENN	SDA Analog Filter. 0: Enable; 1: Disable.
10	Reserved	Reserved, the reset value must be maintained.

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Bit Field	Name	Description
9:8	SDAAFW[1:0]	SDA Analog Filter Width Selection. 00: 5ns; 01: 15ns; 10: 25ns; 11: 35ns.
7:4	SCLDFW[3:0]	SCL Digital Filter Width Selection. 0000: Disable digital filter. Other values: Filtering width = SCLDFW $\times T_{PCLK}$
3:0	SDADFW[3:0]	SDA Digital Filter Width Selection: 0000: Disable digital filter. Other values: Filtering width = SDADFW $\times T_{PCLK}$

9 Universal Asynchronous Receiver Transmitter (UART)

9.1 Introduction

UART is a full-duplex universal synchronous/asynchronous serial transceiver module. This interface is a highly flexible serial communication device that can perform full-duplex data exchange with external devices.

The UART has programmable transmit and receive baud rates and can communicate continuously using DMA. It also supports multiprocessor communication, LIN mode, synchronous mode, single-wire half-duplex communication, smartcard asynchronous protocol, IrDA SIR ENDEC function.

9.2 Main Features

- Support Full duplex communication
- Support Single-wire half-deplex commnication
- Baud rate programmable, up to 4Mbit/s
- Programmable data word length (8 or 9 bits)
- Configurable stop bit, supporting 1 or 2 stop bits
- Support hardware generation of parity bit and check parity bit
- Supports TX/RX swap function
- Supports DMA transmission and reception
- Supports RS-485
- UART3 supports low-power wake-up
- Supports multiprocessor communication: enters silent mode if the address does not match, and can be woken up via idle bus detection or address identification

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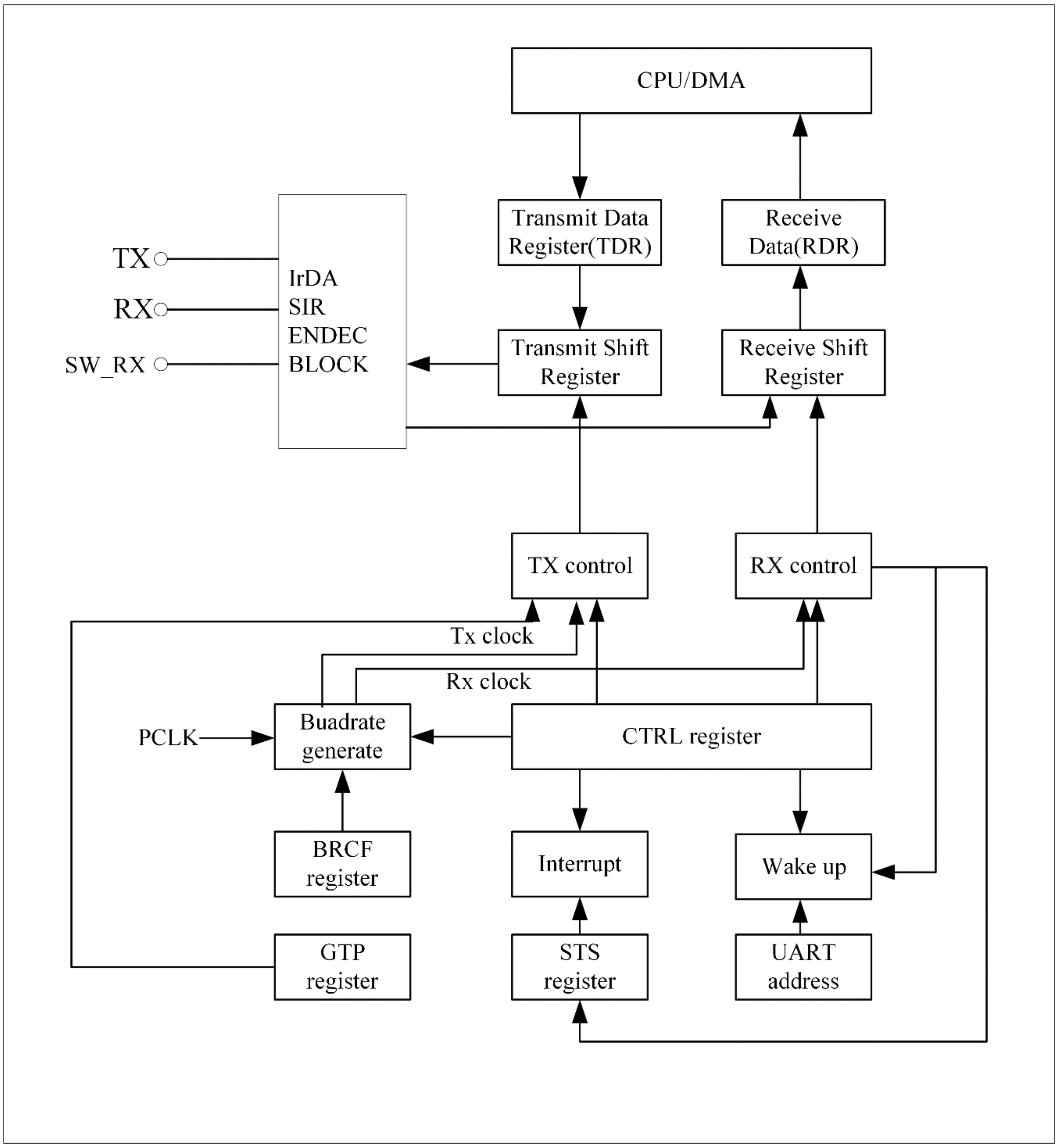
- Supports serial infrared protocol (IrDA SIR) encoding and decoding, providing normal and low-power operation modes
- Supports LIN mode
- Supports multiple error detection types: data overrun error, frame error, noise error, parity error
- Supports multiple interrupt requests: transmit data register empty, transmission complete, data received, data overrun, bus idle, parity error, LIN mode break frame detection, as well as noise flag/overrun error/frame error and reception timeout in multi-buffer communication

9.3 Functional Block Diagram

Figure 9-1 UART Block Diagram



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9.4 Function Description

As shown in the Figure 9-1, the bidirectional communications of any UART need to use the RX and TX pins of the external connection. Among them, TX is the output pin for serial data transmission. When the transmitter is active and not sending data, the TX pin is pulled high. When the transmitter is inactive, the TX pin reverts to the I/O port configuration. RX is an input pin for serial data reception, data is received by the oversampling technique.

The data packets of serial communication are transmitted from the sending device to the RX interface of the receiving device through its own TX interface, and the bus is in an idle state before transmitting or receiving. Frame format is: 1 start bit + 8 or 9 data bits (least significant bit first) + 1 parity bit (optional) + 0.5,1,1.5 or 2 stop bit.

Use the fractional baud rate generator to configure transmit and receive baud rates.

9.4.1 UART Frame Format

Start bit: 1 bit, active low

Data bits: Configurable via UART_CTRL1.WL as 8 or 9 bits, with the LSB first.

Stop bit: Active high.

Idle frame: A complete data frame consisting entirely of '1's, including the start bit. followed by the start bit of a data frame containing the data.

Break frame: A break frame is a complete data frame consisting of '0's, including the stop bit. at the end of the break frame, the transmitter inserts 1 or 2 more stop bits ('1') to acknowledge the start bit.

Figure 9-2 Word Length = 8 Setting

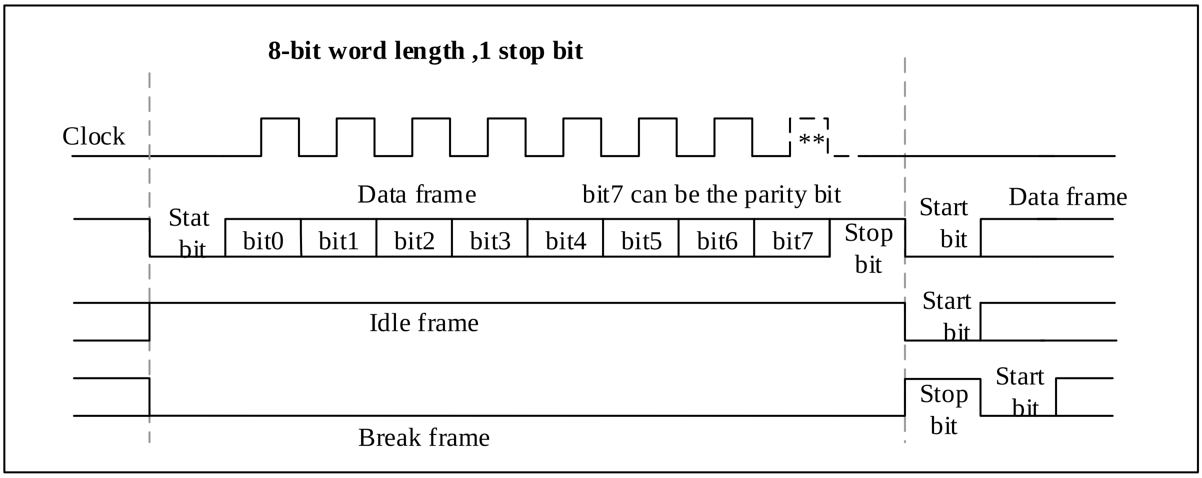

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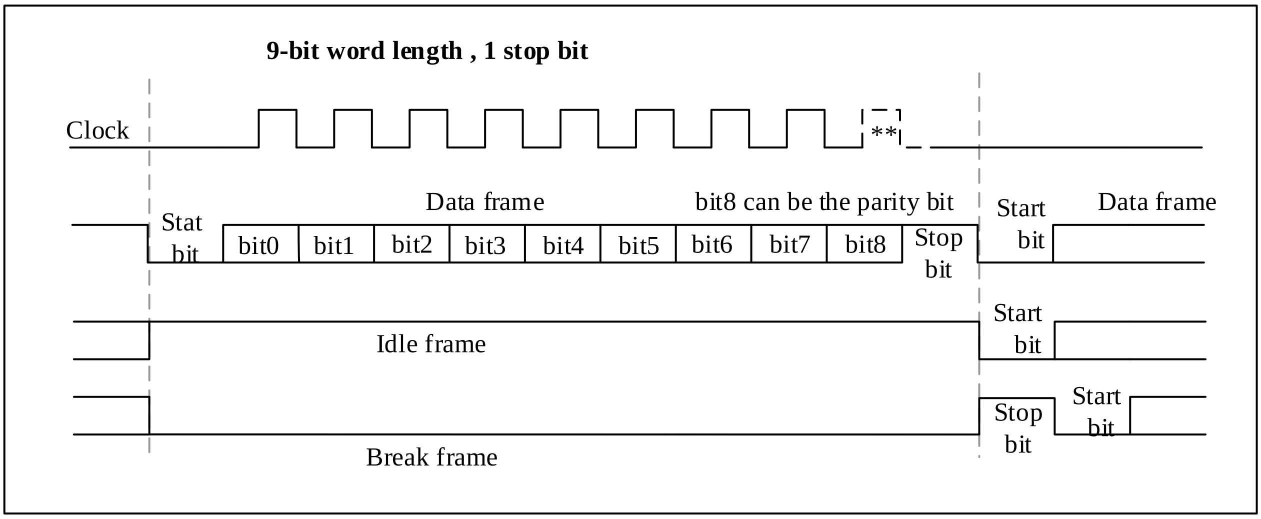
Figure 9-3 Word Length = 9 Setting



9.4.2 Transmitter

After the transmitter is enabled, the data in the transmit shift register is sent out through the TX pin.

9.4.2.1 Idle frame

Setting UART_CTRL1.TXEN will cause the UART to transmit an idle frame before the first data frame.

9.4.2.2 Character transmission

Idle frames are followed by characters sent. Each character is preceded by a low start bit. The transmitter sends 8-bit or 9-bit data according to the configuration of the data bit length, with the least significant bit first. If UART_CTRL1.TXEN is reset during a data transfer, it will cause the baud rate counter to stop counting and the data being transferred will be corrupted.

9.4.2.3 Stop bit

The characters are followed by stop bits, the number of which can be configured by setting UART_CTRL2. STPB[1:0].

Table 9-1 Stop Bit Configuration

UART_CTRL2.STPB[1:0]	Stop Bit Length (Bits)	Functional Description
00	1	Default
01	0.5	
10	2	General UART mode, single-wire mode and modem mode.
11	1.5	

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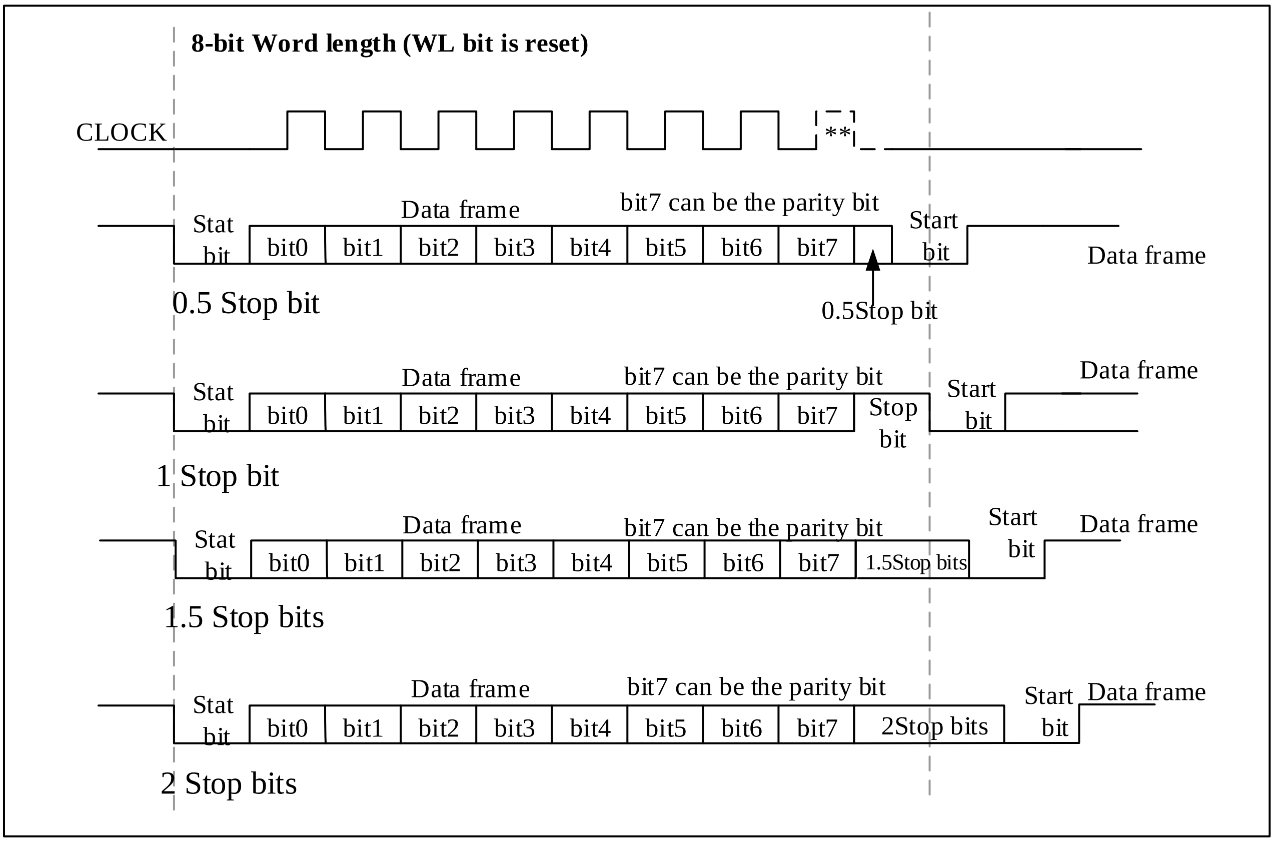
Figure 9-4 Configuration Stop Bit



9.4.2.4 Break frame

Use UART_CTRL1.SDBRK to send the break character. When there is 8-bit data, the break frame consists of 10 bits of low level, followed by a stop bit; when there is 9-bit data, the break frame consists of 11 bits of low level, followed by a stop bit.

After the break frame is sent, UART_CTRL1.SDBRK is cleared by hardware, and the stop bit of the break frame is automatically sent. Therefore, to send a second break frame, UART_CTRL1.SDBRK should be set after the stop bit of the previous break frame has been sent.

If software resets the UART_CTRL1.SDBRK bit before starting to send the break frame, the break frame will not be sent.

9.4.2.5 Sending process

1. Enable UART_CTRL1.UEN to activate UART;

2. Configure the transmitter's baud rate, data bit length, parity bit (optional), the number of stop bits or DMA configuration;

3. Activate the transmitter (UART_CTRL1.TXEN);

4. Send each data to be sent to the UART_DAT register through the CPU or DMA, and the write operation to the UART_DAT register will clear UART_STS.TXDE;

5. After writing the last data word in the UART_DAT register, wait for UART_STS.TXC =1, which indicates the end of the transmission of the last data frame.

Note: There is a delay of 0 to 1 baud rate cycle from writing data to UART_DAT to the data appearing on the UART_TX

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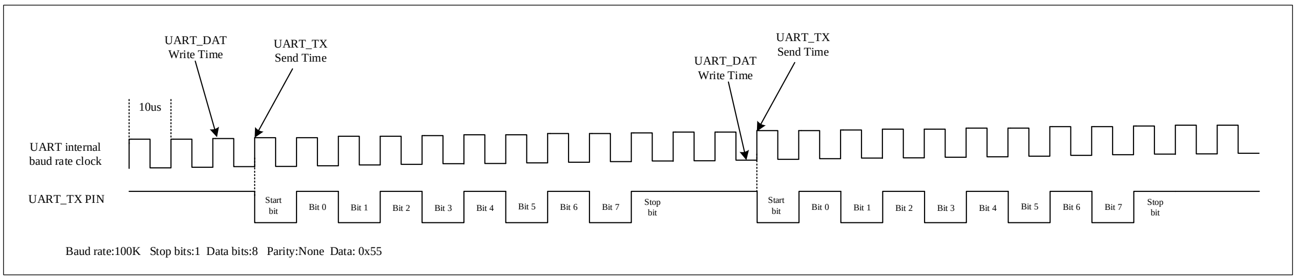
pin. For example, as shown in the figure below with a baud rate of 100 Kbps, if data is written to UART_DAT at any time within one baud rate cycle, the data will be transmitted to the UART_TX pin at the start of the next baud rate cycle.

Figure 9-5 Transmission Time Difference



9.4.2.6 Single byte communication

A write to the UART_DAT register clears the UART_STS.TXDE bit.

The UART_STS.TXDE bit is set by hardware when the data in the TDR register is transferred to the transmit shift register (indicating that data is being transmitted). An interrupt will be generated if UART_CTRL1.TXDEIEN is set. At this point, the next data can be sent to the UART_DAT register because the TDR register has been cleared and will not overwrite the previous data

Write operation to UART_DAT register:

- When the transmit shift register is not sending data and is in an idle state, the data is directly put into the shift register for transmission, and the UART_STS.TXDE bit is set by hardware;
- When the transmit shift register is sending data, the data is stored in the TDR register, and after the current transmission is completed, the data is put into the shift register.

When a frame containing data is sent and UART_STS.TXDE=1, the UART_STS.TXC bit is set to '1' by hardware. An interrupt is generated if UART_CTRL1.TXCIEN is '1'. UART_STS.TXC bit is cleared by a software sequence (read UART_STS register first, then write UART_DAT register).

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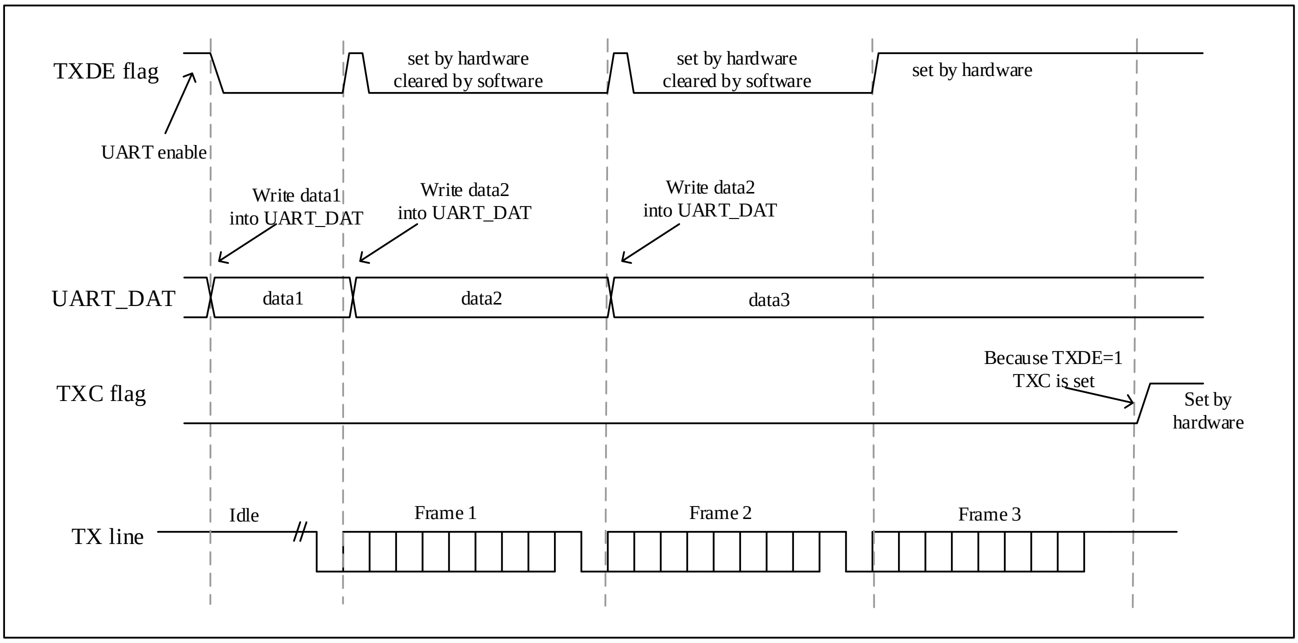
Figure 9-6 TXC/TXDE Changes During Transmission



9.4.3 Receiver

9.4.3.1 Start bit detection

When the received sampling sequence is: 1 1 1 0 X 0 X 0 X 0 0 0 0, it is considered that a start bit is detected.

The samples at the 3rd, 5th, and 7th bits, and the samples at the 8th, 9th, and 10th bits are all '0' (that is, 6 '0'), then confirm the receipt of the start bit, the UART_STS.RXDNE flag bit is set, and if UART_CTRL1.RXDNEIEN=1, an interruption occurs and will not Set the NEF noise flag.

If there are two '0' samples at the 3rd, 5th, 7th bits, and at the same time, there are two '0' samples at the 8th, 9th, 10th bits, a start bit is also confirmed to have been received, but the NE noise flag will be set.

If there are three '0' samples at the 3rd, 5th, 7th bits, and at the same time, there are two '0' samples at the 8th, 9th, 10th bits, a start bit is also confirmed to have been received, and the NE noise flag will be set.

If there are two '0' samples at the 3rd, 5th, 7th bits, and at the same time, there are three '0' samples at the 8th, 9th, 10th bits, a start bit is also confirmed to have been received, and the NE noise flag will be set

If the sampling values in the 3rd, 5th, 7th, 8th, 9th and 10th bits cannot meet the above four requirements, the UART receiver thinks that it has not received the correct start bit, and will exit the start bit detection and return to idle state and wait for falling edge.

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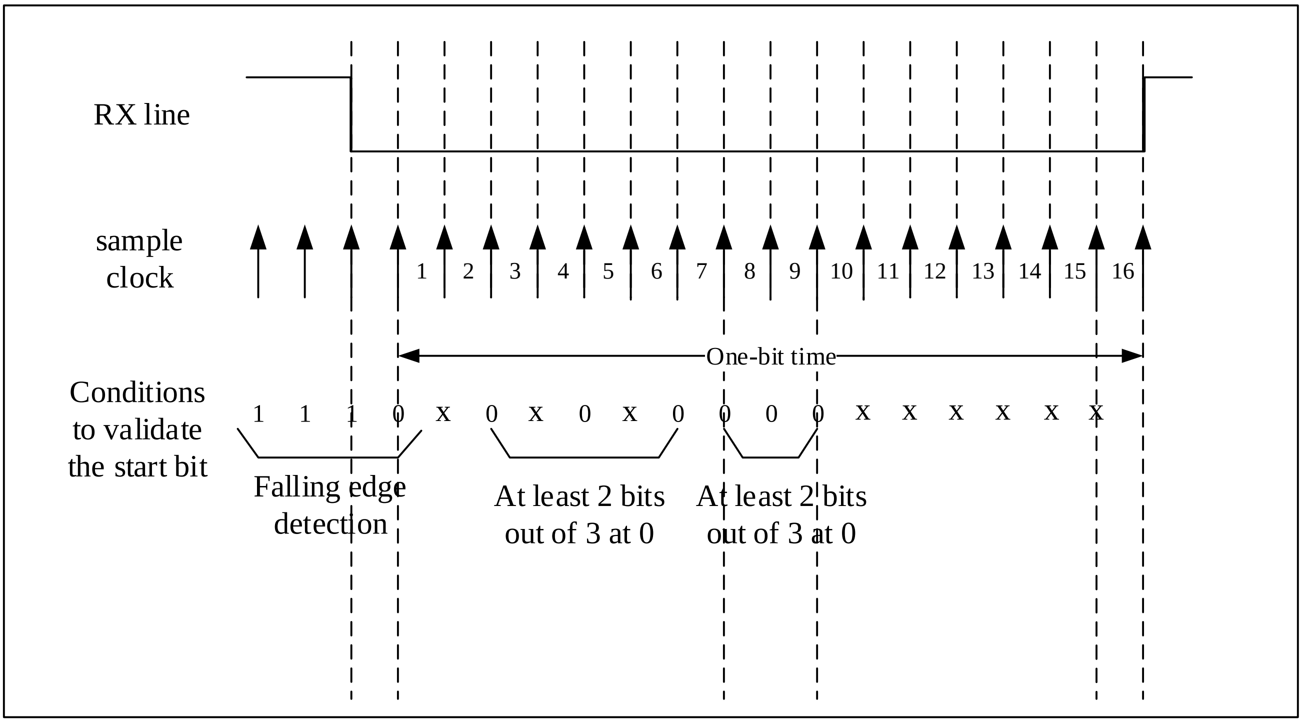
Figure 9-7 Start Bit Detection



9.4.3.2 Stop bit description

1. The number of data stop bits can be configured by the UART_CTRL2.STPB[1:0]. In normal mode, 1 or 2 stop bits can be selected.

2. 0.5 stop bits (receive in smartcard mode): 0.5 stop bits are not sampled. Therefore, if 0.5 stop bits is selected, framing errors and broken frames cannot be detected.

3. 1 stop bit: sampling for 1 stop bit is done on the 8th, 9th and 10th samples.

   a) stop bits: The 1.5 stop bits are sampled at points 16, 17 and 18. The 1.5 stop bits can be divided into two parts: one is 0.5 clock cycles, during which nothing happens. This is followed by the stop bit of 1 clock cycle, which is sampled at the midpoint of this period of time

4. 2 stop bits: the sampling of the 2 stop bits is completed at the 8th, 9th and 10th sampling points of the first stop position. If a frame error is detected during the first stop bit, the frame error flag is set. The second stop bit does not detect framing error. The UART_STS.RXNE flag will be set at the end of the first stop bit.

9.4.3.3 Receiver process

1. Enable UART_CTRL1.UEN to activate UART;

2. Configure the receiver's baud rate, data bit length, parity bit (optional), stop bit number or DMA configuration;

3. Activate the receiver (UART_CTRL1.RXEN) and start looking for the start bit;

4. The receiver receives 8-bit or 9-bit data according to the configuration of the data bit length, and the least significant bit of the data is first shifted from the RX pin into the receive shift register;

5. When the data of the received shift register is moved to the RDR register, UART_STS.RXDNE is set, and the data

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can be read out. If UART_CTRL1.RXNEIEN is 1, an interrupt will be generated;

6. When an overflow error, noise error, or frame error is detected in the received frame, the corresponding error flag status bit will be set. If UART_CTRL1.RXEN is reset during data transmission, the data being received will be lost;

7. UART_STS.RXDNE is set after receiving data, and a read operation of UART_DAT can clear this bit.

- During multi-buffer communication mode, by performing DMA read operations on the data register, the UART RXDNE reset to zero.
- During single-buffer communication mode, by performing software read operations on the data register, the UART RXDNE reset to zero.

9.4.3.4 Idle frame detection

When an idle frame is detected, UART.STS.IDLEF is set to 1. If UARD_CTRL1.IDLEIEN is set to 1 at this time, an interrupt will be generated. UART_STS.IDLEF bit is cleared by a software sequence (read UART_STS register first, then read UART_DAT register).

9.4.3.5 Break frame detection

The frame error flag(UART_STS.FEF) is set by hardware when the receiver detects a break frame. It can be cleared by a software sequence (read UART_STS register first, then read UART_DAT register).

9.4.3.6 Framing error

A framing error occurs when a stop bit is not received and recognized at the expected time. At this time, the frame error flag UART_STS.FEF will be set by hardware, and the invalid data will be transferred from the shift register to the UART_DAT register. During single-byte communication, no interrupt framing error will be generated because it occurs with UART_STS.RXDNE and the hardware will generate an interrupt when the UART_STS.RXDNE flag is set. In multi-buffer communication mode, an interrupt will be generated if the UART_CTRL3.ERRIEN bit is set.

9.4.3.7 Overrun error

When UART_STS.RXDNE is still '1', and the data currently received in the shift register needs to be transferred to the RDR register, an overflow error will be detected, and the hardware will set UART_STS.OREF. When this bit is set, the value in the RDR register is not lost, but the data in the shift register is overwritten. It is cleared by a software sequence (read UART_STS register first, then write UART_DAT register).

When an overflow error occurs, if UART_SS RXDNEIEN has been set to 1, which will generate a receive interrupt. If the UART_CTRL3.ERRIEN bit is set, an interrupt will be generated when the UART_STS.OREF flag is set in multi-buffer communication mode.

9.4.3.8 Noise error

UART_STS.NEF is set by hardware when noise is detected on a received frame. It is cleared by software sequence (read UART_STS register first, then write UART_DAT register). During single-byte communication, no noise interrupt generated because it occurs with UART_STS.RXDNE and the hardware will generate an interrupt when the UART_STS.RXDNE flag is set. In multi-buffer communication mode, an interrupt is generated when the UART_STS.NEF flag is set if the UART_CTRL3.ERRIEN bit is set.

Table 9-2 Data Sampling for Noise Detection

Sample Value	NE Status	Received Bits	Data Validity
000	0	0	Effective

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001	1	0	Be invalid
010	1	0	Be invalid
011	1	1	Be invalid
100	1	0	Be invalid
101	1	1	Be invalid
110	1	1	Be invalid
111	0	1	Effective

9.4.4 Fractional Baud Rate Calculation

The baud rate of the UART can be configured in the UART_BRCF register. This register defines the integer and fractional parts of the baud rate divider. The baud rate of the transmitter and receiver should be configured to the same value. Be careful not to change the value of the UART_BRCF register during communication, because the baud rate counter will be replaced by the new value of the baud rate register

$$\text{TX / RX baud rate} = f_{\text{PCLK}} / (16 * \text{UARTDIV})$$

where f_{PCLK} is the clock provided to the peripheral

- PCLK1 is used for UART1/UART2/UART3, up to 64MHz.

UARTDIV is an unsigned frequency division coefficient.

9.4.4.1 UARTDIV and UART_BRCF register configuration

Oversampling Set to 16:

Example 1:

If UARTDIV = 27.75, then:

DIV_Decimal = 16 × 0.75 = 12 = 0x0C

DIV_Integer = 27 = 0x1B

So, UART_BRCF = 0x1BC

Example 2:

If UARTDIV = 20.98, then:

DIV_Decimal = 16 × 0.98 = 15.68

Round to the nearest integer: DIV_Decimal = 16 = 0x10, which exceeds the configurable range. Thus, a carry must be added to the integer part.

Therefore, DIV_Integer = 20 + 1 = 21 = 0x15

DIV_Decimal = 0x0

So, UART_BRCF = 0x150

Example 3:

If UART_BRCF = 0x19B:

DIV_Integer = 0x19 = 25

DIV_Decimal = 0x0B = 11

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UARTDIV = 25 + 11/16 = 25.6875

Oversampling Set to 8:

Example 1:

If UARTDIV = 27.75, then:

DIV_Decimal = 8 × 0.75 = 6 = 0x06

DIV_Integer = 27 = 0x1B

Therefore, UART_BRCF = 0x1B6

Example 2:

If UARTDIV = 20.98, then:

DIV_Decimal = 8 × 0.98 = 7.84

Round to the nearest integer: DIV_Decimal = 8 = 0x08, which exceeds the configurable range. Thus, a carry must be added to the integer part.

Therefore, DIV_Integer = 20 + 1 = 21 = 0x15

DIV_Decimal = 0x0

So, UART_BRCF = 0x150

Example 3:

If UART_BRCF = 0x196:

DIV_Integer = 0x19 = 25

DIV_Decimal = 0x06 = 6

UARTDIV = 25 + 6/8 = 25.75

Table 9-3 Error Calculation When Setting Baud Rate

using 16× oversampling									
Baud Rate		**f_{PCLK}=32MHz**				**f_{PCLK}=64MHz**			
Serial Number	Kbps	Reality	Oversampling	Set value in register	Error(%)	Reality	Oversampling	Set value in register	Error(%)
1	2.4	2.400	16	833.3125	0%	2.400	16	1666.6875	0%
2	9.6	9.601	16	208.3215	0.01%	9.600	16	416.6875	0%
3	19.2	19.196	16	104.1875	0.02%	19.202	16	208.3125	0.01%
4	57.6	57.554	16	34.750	0.08%	57.606	16	69.4375	0.01%
5	115.2	115.108	16	17.375	0.08%	115.108	16	34.75	0.08%

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6	230.4	230.216	16	8.6875	0.08%	230.216	16	17.375	0.08%
7	460.8	463.768	16	4.3125	0.64%	460.432	16	8.6875	0.08%
8	921.6	914.286	16	2.1875	0.79%	927.536	16	4.3125	0.64%
9	2250	impossible	16	impossible	impossible	2285.714	16	1.75	1.59%
10	3000	impossible	16	impossible	impossible	3047.619	16	1.3125	1.59%
11	4000	impossible	16	impossible	impossible	4000	16	1	0%
using 8× oversampling									
Baud Rate		**f_{PCLK}=32MHz**				**f_{PCLK}=64MHz**			
Serial Number	Kbps	Reality	Oversampling	Set value in register	Error(%)	Reality	Oversampling	Set value in register	Error(%)
1	2.4	2.400	8	1666.6875	0%	2.400	8	3333.3125	0%
2	9.6	9.600	8	416.6875	0%	9.600	8	833.3125	0%
3	19.2	19.202	8	208.3125	0.01%	19.199	8	416.6875	0%
4	57.6	57.606	8	69.4375	0.01%	57.606	8	138.875	0.01%
5	115.2	115.108	8	34.75	0.08%	115.212	8	69.4375	0.01%
6	230.4	230.216	8	17.375	0.08%	230.216	8	34.75	0.08%
7	460.8	460.432	8	8.6875	0.08%	460.432	8	17.375	0.08%
8	921.6	927.536	8	4.3125	0.64%	920.863	8	8.6875	0.08%
9	2250	2285.714	8	1.75	1.59%	2245.614	8	3.5625	0.19%
10	3000	3047.619	8	1.3125	1.59%	2976.744	8	2.6875	0.78%
11	4000	4000	8	1	0%	4000	8	2	0%

Notes: The lower the clock frequency of the CPU, the lower the error for a particular baud rate.

9.4.5 UART Receiver's Tolerance Clock Deviation

Variations due to transmitter errors (including transmitter side oscillator variations), receiver side baud rate rounding errors, receiver side oscillator variations, variations due to transmission lines (usually due to The inconsistency between the low-to-high transition timing of the transceiver and the high-to-low transition timing of the transceiver), these factors will affect the overall clock system variation. Only when the sum of the above four changes is less than the tolerance of the UART

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receiver, the UART asynchronous receiver can work normally.

When receiving data normally, the tolerance of UART receiver is the maximum tolerable variation, depending on the selection of data bit length and whether to use fractional baud rate division coefficient.

Table 9-4 When DIV_Decimal = 0, Tolerance of UART Receiver

WL Bit	NEF Is An Error	NEF Is Don't Care
0	3.75%	4.375%
1	3.41%	3.97%

Table 9-5 When DIV_Decimal != 0, Tolerance of UART Receiver

WL Bit	NEF Is An Error	NEF Is Don't Care
0	3.33%	4.0%
1	3.03%	3.63%

9.4.6 Parity Control

Parity can be enabled by configuring the UART_CTRL1.PCEN bit.

When the parity bit is enabled for transmission, a parity bit is generated, parity check is performed on reception.

Table 9-6 Frame Format

WL Bit	PCEN Bit	UART Frame
0	0	| Start bit | 8-bit data | Stop bit |
0	1	| Start bit | 7 bits of data | Parity bit | Stop bit |
1	0	| Start bit | 9-bit data | Stop bit |
1	1	| start bit | 8-bit data | parity bit | stop bit |

Even parity

Configure UART_CTRL1.PSEL to 0, and even parity can be selected.

Make the number of '1' in the transmitted data (including parity bit) be an even number. For example: if Data=11000101, there are 4 '1's, then the parity bit will be '0' (4 '1' in total). The receiver confirms the number of '1's in the data If it is an even number, the check is passed, indicating that no errors occurred during the transmission process. If it is not even, it means that an error has occurred, the UART_STS.PEF flag is set to '1', and if UART_CTRL1.PEIEN is enabled, an interrupt is generated.

Odd parity

Configure UART_CTRL1.PSEL to 1, you can choose odd parity.

Make the number of '1' in the transmitted data (including parity bit) be an odd number. For example: if Data=11000101, there are 4 '1's, then the parity bit will be '1' (5 '1' in total). The receiver confirms the number of '1's in the data If it is an odd number, the check is passed, indicating that no errors occurred during the transmission process. If it is not an odd number, it means that an error has occurred, the UART_STS.PEF flag is set to '1', and if UART_CTRL1.PEIEN is enabled,

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an interrupt is generated.

9.4.7 DMA Communication

The UART supports the DMA mode using multi-buffer configuration, which can realize high-speed data communication.

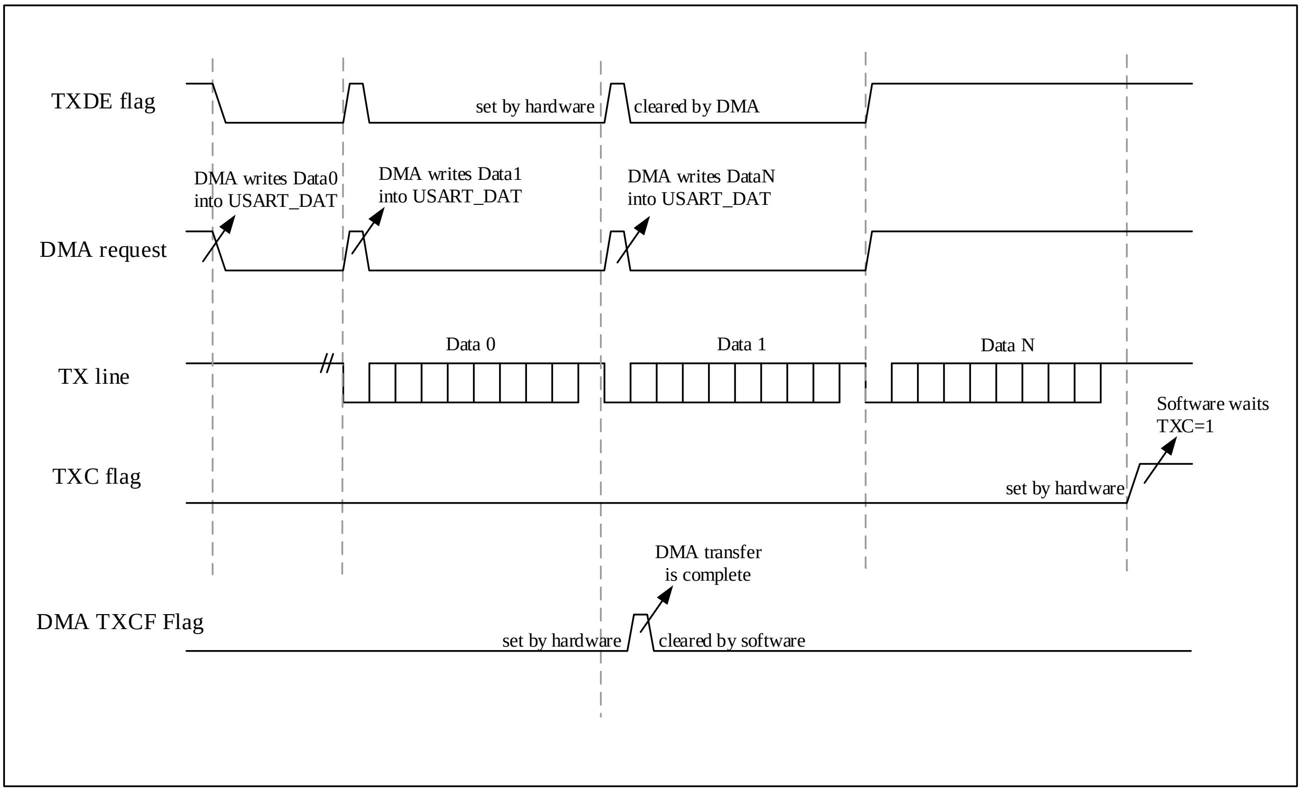
9.4.7.1 DMA transmission

Set UART_CTRL3.DMATXEN to enable DMA mode when transmitting. When the UART's transmit shift register is empty (UART_STS.TXDE=1), the DMA will transfer the data from the SRAM to the UART_DAT register of the UART.

When using DMA transmission, the process of configuring the DMA channel is as follows:

1. Set the address of the data memory. When a data transfer request occurs, the transferred data will be read from this address.
2. Set the address of the UART_DAT register. When a data transfer request occurs, this address will be the destination address of the data transfer.
3. Set the amount of data to transfer.
4. Set the priority of the channel, set whether to use the cyclic mode, the incremental mode of peripherals and memory, the data width of peripherals and memory, the interrupt generated by half of the transfer or the interrupt when the transfer is completed.
5. Start the current DMA channel.
6. After the data transfer is completed, the transfer complete flag (DMA_INTSTS.TXCFx) is set to 1.

Figure 9-8 Transmission Using DMA



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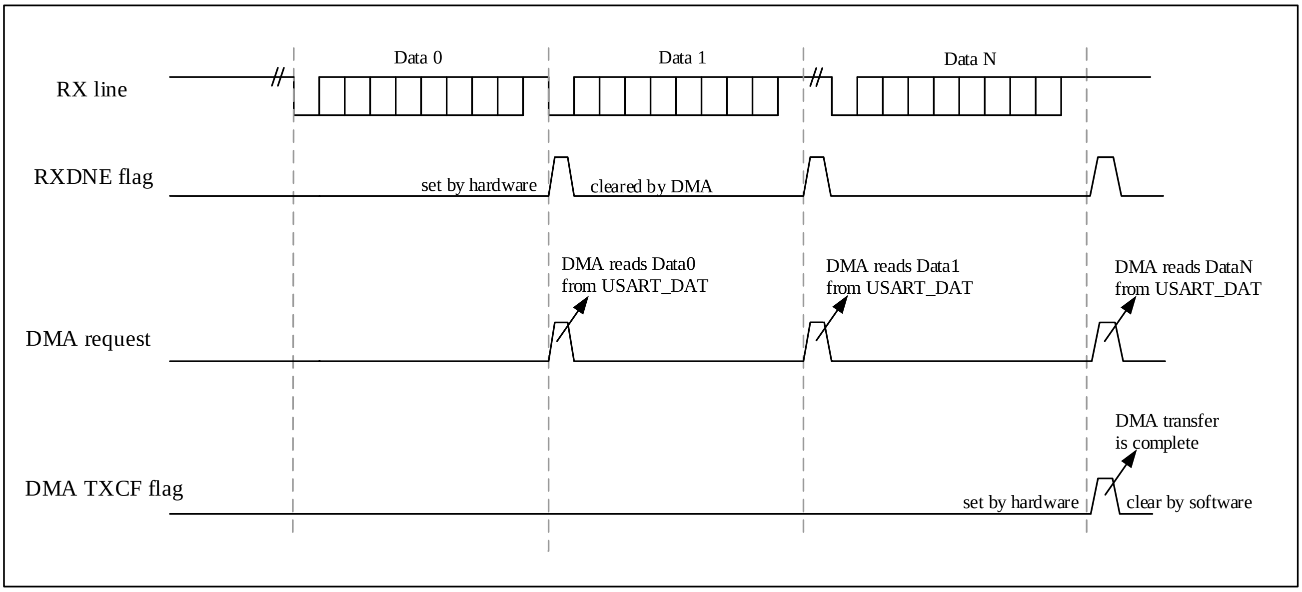
9.4.7.2 DMA reception

Set UART_CTRL3.DMARXEN to enable DMA mode when receiving. When a byte is received (UART_STS.RXDNE=1), the DMA will transfer the data from the UART_DAT register of the UART to the SRAM.

When using DMA reception, the process of configuring the DMA channel is as follows:

1. Set the address of the UART_DAT register. When a data transfer request occurs, this address will be the source address of the data transfer
2. Set the address of the data memory. When a data transfer request occurs, the transferred data will be written to this address
3. Set the amount of data to transfer.
4. Set the priority of the channel, set whether to use the cyclic mode, the incremental mode of peripherals and memory, the data width of peripherals and memory, the interrupt generated by half of the transfer or the interrupt when the transfer is completed.
5. Start the current DMA channel.

Figure 9-9 Reception Using DMA



In multi-buffer communication mode, the error flag will be set when there is a frame error, overrun error or noise error. An interrupt will be generated if the error interrupt is enabled (UART_CTRL3.ERRIEN=1).

9.4.8 Multiprocessor Communication

UART allows multiprocessor communication. When multiple processors communicate through UART, it is necessary to determine who is the master device, and the remaining processors are all slave devices. The TX output of the master device is directly connected to the RX port of all slave device. The TX outputs of the slaves are logically AND together and connected to the RX inputs of the master.

When multi-processor communication is performed, the slave devices are all in mute mode, and the host uses a specific method to wake up a slave device to be communicated when needed, so that the slave device is in an active state and

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transmits data with the master device.

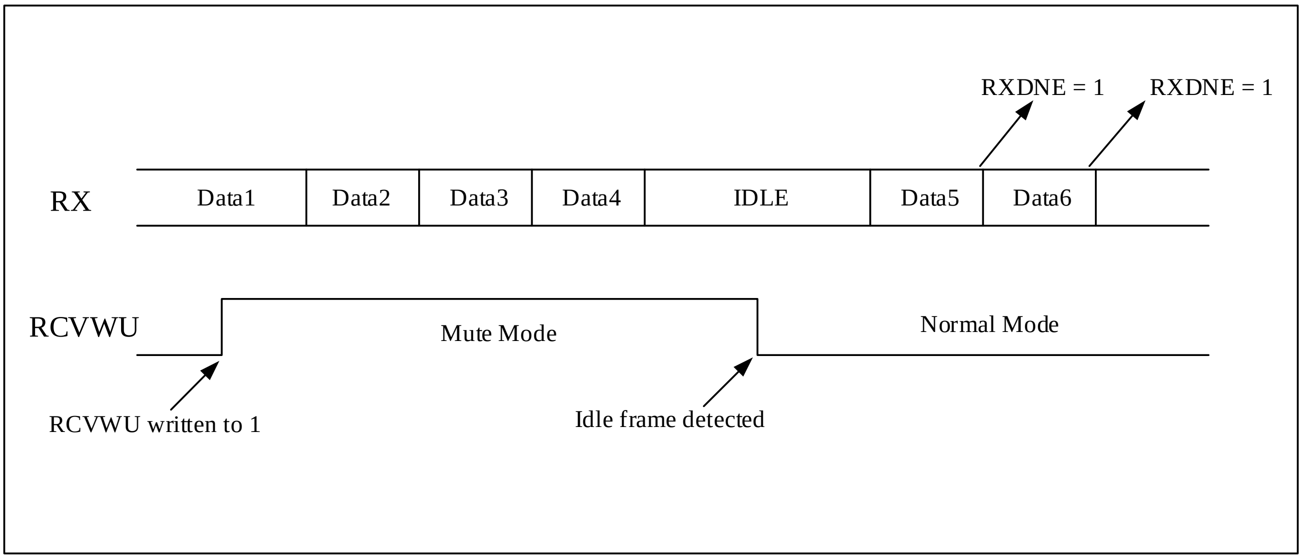
The UART can wake up from mute mode by idle bus line detection or address mark detection.

9.4.8.1 Idle bus line detection

The idle bus line detection configuration process is as follows:

1. Configure the UART_CTRL1.WUM bit to 0, and the UART performs idle bus line detection.
2. When UART_CTRL1.RCVWU is set (which can be automatically controlled by hardware or written by software under certain conditions), UART enters mute mode. In mute mode, none of the receive status bits are set, and all receive interrupts are disabled.
3. As shown in the Figure 9-10, when an idle frame is detected, UART is woken up, and then UART_CTRL1.RCVWU is cleared by hardware. At this time, UART_STS.IDLEF is not set.

Figure 9-10 Mute Mode Using Idle Line Detection



9.4.8.2 Address mark detection

By configuring the UART_CTRL1.WUM bit to 1, the UART performs address mark detection. The address of the receiver is programmable through the UART_CTRL2.ADDR[3:0] bits. If the MSB is 1, the byte is considered as an address, otherwise it is considered as data

In this mode, the UART can enter mute mode by:

1. When the receiver does not contain data, UART_CTRL1.RCVWU can be written to 1 by software, and UART enters mute mode

Note: When the receive buffer contains no data (RXNE=0 in UART_SR), the UART_CTRL1.RCVWU bit can be written to 0 or 1. Otherwise, the write operation is ignored.

2. When the received address does not match the address of the UART_CTRL2.ADDR[3:0] bits, UART_CTRL1.RCVWU is written to 1 by hardware.

In silent mode, none of the receive status bits are set and all receive interrupts are disabled.

When the address received by the receiver matches the preset address identifier, the UART is woken up and

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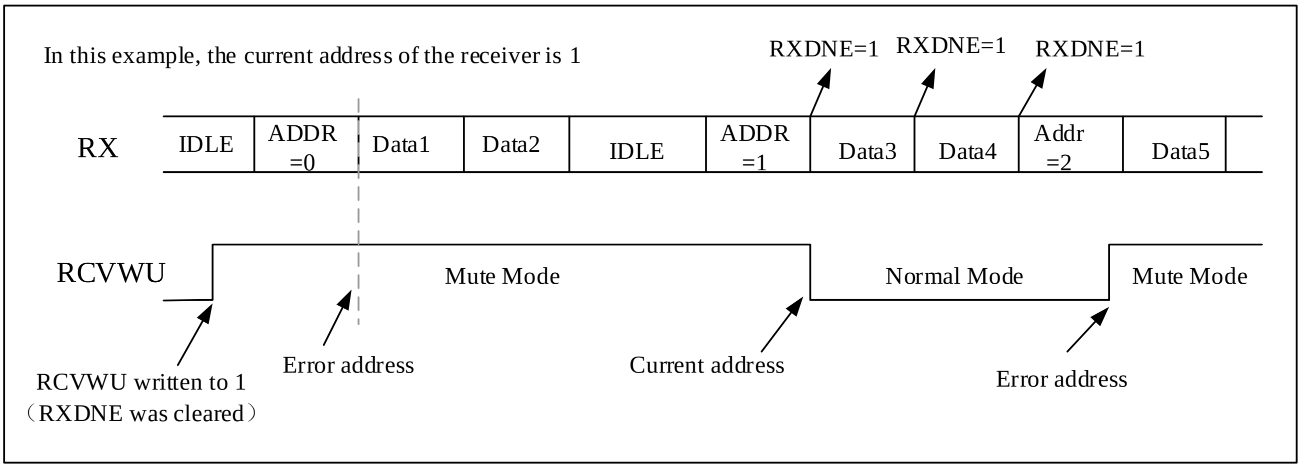
UART_CTRL1.RCVWU is cleared. The UART_STS.RXDNE bit will be set when this matching address is received. Data can then be transmitted normally.

Figure 9-11 Mute Mode Detected Using Address Mark



9.4.9 Single-wire Half-duplex Mode

UART supports single-wire half-duplex communication, allowing data to be transmitted in both directions, but only allows data to be transmitted in one direction at the same time. Communication conflicts are managed by software.

Select the single wire half duplex mode by setting the UARD_CTRL3.HDMEN bit. At this time, all of the following control bits must be reset to zero: UARD_CTRL2.LINMEN、UART_CTRL3.IRDAMEN。

After the half-duplex mode is turned on, the TX pin and the RX pin are internally connected, and the RX pin is no longer used. When there is no data to be transmitted, TX is always released. Therefore, when not driven by the UART, the TX pin must be configured as a floating input or an open-drain output high.

9.4.10 Serial IrDA Infrared Encoding/Decoding Mode

UART supports the IrDA (Infrared Data Association).

Through the UART_CTRL3. IRDAMEN bit, you can choose whether to enable the infrared mode. When using the infrared function, UART_CTRL2.STPB[1:0], UART_CTRL2.LINMEN, UART_CTRL3.HDMEN these bits should be kept clear

Through the UART_CTRL3. IRDALP bit, it can be used to select normal mode or low power infrared mode.

9.4.10.1 IrDA normal mode

When UART_CTRL3.IRDALP=0, select normal infrared mode.

IrDA is a half-duplex communication protocol, so there should be a minimum delay of 10ms between sending and receiving, that uses a inverted return-to-zero modulation scheme (RZI), which uses an infrared light pulse to represent a logic '0', and the pulse width is specified as 3/16 of a bit period in normal mode, as shown in Figure 9-13 the UART only supports up to 115200bps.

The UART sends data to the SIR encoder, and the bit stream output by the UART will be modulated. A modulated stream of pulses is sent from the infrared transmitter and then received by the infrared receiver. The SIR receiver decoder demodulates it and outputs the data to the UART.

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The encoder and decoder have opposite input polarities. When idle, the encoder output is low level, while the decoder input is high level. The encoder outputs a high pulse to represent logic 0 and a low level as logic 1. The decoder input is the opposite.

If the UART is sending data to the IrDA transmit encoder, then the IrDA receive decoder will ignore any data on the IrDA receive line. If the UART is receiving data sent from the SIR receiver decoder, the data sent by the UART to the IrDA transmitter encoder will not be encoded.

Pulse width is programmable. The IrDA specification requires pulses to be wider than 1.41us. For pulse widths less than 2 cycles, the receiver will filter them out. PSCV is the prescaler value programmed in the UART_GTP register.

9.4.10.2 IrDA low power mode

When UART_CTRL3.IRDALP=1, select low power infrared mode.

For the transmitter, when in low power mode, the pulse width is 3 times the low power baud rate, which is a minimum of 1.42MHz. Typically,this value is 1.8432MHz (1.42 MHz < PSC < 2.12 MHz).

For the receiver, the requirement for a valid signal is that the duration of the low level signal must be greater than 2 PSCV cycles.

Figure 9-12 IrDA SIR ENDEC-Block Diagram

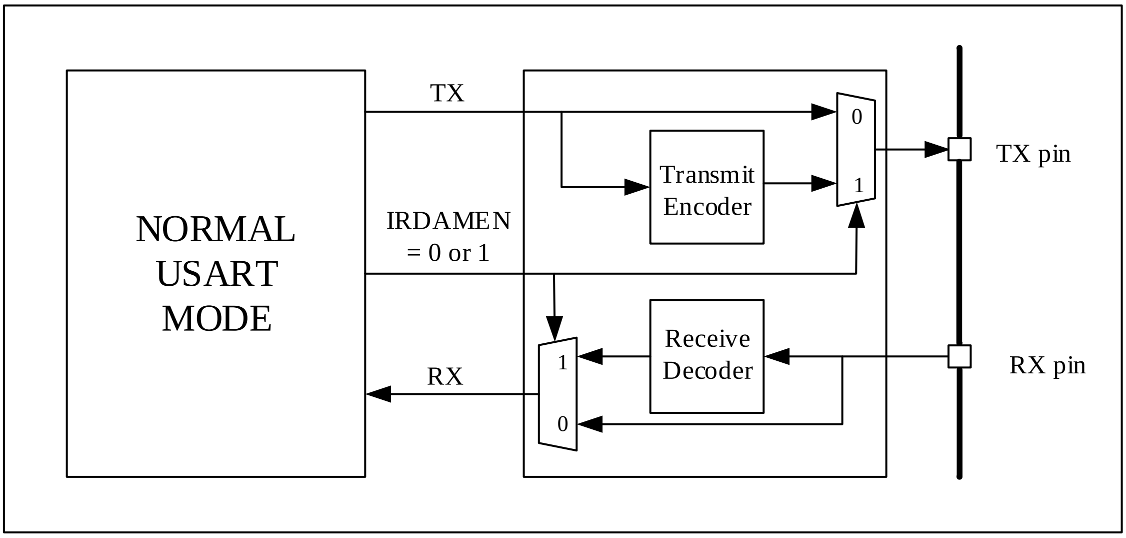

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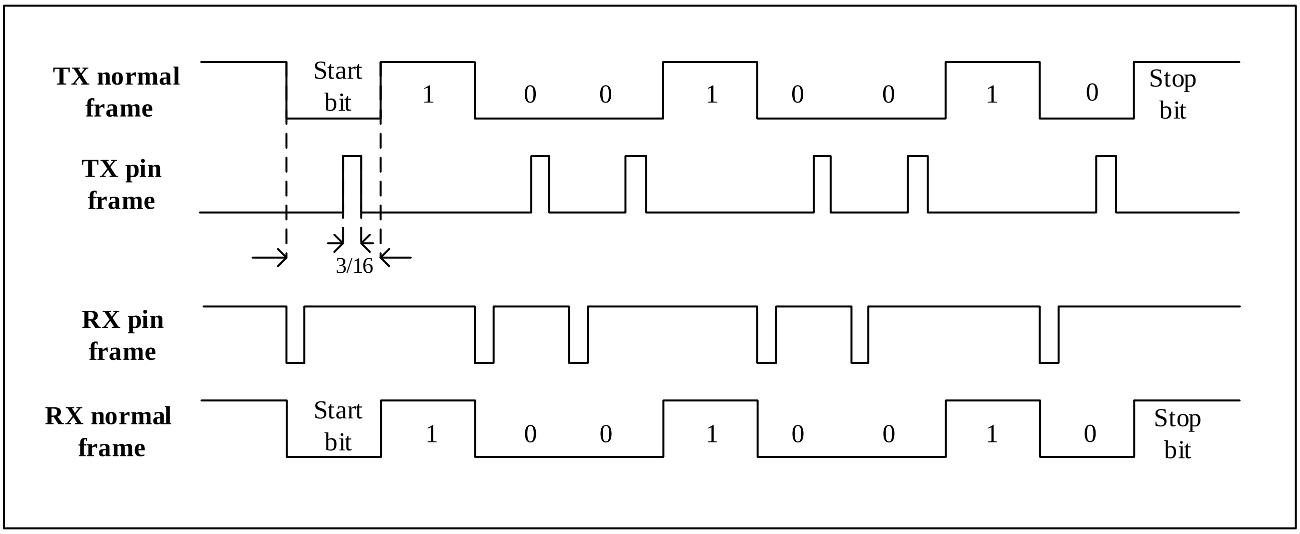
Figure 9-13 IrDA Data Modulation (3/16)-Normal Mode



9.4.11 LIN Mode

UART supports the ability of a LIN(Local interconnection Network) master to send a synchronization break and the ability of a LIN slave to detect a break. LIN mode can be enabled by configuring the UART_CTRL2.LINMEN bit.

Note: When using LIN mode, UART_CTRL2.STPB[1:0], UART_CTRL3.HDMEN, UART_CTRL3. IRDAMEN, these bits should be kept clear.

9.4.11.1 LIN transmission

When LIN is sent, the length of the data bits sent can only be 8 bits. By setting UART_CTRL1.SDBRK, a 13-bit '0' will be sent as the break symbol, and insert a stop bit.

9.4.11.2 LIN reception

Whether the bus is idle or during the transmission of a data frame, as long as the break frame appears, it can be detected. The break symbol detection is independent of the UART receiver.

By configuring the UART_CTRL2.LINBDL bit, 10-bit or 11-bit break character detection can be selected.

When the receiver detects the start bit, the circuit samples each subsequent bit at the 8th, 9th, and 10th oversampling clock points of each bit. When 10 or 11 consecutive bits are detected as '0' and followed by a delimiter, it means that a LIN break is detected, and UART_STS.LINBDF is set. Before confirming the break symbol, check the delimiter as it means the RX line has gone back to high level. An interrupt is generated if the LIN breaker detection interrupt (UART_CTRL2.LINBDIEN) is enabled.

If a '1' is sampled before the 10th or 11th sample point, the current detection is canceled and the start bit is searched again.

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Figure 9-14 Break Detection in LIN Mode (11-bit Break Length, The LINBDL Bit Is Set)

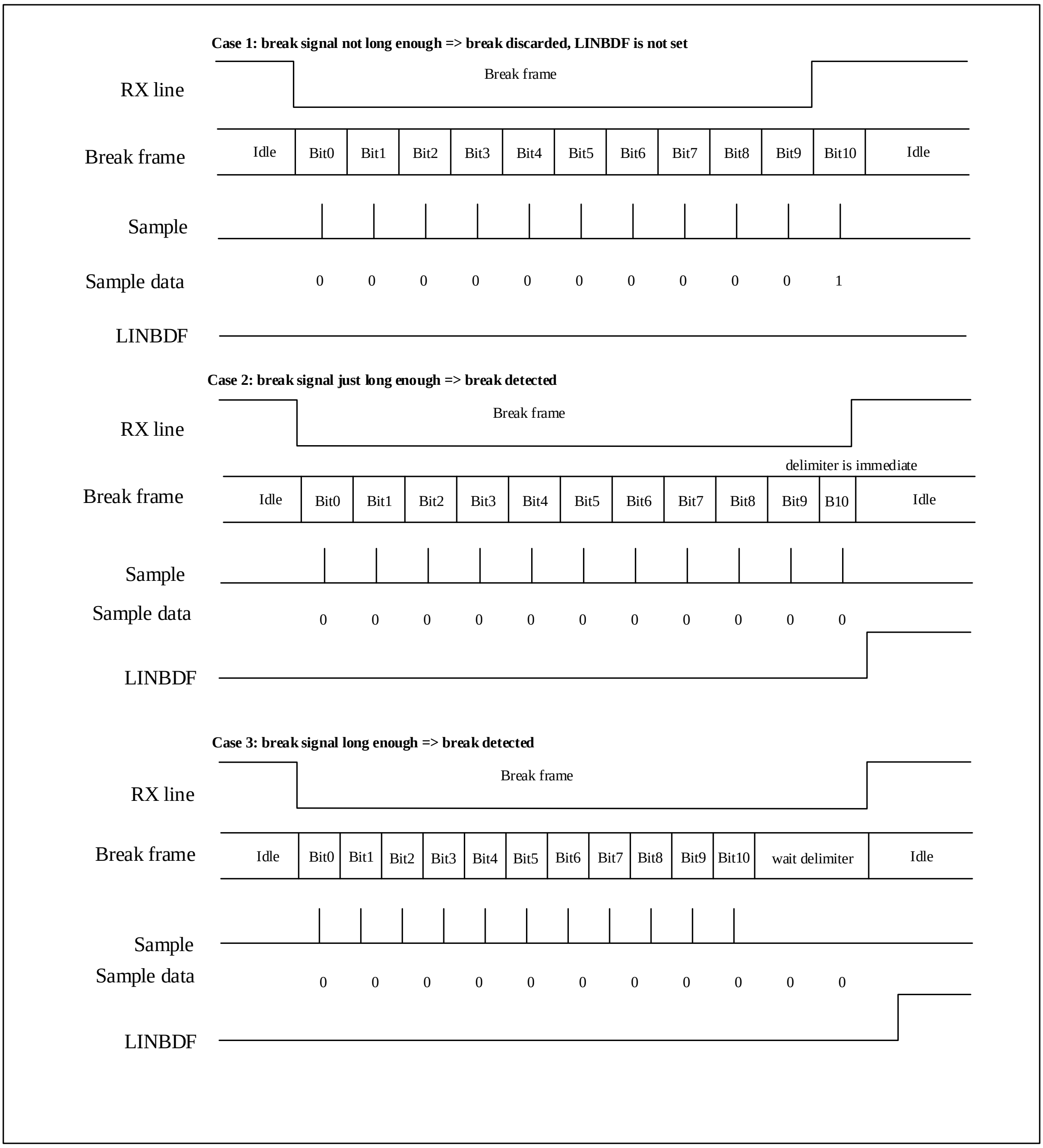

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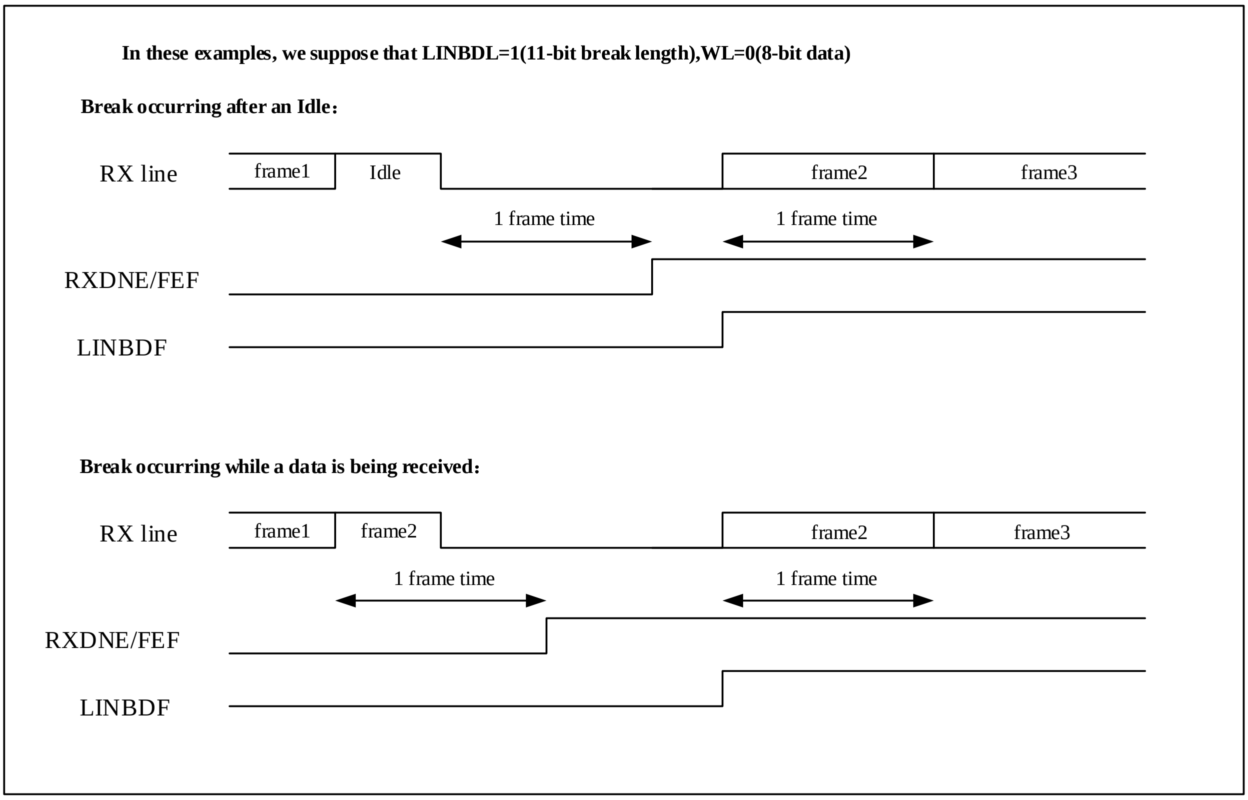
Figure 9-15 Break Detection and Framing Error Detection in LIN Mode



9.4.12 UART3 Low-Power Wakeup

UART3 supports the low-power wakeup function. When the chip is in low-power mode, UART can continue to operate in low-power mode.

The configuration process is as follows:

1. Enable EXTI10 event trigger.
2. Switch the system clock to LSI.
3. Switch the clock source of UART3 to LSI.
4. Configure UART3.
5. Enable UART3 wakeup mode before entering STOP mode.
6. Configure and select the STOP mode type as WFE.
7. Reconfigure the clock and UART3 after exiting STOP mode.

Note: After the system clock is switched to LSI, attention should be paid to the change in the main clock frequency of other peripherals.

9.5 Interrupt Request

The various interrupt events of UART are logical OR relations, if the corresponding enable control bit is set, these events can generate their own interrupts, but only one interrupt request can be generated at the same time.

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Table 9-7 UART Interrupt Request

Interrupt Function	Interrupt Event	Event Flag	Enable Bit
UART global interrupt	Transmission data register is empty.	TXDE	TXDEIEN
	Receiver Timeout	RTOF	RTOIE
	Transmission complete	TXC	TXCIEN
	Receive data ready to be read	RXDNE	RXDNEIEN
	Data overrun error detected.	ORERR	
	Idle line detected	IDLEF	IDLEIEN
	Parity error	PEF	PEIEN
	Break flag	LINBDF	LINBDIEN
	Noise, overrun error and framing error in multi-buffer communication(DMA)	NEF/OREF/FEF	ERRIEN(1)

(1) This flag bit is used only when DMA is used to receive data(UART_CTRL3.DMARXEN=1).

9.6 Mode Support

Table 9-8 UART Mode Setting (1)

Communication Mode	UART1	UART2	UART3
Asynchronous mode	Y	Y	Y
DMA communication mode	Y	Y	Y
Multiprocessor	Y	Y	Y
Single-wire half duplex mode	Y	Y	Y
IrDA infrared mode	Y	Y	Y
LIN	Y	Y	Y

Note:

(1)Y = support this mode, N = do not support this mode.

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9.7 UART Register

9.7.1 UART Register Overview

Table 9-9 UART Register Overview

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x00	UART_CTRL1	Reserved				SWAP	OSPM	DEAT					DEDT					DEP	DEM	SDBRK	PEIEN	TXCIEN	TXDEIEN	RXDNEIE	IDLEIEN	WUM	RCVWU	WL	PCEN	PSEL	TXEN	RXEN	UEN
0x04	UART_CTRL2	Reserved														RTOITE	RTOCF	RTOEN	LINBDL	LINBDIE	LINMEN	Reserved					STPB		Reserved	ADDR			
0x08	UART_CTRL3	Reserved																							IRDALP	IRDAME	ERRIEN	DMARXE	DMATXE	HDMEN	Reserved		
0x0C	UART_STS	Reserved															RTOF	FEF	NEF	OREF	PEF	LINBDF	Reserved	RXDNE	TXC	TXDE	IDLEF	Reserved					
0x10	UART_DAT	Reserved																							DATV								
0x14	UART_BRCF	Reserved																DIV_Integer												DIV_Decimal			
0x18	UART_GTP	Reserved																								PSCV							
0x24	UART_RTO	Reserved				TIME																											
0x28	UART_WKUP	Reserved																														DATCLR	EN

9.7.2 UART Control Register 1 Register (UART_CTRL1)

Address offset : 0x00

Reset value : 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved				SWAP	OSPM	DEAT					DEDT				
				rw	rw	rw					rw				

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DEP	DEM	SDBRK	PEIEN	TXCIEN	TXDEIEN	RXDNEIEN	IDLEIEN	WUM	RCVWU	WL	PCEN	PSEL	TXEN	RXEN	UEN
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Bit Field	Name	Description
31:28	Reserved	Reserved, the reset value must be maintained
27	SWAP	Swap TX/RX pins his bit is set and cleared by software.

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Bit Field	Name	Description
		0: Use TX/RX pins as defined by the standard pinout. 1: Swap the functions of TX and RX pins. Enables operation in cross-connection with another UART. This bitfield can only be written when the UART is disabled (UEN = '0').
26	OSPM	Oversampling mode 0: 16× oversampling 1: 8× oversampling This bit can only be written when the UART is disabled (UE = '0'). *Note: This bit must remain cleared in LIN and IrDA modes.*
25:21	DEAT	Driver Enable assertion time This 5-bit value defines the time between activating the DE (Driver Enable) signal and the start of the start bit. The time is expressed in sampling time units (1/8 or 1/16 bit time, depending on the oversampling rate). This bitfield can only be written when the UART is disabled (UE = '0').
20:16	DEDT	Driver Enable deassertion time This 5-bit value defines the time between the end of the last stop bit in the transmitted message and deactivating the DE (Driver Enable) signal. The time is expressed in sampling time units (1/8 or 1/16 bit time, depending on the oversampling rate). If a write operation to the UART_TDR register is performed during the DEDT time, the new data will only be transmitted after the DEDT and DEAT times have elapsed. This bitfield can only be written when the UART is disabled (UE = '0').
15	DEP	Driver enable polarity selection 0: DE signal is active high. 1: DE signal is active low. This bit can only be written when the UART is disabled (UE = '0').
14	DEM	Driver enable mode This bit is used to activate external transceiver control via the DE signal. 0: Disable DE function. 1: Enable DE function. This bit can only be written when the UART is disabled (UEN = '0').
13	SDBRK	Send Break Character. The software transmits a break character by setting this bit to 1. This bit is cleared by hardware during stop bit of the break frame transmission. 0: No break character was sent. 1: Send a break character.
12	PEIEN	PE interrupt enable If this bit is set to 1, an interrupt is generated when UART_STS.PEF bit is set. 0: Parity error interrupt is disabled. 1: Parity error interrupt is enabled.
11	TXCIEN	Transmit complete interrupt enable. If this bit is set to 1, an interrupt is generated when UART_STS.TXC is set. 0: Transmission completion interrupt is disabled. 1: Transmission completion interrupt is enabled.

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Bit Field	Name	Description
10	TXDEIEN	TXDE interrupt enable If this bit is set to 1, an interrupt is generated when UART_STS.TXDE bit is set. 0: Send buffer empty interrupt is disabled. 1: Send buffer empty interrupt is enabled.
9	RXDNEIEN	RXDNE interrupt enable If this bit is set to 1, an interrupt is generated when UART_STS.RXDNE or UART_STS.OREF is set. 0: Data buffer non-empty interrupt o and overrun error interrupt are disabled. 1: Data buffer non-empty interrupt o and overrun error interrupt are enabled.
8	IDLEIEN	IDLE interrupt enable. If this bit is set to 1, an interrupt is generated when UART_STS.IDLEF is set. 0: IDLE line detection interrupt is disabled. 1: IDLE line detection interrupt is enabled.
7	WUM	Wake up mode from mute mode. 0: Idle frame wake up. 1: Address identifier wake up.
6	RCVWU	The receiver wakes up Software can set this bit to 1 to make UART enter mute mode, and clear this bit to 0 to wake up UART. In idle frame wake-up mode (UART_CTRL1.WUM=0), this bit is cleared by hardware when an idle frame is detected. In address wake-up mode (UART_CTRL1.WUM=1), when an address matching frame is received, this bit is cleared by hardware. Or when an address mismatch frame is received, it is set to 1 by hardware. 0: The receiver is in normal operation mode. 1: The receiver is in mute mode.
5	WL	Word length. 0:8 data bits. 1:9 data bits. *Note: If data is in transit, this bit cannot be configured.*
4	PCEN	Parity control enable 0: Parity control is disabled. 1: Parity control is enabled.
3	PSEL	Parity selection. 0: even check. 1: odd check.
2	TXEN	Transmitter enable. 0: The transmitter is disabled. 1: the transmitter is enabled.
1	RXEN	Receiver enable 0: The receiver is disabled. 1: the receiver is enabled.
0	UEN	UART enable When this bit is cleared, the divider and output of UART stop working after the current

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Bit Field	Name	Description
		byte transmission is completed to reduce power consumption. Software can set or clear this bit. 0: UART is disabled. 1: UART is enabled.

9.7.3 UART Control Register 2 Register (UART_CTRL2)

Address offset :0x04

Reset value : 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved														RTOITE	RTOCF
														rw	rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RTOEN	LINBDL	LINBDIEN	LINMEN	Reserved					STPB[1:0]		Reserved	ADDR[3:0]			
rw	rw	rw	rw						rw			rw			

Bit Field	Name	Description
31:18	Reserved	Reserved, the reset value must be maintained
17	RTOITE	Receiver timeout interrupt enable This bit is set and cleared by software. 0: Disable interrupt. 1: Generate UART interrupt when the RTOF bit in the UART_STS register is set to '1'. Note: If the UART does not support the receiver timeout function, this bit is reserved and forced to '0' by hardware.
16	RTOCF	Receiver timeout clear flag When writing '1' to this bit, the RTOF flag in the UART_STS register is cleared. Note: If the UART does not support the receiver timeout function, this bit is reserved and forced to '0' by hardware.
15	RTOEN	Receiver timeout enable This bit is set and cleared by software. 0: Disable receiver timeout function. 1: Enable receiver timeout function. After enabling this function, if the RX line remains idle (no reception) for the duration programmed in the RTOR (Receiver Timeout Register), the RTOF flag in the UART_STS register is set to '1'. Note: If the UART does not support the receiver timeout function, this bit is reserved and forced to '0' by hardware.
14	LINBDL	LIN break detection length. This bit is used to set the length of the break frame.

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Bit Field	Name	Description
		0:10 bit break detection 1:11 bit break detection *Note: LINBDL can be used to control the detection length of Break Characters in LIN mode and other modes, and the detection length is the same as that in LIN mode.*
13	LINBDIEN	LIN break detection interrupt enable. If this bit is set to 1, an interrupt will be generated when UART_STS.LINBDF bit is set. 0: Disconnect signal detection interrupt is disabled. 1: Turn-off signal detection interrupt enabled
12	LINMEN	LIN mode enable 0:LIN mode is disabled 1:LIN mode enabled
11:7	Reserved	Reserved, the reset value must be maintained
6:5	STPB[1:0]	STOP bits. 00:1 stop bit. 01:0.5 stop bit. 10:2 stop bit. 11:1.5 stop bit. *Note: UART recommends using 1/2 stop bits, while 0.5/1.5 stop bits are generally used for smart card mode.*
4	Reserved	Reserved, the reset value must be maintained
3:0	ADDR[3:0]	UART address. Used in the mute mode of multiprocessor communication, using address identification to wake up a UART device. In address wake-up mode (UART_CTRL1.WUM=1), if the lower four bits of the received data frame are not equal to the ADDR[3:0] value, UART will enter the mute mode; If the lower four bits of the received data frame are equal to the ADDR[3:0] value, UART will be awakened.

9.7.4 UART Control Register 3 Register (UART_CTRL3)

Address offset :0x08

Reset value : 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved							IRDALP	IRDAMEN	ERRIEN	DMARXEN	DMATXEN	HDMEN	Reserved		
							rw	rw	rw	rw	rw	rw			

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Bit Field	Name	Description
31:9	Reserved	Reserved, the reset value must be maintained
8	IRDALP	IrDA low-power mode. This bit is used to select the low power consumption mode for IrDA mode. 0: Normal mode. 1: Low power mode.
7	IRDAMEN	IrDA mode enable. 0:IrDA is disabled. 1:IrDA is enabled.
6	ERRIEN	Error interrupt enable. When DMA receive mode (UART_CTRL3.DMARXEN=1) is enabled, an interrupt will be generated when UART_STS.FEF, UART_STS. OREF or UART_STS. NEF bit is set. 0: Error interrupt is disabled. 1: Error interrupt enabled.
5	DMARXEN	DMA receiver enable. 0:DMA receive mode is disabled. 1:DMA receive mode is enabled.
4	DMATXEN	DMA transmitter enable. 0:DMA transmission mode is disabled. 1:DMA transmission mode is enabled.
3	HDMEN	Half-duplex mode enable. This bit is used to enable half-duplex mode. 0: Half-duplex mode is disabled. 1: Half-duplex mode is enabled.
2:0	Reserved	Reserved, the reset value must be maintained

9.7.5 UART Status Register (UART_STS)

Address offset : 0x0C

Reset value : 0x0000 0180

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															RTOF
															r

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FEF	NEF	OREF	PEF	LINBDF	Reserved	RXDNE	TXC	TXDE	IDLEF	Reserved					
r	r	r	r	rc_w0		rc_w0	rc_w0	r	r						

Bit Field	Name	Description
31:17	Reserved	Reserved, the reset value must be maintained
16	RTOF	recevier timeout

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Bit Field	Name	Description
		After the timeout value programmed in the RTO register has been exceeded, if no communication occurs, this bit is set by hardware. This bit is cleared by software by writing '1' to the RTOCF bit in the UART_CTRL2 register. If RTOITE = '1' in the UART_CTRL2 register, an interrupt is generated. 0: Timeout value not reached1 : Timeout value reached, no data received
15	FEF	Framing error. When the data is not synchronized or a large amount of noise is detected, and the stop bit is not received and recognized at the expected time, it will be judged that a framing error has been detected, and this bit will be set to 1. First read UART_STS, then read UART_DAT can cleared this bit. 0: No framing errors were detected. 1: A framing error or a Break Character is detected. *Note: this bit will not generate an interrupt because it appears with UART_STS.RXDNE, and the hardware will generate an interrupt when setting the UART_STS.RXDNE flag. If the currently transmitted data has both framing errors and overload errors, the hardware will continue to transmit the data and only set the UART_STS.OREF flag bit.* *In the multi-buffer communication mode, if the UART_CTRL3.ERRIEN bit is set, an interrupt will be generated when the FEF flag is set.*
14	NEF	Noise error flag. When noise is detected in the received frame, this bit is set by hardware. It is cleared by the software sequence (read first UART_STS, read UART_DAT again). 0: No noise error detected. 1: Noise error detected. *Note: this bit will not generate an interrupt because it appears with UART_STS.RXDNE, and the hardware will generate an interrupt when setting the UART_STS.RXDNE flag. In the multi-buffer communication mode, if the UART_CTRL3.ERRIEN bit is set, an interrupt will be generated when the NEF flag is set.*
13	OREF	Overrun error With RXDNE set, this bit is set if the UART_DAT register receives data from the shift register. When UART_CTRL3.ERRIEN bit is set, an interrupt will be generated. The software can clear this bit by reading UART_STS first and then reading UART_DAT. 0: No overrun error was detected. 1: Overflow error detected. *Note: In Multi Buffer Communication Mode (DMA), if the UART_CTRL3.ERRIEN bit is set, an interrupt will be generated when setting the OREF flag.* *Note: When OREF is set, the UART_DAT register will no longer update data; if RXDNE is '0' at this time, RXDNE will not be set to '1' again since data is no longer updated.*
12	PEF	Parity error.

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Bit Field	Name	Description
		This bit is set when the parity bit of the received data frame is different from the expected check value. The software can clear this bit by reading UART_STS first and then reading UART_DAT. 0: No parity error was detected. 1: Parity error detected.
11	LINBDF	LIN break detection flag. If UART_CTRL2.LINMEN bit is set, this bit is set by hardware when LIN disconnection is detected. If UART_CTRL2.LINBDIEN bit is set, an interrupt will be generated. This bit is cleared by software. 0: LIN break character not detected. 1: LIN break character detected.
10	Reserved	Reserved, the reset value must be maintained
9	RXDNE	The Read data register not empty. This bit is set when the read data buffer receives data from the shift register. When UART_CTRL1.RXDNEIEN bit is set, an interrupt will be generated. Software can clear this bit by writing 0 to it or reading the UART_DAT register. 0: The read data buffer is empty. 1: The read data buffer is not empty.
8	TXC	Transmission complete. This bit is set to 1 after power-on reset. If UART_STS.TXDE is set, this bit is set when the current data transmission is completed. Setting UART_CTRL1.TXCIEN bit will generate an interrupt. This bit is cleared by software. 0: Transmitting did not complete. 1: Send completed.
7	TXDE	The Transmit data register empty. Set to 1 after power-on reset or data to be sent has been sent to the shift register. Setting UART_CTRL1.TXDEIEN will generate an interrupt. This bit is cleared to 0 when the software writes the data to be sent into UART_DAT. 0: Send data buffer is not empty. 1: The transmitting data buffer is empty.
6	IDLEF	IDLE line detected flag. Within one frame time, the idle state is detected at the RX pin, and this bit is set to 1. When UART_CTRL1.IDLEIEN bit is set, an interrupt will be generated. The software can clear this bit by reading UART_STS first and then reading UART_DAT. 0: No idle frame detected. 1: idle frame detected. *Note: IDLEF bit will not be set high again until UART_STS.RXDNE bit is set (that is, an idle line is detected again).*
5:0	Reserved	Reserved, the reset value must be maintained

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9.7.6 UART Data Register (UART_DAT)

Address offset：0x10

Reset value：undefined（uncertain value）

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved							DATV[8:0]								
							rw								

Bit Field	Name	Description
31:9	Reserved	Reserved, the reset value must be maintained
8:0	DATV[8:0]	Data value Contains the data sent or received; Software can change the transmitted data by writing these bits, or read the values of these bits to obtain the received data. If parity is enabled, when the transmitted data is written into the register, the highest bit of the data (the 7th or 8th bit depends on UART_CTRL1.WL bit) will be replaced by the parity bit.

9.7.7 UART Baud Rate Register (UART_BRCF)

Address offset : 0x14

Reset value : 0x0000 0000

Note: When UART_CTRL1.UEN=1, this register cannot be written;The baud counter stops counting if UART_CTRL1.TXEN or UART_CTRL1.RXEN are disabled respectively.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DIV_Integer[11:0]												DIV_Decimal[3:0]			
rw												rw			

Bit Field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained
15:4	DIV_Integer [11:0]	Integer part of baud rate divider.
3:0	DIV_Decimal[3:0]	Fractional part of baud rate divider.

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9.7.8 UART Guard Time and Prescaler Register (UART_GTP)

Address offset : 0x18

Reset value : 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								PSCV[7:0]							
								rw							

Bit Field	Name	Description
31:8	Reserved	Reserved, the reset value must be maintained
7:0	PSCV[7:0]	Prescaler value） Prescaler Value (PSCV)In IrDA Low-Power mode, these bits are used to set the division factor that divides the peripheral clock (PCLK1/PCLK2) to generate the low-power frequency. 00000000: Reserved – Do not write this value 00000001: Divide the source clock by 1 … 11111111: Divide the source clock by 255 In IrDA Normal mode, PSCV can only be set to 00000001.

9.7.9 UART Receiver Timeout Register (UART_RTO)

Address offset : 0x24

Reset value : 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved				TIME											
				rw											

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TIME															
rw															

Bit Field	Name	Description
31:28	Reserved	Reserved, the reset value must be maintained
27:0	TIME	Receiver timeout value

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Bit Field	Name	Description
		Note: The unit is baud rate time.

9.7.10 UART Low-Power Wakeup Register (UART_WKUP)

Address offset : 0x28

Reset value : 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved														DATCLR	EN
														rw	rw

Bit Field	Name	Description
31:2	Reserved	Reserved, the reset value must be maintained
1	DATCLR	Whether to clear the receive wakeup data 0: Clear the receive wakeup data and clear the RXDNE flag bit 1: Do not clear the receive wakeup data, set the RXDNE flag bit to '1'
0	EN	Low-power Wakeup Enable 0: Disable the UART low-power wakeup function 1: Enable the UART low-power wakeup function

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10 HDIV Divider

10.1 Function description

- only 32-bit operations are supported, and signed or unsigned operations are supported
- input: 32-bit dividend, 32-bit divisor
- output: 32-bit quotient, 32-bit remainder
- complete one signed/unsigned integer division operation in 8 clock cycles
- divisor is zero, warning flag bit, data fixed return 0
- support optional hardware auto enable (write divisor auto enable)
- read quotient or remainder register, without querying the status, it can be read immediately (enabled)

10.2 Operating instructions

10.2.1 Basic use process

Step 1: Initialize Configuration

Check HDIV_CTRLSTS.HDIVDF to ensure it is 1 (except for first-time use, default value is 0), which means the module is in an idle state

Set HDIV_CTRLSTS.HDIVEN=1

Configure HDIV_CTRLSTS.TYPESEL, HDIV_CTRLSTS.BUSHOLD, HDIV_CTRLSTS.AUTSTART according to the scene requirements

Step 2: Write the dividend and divisor

Write dividend to HDIV_DIVIDEND

Write divisor to HDIV_DIVISOR

Step 3: Start the calculation

If HDIV_CTRLSTS.AUTSTART=1, the calculation will automatically start after writing HDIV_DIVISOR;

Otherwise, after writing 1 to HDIV_CTRLSTS.HDIVEN, the calculation will begin

Step 4: Wait for the calculation to complete

If HDIV_CTRLSTS.BUSHOLD=1, there is no need to query HDIV_CTRLSTS.HDIVDF

If HDIV_CTRLSTS.BUSHOLD=0, it is necessary to query HDIV_CTRLSTS.HDIVDF until HDIV_CTRLSTS.HDIVDF=1

Step 5: Read the results

The quotient needs to be read from HDIV_QUOTIENT

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The remainder needs to be read from HDIV_REMAINDER

Step 6: Loop operation

Configuration changes need to start from step 1

Configuration remains unchanged, starting from step 2

10.2.2 Exception Handling

Zeroing error occurs when HDIV_DIVISOR is configured as 0, causing a zeroing exception. HDIV_DIVBY0 and HDIV_DIVBY0 are automatically set to 1. Users need to check this bit after each calculation to confirm if a zeroing exception occurred. This bit will automatically reset to zero at the beginning of the next calculation.

10.3 HDIV registers

10.3.1 HDIV register overview

Table 10-1 HDIV register overview

<table>
<tr><th>Offset</th><th>Register</th><th>31</th><th>30</th><th>29</th><th>28</th><th>27</th><th>26</th><th>25</th><th>24</th><th>23</th><th>22</th><th>21</th><th>20</th><th>19</th><th>18</th><th>17</th><th>16</th><th>15</th><th>14</th><th>13</th><th>12</th><th>11</th><th>10</th><th>9</th><th>8</th><th>7</th><th>6</th><th>5</th><th>4</th><th>3</th><th>2</th><th>1</th><th>0</th></tr>
<tr><td>0x00</td><td>HDIV_CTRLSTS</td><td colspan="23">Reserved</td><td>TYPESEL</td><td>AUTOSTA</td><td>BUSHOLD</td><td colspan="2">Reserved</td><td>HDIVDF</td><td>Reserved</td><td>HDIVSTAR</td><td>HDIVEN</td></tr>
<tr><td>0x04</td><td>HDIV_DIVIDEND</td><td colspan="32">DIVIDEND</td></tr>
<tr><td>0x08</td><td>HDIV_DIVISOR</td><td colspan="32">DIVISOR</td></tr>
<tr><td>0x0c</td><td>HDIV_QUOTIENT</td><td colspan="32">QUOTIENT</td></tr>
<tr><td>0x10</td><td>HDIV_REMAINDER</td><td colspan="32">REMAINDER</td></tr>
<tr><td>0x14</td><td>HDIV_DIVBY0</td><td colspan="31">Reserved</td><td>DIVBY0</td></tr>
</table>

10.3.2 HDIV control status register (HDIV_CTRLSTS)

Offset address: 0x00

Reset value: 0x0000 0000

<table>
<tr><th>31</th><th>30</th><th>29</th><th>28</th><th>27</th><th>26</th><th>25</th><th>24</th><th>23</th><th>22</th><th>21</th><th>20</th><th>19</th><th>18</th><th>17</th><th>16</th></tr>
<tr><td colspan="16">Reserved</td></tr>
</table>

<table>
<tr><th>15</th><th>14</th><th>13</th><th>12</th><th>11</th><th>10</th><th>9</th><th>8</th><th>7</th><th>6</th><th>5</th><th>4</th><th>3</th><th>2</th><th>1</th><th>0</th></tr>
<tr><td colspan="7">Reserved</td><td>TYPESEL</td><td>AUTO START</td><td>BUS HOLD</td><td colspan="2">Reserved</td><td>HDIVDF</td><td>Reserved</td><td>HDIV START</td><td>HDIVEN</td></tr>
</table>

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							rw	rw	rw			rw		rw	rw

Bit field	Name	Description
31:9	Reserved	Reserved,the reset value must be maintained.
8	TYPESEL	Definition of dividend and divisor data types 0: unsigned number 1: Signed number
7	AUTOSTART	Automatic calculation enable, automatic calculation refers to starting a division operation every time a divisor is written 0: Disable 1: Enable
6	BUSHOLD	Bus hold mode during the calculation process 0: When the calculation starts, if the software reads the quotient or remainder before completing the calculation process, the bus will not hold 1: When the calculation starts, if the software reads the quotient or remainder before completing the calculation process, the bus will hold
5:4	Reserved	Reserved,the reset value must be maintained.
3	HDIVDF	This calculation completion flag 0: Uncompleted 1: Completed
2	Reserved	Reserved,the reset value must be maintained.
1	HDIVSTART	Single calculation enable, enable the control bit once, perform a division operation once 0: Disable 1: Enable
0	HDIVEN	HDIV enable, only when this control bit is enabled, can single or automatic calculations be performed 0: Disable 1: Enable

10.3.3 HDIV dividend register (HDIV_DIVISOR)

Offset address: 0x04

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DIVIDEND[31:16]															
rw															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DIVIDEND[15:0]															
rw															

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Bit field	Name	Description
31:0	DIVIDEND	32bit dividend

10.3.4 HDIV quotient register (HDIV_QUOTIENT)

Offset address: 0x08

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DIVISOR[31:16]															
rw															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DIVISOR[15:0]															
rw															

Bit field	Name	Description
31:0	DIVIDEND	32bit divisor

10.3.5 HDIV remainder register (HDIV_REMAINDER)

Offset address: 0x0C

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
QUOTIENT[31:16]															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
QUOTIENT[15:0]															
r															

Bit field	Name	Description
31:0	QUOTIENT	32-bit quotient If the divisor is written as 0, the result is 0

10.3.6 HDIV remainder register (HDIV_REMAINDER)

Offset address: 0x10

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Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
REMAINDER[31:16]															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REMAINDER[15:0]															
r															

Bit field	Name	Description
31:0	REMAINDER	32-bit remainder If the divisor is written as 0, the result is 0

10.3.7 HDIV divide by zero register (HDIV_DIVBY0)

Offset address: 0x14

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved															DIVBY0
															r

Bit field	Name	Description
31:1	Reserved	Reserved,the reset value must be maintained.
0	DIVBY0	Dividing by 0 flag bit 0: The divisor is non-zero 1: The divisor is zero

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11 SQRT Square root calculator

11.1 Function description

- Only supports 32-bit operations
- Input: 32-bit unsigned square root integer
- Output: 16-bit root mean square
- Complete an unsigned integer square root operation in 8 clock cycles
- Support optional hardware auto enable (write open square integer auto enable)
- Read result register, no need to query status, can be read immediately

11.2 Operating instructions

11.2.1 Basic use process

Step 1: Initialize Configuration

Check SQRT_CTRLSTS.SQRRTF to ensure it is 1(excluding first-time use, default value is 0), which means the module is in an idle state

Set SQRT_CTRLSTS. SQRTEN=1

Configure HDIV_CTRLSTS.BUSHOLD and HDIV_CTRLSTS.AUTSTART according to the scene requirements

Step 2: Write the square root number

Write the square root number to SQRT_SADICAND

Step 3: Start the calculation

If SQRT_CTRLSTS.AUTOSTART=1, the calculation will automatically start after SQRT_SADICAND is written

Otherwise, after SQRT_CTRLSTS.SQRTEN writes 1, the calculation begins

Step 4: Wait for the calculation to complete

If SQRT_CTRLSTS.BUSHOLD=1, there is no need to query SQRT_CTRLSTS.SQRTF

If SQRT_CTRLSTS.BUSHOLD=0, it is necessary to query SQRT_CTRLSTS.SQRRTF until SQRT_CTRLSTS.SQRRTF=1

Step 5: Read the results

The square root number needs to be read as SQRT_ROOT

Step 6: Loop operation

Configuration changes need to start from step 1

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Configuration remains unchanged, starting from step 2

11.3 SQRT registers

11.3.1 SQRT register overview

Table 11-1 SQRT register overview

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x00	SQRT_CTRLSTS	Reserved																								AUTOSTA	BUSHOLD	Reserved		SQRTDF	Reserved	SQRTSTAR	SQRTEN
0x04	SQRT_RADICAND	RADICAND																															
0x08	SQRT_ROOD	Reserved																ROOT															

11.3.2 SQRT control status register (SQRT_CTRLSTS)

Offset address: 0x00

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								AUTO START	BUS HOLD	Reserved		SQRTDF	Reserved	SQRT START	SQRTEN
								rw	rw			r		rw	rw

Bit field	Name	Description
31:8	Reserved	Reserved,the reset value must be maintained.
7	AUTOSTART	Automatic calculation enable, automatic calculation refers to starting a square root operation every time the square root is written 0: Disable 1: Enable
6	BUSHOLD	Bus hold mode during the calculation process 0: When the calculation starts and the calculation process is not completed, the software reads the square root number, and the bus will not hold 1: When the calculation starts and the calculation process is not completed, the software reads the square root number, and the bus will hold
5:4	Reserved	Reserved,the reset value must be maintained.
3	SQRTDF	This calculation completion flag 0: Uncompleted

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Bit field	Name	Description
		1: Completed
22	Reserved	Reserved,the reset value must be maintained.
1	SQRTSTART	Single calculation enable, enable the control bit once, perform one square root operation 0: Disable 1: Enable
0	SQRTEN	SQRT enabled, only when this control bit is enabled, can single or automatic calculations be performed 0: Disable 1: Enable

11.3.3 SQRT Radicand register (SQRT_RADICAND)

Offset address: 0x04

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RADICAND[31:16]															
rw															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RADICAND[15:0]															
rw															

Bit field	Name	Description
31:0	RADICAND	32bit radicand

11.3.4 SQRT square root register (SQRT_ROOT)

Offset address: 0x08

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ROOT															
r															

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Bit field	Name	Description
31:16	Reserved	Reserved,the reset value must be maintained.
15:0	ROOT	16-bit square root output

12 Advanced Timer (TIM1)

12.1 Introduction

The advanced control timer (TIM1) are mainly used in the following scenarios: counting the input signals, measuring the pulse width of the input signals and generating the output waveforms, etc.

Advanced-control timer have complementary output function with dead-time insertion and break function, which are suitable for motor control.

12.2 Main Features of TIM1

- 16-bit auto-reload counters. (It can realize up-counting, down-counting, up/down counting)
- 16-bit programmable prescaler. (The prescaler factor can be configured with any value between 1 and 65536)
- Programmable repetition counter
- Up to 7 channels
- 7 compare channels（CH1/2/3/4/5/6/7）, the operating modes are PWM output, ouput compare, one-pulse mode output
- 4 capture channels(CH1/2/3/4), the operating mode is input capture
- The events that generate the interrupt/DMA are as follows:
  - Update event
  - Trigger event
  - Input capture
  - Output compare
  - Break signal input
- Complementary outputs with programmable dead-time
  - For TIM1, channel 1,2,3,4 support this feature
- Timer can be controlled by external signal
- Timer can be linked together internally for timer synchronization or chaining
- TIM1_CC5 is used for comparator blanking
- Incremental (quadrature) encoder interface: used for tracking motion and resolving rotation direction and position
- Hall sensor interface: used to do three-phase motor control

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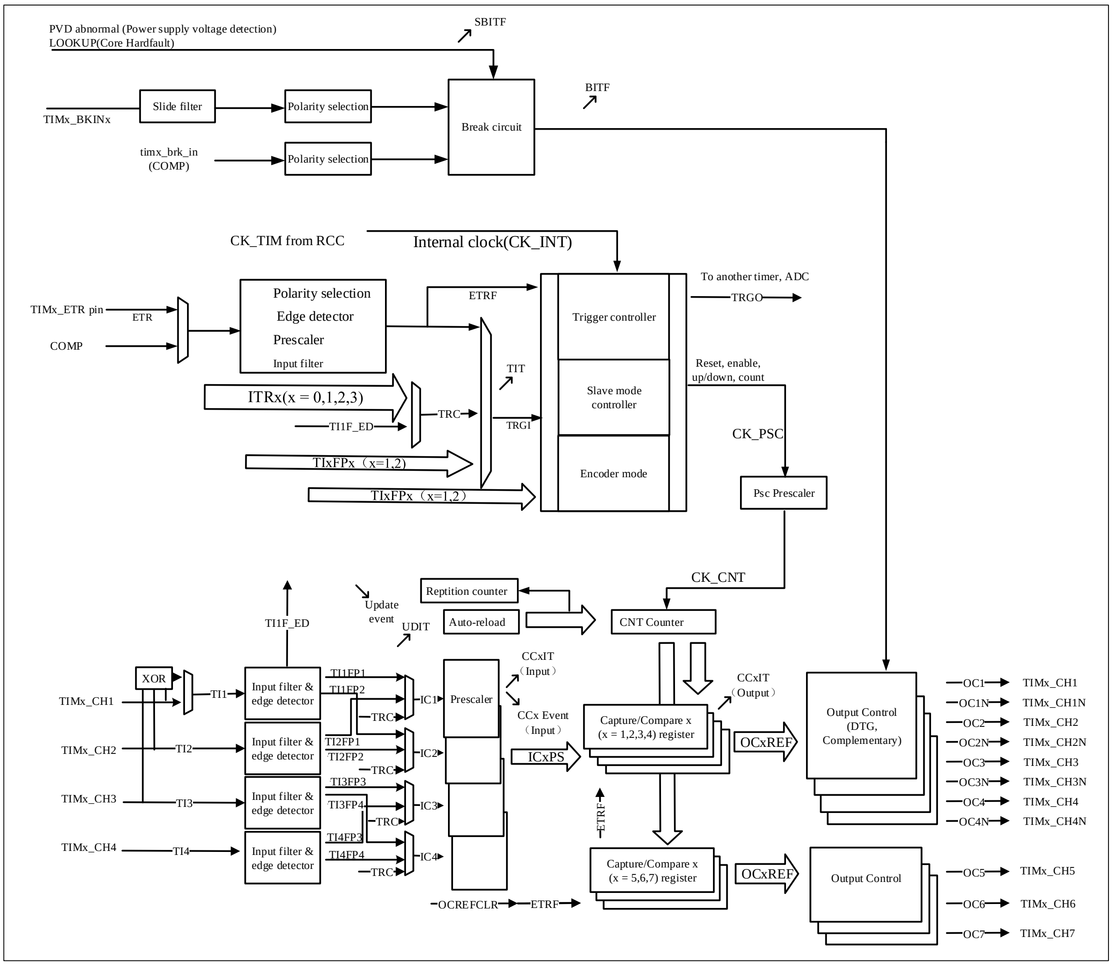
Figure 12-1 Block Diagram of TIM1



↘ *The event* ↗ *Interrupt and DMA output*

The capture channel 1 input can come from IOM or comparator output

12.3 Function Description of TIM1

12.3.1 Time-base Unit

The advanced-control timer's time-base unit mainly includes: prescaler, counter, auto-reload and repetition counter. When the time base unit is operating, the software can read and write the corresponding registers (TIMx_PSC, TIMx_CNT, TIMx_AR and TIMx_REPCNT) at any time.

Depending on the setting of the auto-reload preload enable bit (TIMx_CTRL1.ARPEN), the value of the preload register is transferred to the shadow register immediately or at each update event UEV. When TIMx_CTRL1.UPDIS=0, a counter overflow/underflow or software setting TIMx_EVTGEN.UDGN will generate an update event. The counter CK_CNT is valid only when the TIMx_CTRL1.CNTEN bit is set. The counter starts counting one clock cycle after the TIMx_CTRL1.CNTEN bit is set.

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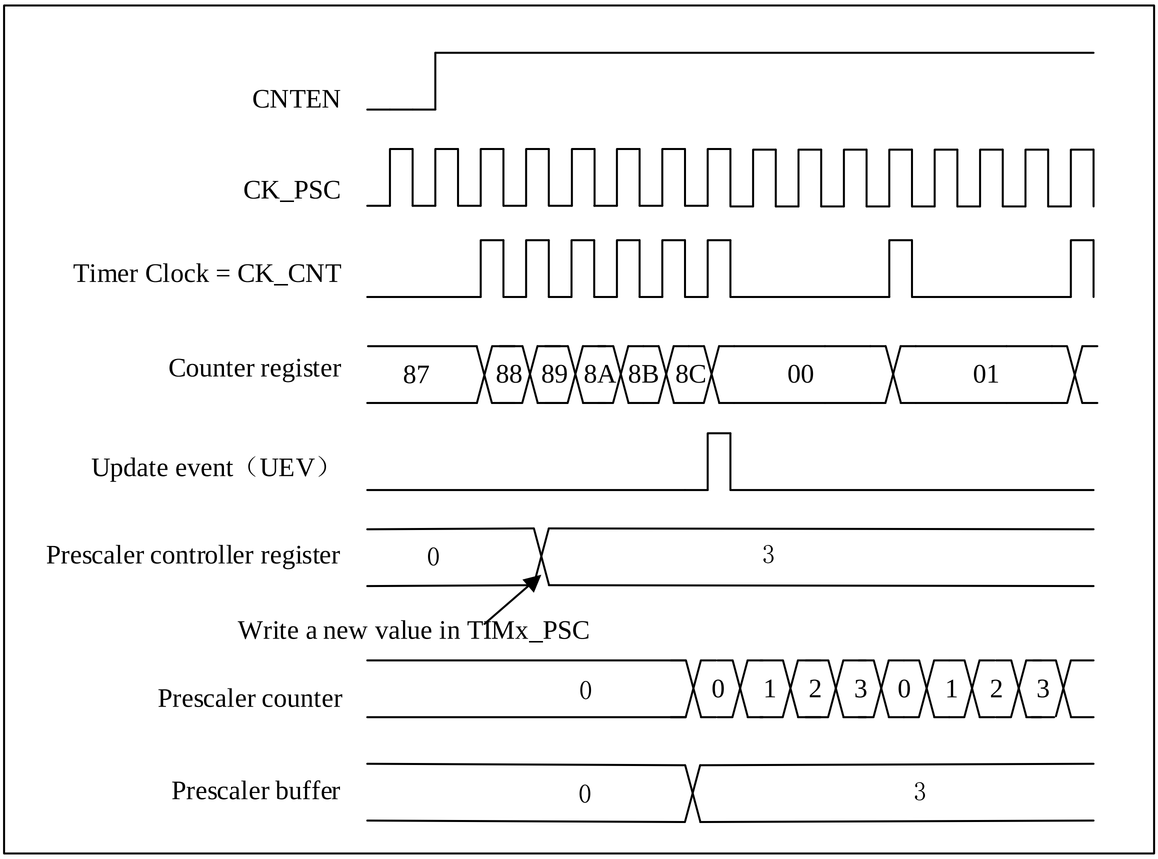
12.3.1.1 **Prescaler description**

The TIMx_PSC register consists of a 16-bit counter that can be used to divide the counter clock frequency by any factor between 1 and 65536. It can be changed on the fly as this register is buffered. The new prescaler value is only taken into account at the next update event.

Figure 12-2 Counter Timing Diagram with Prescaler Division Change from 1 to 4



12.3.2 Counter Mode

12.3.2.1 **Up-counting mode**

In up-counting mode, the counter will count from 0 to the value of the register TIMx_AR, then it restarts from 0 and a counter overflow event is generated.

If the TIMx_CTRL1.UPRS bit (select update request) and the TIMx_EVTGEN.UDGN bit are set, an update event (UEV) will be generated, but the TIMx_STS.UDITF will not be set by hardware, therefore, no update interrupts or update DMA requests are generated. This is to avoid generating an update interrupt when clearing the counter.

Depending on the TIMx_CTRL1.UPRS, when an update event occurs, all registers are updated and the TIMx_STS.UDITF is set:

- The repetition counter reloads the contents of the TIMx_REPCNT
- The auto-reload shadow registers is updated with preload value (TIMx_AR), when TIMx_CTRL1.ARPEN = 1
- The prescaler shadow register is reloaded with the preload value (TIMx_PSC).

To avoid updating the shadow registers when new values are written to the preload registers, you can disable the

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update event by setting TIMx_CTRL1.UPDIS=1.

When an update event is generated, the counter will still be cleared and the prescaler counter will also be set to 0 (but the prescaler value will remain unchanged).

The figure below shows some examples of the counter behavior for different prescaler factors in the up-counting mode.

Figure 12-3 Timing Diagram of Up-counting, The Internal Clock Divider Factor = 2/N

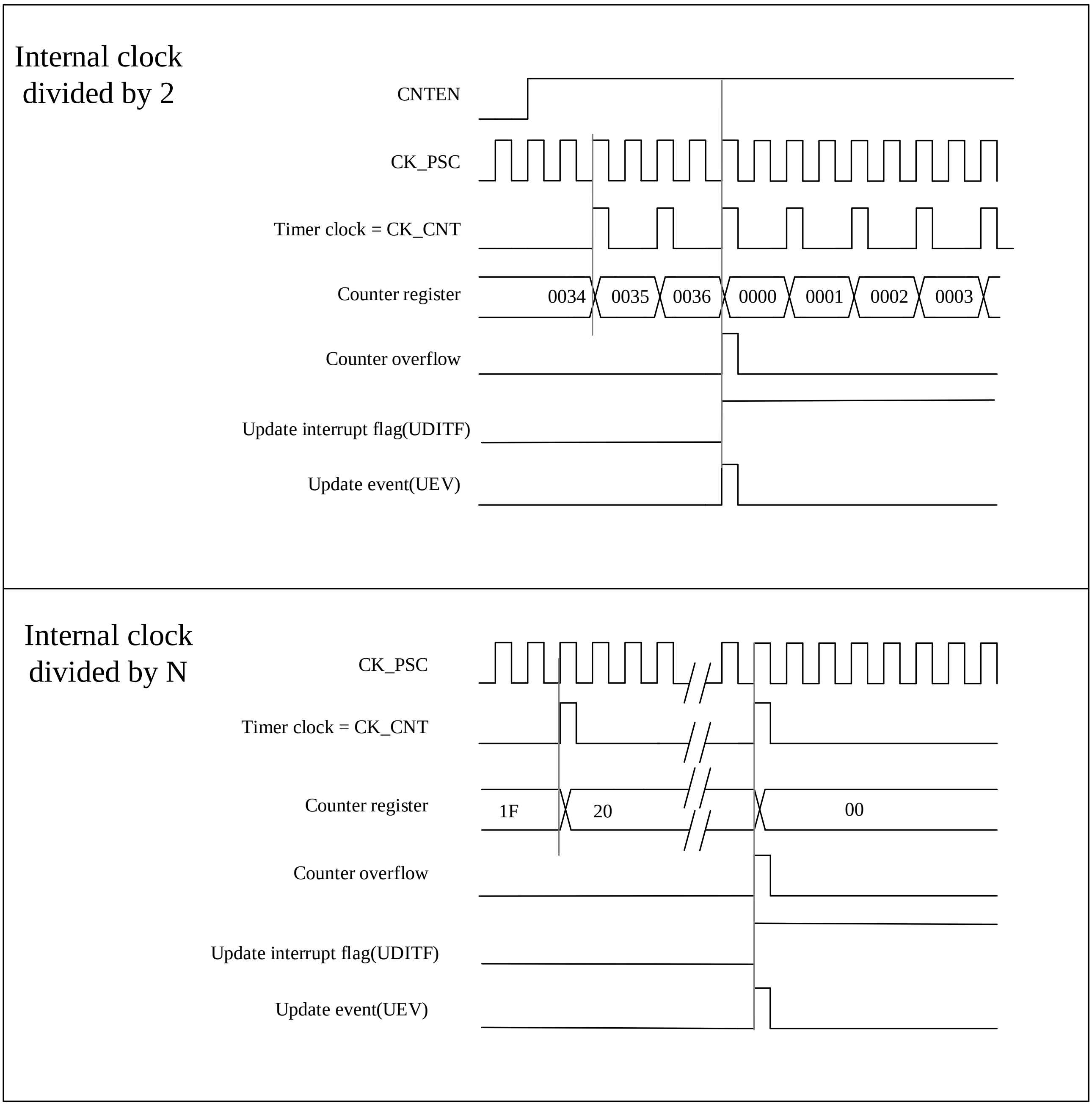

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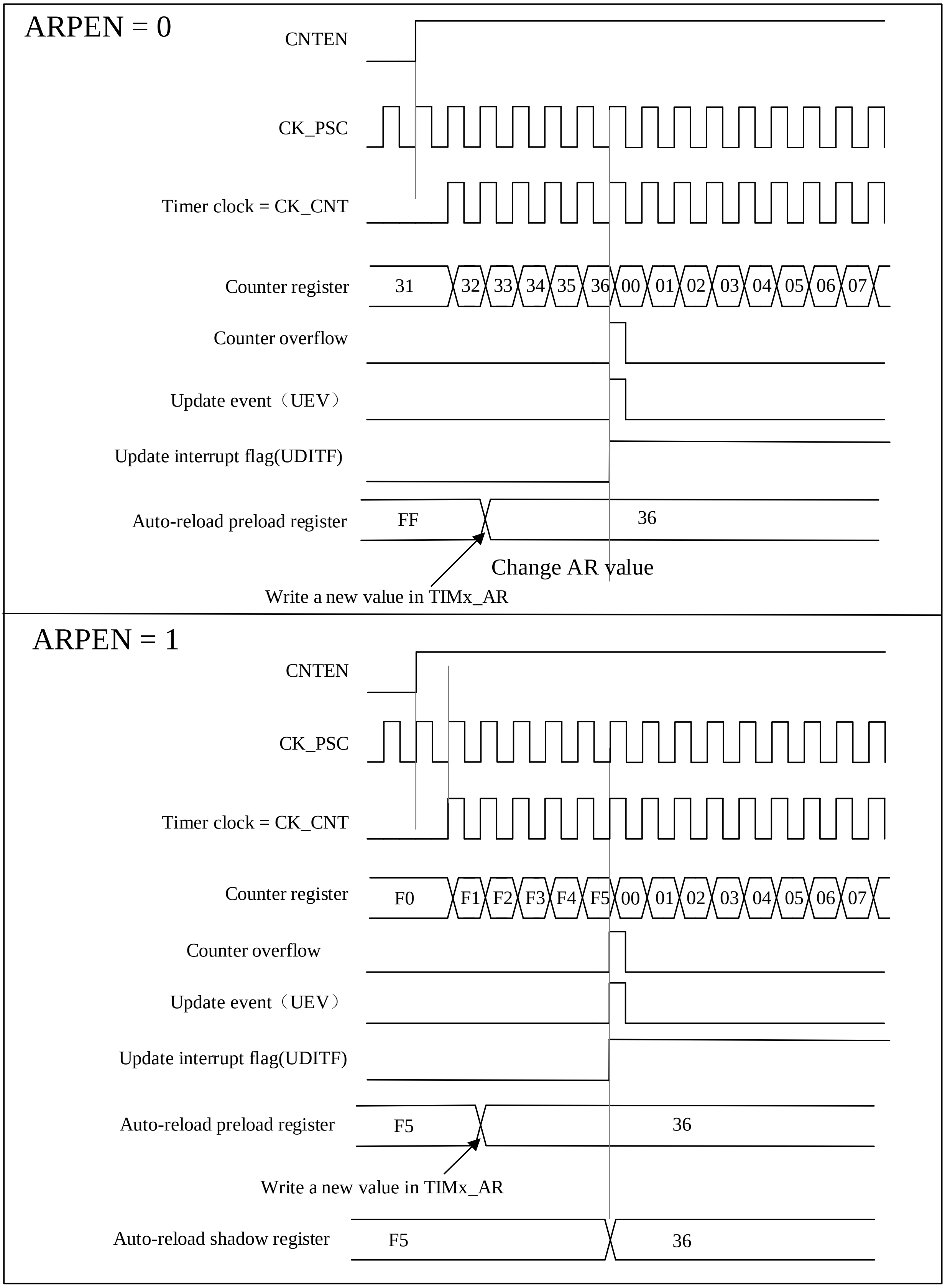
Figure 12-4 Timing Diagram of The Up-counting, Update Event When ARPEN = 0/1



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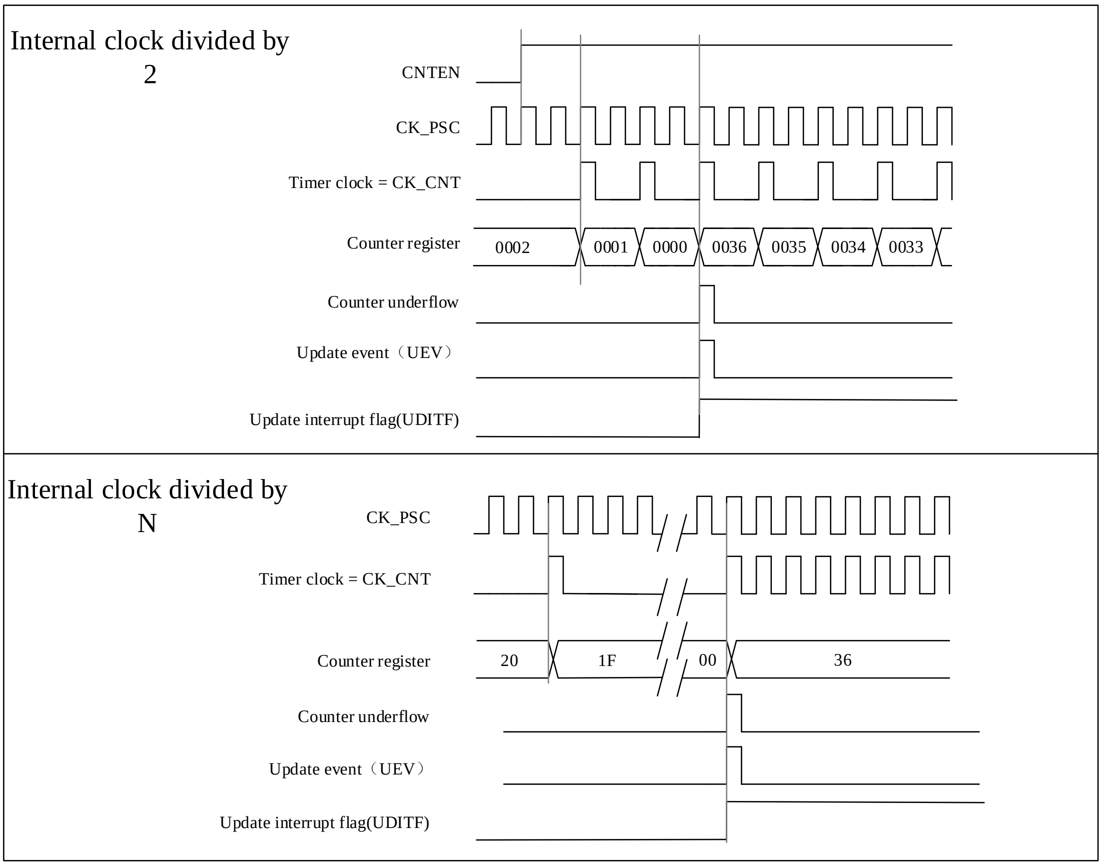
12.3.2.2 Down-counting mode

In down-counting mode, the counter will count from the value of the register TIMx_AR down to 0, then restart from the auto-reload value and generate a counter underflow event.

The process of configuring update events and updating registers in down-counting mode is the same as in up-counting mode, refer to Section 12.3.2.1.

The figure below shows some examples of the counter behavior and the update flags for different prescaler factors in the down-counting mode.

Figure 12-5 Timing Diagram of The Down-counting, Internal Clock Divided Factor = 2/N



12.3.2.3 Center-aligned mode

12.3.2.3.1 Center-aligned symmetric mode

In center-aligned symmetric mode, the counter counts from 0 to the value (TIMx_AR) – 1, a counter overflow event is generated. It then counts from the auto-reload value (TIMx_AR) down to 1 and generates a counter underflow event. Then the counter resets to 0 and starts counting up again.

In this mode, the TIMx_CTRL1.DIR direction bits cannot be written and the count direction is updated and specified by hardware. Center-aligned mode is active when the TIMx_CTRL1. CAMSEL bit is not equal to "00".

An update event can be generated at each counter overflows and at each counter underflows. Alternatively, an update event can also be generated by setting the TIMx_EVTGEN. UDGN bit (either by software or using a slave mode controller). In this case, the counter restarts from 0, and the prescaler counter also restarts from 0.

Note: if an update is generated due to a counter overflow, the auto-reload value will be updated before the counter

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is reload.

Figure 12-6 Timing Diagram of the Center-aligned, Internal Clock Divided Factor = 2/N

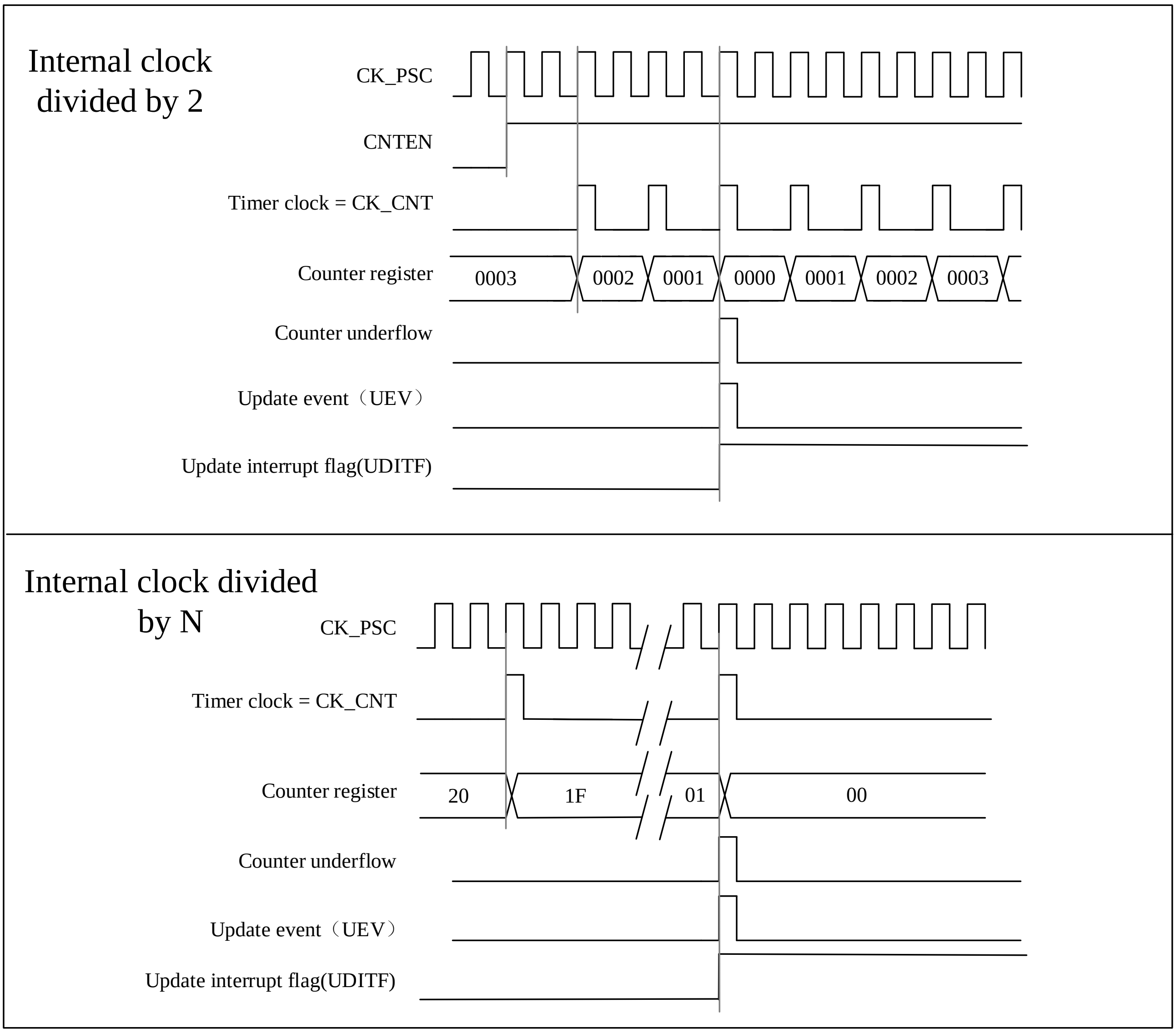

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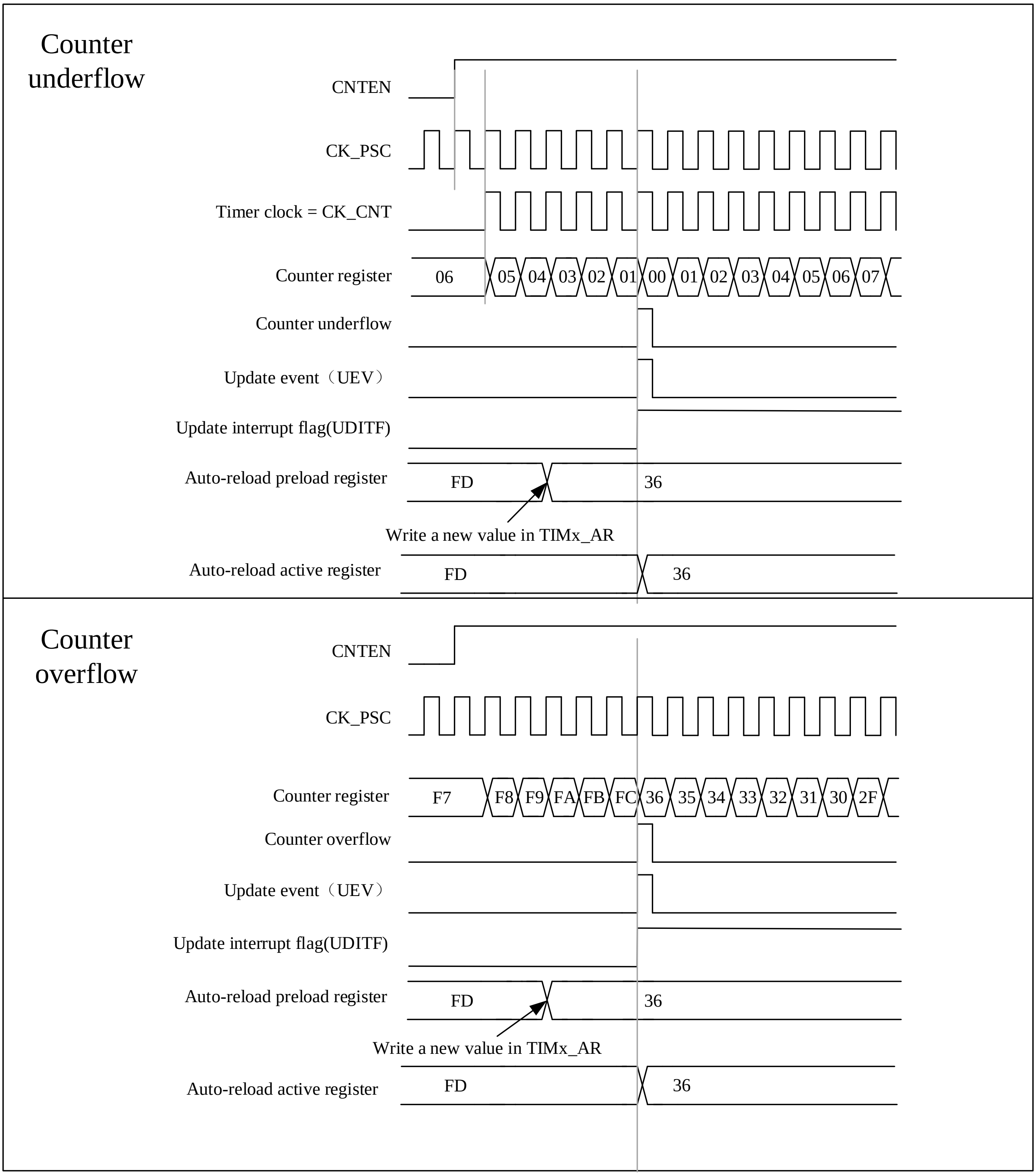
Figure 12-7 A Center-aligned Sequence Diagram That Includes Counter Overflows and Underflows (ARPEN = 1)



12.3.2.3.2 Center-aligned asymmetric mode

In center-aligned asymmetric mode (TIMx_CTRL1. ASYMMETRIC is 1 and TIMx_CTRL1.CAMSEL[1:0] is non-zero), the counter counts from 0 to the auto-reload value (TIMx_AR) – 1 and generates a counter overflow event, then counts from the auto-reload value down to 1 and generates a counter underflow event and then restarts counting from 0.

The TIMx_CTRL1.DIR cannot be written in this mode. It is updated by hardware and indicates the current direction

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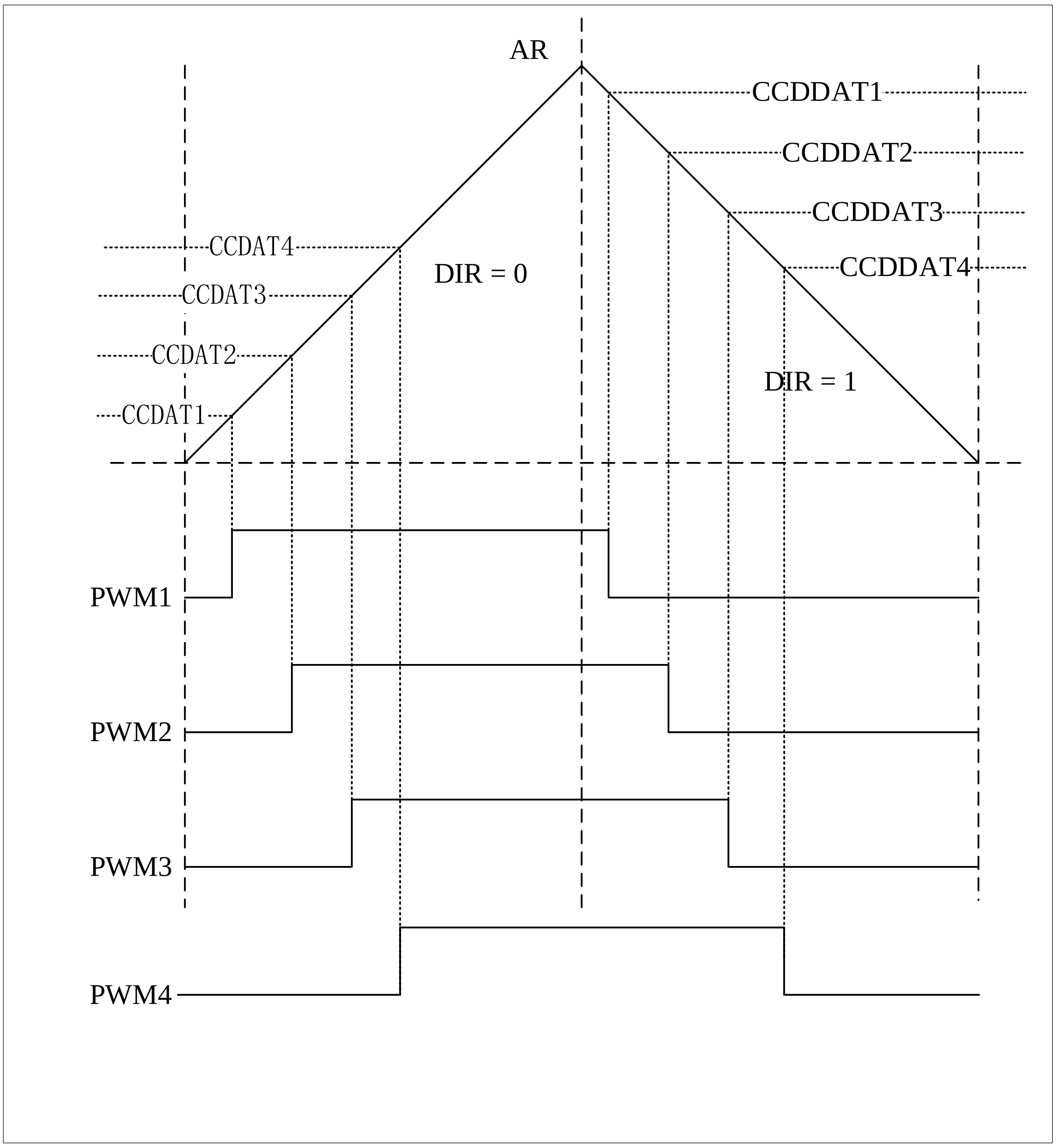
of the counter.

When the channel is not 1,2,3,4, the comparison value are compared with CCDATx. When the dead time generator is turned on, note that when DIR = 0, the dead time insertion point is at which the counter value is equal to CCDATx(x=1,2,3,4), and when DIR = 1, the dead time insertion point is at which the counter value is equal to CCDDATx(x=1,2,3,4).

An update event can be generated each time the counter overflows and each time the counter underflows. Alternatively, an update event can also be generated by setting the TIMx_EVTGEN. UDGN bit (either by software or using a slave mode controller). In this case, the counter restarts from 0, and the prescaler counter also restarts from 0.

Note: if an update is generated due to a counter overflow, the auto-reload value will be updated before the counter is reloaded.

Figure 12-8 The Output Waveform Corresponding to the Asymmetric Mode



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12.3.3 Repetition Counter

The basic unit of Section 12.3.1 describes the conditions for generating an update event (UEV). An update event (UEV) is actually only generated when the repetition counter reaches zero, which is valuable for generating PWM signals.

This means that data are transferred from the preload registers to the shadow registers every N+1 counter overflow or underflow, where N is the value in the TIMx_REPCNT.

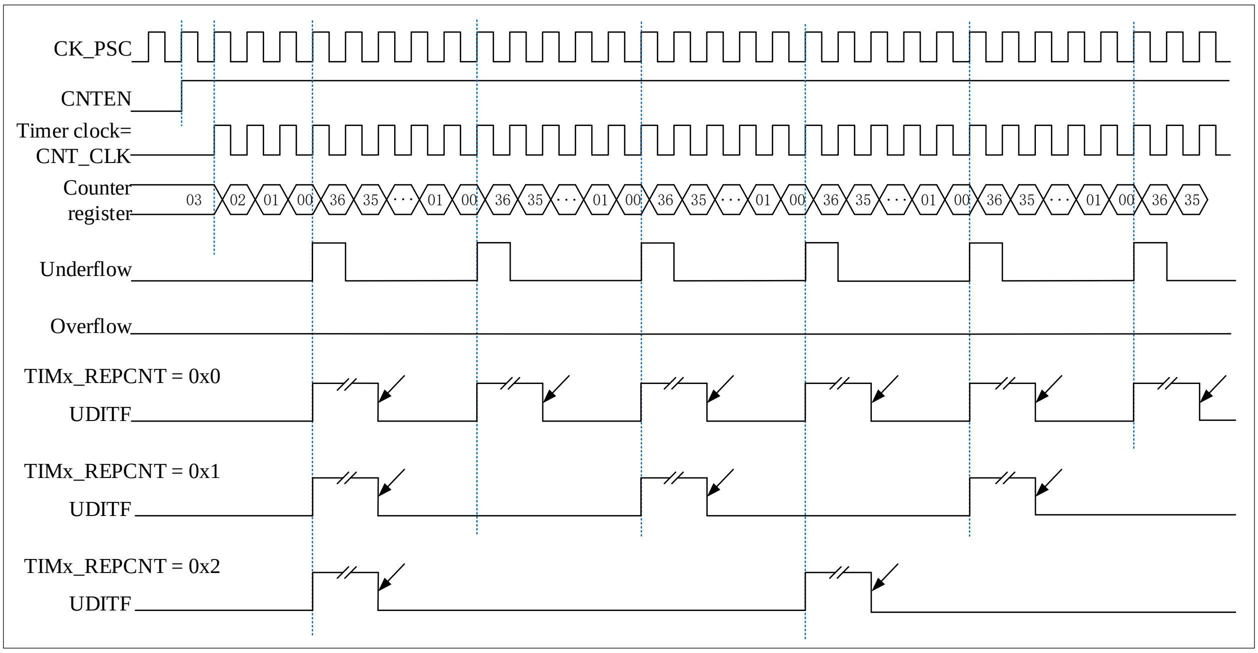
The repetition counter is decremented:

- In the up-counting mode, each time the counter reaches the maximum value, an overflow occurs.
- In down-counting mode, each time the counter decrements to the minimum value, an underflow occurs.
- In center-aligned mode, each time the counter overflows or underflows.

Its repetition rate is defined by the value of the TIMx_REPCNT register.

Repetition counters feature automatic reloading. The update event (generated by setting TIMx_EVTGEN.UDGN or hardware through slave mode controller) occurs immediately, regardless of the value of the repeatition counter.

Figure 12-9 Repeat Count Sequence Diagram in Down-counting Mode



Software clear

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Figure 12-10 Repeat Count Sequence Diagram in Up-counting Mode

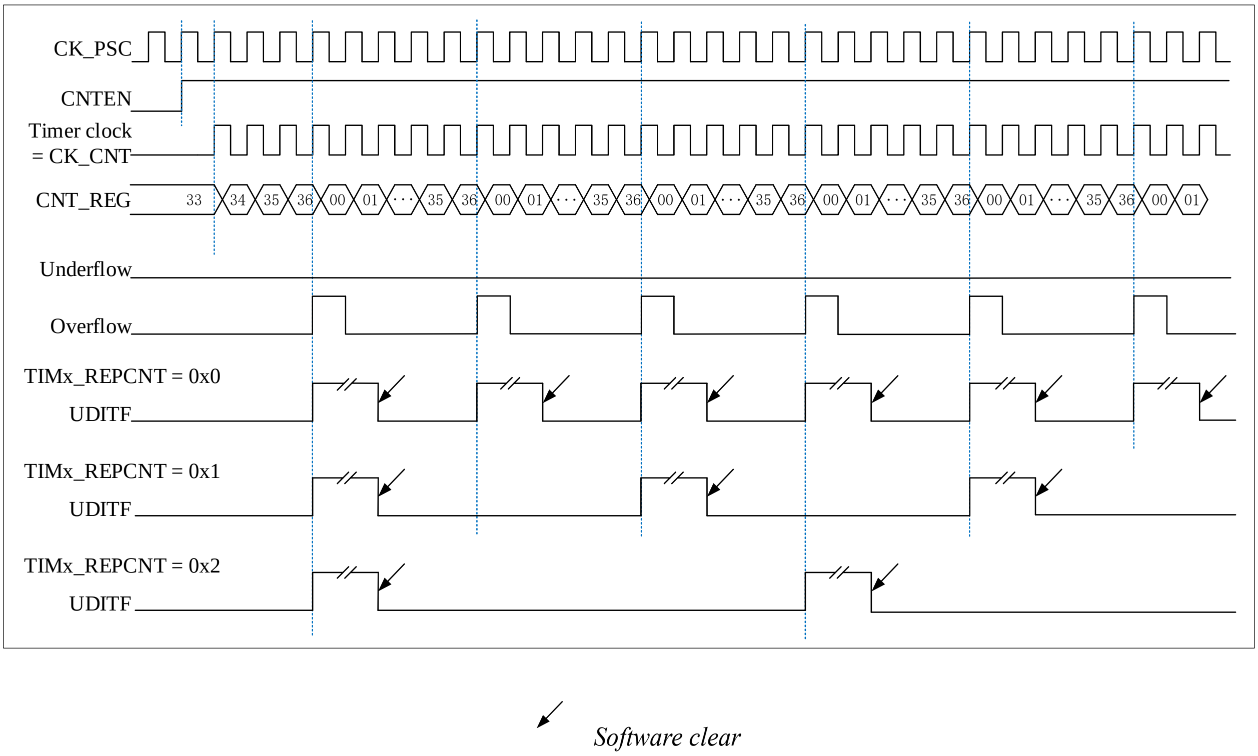
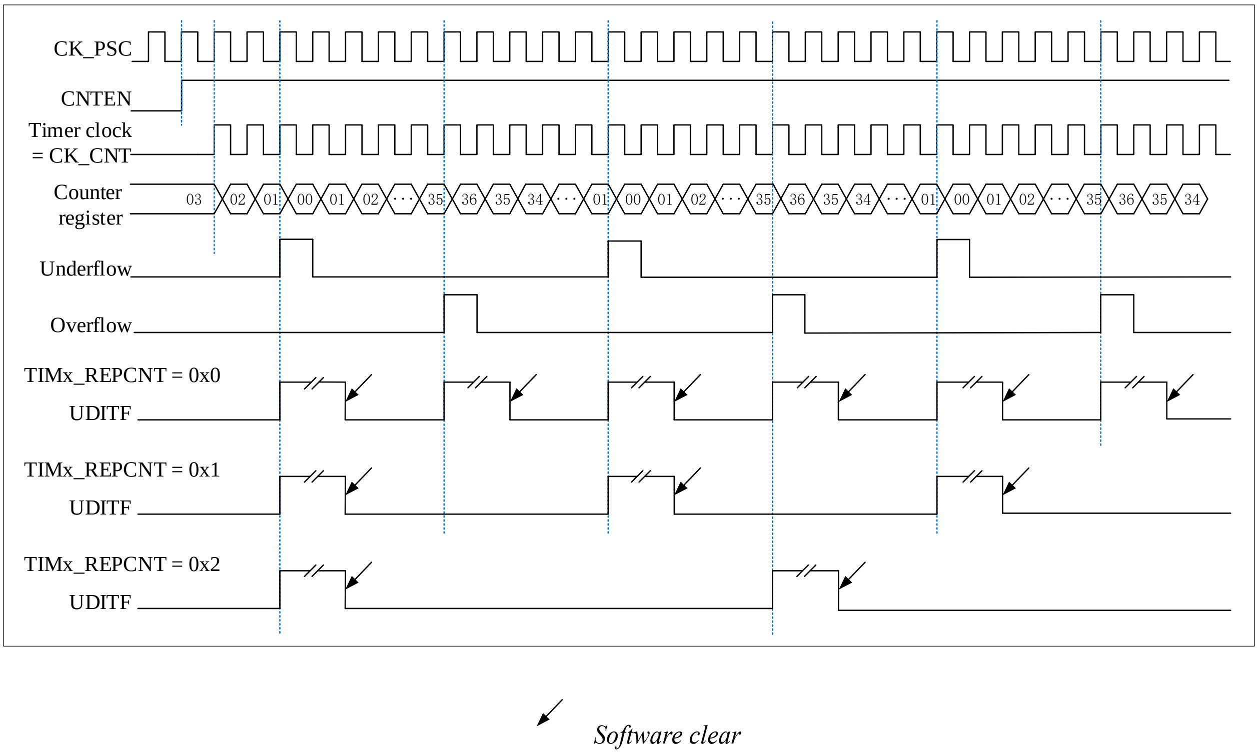


Figure 12-11 Repeat Count Sequence Diagram in Center-aligned Mode



12.3.4 Clock Selection

- The internal clock of Advanced-control timer: CK_INT

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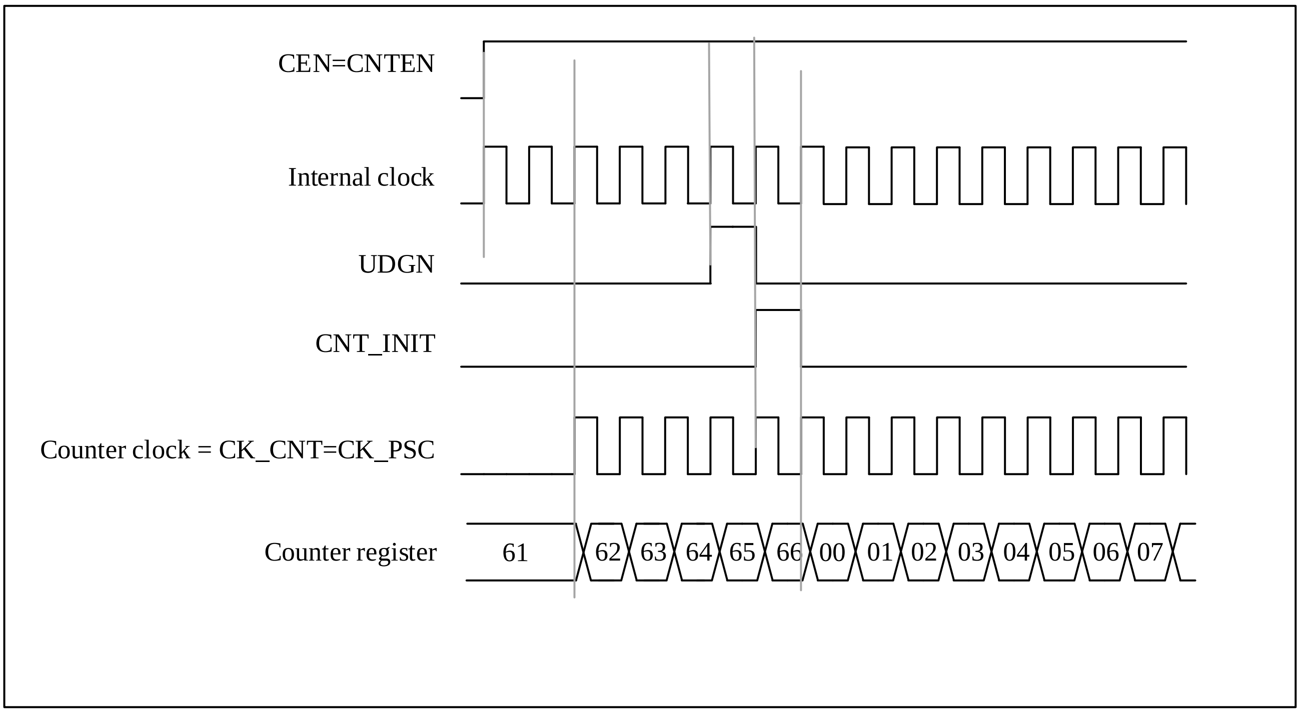
- Two kinds of external clock mode:
  - External input pin
  - External trigger input ETR
- Internal trigger input (ITRx): one timer is used as a prescaler for another timer.

12.3.4.1 Internal clock source (CK_INT)

When the TIMx_SMCTRL.SMSEL is equal to "0000", the slave mode controller is disabled. The three control bits (TIMx_CTRL1.CNTEN, TIMx_CTRL1.DIR, TIMx_EVTGEN.UDGN) can only be changed by software (except TIMx_EVTGEN. UDGN, which remains cleared automatically). It is provided that the TIMx_CTRL1.CNTEN bit is written as '1' by software, the clock source of the prescaler is provided by the internal clock CK_INT.

Figure 12-12 Control Circuit in Normal Mode, Internal Clock Divided By 1



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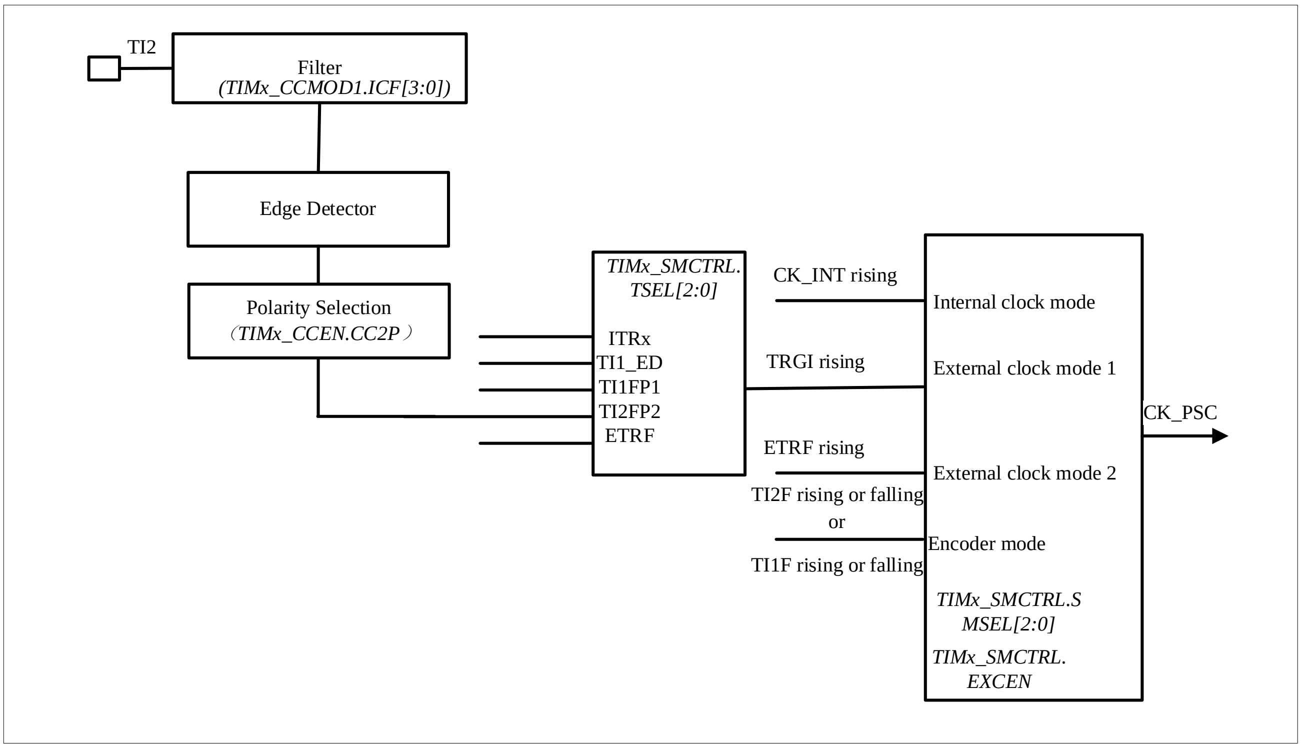
12.3.4.2 External clock source mode 1

Figure 12-13 TI2 External Clock Connection Example



This mode is selected by configuring TIMx_SMCTRL.SMSEL=0111. The counter can be configured to count on the rising or falling edge of the clock at the selected input.

For example, to configure up-counting mode to count on the rising edge of the clock at the T12 input, the configuration steps are as follows:

- Configure TIMx_CCMOD1.CC2SEL equal to ‘01’, CC2 channel is configured as input, IC2 is mapped to TI2
- Configure TIMx_CCEN.CC2P equal to ‘0’, select clock rising edge polarity
- To select input filter bandwidth by configuring TIMx_CCMOD1.IC2F[3:0] (if filter is not needed, keep IC2F bit at ‘0000’)
- Configure TIMx_SMCTRL.SMSEL equal to ‘0111’, select timer external clock mode 1
- Configure TIMx_SMCTRL.TSEL equal to ‘110’, select TI2 as the trigger input source
- Configure TIMx_CTRL1.CNTEN equal to ‘1’ to start the counter

Note: the capture prescaler is not used for triggering, so it does not need to be configured

When the rising edge of the timer clock occurs at TI2=1, the counter counts once and the TIMx_STS .TITF flag is set.

The delay between the rising edge of TI2 and the actual clock of the counter depends on the resynchronization circuit at the input of TI2.

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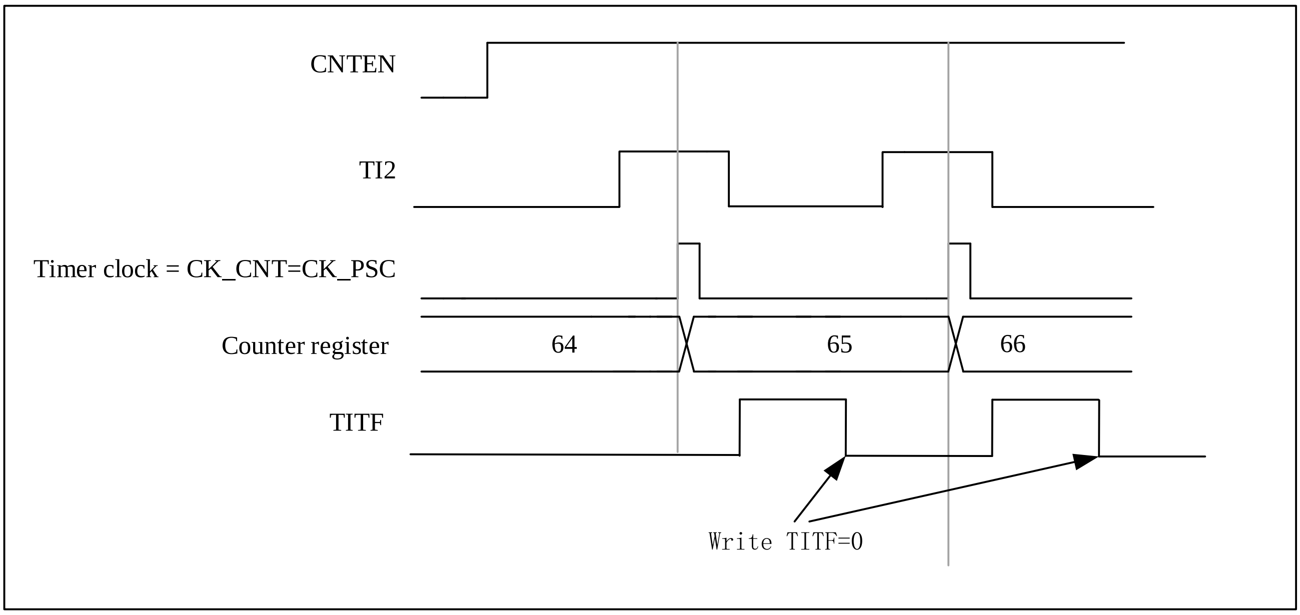
Figure 12-14 Control Circuit in External Clock Mode 1

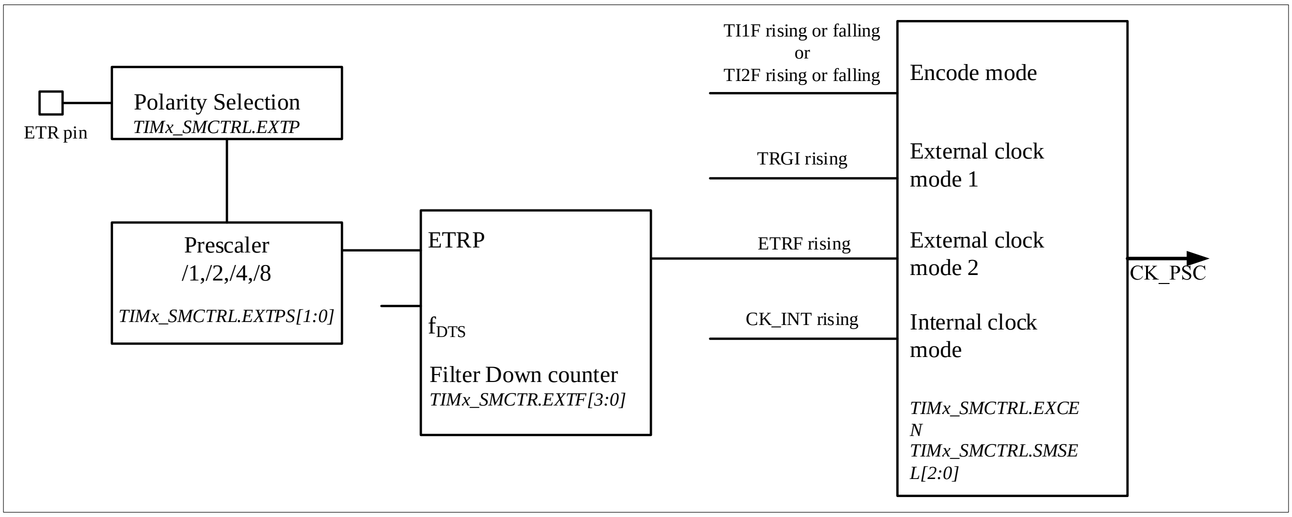


12.3.4.3 External clock source mode 2

This mode is set by configuring TIMx_SMCTRL .EXCEN equal to 1. The counter can count on every rising or falling edge of the external trigger input ETR.

The following figure is a schematic diagram of the external trigger input module in external clock source mode 2.

Figure 12-15 External Trigger Input Block Diagram



For example, use the following configuration steps to make the upcounter count every 2 rising edges on ETR.

- Since no filter is needed in this case, make TIMx_SMCTRL .EXTF[3:0] equal to '0000'
- Configure the prescaler by making TIMx_SMCTRL.EXTPS[1:0] equal to '01'
- Select the polarity on ETR pin by setting TIMx_SMCTRL.EXTP equal to '0', the rising edge of ETR is valid
- External clock mode 2 is selected by setting TIMx_SMCTRL .EXCEN equal to '1'
- Turn on the counter by setting TIMx_CTRL1. CNTEN equal to '1'

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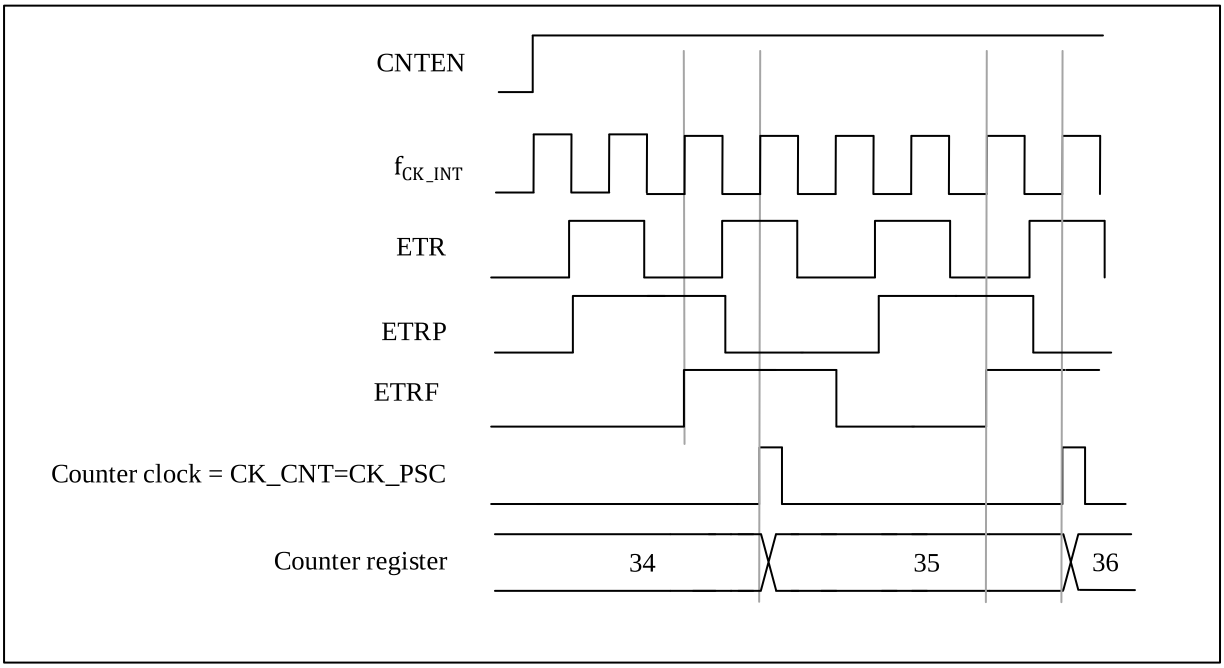
The counter counts every 2 rising edges of ETR. The delay between the rising edge of ETR and the actual clock of the counter is due to a resynchronization circuit on the ETRP signal.

Figure 12-16 Control Circuit in External Clock Mode 2



12.3.5 Capture/Compare Channels

The capture/compare channels include capture/compare registers and shadow registers. The input stage consists of digital filters, multiplexers and prescalers. The output section includes comparators and output controls.

The input signal TIx is sampled and filtered to generate the signal TIxF. A signal (TIxF_rising or TIxF_falling) is then generated by the edge detector of the polarity select function, the polarity of which is selected by the TIMx_CCEN.CCxP bits. This signal can be used as a trigger input for the slave mode controller. At the same time, the signal ICx is sent to the capture register after frequencyprecaler. The following figure shows a block diagram of a capture/compare channel.

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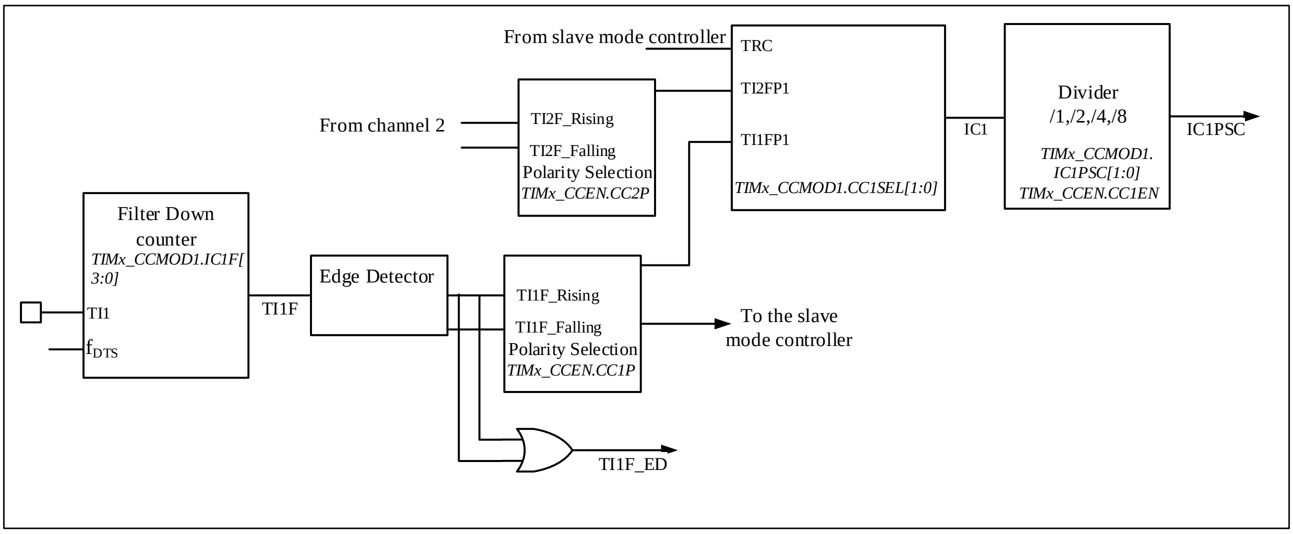
Figure 12-17 Capture/Compare Channel (Example: Channel 1 Input Stage)



The output stage generates an intermediate waveform OCxRef (active high) as reference. The polarity acts at the end of the chain.

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Figure 12-18 Capture/Compare Channel 1 Main Circuit

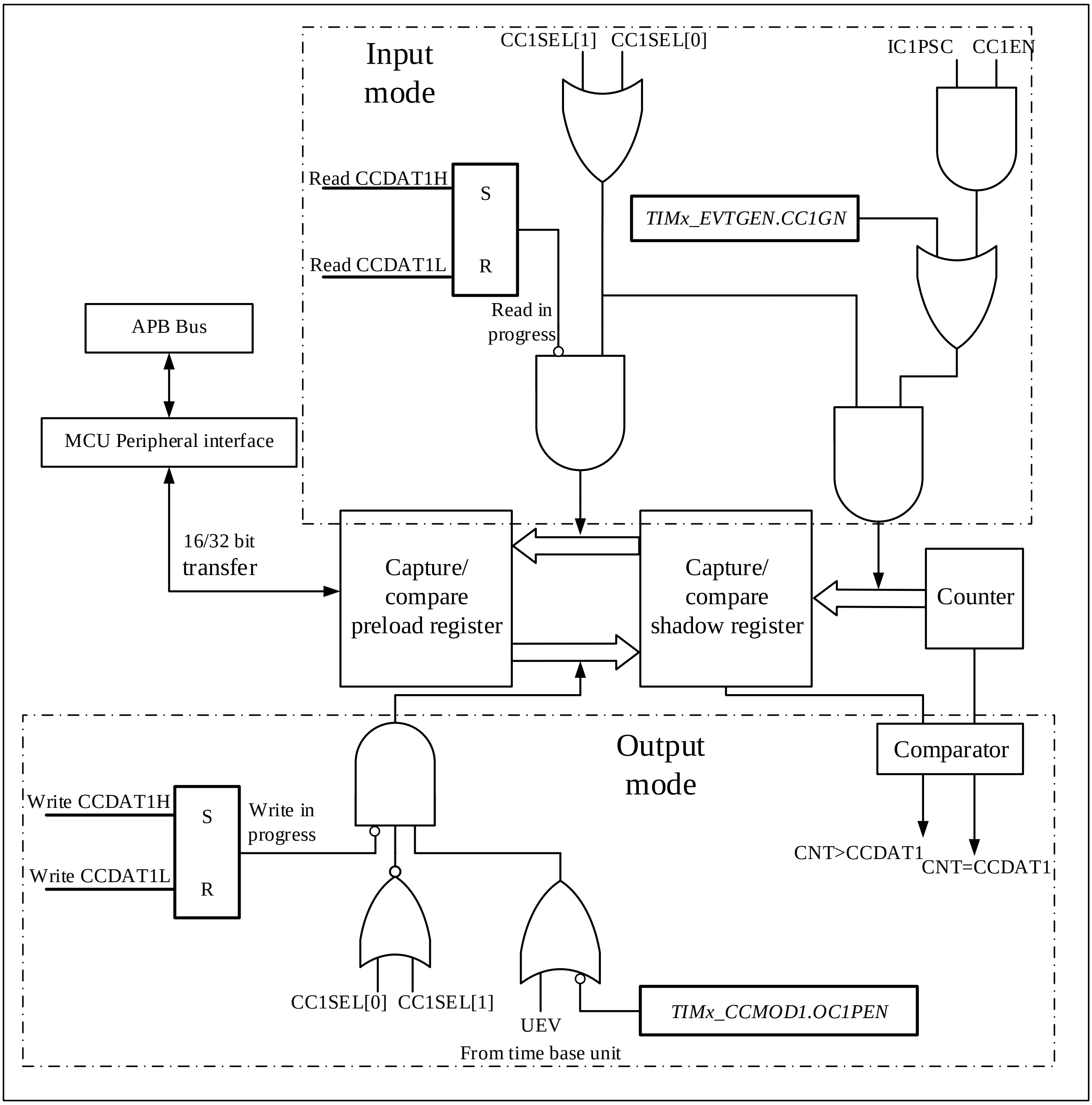

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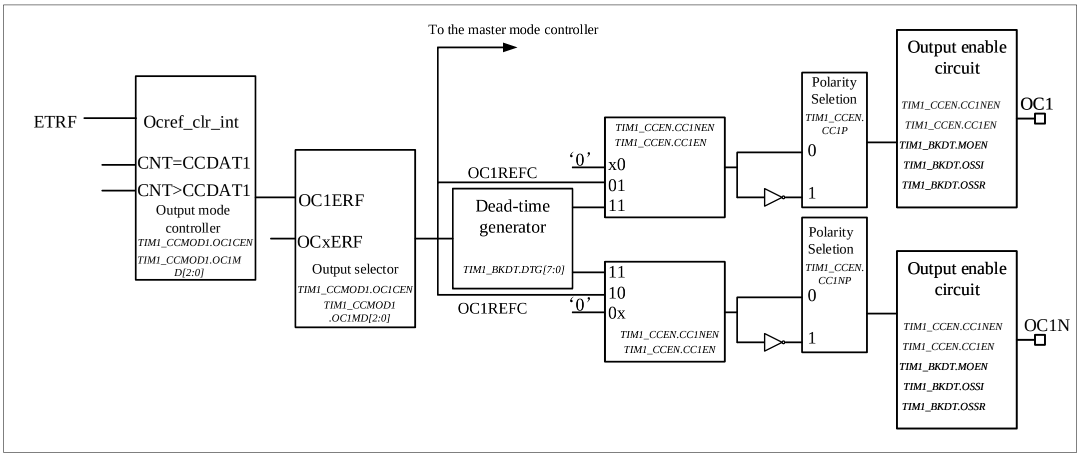
Figure 12-19 Output Part of Channelx (Take Channel 1 as Example)



Reads and writes operations always access the preload registers when capturing/comparing. The two specific working processes are as follows:

In capture mode, the capture is actually done in the shadow register, and then the value in the shadow register is copied into the preload register.

In compare mode, the value of the preload register is copied into the shadow register, which is compared with the counter.

12.3.6 Input Capture Mode

In input capture mode, the TIMx_CCDATx registers are used to latch the counter value after the ICx signal detects.

There is a capture interrupt flag TIMx_STS.CCxITF, which can trigger an interrupt or DMA request if the corresponding interrupt enable is set.

The TIMx_STS. CCxITF bit is set by hardware when a capture event occurs and is cleared by software or by reading the TIMx_CCDATx register.

The overcapture flag TIMx_STS.CCxOCF is set equal to 1 when the counter value is captured in the TIMx_CCDATx register and TIMx_STS.CC1ITF is already set. Unlike the former, TIMx_STS.CCxOCF is cleared by writing 0 to it.

To achieve a rising edge of the TI1 input to capture the counter value into the TIMx_CCDAT1 register, the configuration flow is as follows:

- To select a valid input:

  Configure TIMx_CCMOD1.CC1SEL to '01'. At this time, the input is the CC1 channel, and IC1 is mapped to TI1.

- Define the input filter duration required for programming:

  Define the sampling frequency of the TI1 input and the length of the digital filter by configuring the TIMx_CCMODx.ICxF bits. Example: If the input signal jitters up to 5 internal clock cycles, we must choose a filter duration longer than these 5 clock cycles. When 8 consecutive samples (sampled at $f_{TIM1FILTCLK}$ frequency) with the new level are detected, we can validate the transition on TI1. Then configure TIMx_CCMOD1. IC1F to '1xxx'.

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- Select the rising edge as the valid transition polarity on the TI1 channel by configuring TIMx_CCEN .CC1P=0.
- Configure the input prescaler. In this example, configure TIMx_CCMOD1.IC1PSC= '00' to disable the prescaler because we want to capture every valid transition.
- Enable capture by configuring TIMx_CCEN. CC1EN = '1'.

If you want to enable DMA request, you can configure TIMx_DINTEN.CC1DEN=1.If you want enable related interrupt request, you can configureTIMx_DINTEN.CC1IEN bit=1

12.3.7 PWM Input Mode

There are some differences between PWM input mode and normal input capture mode, including:

- Two ICx signals are mapped to the same TIx input.
- The two ICx signals are active on edges of opposite polarity.
- Select one of two TIxFP signals as trigger input.
- The slave mode controller is configured in reset mode.

For example, the following configuration flow can be used to know the period and duty cycle of the PWM signal on TI1 (It depends on the frequency of CK_INT and the value of the prescaler).

- Configure TIMx_CCMOD1.CC1SEL equal to '01' to select TI1 as valid input for TIMx_CCDAT1.
- Configure TIMx_CCEN.CC1P equal to '0' to select the active polarity of filtered timer input 1(TI1FP1), active on the rising edge.
- Configure TIMx_CCMOD1.CC2SEL equal to '10' select TI1 as valid input for TIMx_CCDAT2.
- Configure TIMx_CCEN.CC2P equal to 1 to select the valid polarity of filtered timer input 2(TI1FP2), active on the falling edge.
- Configure TIMx_SMCTRL.TSEL=101 to select filtered timer input 1 (TI1FP1) as valid trigger input.
- Configure TIMx_SMCTRL.SMSEL=0100 to configure the slave mode controller to reset mode.
- Configure TIMx_CCEN. CC1EN=1 and TIMx_CCEN.CC2EN=1 to enable capture.

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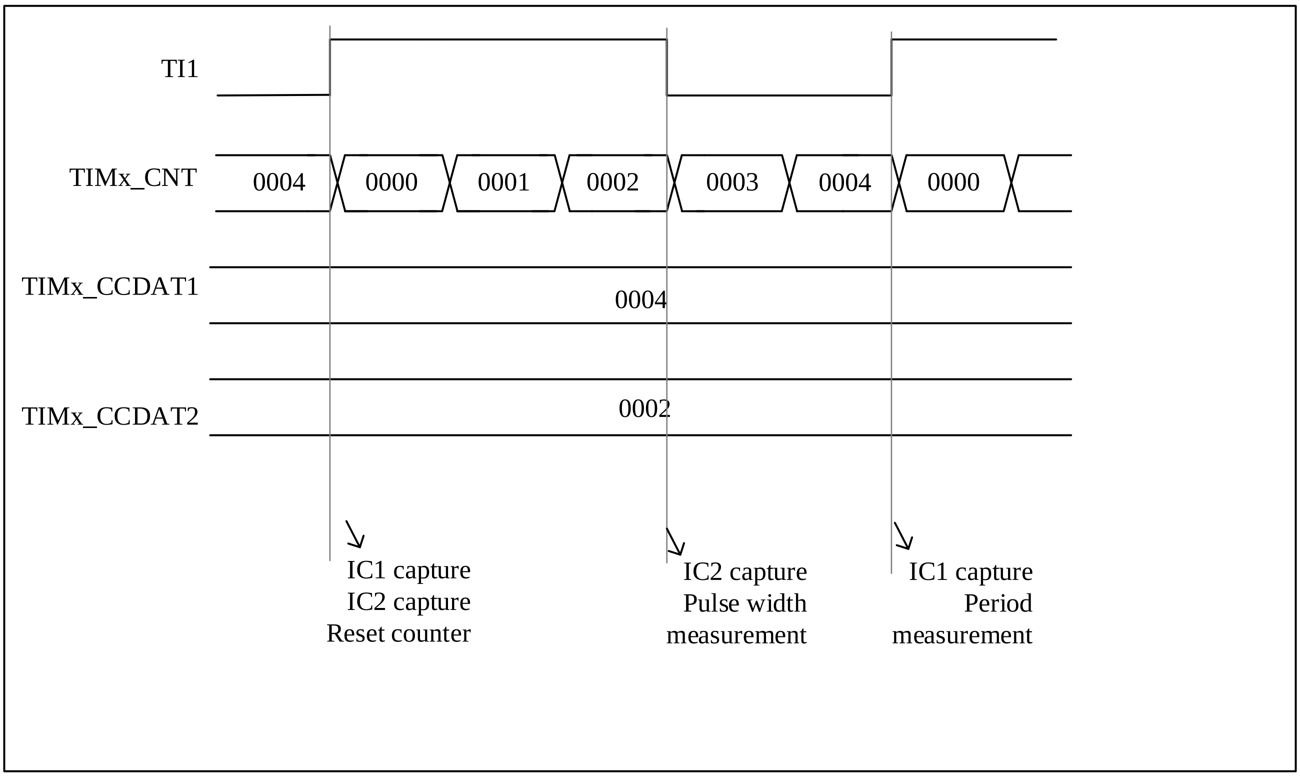
Figure 12-20 PWM Input Mode Timing



Because of only filter timer input 1 (TI1FP1) and filter timer input 2 (TI2FP2) are connected to the slave mode controller, the PWM input mode can only be used with the TIMx_CH1/TIMx_CH2 signals.

12.3.8 Forced Output Mode

In output mode (TIMx_CCMODx.CCxSEL=00), software can force output compare signals to active or inactive level directly.

User can set TIMx_CCMODx. OCxMD=101 to force the output compare signal to active level. And the OCxREF will be forced high, OCx get opposite value to CCxP polarity bit. On the other hand, user can set TIMx_CCMODx. OCxMD=100 to force the output compare signal to low level.

The values of the TIMx_CCDATx shadow register and the counter still comparing with each other in this mode.

The comparison between the output compare register TIMx_CCDATx and the counter TIMx_CNT has no effect on OCxREF. And the flag still can be set. Therefore, the interrupt and DMA requests still can be sent.

12.3.9 Output Compare Mode

User can use this mode to control the output waveform, or to indicate that a period of time has elapsed.

When the capture/compare register and the counter have the same value, the output compare function's operations are as follow:

- TIMx_CCMODx.OCxMD is for output compare mode, and TIMx_CCEN.CCxP is for output polarity. When the compare matches, if set TIMx_CCMODx.OCxMD=000, the output pin will keep its level;if set TIMx_CCMODx.OCxMD=001, the output pin will be set active;if set TIMx_CCMODx.OCxMD=010, the

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output pin will be set inactive;if set TIMx_CCMODx.OCxMD=011, the output pin will be set to toggle.

- Set TIMx_STS.CCxITF.
- If user set TIMx_DINTEN.CCxIEN, a corresponding interrupt will be generated.
- If user set TIMx_DINTEN.CCxDEN and set TIMx_CTRL2.CCDSEL to select DMA request, and DMA request will be sent.

The TIMx_CCDATx registers can be programmed with or without preload registers using the TIMx_CCMODx.OCxPEN register.

The time resolution is one count period of the counter.

In one-pulse mode, the output compare mode can also be used to output a single pulse.

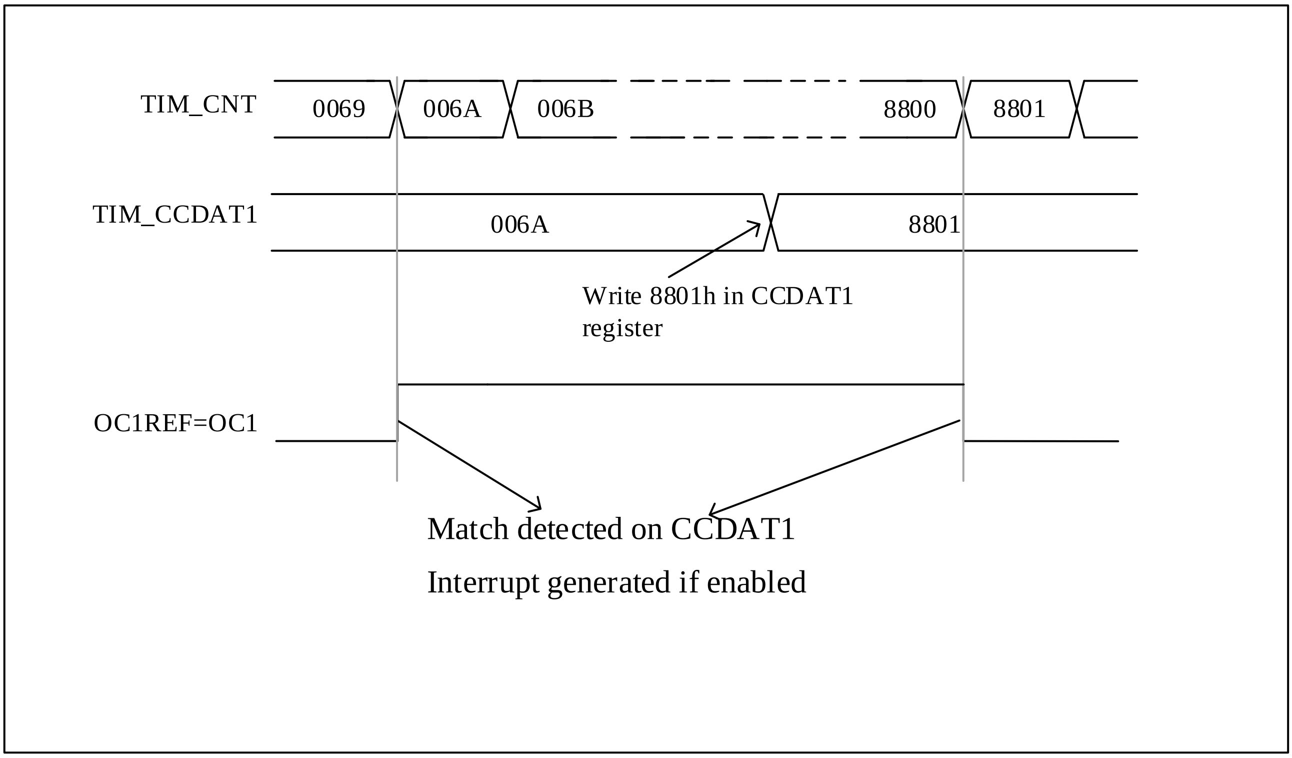
Here are the configuration steps for output compare mode:

- First of all, user should select the counter clock.
- Secondly, write the desired data in the TIMx_AR and TIMx_CCDATxregisters.
- If user need to generate an interrupt, set TIMx_DINTEN.CCxIEN.
- Then select the output mode by set TIMx_CCEN.CCxP, TIMx_CCMODx.OCxMD, TIMx_CCEN.CCxEN, etc.
- At last, set TIMx_CTRL1.CNTEN to enable the counter.

User can update the output waveform by writting TIMx_CCDATx at any time, as long as the preload register is not enabled. Otherwise the TIMx_CCDATx shadow register will be updated at the next update event.

Here is an example.

Figure 12-21 Output Compare Mode, Toggle on OC1



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12.3.10 PWM Mode

Pulse width modulation mode is used to generate a signal with a frequency determined by the value of the TIMx_AR register and a duty cycle determined by the value of the TIMx_CCDATx register. And depending on the value of TIMx_CTRL1.CAMSEL, the TIM can generate PWM signal in edge-aligned mode or center-aligned mode.

User can select PWM mode 1 or PWM mode 2 by setting TIMx_CCMODx. OCxMD=110 or setting TIMx_CCMODx. OCxMD=111. To enable preload register, user must set corresponding TIMx_CCMODx.OCxPEN, and then set TIMx_CTRL1.ARPEN to auto-reload preload register eventually.

User can program polarity of OCx by setting TIMx_CCEN.CCxP. On the other hand, to enable the output of OCx, user need to set the combination of the value of CCxEN, CCxNEN, MOEN, OSSI, and OSSR in TIMx_CCEN and TIMx_BKDT.

The values of TIMx_CNT and TIMx_CCDATx are always compared with each other when the TIM is under PWM mode.

Only when an update event occurs, the preload register will be transferred to the shadow register. Therefore user must reset all the registers by setting TIMx_EVTGEN.UDGN before the counter starts counting.

12.3.10.1 PWM center-aligned mode

If user set TIMx_CTRL1.CAMSEL equal to 01, 10 or 11, the PWM center-aligned mode will be active. The setting of the compare flag depends on the value of TIMx_CTRL1.CAMSEL. There are three kinds of situation that the compare flag is set, only when the counter counts up, only when the counter counts down, or both when the counter counts up and counts down. User should not modified TIMx_CTRL1.DIR by software, it is updated by hardware.

Examples of center-aligned PWM waveforms is as follow, and the setting of the waveform are: TIMx_AR=8, PWM mode 1, the compare flag is set when the counter counts down corresponding to TIMx_CTRL1. CAMSEL=01.

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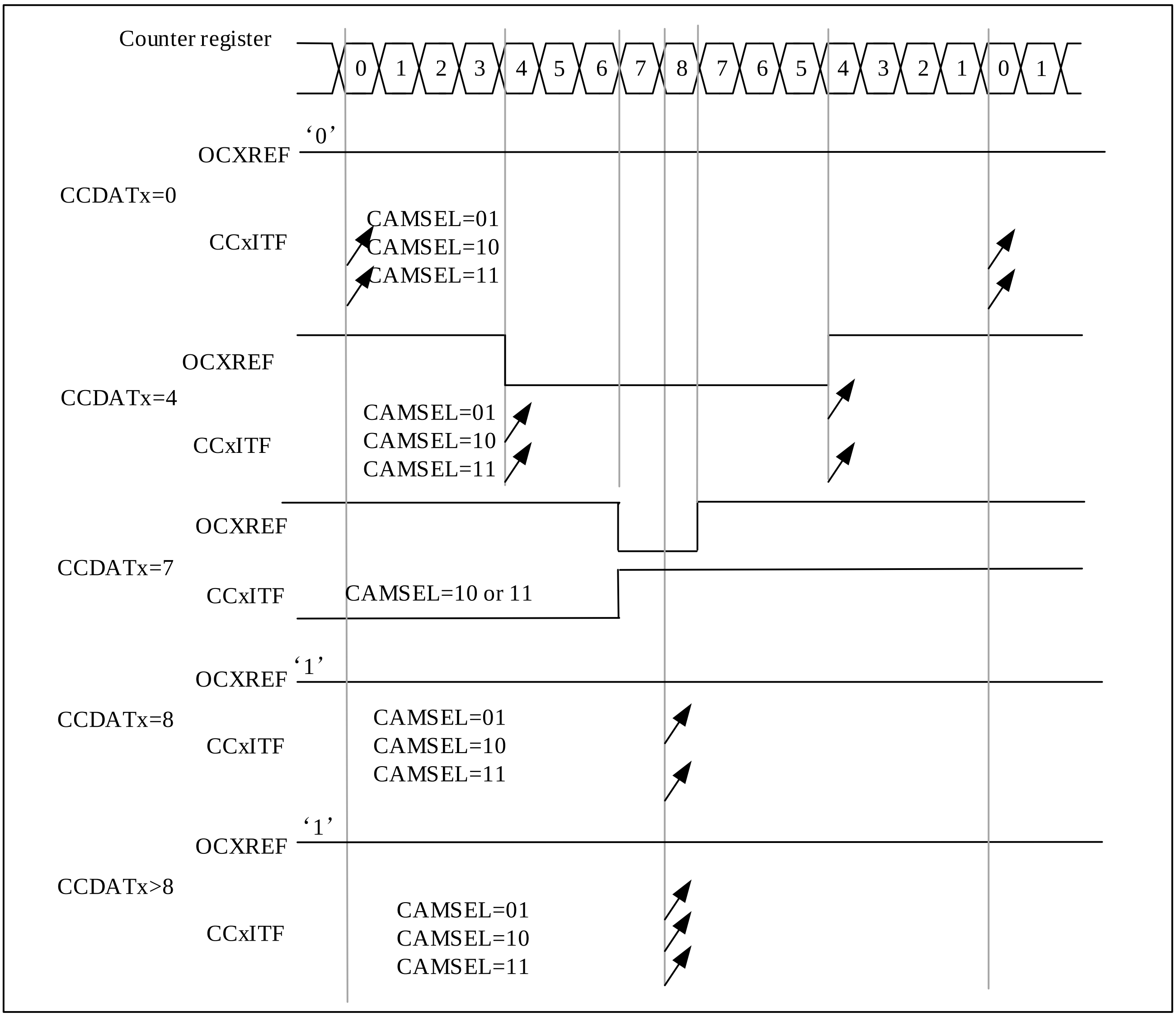
Figure 12-22 Center-aligned PWM Waveform (AR=8)



When using center-aligned mode, users should pay attention to the following considrations:

- It depends on the value of TIMx_CTRL1.DIR that the counter counts up or down. Cautions that the DIR and CAMSEL bits should not be changed at the same time.
- User should not write the counter while running in center-aligned mode, otherwise it will cause unexpected results. Here are some example:
  - If the value written into the counter is 0 or is the value of TIMx_AR, the direction will be updated but the update event will not be generated.
  - If the value written into the counter is greater than the value of auto-reload, the direction will not be updated.
- For safety reasons, it is recommended that users set TIMx_EVTGEN.UDGN to generate an update by software before starting the counter, and do not write the counter while it is running.

12.3.10.2 PWM center-aligned asymmetric mode

About PWM center-aligned asymmetric mode, refer to Section 12.3.2.3.2.

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12.3.10.3 PWM edge-aligned mode

There are two kinds of configuration in edge-aligned mode, up-counting and down-counting.

- **Up-counting**

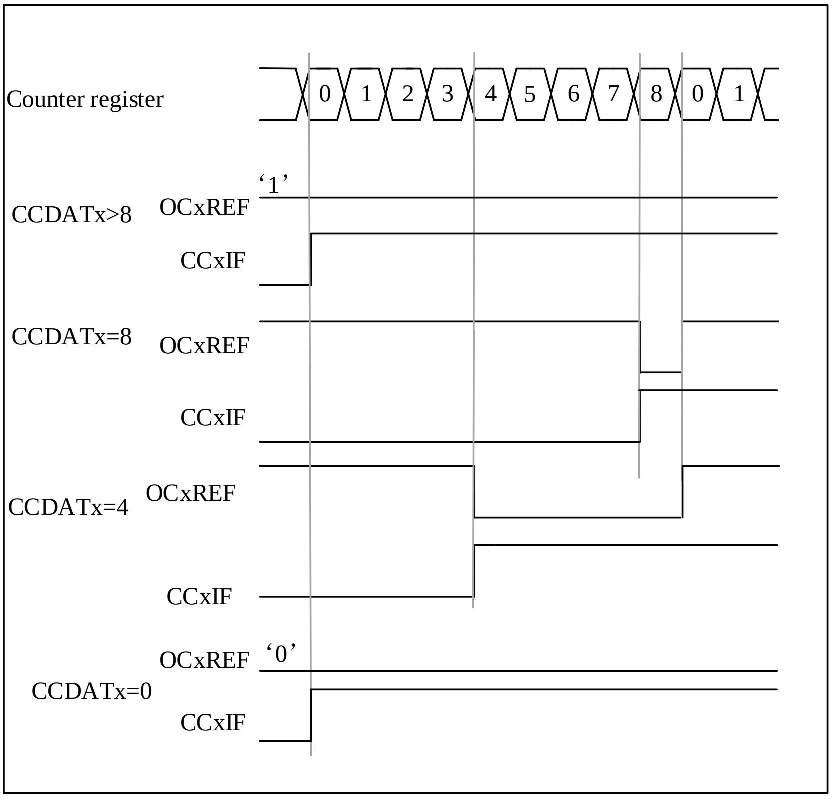
User can set TIMx_CTRL1.DIR=0 to make counter count up.

Example for PWM mode1:

When TIMx_CNT < TIMx_CCDATx, the reference PWM signal OCxREF is high. Otherwise it will be low. If the compare value in TIMx_CCDATx is greater than the auto-reload value, the OCxREF will remains 1. Conversely, if the compare value is 0, the OCxREF will remains 0.

When TIMx_AR=8, the PWM waveforms are as follows.

Figure 12-23 Edge-aligned PWM Waveform (APR=8)



- **Down-counting**

User can set TIMx_CTRL1.DIR=1 to make counter counts down.

Example for PWM mode1:

When TIMx_CNT > TIMx_CCDATx, the reference PWM signal OCxREF is low. Otherwise it will be high. If the compare value in TIMx_CCDATx is greater than the auto-reload value, the OCxREF will remains 1.

Note: if the n_{th} PWM cycle CCDATx shadow register >= AR value, the shadow register value of CCDATx in the $(n+1)_{th}$ PWM cycle is 0. At the moment when the counter is 0 in the $(n+1)_{th}$ PWM cycle, although the value of the counter = CCDATx shadow register = 0 and OCxREF = '0', no compare event will be generated.

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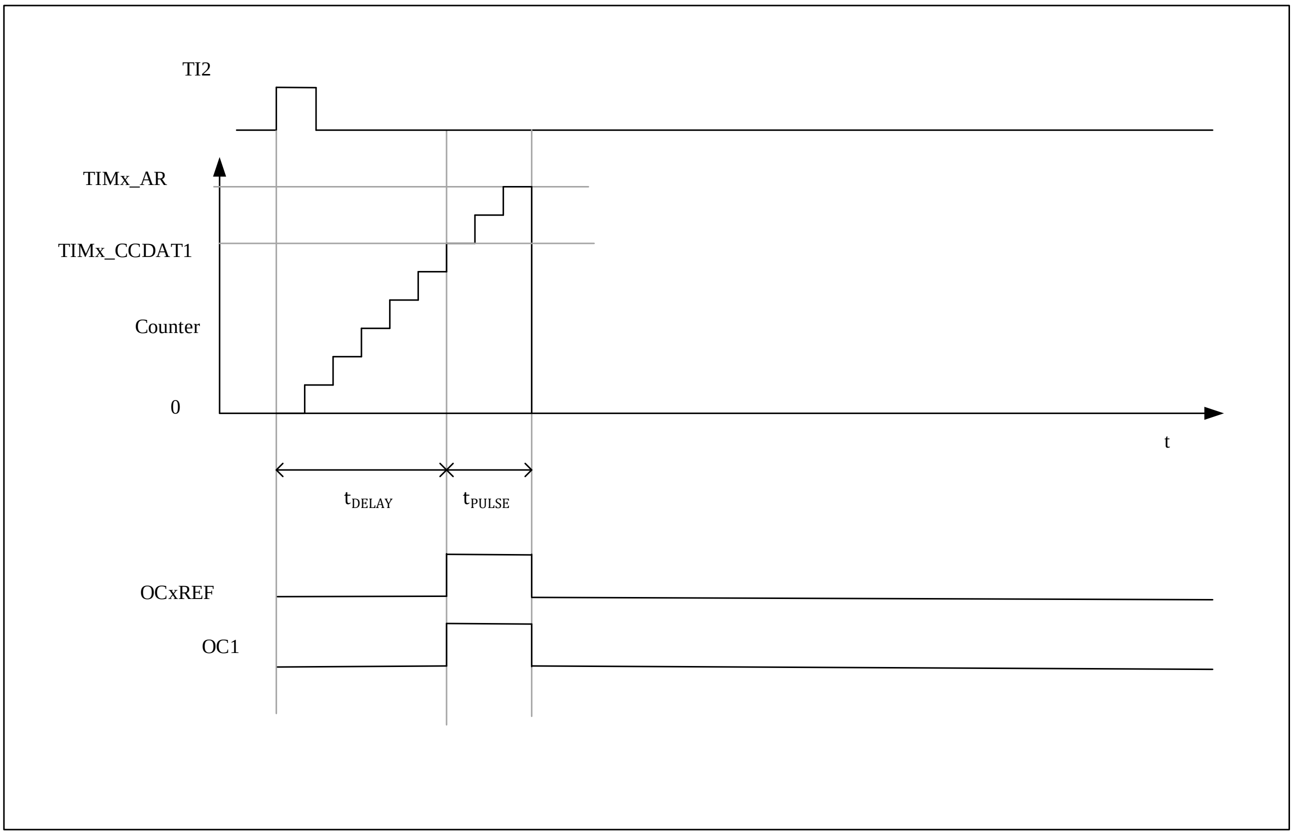
12.3.11 One-pulse Mode

In the one-pulse mode (ONEPM), a trigger signal is received, and a pulse t_{PULSE} with a controllable pulse width is generated after a controllable delay t_{DELAY}. The output mode needs to be configured as output compare mode or PWM mode. After selecting one-pulse mode, the counter will stop counting after the update event UEV is generated.

Figure 12-24 Example of One-pulse Mode



The following is an example of a one-pulse mode:

A rising edge trigger is detected from the TI2 input, and a pulse with a width of t_{PULSE} is generated on OC1 after a delay of t_{DELAY}.

1. Counter configuration: count up, counter TIMx_CNT < TIMx_CCDAT1 ≤ TIMx_AR;
2. TI2FP2 is mapped to TI2, TIMx_CCMOD1.CC2SEL= ‘01’; TI2FP2 is configured for rising edge detection, TIMx_CCEN.CC2P= ‘0’;
3. TI2FP2 acts as the trigger (TRGI) of the slave mode controller and starts the counter, TIMx_SMCTRL.TSEL= ‘110’, TIMx_SMCTRL.SMSEL= ‘0110’ (trigger mode);
4. TIMx_CCDAT1 writes the count value to be delayed (t_{DELAY}), TIMx_AR - TIMx_CCDAT1 is the count value of the pulse width t_{PULSE};
5. Configure TIMx_CTRL1.ONEPM=1 to enable single pulse mode, configure TIMx_CCMOD1.OC1MD = ‘111’ to select PWM2 mode;
6. Wait for an external trigger event on TI2, and a one pulse waveform will be output on OC1.

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12.3.11.1 Special case: OCx fast enable

In one-pulse mode, an edge is detected through the TIx input, and triggers the start of the counter to count to the comparison value and then output a pulse. These operations limit the minimum delay t_{DELAY} that can be achieved.

You can set TIMx_CCMODx.OCxFEN=1 to turn on OCx fast enable, after triggering the rising edge, the OCxREF signal will be forced to be converted to the same level as the comparison match occurs immediately, regardless of the comparison result. OCxFEN fast enable only takes effect when the channel mode is configured for PWM1 and PWM2 modes.

12.3.12 Clearing the OCxREF signal on an external event

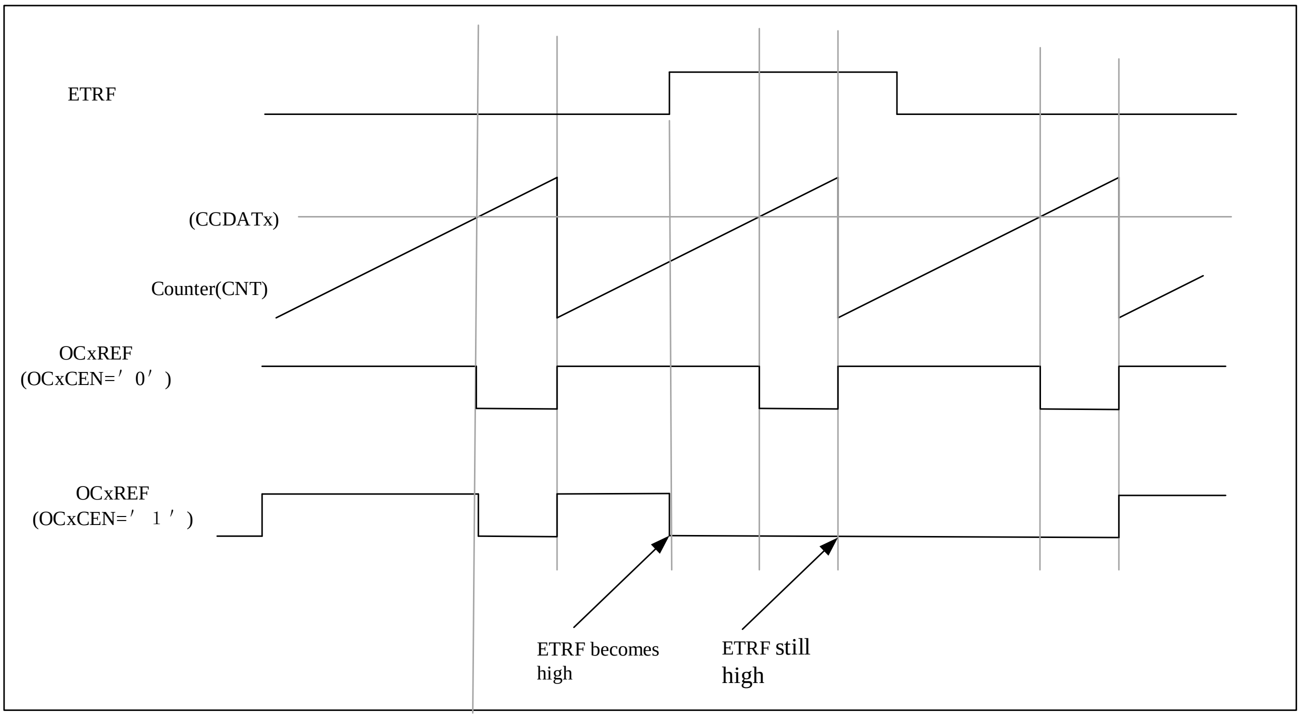
If the user sets TIMx_CCMODx.OCxCEN=1, high level of ETRF input can be used to driven the OCxREF signal to low, and the OCxREF signal will remains low, until the next UEV happens. Only Output Compare and PWM modes can use this function. This cannot be used when it is in forced mode.

Example: When the tim_ocref_clr_in signal is selected as ETRF, the tim_etr_in configuration is as follows:

- Set TIMx_SMCTRL.EXTPS=00 to disable the external trigger prescaler.
- Set TIMx_SMCTRL.EXCEN=0 to disable the external clock mode 2.
- Set TIMx_SMCTRL.EXTP and TIMx_SMCTRL.EXTF to configure the external trigger polarity and external trigger filter according to the need.

For example: The following diagram shows when ETRF input becomes high, the behavior of OCxREF signal for different value of OCxCEN. Timer is set to be in PWM mode in this case.

Figure 12-25 Clearing the OCxREF of TIMx



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12.3.13 Complementary Outputs and Dead-time Insertion

The advanced-control timer can output two complementary signals, and manage the switching-off and switching-on instants of outputs. This time is generally known as dead-time. User should adjust dead-time depending on the devices connected to the outputs and their characteristics.

User can select the polarity of outputs by setting TIMx_CCEN.CCxP and TIMx_CCEN.CCxNP. And this selection is independently for each output.

User can control the complementary signals OCx and OCxN by setting the combination of several control bits, which are TIMx_CCEN.CCxEN, TIMx_CCEN.CCxNEN, TIMx_BKDT.MOEN, TIMx_CTRL2.OIx, TIMx_CTRL2.OIxN, TIMx_BKDT.OSSI, and TIMx_BKDT.OSSR. When switching to the IDLE state, the dead-time will be activated.

If user set TIMx_CCEN.CCxEN and TIMx_CCEN.CCxNEN at the same time, a dead-time will be insert. If there is a break circuit, the TIMx_BKDT.MOEN should be set too. There are 10-bit dead-time generators for each channel.

Reference waveform OCxREF can generates 2 outputs OCx and OCxN. And if OCx and OCxN are active high, the OCx ouput signal is the same as the reference signal and the OCxN output signal is the opposite of the reference signal. However, OCx output signal will be delayed relative to the reference rising edge and the OCxN output signal will be delayed relative to the reference falling edge. If the delay is greater than the width of the active OCx or OCxN output, the corresponding pulse will not generated.

The relationships between the output signals of the dead-time generator and the reference signal OCxREF are as follow.

Assume that TIMx_CCEN.CCxP=0, TIMx_CCEN.CCxNP=0, TIMx_BKDT.MOEN=1, TIMx_CCEN.CCxEN=1, TIMx_CCEN.CCxNEN=1.

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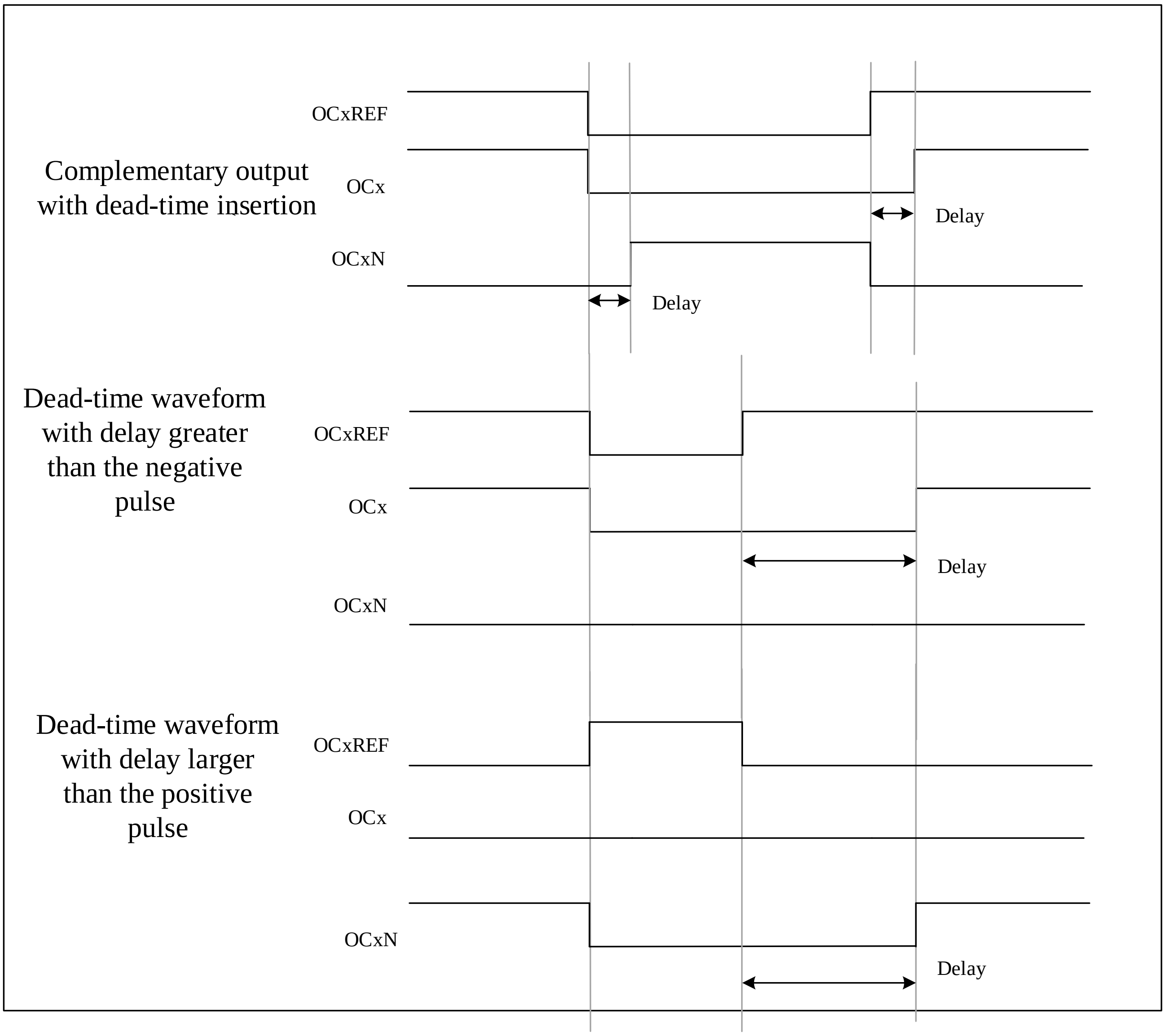
Figure 12-26 Complementary Output with Dead-time Insertion



User can set TIMx_BKDT.DTGN to programme the dead-time delay for each of the channels.

12.3.13.1 Redirecting OCxREF to OCx or OCxN

In output mode, user can set TIMx_CCEN.CCxEN and TIMx_CCEN.CCxNEN to re-directed OCxREF to the OCx output or to OCxN output.

Here are two ways to use this function. When the complementary remains at its inactive level, user can use this function to send a specific waveform, such as PWM or static active level. User can also use this function to set both outputs in their inactive level or both outputs active and complementary with dead-time.

If user set TIMx_CCEN.CCxEN=0 and TIMx_CCEN.CCxNEN=1, it will not complemented, and OCxN will become active when OCxREF is high. On the other hand, if user set TIMx_CCEN.CCxEN=1 and TIMx_CCEN.CCxNEN=1, OCx will become active when OCxREF is high. On the contrary, OCxN will become active when OCxREF is low.

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12.3.14 Break Function

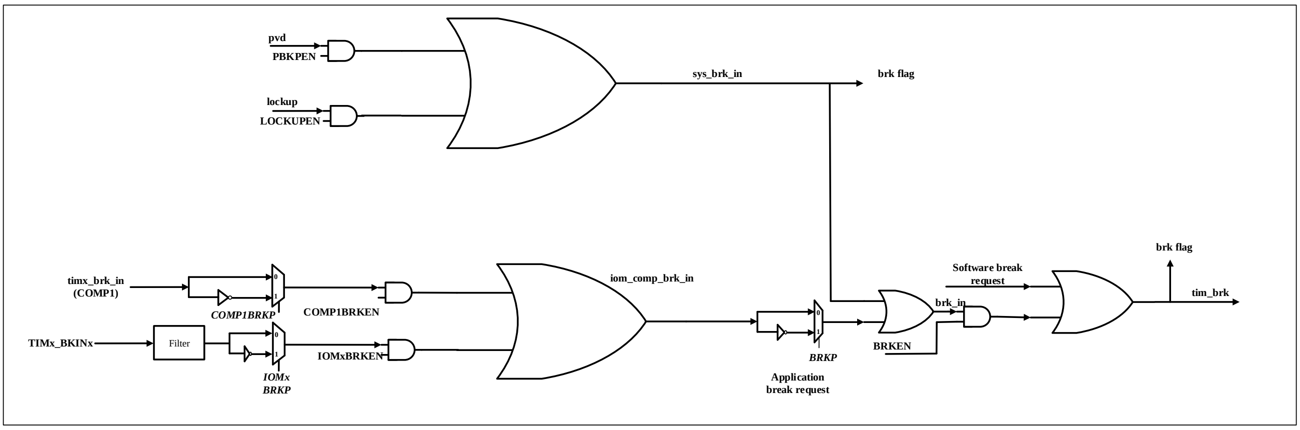
The output enable signals and inactive levels will be modified when setting the corresponding control bits when using the break function. However, the output of OCx and OCxN cannot at the active level at the same time no matter when, that is, (CCxP ^ OIx) ^ (CCxNP^OIxN)! = 0. The TIM1 brake function is only effective for OC1 to OC4 and their complementary channels; it is ineffective for OC5 to OC7.

When multiple break signals are enabled, each break signal constitutes an OR logic. Here are some signal which can be the source of break and break2.

Break:

- The break input pin (4 I/O pins)
- A PVD failure event
- Core Hardfault event
- The output signal of the comparator
- By software through the TIMx_EVTGEN.BGN

Figure 12-27 Brake input



The break circuit will be disable after reset. And the MOEN bit will be low. User can set TIMx_BKDT.BKEN to enable the break function. The polarity of break input signal can be selected by setting TIMx_BKDT.BKP. User can modify the TIMx_BKDT.BKEN and TIMx_BKDT.BKP at the same time. After user set the TIMx_BKDT.BKEN and TIMx_BKDT.BKP, there is 1 APB clock cycle delay before the configuration take effect. Therefore, user need to wait 1 APB clock cycle to read back the written bit value.

The falling edge of MOEN can be asynchronous, so a resynchronization circuit has been inserted between the actual signal and the synchronous control bit. This circuit will cause a delay between the asynchronous and the synchronous signal. When user set TIMx_BKDT.MOEN while it is low, user need to insert a delay before reading the value. Because an asynchronous signal was written but user read the synchronous signal.

The behaviors that after a break occurs are as follow:

- TIMx_BKDT.MOEN will be cleared asynchronously, and then the outputs will be put in inactive state, idle state or reset state. The state of output is selected by setting TIMx_BKDT.OSSI. This will take effect even if the MCU oscillator is off.

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- Once TIMx_BKDT.MOEN=0, the output of each output channel will be driven with the level programmed in TIMx_CTRL2.OIx. Timer will release the enable outputs (taken over by GPIO controller) if TIMx_BKDT.OSSI=0, otherwise it will remain high.
- If user choose to use complementary outputs, the behaviors of TIM are as follow:
  - Depends on the polarity, the outputs will be set in reset state first. It is an asynchronous option so it still works even if there is no clock provided to the timer.
  - The dead-time generator will be reactivated if the timer clock is still provided, and drive the outputs according to the value of TIMx_CTRL2.OIx and TIMx_CTRL2.OIxN after the dead-time when (CCxP ^ OIx) ^ (CCxNP^OIxN)! = 0, that is, the OCx and OCxN still cannot be driven to active level at the same time. Note that the dead-time will be longer than usual because of the resynchronization on MOEN (almost 2 cycles of ck_tim).
  - Timer will release the output control if TIMx_BKDT.OSSI=0. Otherwise, if the enable output was high, it will remain high. If it was low, it will become high when TIMx_CCEN.CCxEN or TIMx_CCEN.CCxNEN is high.
- If TIMx_DINTEN.BIEN=1, when TIMx_STS.BITF=1, an interrupt will be generated.
- If user set TIMx_BKDT.AOEN, the TIMx_BKDT.MOEN will be set automatically when the next UEV happened. User can use this to regulate. If user did not set TIMx_BKDT.AOEN, the TIMx_BKDT.MOEN will remain low until been set 1 again. At this situation, user can use this for security. User can connect the break input to thermal sensors, alarm for power drivers, or other security components.
- When the break input is active, TIMx_BKDT.MOEN cannot be set automatically or by software at the same time, and the TIMx_STS.BITF cannot be cleared. Because the break inputs are active on level.

To ensure the security of application, the break circuit has the write protection function, and there is break input and output management too. It allow user to freeze some parameters, such as dead-time duration, OCx/OCxN polarities and state when disabled, OCxMD configurations, break enable and polarity. User can choose one of the 3 levels of protection to use by setting TIMx_BKDT.LCKCFG. However, the TIMx_BKDT.LCKCFG can only be written once after an MCU reset.

An example for output behavior in response to a break is as follow.

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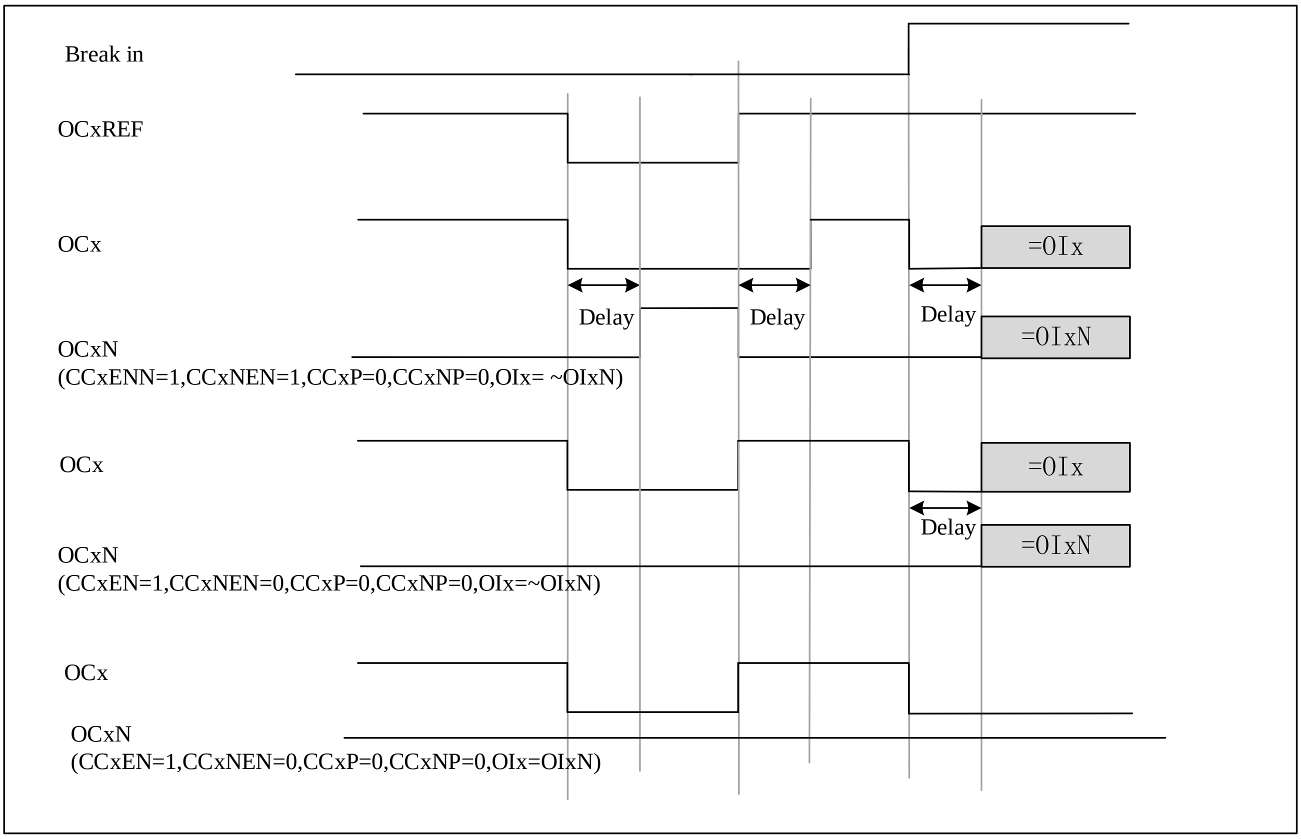
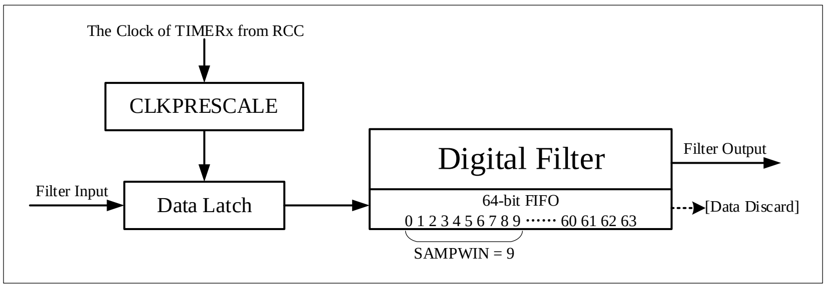
Figure 12-28 Output Behavior in Response to a Break



12.3.14.1 Break filter

Register TIMx_BKFR description are as follow:

Figure 12-29 Silde Filter



- The digital filter samples break signal at the clock of TIMx from RCC, accumulating samples in a 64-bits FIFO. Only sampled data within window size defined in TIMx_BKFR.WSIZE [5:0] with maximum size 64.
- The filter outputs the majority value inside sample window which is defined by the threshold value in TIMx_BKFR.THRESH [5:0] with maximum threshold of 63. This value should be equal or more than half of window size. If neither logic 1 nor logic 0 counts inside sampling window is more than threshold, digital filter maintain previous output value.
- RCC_TIMFILTCFG.TIM1FILTCLK[4:0] register determines sample rate of corresponding digital filter. Filter FIFO capture one sample value from input at every sample clock.
- If digital filter is off, filter input will bypass to output like a wire.

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12.3.15 Debug Mode

When the microcontroller is in debug mode (the Cortex-M0 core halted), depending on the DBG_CTRL.TIMx_STOP configuration in the DBG module, the TIMx counter can either continue to work normally or stop. Refer to Section 3.3.1 for detail.

12.3.16 TIMx and External Trigger Synchronization

TIMx can be synchronized by a trigger in slave modes (reset, trigger and gated).

12.3.16.1 Slave mode: reset mode

In reset mode, the trigger event can reset the counter and the prescaler updates the preload registers TIMx_AR, TIMx_CCDATx, and generates the update event UEV (TIMx_CTRL1.UPRS=0).

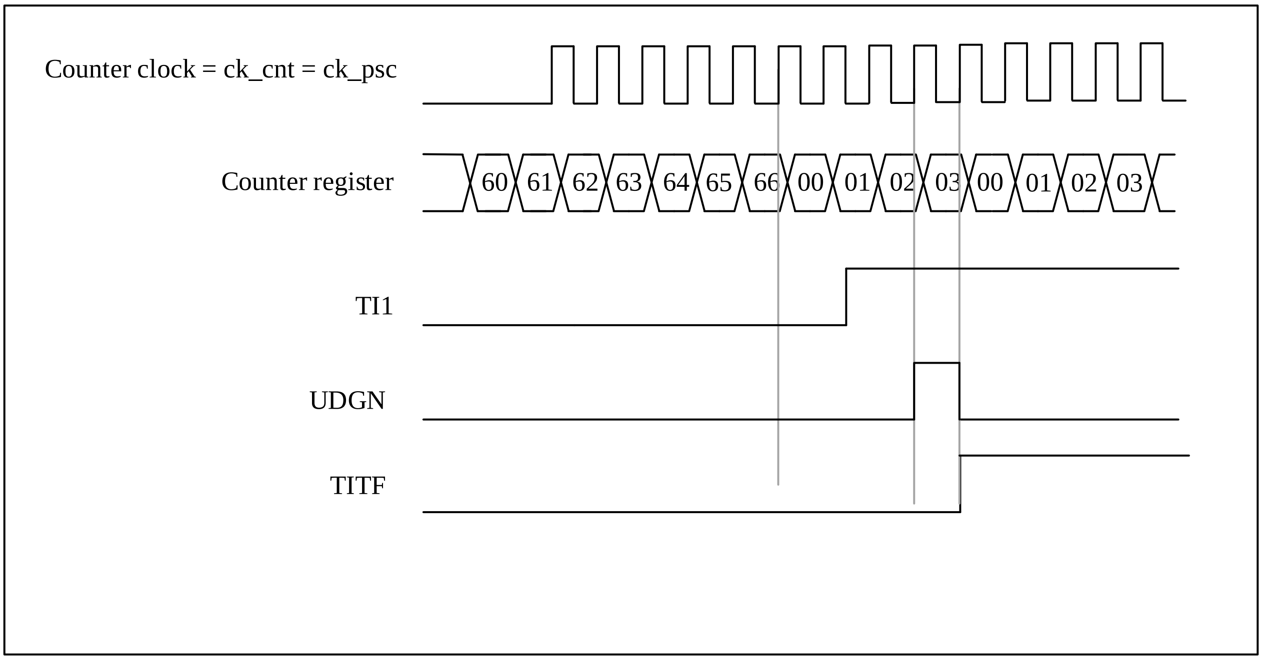
The following is an example of a reset mode:

- Channel 1 is configured as input to detect the rising edge of TI1 (TIMx_CCMOD1.CC1SEL=01, TIMx_CCEN.CC1P=0);
- The slave mode is selected as reset mode (TIMx_SMCTRL.SMSEL=0100), and the trigger input is selected as TI1 (TIMx_SMCTRL.TSEL=101);
- Setting TIMx_CTRL1.CNTEN = 1 to start counter;

After starting the timer, when TI1 detects a rising edge, the counter resets and restarts counting, and the trigger flag is set (TIMx_STS.TITF=1);

The delay between the rising edge on TI1 and the actual reset of the counter is due to the resynchronization circuit on TI1 input.

Figure 12-30 Control Circuit in Reset Mode



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12.3.16.2 Slave mode: trigger mode

In trigger mode, the trigger event (rising edge/falling edge) of the input port can trigger the counter to start counting.

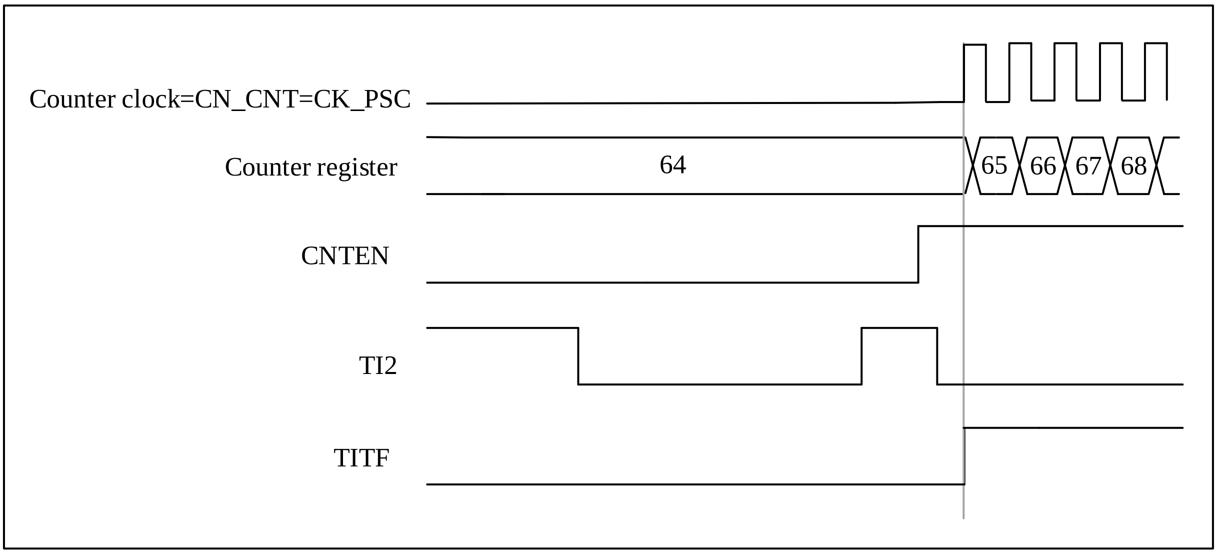
The following is an example of a trigger pattern:

- Channel 2 is configured as input to detect the rising edge of TI2 (TIMx_CCMOD1.CC2SEL=01, TIMx_CCEN.CC2P=0);
- Select from mode to trigger mode (TIMx_SMCTRL.SMSEL=0110), select TI2 for trigger input (TIMx_SMCTRL.TSEL=110);

When a rising edge is detected on TI2, the counter starts counting, and the trigger flag is set (TIMx_STS.TITF=1);

The delay between the rising edge on TI2 and the actual start of the counter is due to the resynchronization circuit on TI2 input.

Figure 12-31 Control Circuit in Trigger Mode



12.3.16.3 Slave mode: gated mode

In gated control mode, the level polarity of the input port can control whether the counter counts or not.

The following is an example of a gated mode:

- Channel 1 is configured as input detection active low on TI1 (TIMx_CCMOD1.CC1SEL=01, TIMx_CCEN.CC1P=1);
- Select the slave mode as the gated mode (TIMx_SMCTRL.SMSEL=0101), and select TI1 as the trigger input (TIMx_SMCTRL.TSEL=101);
- Setting TIMx_CTRL1.CNTEN = 1 to start counter

When TI1 detects that the level changes from low to high, the counter stops counting, and when TI1 detects that the level changes from high to low, the counter starts counting, and the trigger flag will be set (TIMx_STS.TITF=1) when it starts or stops counting;

The delay between the rising edge on TI1 and the actual stop of the counter is due to the resynchronization circuit on TI1 input.

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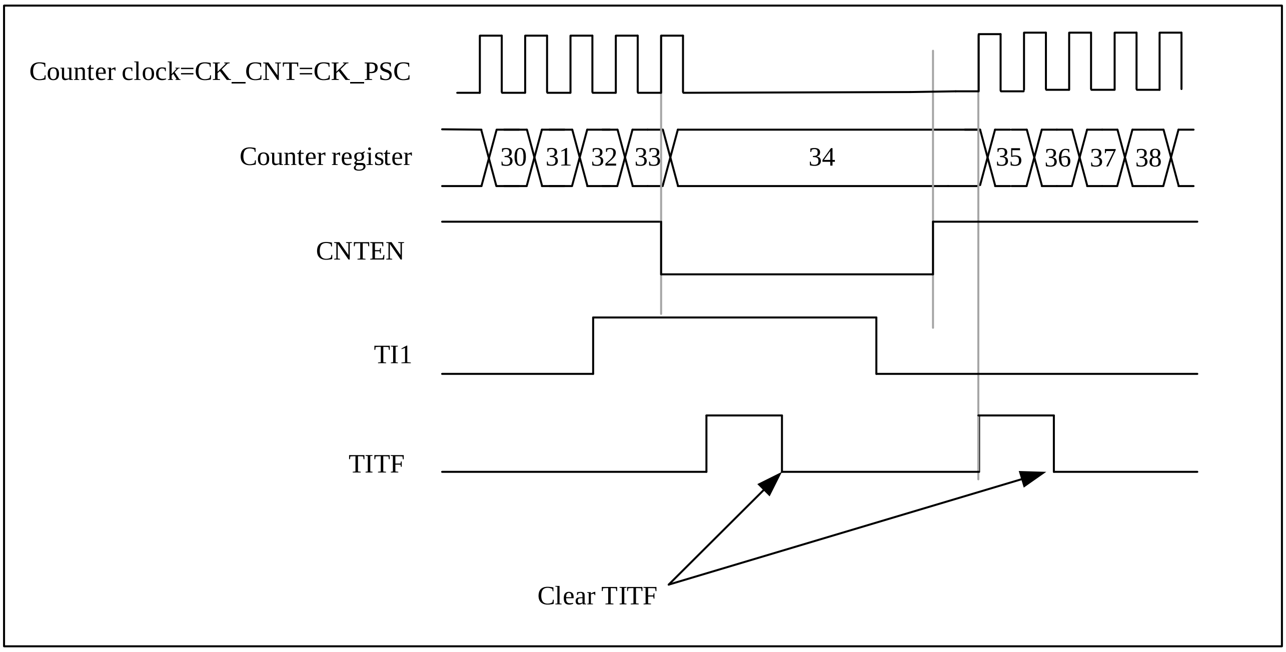
Figure 12-32 Control Circuit in Gated Mode



12.3.16.4 Slave mode: trigger mode + external clock mode 2

In reset mode, trigger mode and gate control mode, the counter clock can be selected as external clock mode 2, and the ETR signal is used as the external clock source input. At this time, the trigger selection needs to select non-ETRF (TIMx_SMCTRL.TSEL=111).

Here is an example:

- Channel 1 is configured as input to detect the rising edge of TI1 (TIMx_CCMOD1.CC1SEL=01, TIMx_CCEN.CC1P=0),
- Enable external clock mode 2 (TIMx_SMCTRL.EXCEN=1), select rising edge for external trigger polarity (TIMx_SMCTRL.EXTP=0), select slave mode as trigger mode (TIMx_SMCTRL.SMSEL=0110), select TI1 for trigger input (TIMx_SMCTRL.TSEL=101),

When TI1 detects a rising edge, the counter starts counting on the rising edge of ETR, and the trigger flag is set (TIMx_STS.TITF=1).

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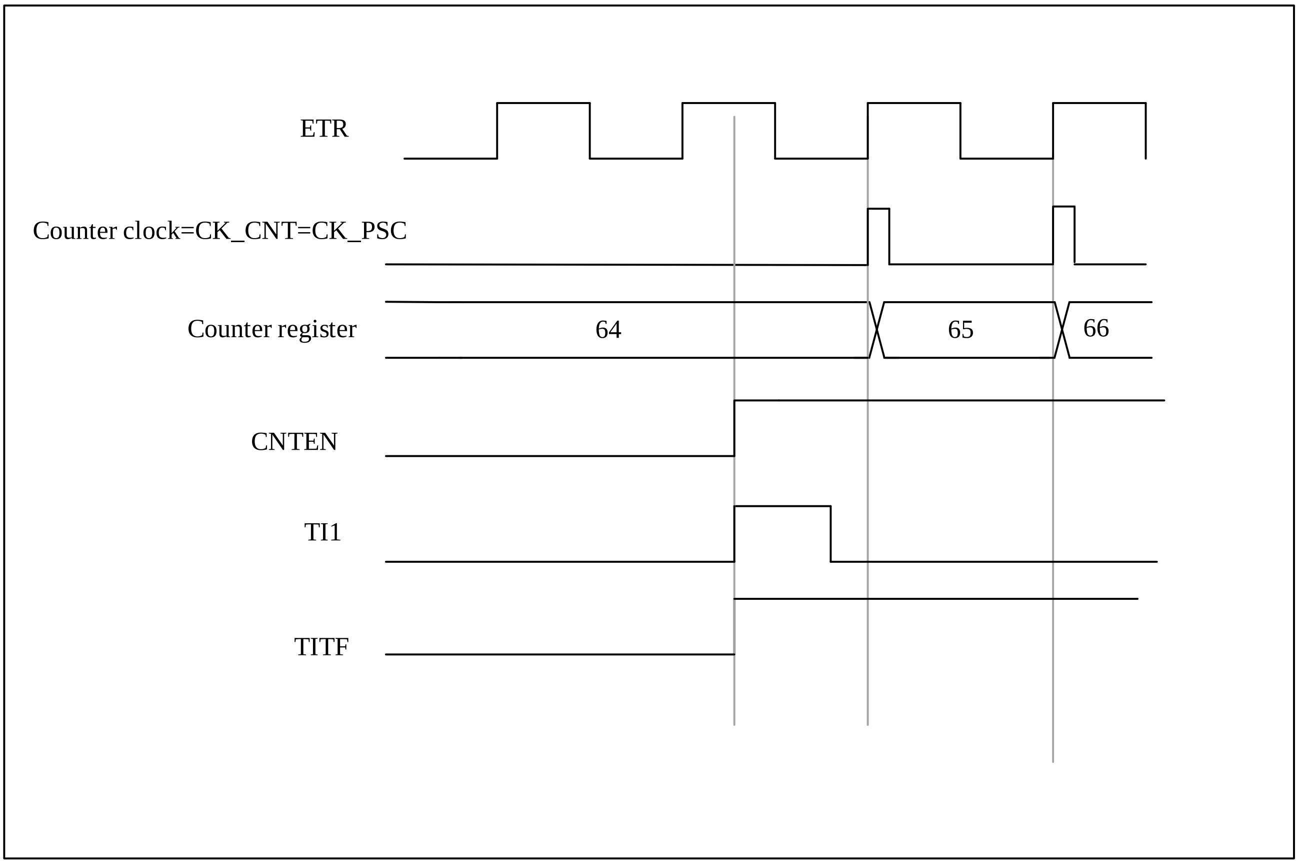
Figure 12-33 Control Circuit in Trigger Mode + External Clock Mode2



12.3.16.5 Slave mode: Combined Reset + Trigger Mode

In this case, the rising edge of the selected trigger input (TRGI) will reset the counter, generate register updates, and start the counter.

This mode is used for one-pulse mode.

The event selected on the input resets and enables the counter.

In the following example, the counter is reset and starts counting up on the rising edge of the TI2 input:

- Configure channel 2 to detect the rising edge of TI2. Set the input filter bandwidth (in this example, no filter is needed, keep TIMx_CCMOD1.IC2F=0000). No capture prescaler is used in the trigger operation, so no configuration is required. The TIMx_CCMOD1.CC2SEL bit is used to select the input capture source, set TIMx_CCMOD1.CC2SEL=01. Set TIMx_CCEN.CC2P=1 to determine the polarity (detect only low level).
- Configure TIMx_SMCTRL.SMSEL=1110 to set the timer in Combined Reset + Trigger mode; set TIMx_SMCTRL.TSEL=110 to select TI2 as the input source.

When a rising edge occurs on TI2, the counter starts counting under the internal clock drive, and the TITF flag is set.

The delay between the rising edge on TI2 and the actual stop of the counter is due to the resynchronization circuit on TI2 input.

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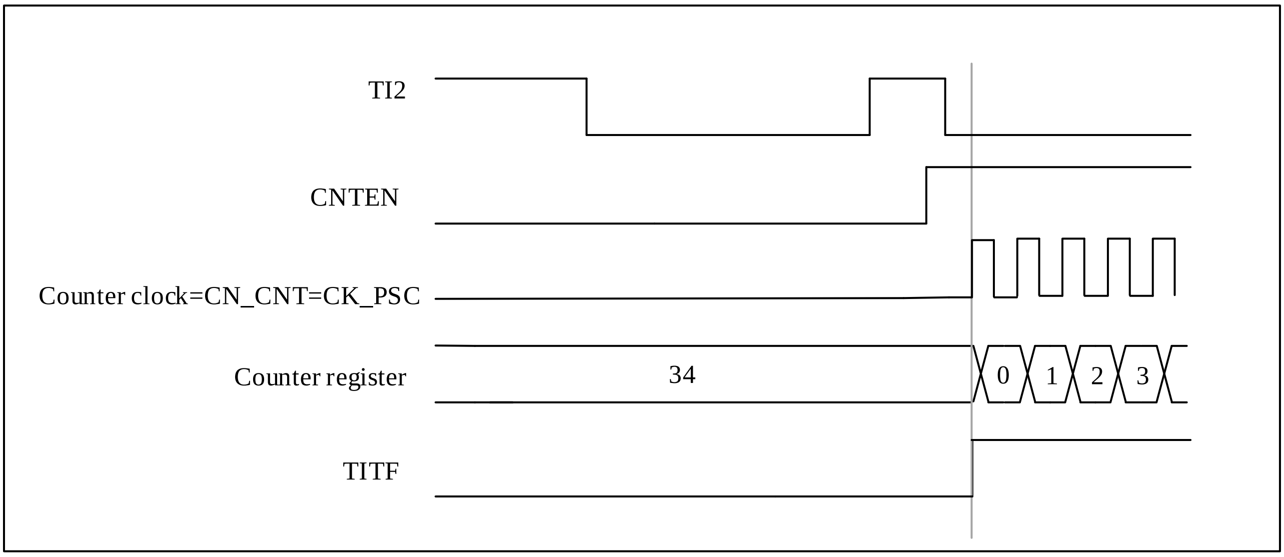
Figure 12-34 Control Circuit in Combined Reset + Trigger Mode



12.3.16.6 Slave mode: Combined Gated + Reset Mode

When the trigger input (TRGI) is high, the counter is enabled. Once the trigger goes low, the counter stops and is reset. The start and stop of the counter are both controlled.

This mode can detect out-of-range PWM signals (duty cycle exceeding the maximum expected value).

In the following example, the counter counts up only when TI1 is low, and the counter stops and resets when TI1 goes high:

- Configure channel 1 to detect low level on TI1. Set the input filter bandwidth (in this example, no filter is needed, so keep TIMx_CCMOD1.IC1F=0000). No capture prescaler is used in the trigger operation, so no configuration is required. The TIMx_CCMOD1.CC1SEL bit is used to select the input capture source, set TIMx_CCMOD1.CC1SEL=01. Set TIMx_CCEN.CC1P=1 to determine the polarity (detect only low level).
- Configure TIMx_SMCTRL.SMSEL=1101 to set the timer in Gated + Reset mode; set TIMx_SMCTRL.TSEL=101 to select TI1 as the input source.
- Set CNTEN=1 in the TIMx_CTRL1 register to start the counter. In Gated + Reset mode, if CNTEN=0, the counter cannot start, regardless of the trigger input level.

The counter starts counting based on the internal clock as long as TI1 is low, and it stops counting once TI1 goes high. The TITF flag in TIMx_STS is set when the counter starts or stops.

The delay between the rising edge on TI1 and the actual stop of the counter is due to the resynchronization circuit on TI1 input.

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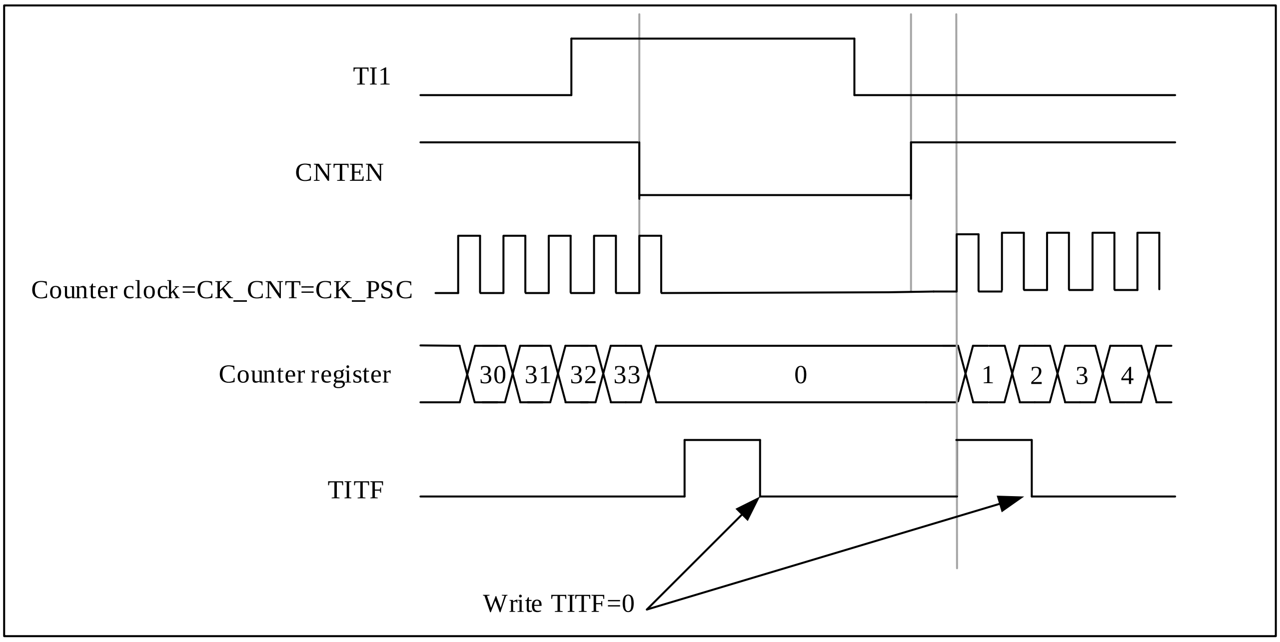
Figure 12-35 Control Circuit in Combined Gated + Reset Mode



12.3.17 Timer Synchronization

All TIMx are internally interconnected for timer synchronization or chaining. Refer to Section 14.3.15 for detail.

12.3.18 ADC Triggers

The timer can generate ADC trigger events through various internal signals, such as reset, enable, or comparison events, and can also generate pulse triggers issued by internal edge detectors.

users can trigger the ADC by selecting the internal lines TRGO using the MMSEL[3:0] bits in the TIMx_CTRL2 register. The ADC may also be triggered via channels 1/2/3/4/5/6/7.

12.3.19 Generating Six-step PWM Output

In order to modify the configuration of all channels at the same time, the configuration of the next step can be set in advance (the preloaded bits are OCxMD, CCxEN and CCxNEN). When a COM commutation event occurs, the OCxMD, CCxEN, and CCxNEN preload bits are transferred to the shadow register bits.

Methods to generate a COM commutation event:

- A software sets TIMx_EVTGEN.CCUDGN;
- Generated by hardware on the rising edge of TRGI;

When a COM commutation event occurs, the TIMx_STS.COMITF flag will be set, enabling interrupts (TIMx_DINTEN.COMIEN) will generate interrupts, and enabling DMA requests (TIMx_DINTEN.COMDEN) will generate DMA requests.

The following figure shows the output timing diagram of OCx and OCxN when a COM commutation event occurs in three different configurations:

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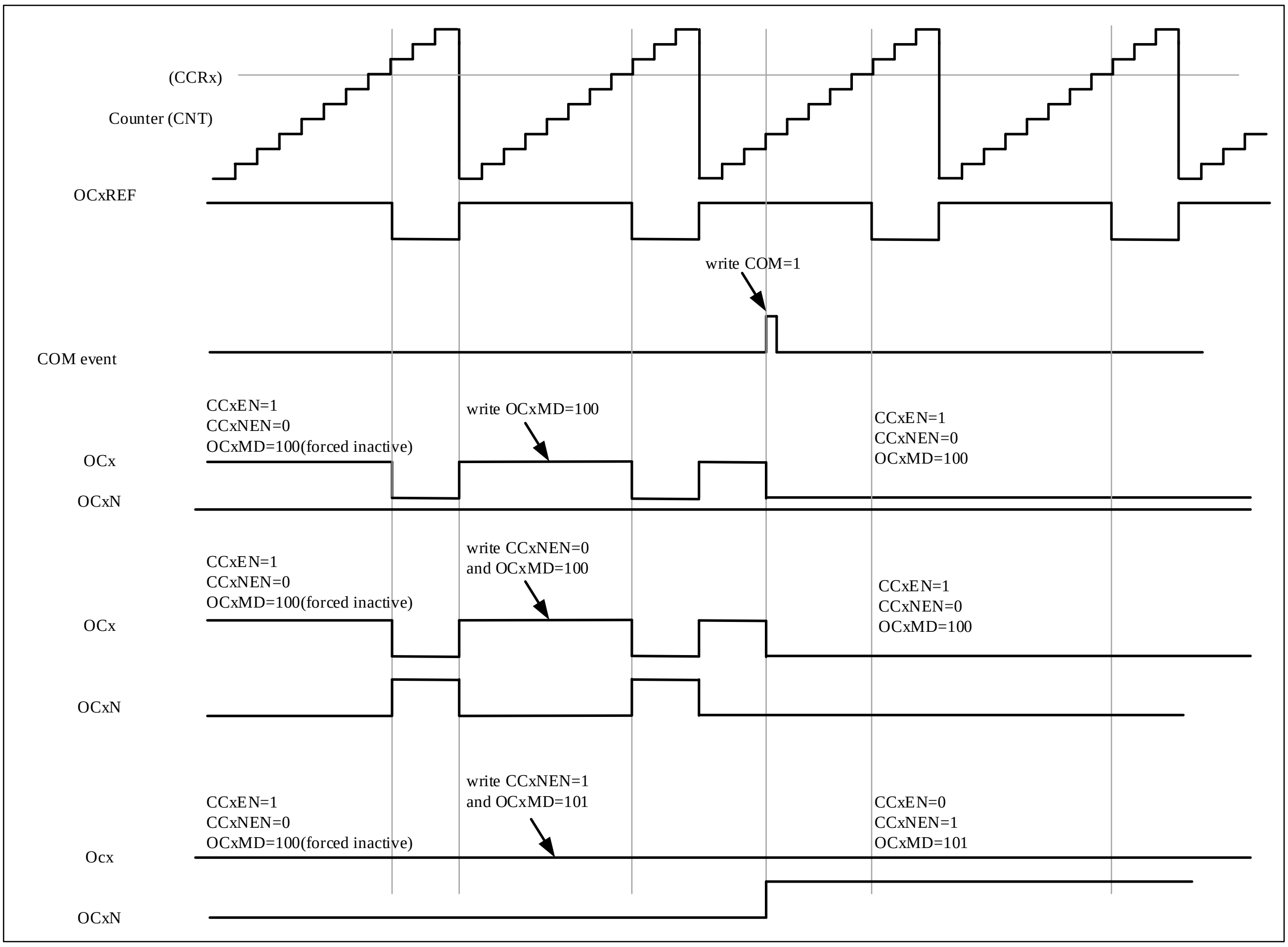
Figure 12-36 6-step PWM Generation, COM Example (OSSR=1)



12.3.20 Encoder Interface Mode

The encoder uses two inputs, TI1 and TI2 as the interface and the counter counts on every edge change on TI1FP1 or TI2FP2. The counting direction is automatically controlled by hardware TIMx_CTRL1.DIR. There are five types of quadrature encoder counting modes:

- Encoder mode 1: The counter counts only on the edges of TI1, TIMx_SMCTRL.SMSEL = '0001';
- Encoder mode 2: The counter counts only on the edges of TI2, TIMx_SMCTRL.SMSEL = '0010';
- Encoder mode 3: The counter counts on the edges of both TI1 and TI2, TIMx_SMCTRL.SMSEL = '0011';

The encoder interface is equivalent to using an external clock with direction selection, and the counter only counts continuously between 0 and the auto-reload value (TIMx_AR.AR [15:0]). Therefore, it is necessary to configure the auto-reload register TIMx_AR in advance.

Note: encoder mode and external clock mode 2 are not compatible and must not be selected together.

The relationship between the counting direction and the encoder signal is as follows:

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Table 12-1 The Relationship between the Counting Direction and the Encoder Signal (CC1P=CC2P=0)

Active Edge	Level on Opposite Signals (TI1FP1 for TI2, TI2FP2 for TI1)	TI1FP1 Signal		TI2FP2 Signal	
		Rising	Falling	Rising	Falling
Counting only on TI1	High	Counting down	Counting up	Don't count	Don't count
	Low	Counting up	Counting down	Don't count	Don't count
Counting only on TI2	High	Don't count	Don't count	Counting up	Counting down
	Low	Don't count	Don't count	Counting down	Counting up
Counting on Both TI1 and TI2	High	Counting down	Counting up	Counting up	Counting down
	Low	Counting up	Counting down	Counting down	Counting up

Here is an example of an encoder with dual edge selected for triggering to suppress input jitter:

- IC1FP1 is mapped to TI1 (TIMx_CCMOD1.CC1SEL= '01'), IC1FP1 is not inverted (TIMx_CCEN.CC1P= '0');
- IC1FP2 is mapped to TI2 (TIMx_CCMOD2.CC2SEL= '01'), IC2FP2 is not inverted (TIMx_CCEN.CC2P= '0');
- The input is valid on both rising and falling edges (TIMx_SMCTRL.SMSEL = '0011');
- Enable counter TIMx_CTRL1.CNTEN= '1'.

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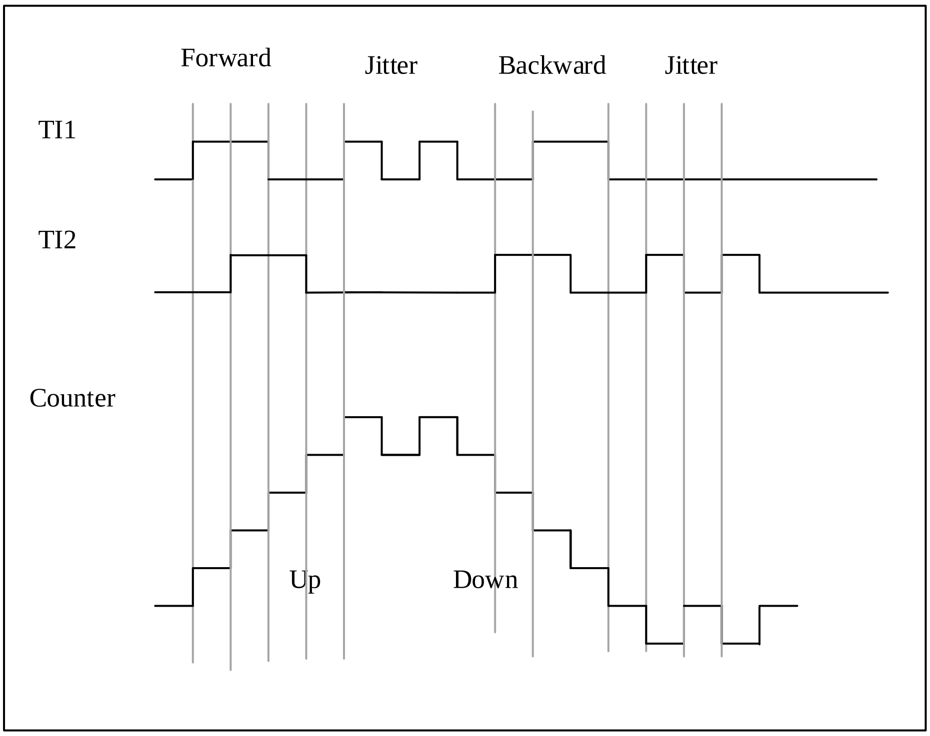
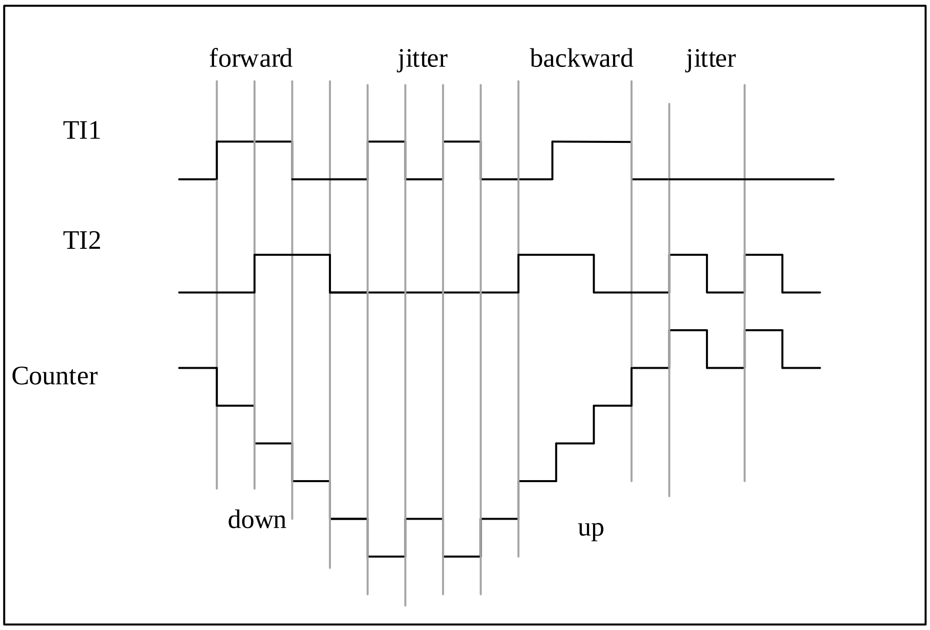
Figure 12-37 Example of Counter Operation in Encoder Interface Mode



The following figure shows the example of counter behavior when IC1FP1 polarity is inverted (CC1P= '1', other configurations are the same as above).

Figure 12-38 Encoder Interface Mode Example with IC1FP1 Polarity Inverted



12.3.21 Interfacing with Hall Sensor

Connect the Hall sensor to the three input pins (CC1, CC2 and CC3) of the timer, and then select the XOR function to pass the inputs of TIMx_CH1, TIMx_CH2 and TIMx_CH3 through the XOR gate as the output of TI1 to channel

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1 for capture signal.

The timer needs to be configured as the reset mode in slave mode (TIMx_SMCTRL.SMSEL= ‘0100’); the edge of the trigger select TI1 triggers TI1F_ED (TIMx_SMCTRL.TSEL= ‘100’), any change in the Hall 3 inputs will trigger the counter to recount, so it is used as a time reference; the capture/compare channel 1 is configured to capture the TRC signal in capture mode (TIMx_CCMOD1.CC1SEL= ‘11’), which is used to calculate the two input time intervals, thereby reflecting the motor speed.

Select timer channel 2 to output pulses to the advanced timer to trigger the COM event of the advanced timer to update the control bits of the output PWM. The trigger selection of the advanced timer needs to select the corresponding internal trigger signal (TIMx_SMCTRL.TSEL="ITRx"), the capture/compare preload control bit needs to be configured to support preload (TIMx_CTRL2.CCPCTL=1) and support the rising edge of TRGI Trigger an update (TIMx_CTRL2.CCUSEL=1).

This example is shown in the following figure.

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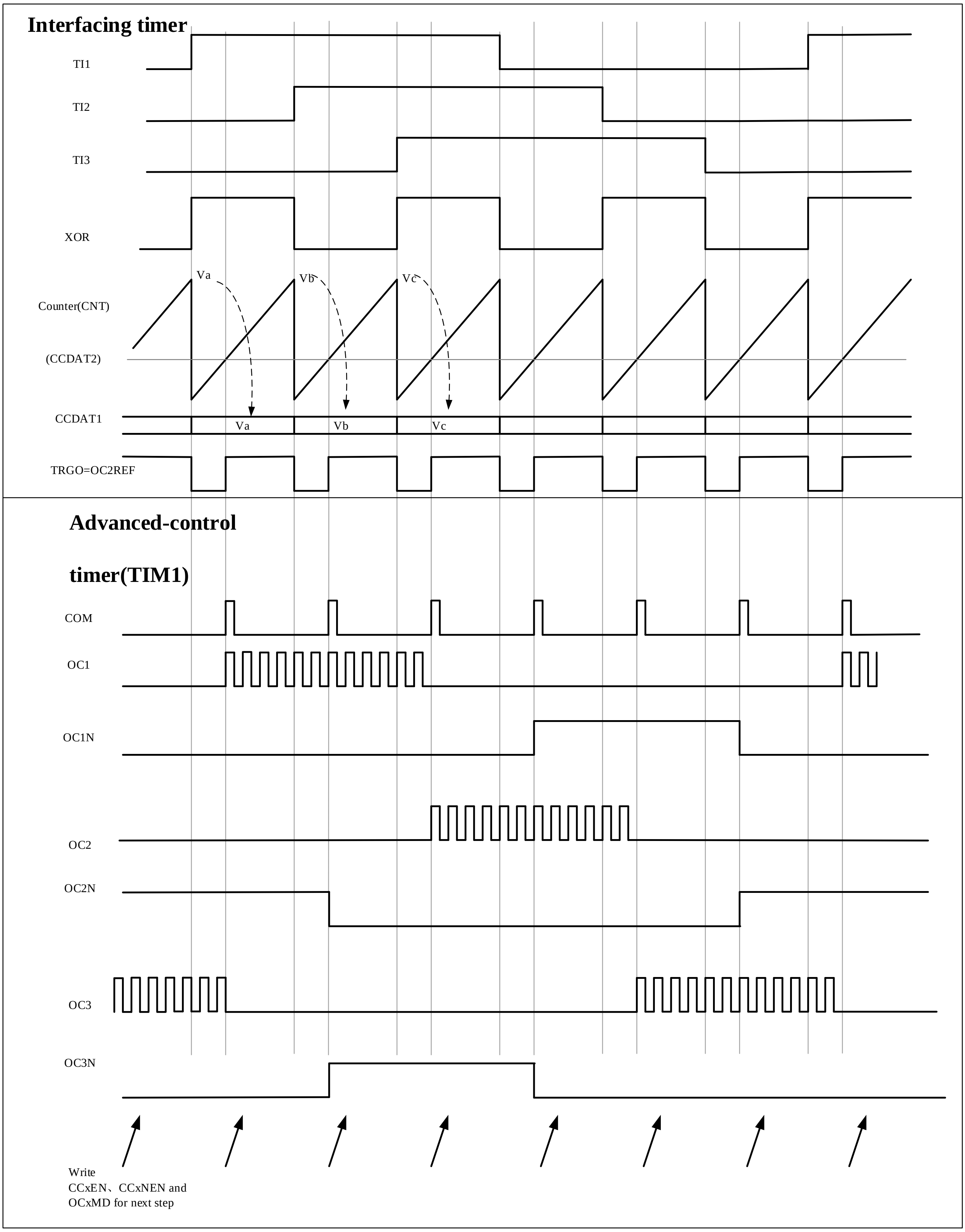
Figure 12-39 Example of Hall Sensor Interface



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12.4 TIM1 Register Description

For abbreviations used in the registers, please refer to Section 1.1.

These peripheral registers can be operated as half word (16-bits) or one word (32-bits).

12.4.1 Register Overview

Table 12-2 TIM1 Register Overview

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
000h	TIM_CTRL1	Reserve								ASYMMETRIC	Reserve						C1SEL
004h	TIM_CTRL2	Reserve												T1SEL	CCPCTL	CCDSEL	CCUSEL
008h	TIM_STS	Reserve				IOMBITF	Reserve		CC7ITF	COMPBITF	PBKPITF	LBKPITF	Reserve	BITF	TITF	COMITF	UDITF
00Ch	TIM_EVTGEN	Reserve															
010h	TIM_SMCTRL	Reserve															MSMD
014h	TIM_DINTEN	Reserve									COMIEN	TDEN	COMDEN	UDEN	BIEN	TIEN	UIEN
018h	TIM_CCMOD1_OUT	Reserve															
	TIM_CCMOD1_IN	Reserve															
01Ch	TIM_CCMOD2_OUT	Reserve															
	TIM_CCMOD2_IN	Reserve															
020h	TIM_CCMOD3_OUT	Reserve				OC7MD[2:0]			Reserve						OC7CEN	OC7FEN	0C7PEN
024h	TIM_CCEN	Reserve						CC7P	CC7EN	CC6P	CC6EN	Reserve		CC5P	CC5EN	Reserve	

Offset	Register	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
000h	TIM_CTRL1	Reserve		CLRSEL	Reserve	PBKPEN	LBKPEN	ARPEN	ONEPM	CLKD[1:0]		UPDIS	UPRS	CAMSEL[1:0]		DIR	CNTEN
004h	TIM_CTRL2	MMSEL[3:0]				Reserve				OI4N	OI4	OI3N	OI3	OI2N	OI2	OI1N	OI1
008h	TIM_STS	Reserve				CC4OCF	CC3OCF	CC2OCF	CC1OCF	Reserve		CC6ITF	CC5ITF	CC4ITF	CC3ITF	CC2ITF	CC1ITF
00Ch	TIM_EVTGEN	Reserve				BGN	TGN	CCUDGN	UDGN	Reserve				CC4GN	CC3GN	CC2GN	CC1GN
010h	TIM_SMCTRL	EXTF[3:0]				EXTP	EXCEN	EXTPS[1:0]		SMSEL[3:0]				Reserve	TSEL[2:0]		
014h	TIM_DINTEN	Reserve				CC4DEN	CC3DEN	CC2DEN	CC1DEN	Reserve	CC7IEN	CC6IEN	CC5IEN	CC4IEN	CC3IEN	CC2IEN	CC1IEN
018h	TIM_CCMOD1_OUT	OC2MD[2:0]			OC2CEN	OC2FEN	OC2PEN	CC2SEL[1:0]		OC1MD[2:0]			OC1CEN	OC2FEN	OC1PEN	CC1SEL[1:0]	
	TIM_CCMOD1_IN	IC2F[3:0]				IC2PSC[1:0]		CC2SEL[1:0]		IC1F[3:0]				IC1PSC[1:0]		CC1SEL[1:0]	
01Ch	TIM_CCMOD2_OUT	OC4MD[2:0]			OC4CEN	OC4FEN	OC4PEN	CC4SEL[1:0]		OC3MD[2:0]			OC3CEN	OC3FEN	OC3PEN	CC3SEL[1:0]	
	TIM_CCMOD2_IN	IC4F[3:0]				IC4PSC[1:0]		CC4SEL[1:0]		IC3F[3:0]				IC3PSC[1:0]		CC3SEL[1:0]	
020h	TIM_CCMOD3_OUT	OC6MD[2:0]			OC6CEN	OC6FEN	0C6PEN	Reserve		OC5MD[2:0]			OC5CEN	OC5FEN	0C5PEN	Reserve	
024h	TIM_CCEN	CC4P	CC4EN	CC4NP	CC4NEN	CC3P	CC3EN	CC3NP	CC3NEN	CC2P	CC2EN	CC2NP	CC2NEN	CC1P	CC1EN	CC1NP	CC1NEN

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028h	TIM_CCDAT1	CCDDAT1[15:0]	CCDAT1[15:0]											
02Ch	TIM_CCDAT2	CCDDAT2[15:0]	CCDAT2[15:0]											
030h	TIM_CCDAT3	CCDDAT3[15:0]	CCDAT3[15:0]											
034h	TIM_CCDAT4	CCDDAT4[15:0]	CCDAT4[15:0]											
038h	TIM_CCDAT5	Reserve	CCDAT5[15:0]											
03Ch	TIM_CCDAT6	Reserve	CCDAT6[15:0]											
040h	TIM_PSC	Reserve	PSC[15:0]											
044h	TIM_AR	Reserve	AR[15:0]											
048h	TIM_CNT	Reserve	CNT[15:0]											
04Ch	TIM_REPCNT	Reserve	REPCNT[7:0]											
050h	TIM_BKDT	Reserve	LCKCFG[1:0]	OSSR	OSSI	BKEN	BKP	AOEN	MOEN	DTGN[7:0]				
054h	TIM_CCDAT7	Reserve	CCDAT7[15:0]											
060h	TIM_BKFR	Reserve	THRESH[5:0]	Reserve	WSIZE[5:0]	FILTEN	Reserve							
07Ch	TIM_AF1	Reserve	IOM4BRKP	IOM3BRKP	IOM2BRKP	IOM4BRKEN	IOM3BRKEN	IOM2BRKEN	Reserve	COMP1BRKP	IOM1BRKP	Reserve	COMP1BRKEN	IOM1BRKEN
094h	TIM_DCTRL	Reserve	DBADDR[5:0]	Reserve	DBLEN[5:0]									
098h	TIM_DADDR	BURST[31:0]												

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12.4.2 Control Register 1 (TIMx_CTRL1)

Offset address: 0x00

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved								ASYMMETRIC	Reserved						C1SEL
								rw							rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved		CLRSEL	Reserved	PBKPEN	LBKPEN	ARPEN	ONEPM	CLKD[1:0]		UPDIS	UPRS	CAMSEL[1:0]		DIR	CNTEN
		rw		rw	rw	rw	rw	rw		rw	rw	rw		rw	rw

Bit Field	Name	Description
31:24	Reserved	Reserved, the reset value must be maintained
23	ASYMMETRIC	Asymmetric mode enable in center-aligned mode 0: Disabled 1: Enabled (valid when TIMx_CTRL1.CAMSEL[1:0] is non-zero, each channel will compare to CCDATx when counting up, and compare to CCDDATx when counting down) *Note: this function is only for TIM1*
22:17	Reserved	Reserved, the reset value must be maintained
16	C1SEL	Channel 1 selection 0: Select the external CH1 (from IOM) signal. 1: Select internal CH1 (from COMP) signal.
15:14	Reserved	Reserved, the reset value must be maintained
13	CLRSEL	OcxRef clear selection 0: Select the external Ocxclr (ETR) signal 1: Select the internal Ocxclr (from COMP) signal
12	Reserved	Reserved, the reset value must be maintained
11	PBKPEN	PVD break Enable 0: Disable 1: Enable *Note: This position can only be cleared after the system is reset.*
10	LBKPEN	LockUp break Enable（Core Hardfault） 0: Disable 1: Enable *Note: This position can only be cleared after the system is reset.*
9	ARPEN	Auto-reload preload enable 0: Shadow register disable for TIMx_AR register 1: Shadow register enable for TIMx_AR register
8	ONEPM	One pulse mode 0: Disable one-pulse mode, the counter counts are not affected when an update event occurs.

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Bit Field	Name	Description
		1: Enable one-pulse mode, the counter stops counting when the next update event occurs
7:6	CLKD[1:0]	Clock division CLKD[1:0] indicates the division ratio between CK_INT (timer clock) and DTS (clock used for dead-time generator and digital filters (ETR, TIx)) 00: tDTS = tCK_INT · 01: tDTS = 2 x tCK_INT 10: tDTS = 4 x tCK_INT 11: Reserved, do not use this configuration
5	UPDIS	Update disable This bit is set and cleared by software to enable/disable UEV event generation. 0: UEV Enable. UEV will be generated if one of following condition been fulfilled: – Counter overflow/underflow – The TIMx_EVTGEN.UDGN bit is set – Update generation from the slave mode controller Shadow registers will update with preload value. 1: UEV disabled. No update event is generated, and the shadow registers (AR, PSC, and CCDATx) keep their values. If the TIMx_EVTGEN.UDGN bit is set or a hardware reset is issued by the slave mode controller, the counter and prescaler are reinitialized.
4	UPRS	Update request source This bit is used to select the UEV event sources by software. 0: If update interrupt or DMA request is enabled, any of the following events will generate an update interrupt or DMA request: –Counter overflow/underflow –The TIMx_EVTGEN.UDGN bit is set –Update generation from the slave mode controller 1: If update interrupt or DMA request is enabled, only counter overflow/underflow will generate update interrupt or DMA request
3:2	CAMSEL[1:0]	Center-aligned mode selection 00: Edge-aligned mode. TIMx_CTRL1.DIR specifies up-counting or down-counting. 01: Center-aligned mode 1. The counter counts in center-aligned mode, and the output compare interrupt flag bit is set to 1 when down-counting. 10: Center-aligned mode 2. The counter counts in center-aligned mode, and the output compare interrupt flag bit is set to 1 when up-counting. 11: Center-aligned mode 3. The counter counts in center-aligned mode, and the output compare interrupt flag bit is set to 1 when up-counting or down-counting. *Note: switching from edge-aligned mode to center-aligned mode is not allowed when the counter is still enabled (TIMx_CTRL1.CNTEN = 1).*
1	DIR	Direction 0: Up-counting 1: Down-counting *Note: this bit is read-only when the counter is configured in center-aligned mode or encoder mode.*
0	CNTEN	Counter Enable

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Bit Field	Name	Description
		0: Disable counter 1: Enable counter *Note: external clock, gating mode and encoder mode can only work after TIMx_CTRL1.CNTEN bit is set in the software. Trigger mode can automatically set TIMx_CTRL1.CNTEN bit by hardware.* *Note: After setting the CNTEN bit in the software, it is necessary to wait for at least two TIMx_CLK cycles for the CNTEN synchronisation from TIMx_PCLK to TIMx_CLK to take effect.*

12.4.3 Control Register 2 (TIMx_CTRL2)

Offset address: 0x04

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved												TI1SEL	CCPCTL	CCDSEL	CCUSEL
												rw	rw	rw	rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MMSEL[3:0]				Reserved				OI4N	OI4	OI3N	OI3	OI2N	OI2	OI1N	OI1
rw								rw	rw	rw	rw	rw	rw	rw	rw

Bit Field	Name	Description
31:20	Reserved	Reserved, the reset value must be maintained
19	TI1SEL	TI1 selection 0: TIMx_CH1 pin connected to TI1 input. 1: TIMx_CH1, TIMx_CH2, and TIMx_CH3 pins are XOR connected to the TI1 input.
18	CCPCTL	Capture/compare preloaded control 0: CCxEN, CCxNEN and OCxMD bits are not preloaded. 1: CCxEN, CCxNEN and OCxMD bits are preloaded. they are updated only when a commutation event COM occurs (CCUDGN bit set or rising edge on TRGI depending on CCUSEL bit) *Note: this bit only applied to channels with complementary outputs.*
17	CCDSEL	Capture/compare DMA selection 0: When a CCx event occurs, a DMA request for CCx is sent. 1: When an update event occurs, a DMA request for CCx is sent.
16	CCUSEL	Capture/compare control update selection 0: If TIMx_CTRL2.CCPCTL = 1, they can only be updated by setting CCUDGN bit 1: If TIMx_CTRL2.CCPCTL = 1, they can be updated by setting CCUDGN bit or a rising edge on TRGI. *Note: this bit only applied to channels with complementary outputs.*
15:12	MMSEL[3:0]	Master Mode Selection These 4 bits are used to select the synchronization information (TRGO) sent to the slave timer in

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Bit Field	Name	Description
		the master mode. Possible combinations are as follows: 0000: Reset –When the TIMx_EVTGEN.UDGN is set or a reset is generated by the slave mode controller, a TRGO pulse occurs. And in the latter case, the signal on TRGO is delayed compared to the actual reset. 0001: Enable - The TIMx_CTRL1.CNTEN bit is used as the trigger output (TRGO). Sometimes you need to start multiple timers at the same time or enable slave timer for a period of time. The counter enable signal is set when TIMx_CTRL1.CNTEN bit is set or the trigger input in gated mode is high. When the counter enable signal is controlled by the trigger input, there is a delay on TRGO except if the master/slave mode is selected (refer to the description of the TIMx_SMCTRL.MSMD bit). 0010: Update - The update event is selected as the trigger output (TRGO). For example, a master timer clock can be used as a slave timer prescaler. 0011: Compare pulse - Triggers the output to send a positive pulse (TRGO) when the TIMx_STS.CC1ITF is to be set (even if it is already high), when a capture or a comparison succeeds. 0100: Compare - OC1REF signal is used as the trigger output (TRGO). 0101: Compare - OC2REF signal is used as the trigger output (TRGO). 0110: Compare - OC3REF signal is used as the trigger output (TRGO). 0111: Compare - OC4REF signal is used as the trigger output (TRGO). 1xxx: Compare-If the counter is center-aligned mode: The corresponding edge signal of OC4REF/OC7REF/OC8REF/OC9REF used as the trigger output (TRGO), up counting and down counting are configurable, refer specifically to the TIMx_CTRL1.CMODE. If the counter is edge alignment mode: The OC4REF signal is used as the trigger output (TRGO).
11:8	Reserved	Reserved, the reset value must be maintained
7	OI4N	Output idle state 4 (OC4N output). Refer to TIMx_CTRL2.OI1N bit.
6	OI4	Output idle state 4 (OC4 output). Refer to TIMx_CTRL2.OI1 bit.
5	OI3N	Output idle state 3 (OC3N output). Refer to TIMx_CTRL2.OI1N bit.
4	OI3	Output idle state 3 (OC3 output). Refer to TIMx_CTRL2.OI1 bit.
3	OI2N	Output idle state 2 (OC2N output). Refer to TIMx_CTRL2.OI1N bit.
2	OI2	Output idle state 2 (OC2 output). Refer to TIMx_CTRL2.OI1 bit.
1	OI1N	Output Idle state 1 (OC1N Output) 0: When TIMx_BKDT.MOEN = 0, after dead-time OC1N = 0 1: When TIMx_BKDT.MOEN = 0, after dead-time OC1N = 1 *Note: Once TIMx_BKDT.LCKCFG level 1, 2, or 3 has been set, this bit cannot be modified.*
0	OI1	Output Idle state 1 0: When TIMx_BKDT.MOEN = 0, if OC1N is implemented, after dead-time OC1 = 0 1: When TIMx_BKDT.MOEN = 0, if OC1N is implemented, after dead-time OC1 = 1 *Note: Once TIMx_BKDT.LCKCFG level 1, 2, or 3 has been set, this bit cannot be modified.*

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12.4.4 Status Register (TIMx_STS)

Offset address: 0x08

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved				IOMBITF	Reserved		CC7ITF	COMP BITF	PBKPITF	LBKPITF	Reserved	BITF	TITF	COMITF	UDITF
				rc_w0			rc_w0	rc_w0	rc_w0	rc_w0		rc_w0	rc_w0	rc_w0	rc_w0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved				CC4OCF	CC3OCF	CC2OCF	CC1OCF	Reserved		CC6ITF	CC5ITF	CC4ITF	CC3ITF	CC2ITF	CC1ITF
				rc_w0	rc_w0	rc_w0	rc_w0			rc_w0	rc_w0	rc_w0	rc_w0	rc_w0	rc_w0

Bit Field	Name	Description
31:28	Reserved	Reserved, the reset value must be maintained
27	IOMBITF	IOM Break interrupt flag This bit is set by hardware once the IOM break input is active. This bit is cleared by software when the break input becomes inactive. 0: No break event occurred 1: An active level has been detected on IOM break input
26:25	Reserved	Reserved, the reset value must be maintained
24	CC7ITF	Capture/Compare 7 overcapture flag Refer to TIMx_STS.CC1OCF description.
23	COMPBITF	COMP Break interrupt flag This bit is set by hardware once the COMP break input is active. This bit is cleared by software when the break input becomes inactive. 0: No break event occurred 1: An active level has been detected on COMP break input
22	PBKPITF	PVD Break interrupt flag This bit is set by hardware once the PVD break input is active. This bit is cleared by software when the break input becomes inactive. 0: No break event occurred 1: An active level has been detected on PVD break input
21	LBKPITF	Lockup Break interrupt flag This bit is set by hardware once the Lockup break input is active. This bit is cleared by software when the break input becomes inactive. 0: No break event occurred 1: An active level has been detected on Lockup break input
20	Reserved	Reserved, the reset value must be maintained
19	BITF	Break1 interrupt flag This bit is set by hardware once the break1 input is active. This bit is cleared by software when the break input becomes inactive.

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Bit Field	Name	Description
		0: No break1 event occurred 1: An active level has been detected on break input
18	TITF	Trigger interrupt flag When a trigger event occurs (when an effective edge is detected at the TRGI input, except in gated mode, or any edge in gated mode) the hardware sets this bit to '1'. It is cleared by software to '0'. 0: No trigger event occurred 1: Trigger interrupt pending
17	COMITF	COM interrupt flag This bit is set by hardware once a COM event is generated (when TIMx_CCEN.CCxEN, TIMx_CCEN.CCxNEN, TIMx_CCMOD1.OCxMD have been updated). This bit is cleared by software. 0: No COM event occurred 1: COM interrupt pending
16	UDITF	Update interrupt flag This bit is set by hardware when an update event occurs under the following conditions: –When TIMx_CTRL1.UPDIS = 0, and repeat counter value overflow or underflow (An update event is generated when the repeat counter equals 0). –When TIMx_CTRL1.UPRS = 0, TIMx_CTRL1.UPDIS = 0, and set the TIMx_EVTGEN.UDGN bit by software to reinitialize the CNT. –When TIMx_CTRL1.UPRS = 0, TIMx_CTRL1.UPDIS = 0, and the counter CNT is reinitialized by the trigger event. (See TIMx_SMCTRL Register description) This bit is cleared by software. 0: No update event occurred 1: Update interrupt occurred
15:12	Reserved	Reserved, the reset value must be maintained
11	CC4OCF	Capture/Compare 4 overcapture flag Refer to TIMx_STS.CC1OCF description.
10	CC3OCF	Capture/Compare 3 overcapture flag Refer to TIMx_STS.CC1OCF description.
9	CC2OCF	Capture/Compare 2 overcapture flag Refer to TIMx_STS.CC1OCF description.
8	CC1OCF	Capture/Compare 1 overcapture flag This bit is set by hardware only when the corresponding channel is configured in input capture mode. Cleared by software writing 0. 0: No overcapture occurred 1: TIMx_STS.CC1ITF was already set when the value of the counter has been captured in the TIMx_CCDAT1 register.
7:6	Reserved	Reserved, the reset value must be maintained
5	CC6ITF	Capture/Compare 6 interrupt flag Refer to TIMx_STS.CC1ITF description.
4	CC5ITF	Capture/Compare 5 interrupt flag Refer to TIMx_STS.CC1ITF description.

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Bit Field	Name	Description
3	CC4ITF	Capture/Compare 4 interrupt flag Refer to TIMx_STS.CC1ITF description.
2	CC3ITF	Capture/Compare 3 interrupt flag Refer to TIMx_STS.CC1ITF description.
1	CC2ITF	Capture/Compare 2 interrupt flag Refer to TIMx_STS.CC1ITF description.
0	CC1ITF	Capture/Compare 1 interrupt flag **If channel CC1 is configured as an output mode:** Except in center-aligned mode, this bit is set by hardware when the counter value is the same as the compare value (see TIMx_CTRL1.CAMSEL bit description). This bit is cleared by software. 0: No match occurred. 1: The value of TIMx_CNT is the same as the value of TIMx_CCDAT1. When the value of TIMx_CCDAT1 is greater than the value of TIMx_AR, the TIMx_STS.CC1ITF bit will go high if the counter overflows (in up-counting and up/down-counting modes) and underflows in down-counting mode. **If channel CC1 is configured as an input mode:** This bit is set by hardware when the capture event occurs. This bit is cleared by software or by reading TIMx_CCDAT1. 0: No input capture occurred. 1: Input capture occurred. Counter value has captured in the TIMx_CCDAT1. An edge with the same polarity as selected has been detected on IC1.

12.4.5 Event Generation Register (TIMx_EVTGEN)

Offset address: 0x0C

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved				BGN	TGN	CCUDGN	UDGN	Reserved				CC4GN	CC3GN	CC2GN	CC1GN
				w	w	w	w					w	w	w	w

Bit Field	Name	Description
31:12	Reserved	Reserved, the reset value must be maintained
11	BGN	Break1 generation This bit can generate a break1 event when set by software. And at this time TIMx_BKDT.MOEN = 0, TIMx_STS.BITF = 1, if the corresponding interrupt and DMA are enabled, the corresponding interrupt and DMA will be generated. This bit is automatically cleared by hardware. 0: No action

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Bit Field	Name	Description
		1: Generated a break1 event
10	TGN	Trigger generation This bit can generate a trigger event when set by software. And at this time TIMx_STS.TITF = 1, if the corresponding interrupt and DMA are enabled, the corresponding interrupt and DMA will be generated. This bit is automatically cleared by hardware. 0: No action 1: Generated a trigger event
9	CCUDGN	Capture/Compare control update generation This bit is set by software. And if TIMx_CTRL2.CCPCTL = 1 at this time, the CCxEN, CCxNEN and OCxMD bits are allowed to be updated. This bit is automatically cleared by hardware. 0: No action 1: Generated a COM event *Note: This bit is only valid for channels with complementary outputs.*
8	UDGN	Update generation This bit is set to '1' by software and automatically cleared to '0' by hardware. This bit can generate an update event when set by software. And at this time the counter will be reinitialized, the prescaler counter will be cleared, the counter will be cleared in center-aligned or up-counting mode, but take TIMx_AR in down-counting mode the value of the register. This bit is automatically cleared by hardware. 0: No action 1: Generated an update event
7:4	Reserved	Reserved, the reset value must be maintained
3	CC4GN	Capture/Compare 4 generation See TIMx_EVTGEN.CC1GN description.
2	CC3GN	Capture/Compare 3 generation See TIMx_EVTGEN.CC1GN description.
1	CC2GN	Capture/Compare 2 generation See TIMx_EVTGEN.CC1GN description.
0	CC1GN	Capture/Compare 1 generation This bit can generate a capture/compare event when set by software. This bit is automatically cleared by hardware. **When the corresponding channel of CC1 is in output mode:** The TIMx_STS.CC1ITF flag will be set to 1, if the corresponding interrupt and DMA are enabled, the corresponding interrupt and DMA will be generated. **When the corresponding channel of CC1 is in input mode:** TIMx_CCDAT1 will capture the current counter value, and the TIMx_STS.CC1ITF flag will be set to 1, if the corresponding interrupt and DMA are enabled, the corresponding interrupt and DMA will be generated. If the TIMx_STS.CC1ITF is already pulled high, pull TIMx_STS.CC1OCF high. 0: No action 1: Generated a CC1 capture/compare event

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12.4.6 Slave Mode Control Register (TIMx_SMCTRL)

Offset address: 0x10

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															MSMD
															rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EXTF[3:0]				EXTP	EXCEN	EXTPS		SMSEL[3:0]				Reserved	TSEL[2:0]		
rw				rw	rw	rw		rw					rw		

Bit Field	Name	Description
31:17	Reserved	Reserved, the reset value must be maintained
16	MSMD	Master/slave mode 0: No action 1: Events on the trigger input (TRGI) are delayed to allow a perfect synchronization between the current timer (via TRGO) and its slaves. This is useful when several timers are required to be synchronized to a single external event.
15:12	EXTF[3:0]	External trigger filter These bits define the length of the ETRP digital filter (the RCC_TIMFILTCFG.TIM1FILTCLK[4:0] register determines the sampling frequency of the corresponding digital filter). The digital filter consists of an event counter which generates an output transition after recording N events: 0000：No filter, sampled using TIM's internal operating clock 0001：N=1 0010：N=2 0011：N=3 0100：N=4 0101：N=5 0110：N=6 0111：N=7 1xxx：N=8
11	EXTP	External trigger polarity This bit is used to select whether the trigger operation is to use tim_etr_in or the inversion of tim_etr_in. 0: tim_etr_in active at high level or rising edge. 1: tim_etr_in active at low level or falling edge.
10	EXCEN	External clock enable This bit is used to enable external clock mode 2, and the counter is driven by any active edge on the ETRF signal in this mode.

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Bit Field	Name	Description
		0: External clock mode 2 disable. 1: External clock mode 2 enable. *Note 1: when external clock mode 1 and external clock mode 2 are enabled at the same time, the input of the external clock is ETRF.* *Note 2: the following slave modes can be used simultaneously with external clock mode 2: reset mode, gated mode and trigger mode; However, TRGI cannot connect to ETRF (TIMx_SMCTRL.TSEL ≠ '111').* *Note 3: setting the TIMx_SMCTRL.EXCEN bit has the same effect as selecting external clock mode 1 and connecting TRGI to ETRF (TIMx_SMCTRL.SMSEL = 0111 and TIMx_SMCTRL.TSEL = 111).*
9:8	EXTPS[1:0]	External trigger prescaler The frequency of the external trigger signal ETRP must be at most 1/4 of TIMxCLK frequency. When a faster external clock is input, a prescaler can be used to reduce the frequency of ETRP. 00: Prescaler disable 01: ETRP frequency divided by 2 10: ETRP frequency divided by 4 11: ETRP frequency divided by 8
7:4	SMSEL[3:0]	Slave mode selection When an external signal is selected, the active edge of the trigger signal (TRGI) is linked to the selected external input polarity (refer to input control register and control register description) 0000: Disable slave mode. If TIMx_CTRL1.CNTEN = 1, the prescaler is driven directly by the internal clock. 0001: Encoder mode 1. According to the level of TI2FP2, the counter up-counting or down-counting on the edge of TI1FP1. 0010: Encoder mode 2. According to the level of TI1FP1, the counter up-counting or down-counting on the edge of TI2FP2. 0011: Encoder mode 3. According to the input level of another signal, the counter up-counting or down-counting on the edges of TI2FP1 and TI2FP2. 0100: Reset mode. On the rising edge of the selected trigger input (TRGI), the counter is reinitialized and the shadow register is updated. 0101: Gated mode. When the trigger input (TRGI) is high, the clock of the counter is enabled. Once the trigger input becomes low, the counter stops counting, but is not reset. In this mode, the start and stop of the counter are controlled. 0110: Trigger mode. When a rising edge occurs on the trigger input (TRGI), the counter is started but not reset. In this mode, only the start of the counter is controlled. 0111: External clock mode 1. The counter is clocked by the rising edge of the selected trigger input (TRGI). 1000~1100：Reserved. 1101: Combined Gated + Reset mode, the counter is enabled when the trigger input (TRGI) is high. Once the trigger input goes low, the counter stops (and resets). The start and stop of the counter are both controlled. 1110: Combined Reset + Trigger Mode - The counter starts (and resets) on the rising edge of the

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Bit Field	Name	Description
		trigger input TRGI, only the start of the counter is controlled. 1111：Reserved. *Note: do not use gated mode if TI1F_ED is selected as the trigger input (TIMx_SMCTRL.TSEL=100). This is because TI1F_ED outputs a pulse for each TI1F transition, whereas gated mode checks the level of the triggered input.*
3	Reserved	Reserved, the reset value must be maintained

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2:0	TSEL[2:0]	Trigger selection These 3 bits are used to select the trigger input of the synchronous counter. 000：Internal trigger 0（ITR0） 001：Internal trigger 1（ITR1） 010：Internal trigger 2（ITR2） 011：Internal trigger 3（ITR3） 100: TI1 edge detector (TI1F_ED) 101: Filtered timer input 1 (TI1FP1) 110: Filtered timer input 2 (TI2FP2) 111: External triggered Input (ETRF) For further details regarding ITRx, see **Table 12-3** *Note: these bits must be changed only when not in use (e. g. TIMx_SMCTRL.SMSEL=0000) to avoid false edge detection at the transition.*

Table 12-3 Internal trigger connection for TIMx

Slave timer	ITR0 (TSEL = 000)	ITR1 (TSEL = 001)	ITR2 (TSEL = 010)	ITR3 (TSEL = 011)
TIM1	TIM3	NA	NA	NA
TIM3	TIM1	NA	NA	NA
TIM4	NA	NA	NA	NA

12.4.7 DMA/Interrupt Enable Register (TIMx_DINTEN)

Offset address: 0x14

Reset values: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved									COMIEN	TDEN	COMDEN	UDEN	BIEN	TIEN	UIEN
									rw	rw	rw	rw	rw	rw	rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved				CC4DEN	CC3DEN	CC2DEN	CC1DEN	Reserved	CC7IEN	CC6IEN	CC5IEN	CC4IEN	CC3IEN	CC2IEN	CC1IEN
				rw	rw	rw	rw		rw	rw	rw	rw	rw	rw	rw

Bit Field	Name	Description
31:23	Reserved	Reserved, the reset value must be maintained
22	COMIEN	COM interrupt enable 0: Disable COM interrupt 1: Enable COM interrupt
21	TDEN	Trigger DMA request enable 0: Disable trigger DMA request 1: Enable trigger DMA request
20	COMDEN	COM DMA request enable 0: Disable COM DMA request

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Bit Field	Name	Description
		1: Enable COM DMA request
19	UDEN	Update DMA request enable 0: Disable update DMA request 1: Enable update DMA request
18	BIEN	Break interrupt enable 0: Disable break interrupt 1: Enable break interrupt
17	TIEN	Trigger interrupt enable 0: Disable trigger interrupt 1: Enable trigger interrupt
16	UIEN	Update interrupt enable 0: Disable update interrupt 1: Enables update interrupt
15:12	Reserved	Reserved, the reset value must be maintained
11	CC4DEN	Capture/Compare 4 DMA request enable 0: Disable capture/compare 4 DMA request 1: Enable capture/compare 4 DMA request
10	CC3DEN	Capture/Compare 3 DMA request enable 0: Disable capture/compare 3 DMA request 1: Enable capture/compare 3 DMA request
9	CC2DEN	Capture/Compare 2 DMA request enable 0: Disable capture/compare 2 DMA request 1: Enable capture/compare 2 DMA request
8	CC1DEN	Capture/Compare 1 DMA request enable 0: Disable capture/compare 1 DMA request 1: Enable capture/compare 1 DMA request
7	Reserved	Reserved, the reset value must be maintained
6	CC7IEN	Capture/Compare 7 interrupt enable 0: Disable capture/compare 7 interrupt 1: Enable capture/compare 7 interrupt
5	CC6IEN	Capture/Compare 6 interrupt enable 0: Disable capture/compare 6 interrupt 1: Enable capture/compare 6 interrupt
4	CC5IEN	Capture/Compare 5 interrupt enable 0: Disable capture/compare 5 interrupt 1: Enable capture/compare 5 interrupt
3	CC4IEN	Capture/Compare 4 interrupt enable 0: Disable capture/compare 4 interrupt 1: Enable capture/compare 4 interrupt
2	CC3IEN	Capture/Compare 3 interrupt enable 0: Disable capture/compare 3 terrupt 1: Enable capture/compare 3 nterrupt
1	CC2IEN	Capture/Compare 2 interrupt enable

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Bit Field	Name	Description
		0: Disable capture/compare 2 nterrupt 1: Enable capture/compare 2 nterrupt
0	CC1IEN	Capture/Compare 1 interrupt enable 0: Disable capture/compare 1 nterrupt 1: Enable capture/compare 1 nterrupt

12.4.8 Capture/Compare Mode Register 1 (TIMx_CCMOD1)

Offset address: 0x18

Reset value: 0x0000 0000

Channels can be used for input (capture mode) or output (compare mode), and the direction of the channel is defined by the corresponding CCxSEL bit. The other bits of the register act differently in input and output modes. OCx describes the function of a channel in output mode, ICx describes the function of a channel in input mode. Hence, please note that the same bit can have different meanings for output mode and for input mode.

Output compare mode:

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OC2MD[2:0]			OC2CEN	OC2FEN	OC2PEN	CC2SEL[1:0]		OC1MD[2:0]			OC1CEN	OC1FEN	OC1PEN	CC1SEL[1:0]	
rw			rw	rw	rw	rw		rw			rw	rw	rw	rw	

Bit Field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained
15:13	OC2MD[2:0]	Output Compare 2 mode
12	OC2CEN	Output Compare 2 clear enable
11	OC2FEN	Output Compare 2 fast enable
10	OC2PEN	Output Compare 2 preload enable
9:8	CC2SEL[1:0]	Capture/Compare 2 selection These bits are used to select the input/output and input mapping of the channel 00: CC2 channel is configured as output 01: CC2 channel is configured as input, IC2 is mapped on TI2 10: CC2 channel is configured as input, IC2 is mapped on TI1 11: CC2 channel is configured as input, IC2 is mapped on TRC. This mode is only active when the internal trigger input is selected by TIMx_SMCTRL.TSEL. *Note: CC2SEL is writable only when the channel is off (TIMx_CCEN.CC2EN = 0).*
7:5	OC1MD[2:0]	Output Compare 1 mode These bits are used to manage the output reference signal OC1REF, which determines the values of OC1 and OC1N, and is valid at high levels, while the active levels of OC1 and OC1N depend on the TIMx_CCEN.CC1P and TIMx_CCEN.CC1NP bits. 000: Frozen. Comparison between TIMx_CCDAT1 register and counter TIMx_CNT has no

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Bit Field	Name	Description
		effect on OC1REF signal. 001: Set channel 1 to the active level on match. When TIMx_CCDAT1 = TIMx_CNT, OC1REF signal will be forced high. 010: Set channel 1 as inactive level on match. When TIMx_CCDAT1 = TIMx_CNT, OC1REF signal will be forced low. 011: Toggle. When TIMx_CCDAT1 = TIMx_CNT, OC1REF signal will be toggled. 100: Force to inactive level. OC1REF signal is forced low. 101: Force to active level. OC1REF signal is forced high. 110: PWM mode 1 - In up-counting mode, if TIMx_CNT < TIMx_CCDAT1, OC1REF signal of channel 1 is high, otherwise it is low. In down-counting mode, if TIMx_CNT > TIMx_CCDAT1, OC1REF signal of channel 1 is low, otherwise it is high. 111: PWM mode 2 - In up-counting mode, if TIMx_CNT < TIMx_CCDAT1, OC1REF signal of channel 1 is low, otherwise it is high. In down-counting mode, if TIMx_CNT > TIMx_CCDAT1, OC1REF signal of channel 1 is high, otherwise it is low. *Note 1: In PWM mode 1 or PWM mode 2, the OC1REF level changes only when the comparison result changes or when the output compare mode is switched from frozen mode to PWM mode.*
4	OC1CEN	Output Compare 1 clear enable 0: OC1REF is not affected by tim_ocref_clr_in input level 1: OC1REF is cleared immediately when the tim_ocref_clr_in input level is detected as high (tim_ocref_clr_in is controlled by the TIMx_CTRL1.CLRSEL register).
3	OC1FEN	Output Compare 1 fast enable This bit is used to speed up the response of the CC output to the trigger input event. 0: CC1 behaves normally depending on the counter and CCDAT1 values, even if the trigger is ON. The minimum delay for activating CC1 output when an edge occurs on the trigger input is 5 clock cycles. 1: An active edge of the trigger input acts like a comparison match on CC1 output. Therefore, OC is set to the comparison level regardless of the comparison result. The delay time for sampling the trigger input and activating the CC1 output is reduced to 3 clock cycles. OCxFEN only works if the channel is configured in PWM1 or PWM2 mode.
2	OC1PEN	Output Compare 1 preload enable 0: Disable preload function of TIMx_CCDAT1 register. Supports write operations to TIMx_CCDAT1 register at any time, and the written value is effective immediately. 1: Enable preload function of TIMx_CCDAT1 register. Only read and write operations to preload registers. When an update event occurs, the value of TIMx_CCDAT1 is loaded into the active register. *Note 1: Only when TIMx_CTRL1.ONEPM = 1(In one-pulse mode), PWM mode can be used without verifying the preload register, otherwise no other behavior can be predicted.*
1:0	CC1SEL[1:0]	Capture/compare 1 selection These bits are used to select the input/output and input mapping of the channel 00: CC1 channel is configured as output 01: CC1 channel is configured as input, IC1 is mapped on TI1 10: CC1 channel is configured as input, IC1 is mapped on TI2

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Bit Field	Name	Description
		11: CC1 channels are configured as inputs and IC1 is mapped to TRC. This mode is only active when the internal trigger input is selected by TIMx_SMCTRL.TSEL. *Note: CC1SEL is writable only when the channel is off (TIMx_CCEN.CC1EN = 0).*

Intput capture mode:

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IC2F[3:0]				IC2PSC[1:0]		CC2SEL[1:0]		IC1F[3:0]				IC1PSC[1:0]		CC1SEL[1:0]	
rw				rw		rw		rw				rw		rw	

Bit Field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained
15:12	IC2F[3:0]	Input capture 2 filter
11:10	IC2PSC[1:0]	Input capture 2 prescaler
9:8	CC2SEL[1:0]	Capture/Compare 2 selection These bits are used to select the input/output and input mapping of the channel 00: CC2 channel is configured as output 01: CC2 channel i s configured as input, IC2 is mapped on TI2 10: CC2 channel is configured as input, IC2 is mapped on TI1 11: CC2 channel is configured as input, IC2 is mapped on TRC. This mode is only active when the internal trigger input is selected by TIMx_SMCTRL.TSEL. *Note: CC2SEL is writable only when the channel is off (TIMx_CCEN.CC2EN = 0).*
7:4	IC1F[3:0]	Input Capture 1 filter These bits define the length of the ETRP digital filter (the RCC_TIMFILTCFG.TIM1FILTCLK[4:0] register determines the sampling frequency of the corresponding digital filter). The digital filter consists of an event counter which generates an output transition after recording N events: 0000：No filter, sampled using TIM's internal operating clock 0001：N=1 0010：N=2 0011：N=3 0100：N=4 0101：N=5 0110：N=6 0111：N=7 1xxx：N=8
3:2	IC1PSC[1:0]	Input Capture 1 prescaler

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		These bits are used to select the ratio of the prescaler for IC1 (CC1 input). When TIMx_CCEN.CC1EN = 0, the prescaler will be reset. 00: No prescaler, capture is done each time an edge is detected on the capture input 01: Capture is done once every 2 events 10: Capture is done once every 4 events 11: Capture is done once every 8 events
1:0	CC1SEL[1:0]	Capture/Compare 1 selection These bits are used to select the input/output and input mapping of the channel 00: CC1 channel is configured as output 01: CC1 channel is configured as input, IC1 is mapped on TI1 10: CC1 channel is configured as input, IC1 is mapped on TI2 11: CC1 channel is configured as input, IC1 is mapped to TRC. This mode is only active when the internal trigger input is selected by TIMx_SMCTRL.TSEL. *Note: CC1SEL is writable only when the channel is off (TIMx_CCEN.CC1EN = 0).*

12.4.9 Capture/Compare Mode Register 2 (TIMx_CCMOD2)

Offset address: 0x1C

Reset value: 0x0000 0000

Refer to the description of the CCMOD1 register above.

Output compare mode:

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OC4MD[2:0]			OC4CEN	OC4FEN	OC4PEN	CC4SEL[1:0]		OC3MD[2:0]			OC3CEN	OC3FEN	OC3PEN	CC3SEL[1:0]	
rw			rw	rw	rw	rw		rw			rw	rw	rw	rw	

Bit Field	**Name**	**Description**
31:16	Reserved	Reserved, the reset value must be maintained
15:13	OC4MD[2:0]	Output compare 4 mode
12	OC4CEN	Output compare 4 clear enable
11	OC4FEN	Output compare 4 fast enable
10	OC4PEN	Output compare 4 preload enable
9:8	CC4SEL[1:0]	Capture/Compare 4 selection These bits are used to select the input/output and input mapping of the channel 00: CC4 channel is configured as output 01: CC4 channel is configured as input, IC4 is mapped on TI4 10: CC4 channel is configured as input, IC4 is mapped on TI3 11: CC4 channel is configured as input, IC4 is mapped on TRC. This mode is only active when the internal trigger input is selected by TIMx_SMCTRL.TSEL. Note: CC4SEL is writable only when the channel is off (TIMx_CCEN.CC4EN = 0).

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Bit Field	Name	Description
7:5	OC3MD[2:0]	Output compare 3 mode
4	OC3CEN	Output compare 3 clear enable
3	OC3FEN	Output compare 3 fast enable
2	OC3PEN	Output compare 3 preload enable
1:0	CC3SEL[1:0]	Capture/Compare 3 selection These bits are used to select the input/output and input mapping of the channel 00: CC3 channel is configured as output 01: CC3 channel is configured as input, IC3 is mapped to TI3 10: CC3 channel is configured as input, IC3 is mapped on TI4 11: CC3 channel is configured as input, IC3 is mapped to TRC. This mode is only active when the internal trigger input is selected by TIMx_SMCTRL.TSEL. *Note: CC3SEL is writable only when the channel is off (TIMx_CCEN.CC3EN = 0).*

Input capture mode:

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IC4F[3:0]				IC4PSC[1:0]		CC4SEL[1:0]		IC3F[3:0]				IC3PSC[1:0]		CC3SEL[1:0]	
rw				rw		rw		rw				rw		rw	

Bit Field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained
15:12	IC4F[3:0]	Input capture 4 filter
11:10	IC4PSC[1:0]	Input capture 4 prescaler
9:8	CC4SEL[1:0]	Capture/Compare 4 selection These bits are used to select the input/output and input mapping of the channel 00: CC4 channel is configured as output 01: CC4 channel is configured as input, IC4 is mapped on TI4 10: CC4 channel is configured as input, IC4 is mapped on TI3 11: CC4 channel is configured as input, IC4 is mapped on TRC. This mode is only active when the internal trigger input is selected by TIMx_SMCTRL.TSEL. *Note: CC4SEL is writable only when the channel is off (TIMx_CCEN.CC4EN = 0).*
7:4	IC3F[3:0]	Input capture 3 filter
3:2	IC3PSC[1:0]	Input capture 3 prescaler
1:0	CC3SEL[1:0]	Capture/compare 3 selection These bits are used to select the input/output and input mapping of the channel 00: CC3 channel is configured as output 01: CC3 channel is configured as input, IC3 is mapped to TI3 10: CC3 channel is configured as input, IC3 is mapped on TI4 11: CC3 channel is configured as input, IC3 is mapped to TRC. This mode is only active when

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Bit Field	Name	Description
		the internal trigger input is selected by TIMx_SMCTRL.TSEL. *Note: CC3SEL is writable only when the channel is off (TIMx_CCEN.CC3EN = 0).*

12.4.10 Capture/Compare Mode Register 3 (TIMx_CCMOD3)

Offset address: 0x20

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved				OC7MD[2:0]			Reserved						OC7CEN	OC7FEN	OC7PEN
					rw								rw	rw	rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OC6MD[2:0]			OC6CEN	OC6FEN	OC6PEN	Reserved		OC5MD[2:0]			OC5CEN	OC5FEN	OC5PEN	Reserved	
	rw		rw	rw	rw				rw		rw	rw	rw		

Bit Field	Name	Description
31:28	Reserved	Reserved, the reset value must be maintained
27:25	OC7MD[2:0]	Output compare 7 mode
24:19	Reserved	Reserved, the reset value must be maintained
18	OC7CEN	Output compare 7 clear enable
17	OC7FEN	Output compare 7 fast enable
16	OC7PEN	Output compare 7 preload enable
15:13	OC6MD[2:0]	Output compare 6 mode
12	OC6CEN	Output compare 6 clear enable
11	OC6FEN	Output compare 6 fast enable
10	OC6PEN	Output compare 6 preload enable
9:8	Reserved	Reserved, the reset value must be maintained
7:5	OC5MD[2:0]	Output compare 5 mode
4	OC5CEN	Output compare 5 clear enable
3	OC5FEN	Output compare 5 fast enable
2	OC5PEN	Output compare 5 preload enable
1:0	Reserved	Reserved, the reset value must be maintained

12.4.11 Capture/Compare Enable Register (TIMx_CCEN)

Offset address: 0x24

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved								CC6P	CC6EN	Reserved		CC5P	CC5EN	Reserved	

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								rw	rw			rw	rw		
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CC4P	CC4EN	CC4NP	CC4NEN	CC3P	CC3EN	CC3NP	CC3NEN	CC2P	CC2EN	CC2NP	CC2NEN	CC1P	CC1EN	CC1NP	CC1NEN
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Bit Field	Name	Description
31:24	Reserved	Reserved, the reset value must be maintained
23	CC6P	Capture/Compare 6 output polarity See TIMx_CCEN.CC1P description.
22	CC6EN	Capture/Compare 6 output enable See TIMx_CCEN.CC1EN description.
21:20	Reserved	Reserved, the reset value must be maintained
19	CC5P	Capture/Compare 5 output polarity See TIMx_CCEN.CC1P description.
18	CC5EN	Capture/Compare 5 output enable See TIMx_CCEN.CC1EN description.
17:16	Reserved	Reserved, the reset value must be maintained
15	CC4P	Capture/Compare 4 output polarity See TIMx_CCEN.CC1P description.
14	CC4EN	Capture/Compare 4 output enable See TIMx_CCEN.CC1EN description.
13	CC4NP	Capture/Compare 4 complementary output polarity See TIMx_CCEN.CC1NP description.
12	CC4NEN	Capture/Compare 4 complementary output enable See TIMx_CCEN.CC1NEN description.
11	CC3P	Capture/Compare 3 output polarity See TIMx_CCEN.CC1P description.
10	CC3EN	Capture/Compare 3 output enable See TIMx_CCEN.CC1EN description.
9	CC3NP	Capture/Compare 3 complementary output polarity See TIMx_CCEN.CC1NP description.
8	CC3NEN	Capture/Compare 3 complementary output enable See TIMx_CCEN.CC1NEN description.
7	CC2P	Capture/Compare 2 output polarity See TIMx_CCEN.CC1P description.
6	CC2EN	Capture/Compare 2 output enable See TIMx_CCEN.CC1EN description.
5	CC2NP	Capture/Compare 2 complementary output polarity See TIMx_CCEN.CC1NP description.
4	CC2NEN	Capture/Compare 2 complementary output enable See TIMx_CCEN.CC1NEN description.
3	CC1P	Capture/Compare 1 output polarity

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Bit Field	Name	Description
		When the corresponding channel of CC1 is in output mode: 0: OC1 active high 1: OC1 active low **When the corresponding channel of CC1 is in input mode:** At this time, this bit is used to select whether IC1 or the inverse signal of IC1 is used as the trigger or capture signal. 0: non-inverted: Capture action occurs when IC1 generates a rising edge. When used as external trigger, IC1 is non-inverted. 1: inverted: Capture action occurs when IC1 generates a falling edge. When used as external trigger, IC1 is inverted. *Note: If TIMx_BKDT.LCKCFG = 3 or 2, these bits cannot be modified.*
2	CC1EN	Capture/Compare 1 output enable **When the corresponding channel of CC1 is in output mode:** 0: Disable - Disable output OC1 signal. The level of OC1 depends on the value of these bits TIMx_BKDT.MOEN, TIMx_BKDT.OSSI, TIMx_BKDT.OSSR, TIMx_CTRL2.OI1, TIMx_CTRL2.OI1N and TIMx_CCEN.CC1NEN. 1: Enable - Enable output OC1 signal. The level of OC1N depends on the value of these bits TIMx_BKDT.MOEN, TIMx_BKDT.OSSI, TIMx_BKDT.OSSR, TIMx_CTRL2.OI1, TIMx_CTRL2.OI1N and TIMx_CCEN.CC1NEN. **When the corresponding channel of CC1 is in input mode:** At this time, this bit is used to disable/enable the capture function. 0: Disable capture 1: Enable capture
1	CC1NP	Capture/Compare 1 complementary output polarity 0: OC1N active high 1: OC1N active low
0	CC1NEN	Capture/Compare 1 complementary output enable 0: Disable - Disable output OC1N signal. The level of OC1N depends on the value of these bits TIMx_BKDT.MOEN, TIMx_BKDT.OSSI, TIMx_BKDT.OSSR, TIMx_CTRL2.OI1, TIMx_CTRL2.OI1N and TIMx_CCEN.CC1EN. 1: Enable - Enable output OC1N signal. The level of OC1N depends on the value of these bits TIMx_BKDT.MOEN, TIMx_BKDT.OSSI, TIMx_BKDT.OSSR, TIMx_CTRL2.OI1, TIMx_CTRL2.OI1N and TIMx_CCEN.CC1EN.

Table 12-4 Output Control Bits of Complementary OCx and OCxN Channels with Break Function

Control Bits					Output State (1)	
MOEN	**OSSI**	**OSSR**	**CCxEN**	**CCxNEN**	**OCx Output State**	**OCxN Output State**
1	X	0	0	0	Output disabled (not driven by timer)	Output disabled (not driven by timer)
					OCx=0, OCx_EN=0	OCxN=0, OCxN_EN=0
		0	0	1	Output disabled (not driven by timer)	OCxREF + polarity
					OCx=0, OCx_EN=0	OCxN= OCxREF xor CCxNP, OCxN_EN=1
		0	1	0	OCxREF + polarity	Output disabled (not driven by timer)

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Control Bits					Output State (1)	
MOEN	OSSI	OSSR	CCxEN	CCxNEN	OCx Output State	OCxN Output State
					OCx= OCxREF xor CCxP, OCx_EN=1	OCxN=0, OCxN_EN=0
		0	1	1	OCxREF + polarity + dead-time, OCx_EN=1	Complementary to OCxREF + polarity + dead-time, OCxN_EN=1
		1	0	0	Output disabled (not driven by timer)	Output disabled (not driven by timer)
					OCx=CCxP, OCx_EN=0	OCxN=CCxNP, OCxN_EN=0
		1	0	1	Off-state (Output enabled with inactive state)	OCxREF + polarity
					OCx=CCxP, OCx_EN=1	OCxN= OCxREF xor CCxNP, OCxN_EN=1
		1	1	0	OCxREF + polarity	Off-state (Output enabled with inactive state)
					OCx= OCxREF xor CCxP, OCx_EN=1	OCxN=CCxNP, OCxN_EN=1
		1	1	1	OCxREF + polarity + dead-time OCx_EN=1	Complementary to OCxREF + polarity + dead-time OCxN_EN=1
0	0	X	0	0	Output disabled (not driven by timer)	
	0		0	1	Asynchronously: OCx=CCxP, OCx_EN=0, OCxN=CCxNP,OCxN_EN=0;	
	0		1	0	Then if the clock is present: if (CCxP ^ OIx) ^ (CCxNP^OIxN)! = 0,	
	0		1	1	OCx=OIx, OCxN=OIxN after a dead-time	
	1		0	0	Off-state (Output enabled with inactive state)	
	1		0	1	Asynchronously: OCx=CCxP, OCx_EN=1, OCxN=CCxNP,OCxN_EN=1;	
	1		1	0	Then if the clock is present: if (CCxP ^ OIx) ^ (CCxNP^OIxN)! = 0,	
	1		1	1	OCx=OIx , OCxN=OIxN after a dead-time	

Note: (1) If both outputs of a channel are not used (CCxEN = CCxNEN = 0), OIx, OIxN, CCxP and CCxNP must all be cleared.

Note: the status of external I/O pins connected to complementary OCx and OCxN channels depends on the OCx and OCxN channel states and GPIO and AFIO registers.

12.4.12 Capture/Compare Register 1 (TIMx_CCDAT1)

Offset address: 0x28

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CCDDAT1[15:0]															
rw															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CCDAT1[15:0]															

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rw

Bit Field	Name	Description
31:16	CCDDAT1[15:0]	Capture/Compare 1 down-counting value, dedicated to center-aligned asymmetric mode. ■ CC1 channel can only configured as output: CCDDAT1 contains the value to be compared to the counter TIMx_CNT (only when TIMx_CTRL1.DIR = 1 and in asymmetric mode), signal is sent out on the OC1 output. If the preload feature is not selected in TIMx_CCMOD1.OC1PEN bit, the written value is immediately transferred to the active register. Otherwise, this preloaded value is transferred to the active register only when an update event occurs.
15:0	CCDAT1[15:0]	Capture/Compare 1 value ■ CC1 channel is configured as output: CCDAT1 contains the value to be compared to the counter TIMx_CNT (except when TIMx_CTRL1.DIR = 1 and in asymmetric mode), signal is sent out on the OC1 output. If the preload feature is not selected in TIMx_CCMOD1.OC1PEN bit, the written value is immediately transferred to the active register. Otherwise, this preloaded value is transferred to the active register only when an update event occurs. ■ CC1 channel is configured as input: CCDAT1 contains the counter value transferred by the last input capture 1 event (IC1). When configured as input mode, register CCDAT1 and CCDDAT1 are only readable. When configured as output mode, register CCDAT1 and CCDDAT1 are readable and writable.

12.4.13 Capture/Compare Register 2 (TIMx_CCDAT2)

Offset address: 0x2C

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CCDDAT2[15:0]															
rw															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CCDAT2[15:0]															
rw															

Bit Field	Name	Description
31:16	CCDDAT2[15:0]	Capture/Compare 2 down-counting value, dedicated to center-aligned asymmetric mode ■ CC2 channel can only configured as output: CCDDAT2 contains the value to be compared to the counter TIMx_CNT (only when

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Bit Field	Name	Description
		TIMx_CTRL1.DIR = 1 and in asymmetric mode), signal is sent out on the OC2 output. If the preload feature is not selected in TIMx_CCMOD1.OC2PEN bit, the written value is immediately transferred to the active register. Otherwise, this preloaded value is transferred to the active register only when an update event occurs.
15:0	CCDAT2[15:0]	Capture/Compare 2 value ■ CC2 channel is configured as output: CCDAT2 contains the value to be compared to the counter TIMx_CNT (except when TIMx_CTRL1.DIR = 1 and in asymmetric mode), signal is sent out on the OC2 output. If the preload feature is not selected in TIMx_CCMOD1.OC2PEN bit, the written value is immediately transferred to the active register. Otherwise, this preloaded value is transferred to the active register only when an update event occurs. ■ CC2 channel is configured as input: CCDAT2 contains the counter value transferred by the last input capture 2 event (IC2). When configured as input mode, register CCDAT2 and CCDDAT2 are only readable. When configured as output mode, register CCDAT2 and CCDDAT2 are readable and writable.

12.4.14 Capture/Compare Register 3 (TIMx_CCDAT3)

Offset address: 0x30

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CCDDAT3[15:0]															
rw															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CCDAT3[15:0]															
rw															

Bit Field	Name	Description
31:16	CCDDAT3[15:0]	Capture/Compare 3 down-counting value, dedicated to center-aligned asymmetric mode ■ CC3 channel can only configured as output: CCDDAT3 contains the value to be compared to the counter TIMx_CNT (only when TIMx_CTRL1.DIR = 1 and in asymmetric mode), signal is sent out on the OC3 output. If the preload feature is not selected in TIMx_CCMOD2.OC3PEN bit, the written value is immediately transferred to the active register. Otherwise, this preloaded value is transferred to the active register only when an update event occurs.
15:0	CCDAT3[15:0]	Capture/Compare 3 value ■ CC3 channel is configured as output: CCDAT3 contains the value to be compared to the counter TIMx_CNT (except when TIMx_CTRL1.DIR = 1 and in asymmetric mode), signal is sent out on the OC3 output.

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Bit Field	Name	Description
		If the preload feature is not selected in TIMx_CCMOD2.OC3PEN bit, the written value is immediately transferred to the active register. Otherwise, this preloaded value is transferred to the active register only when an update event occurs. ■ CC3 channel is configured as input: CCDAT3 contains the counter value transferred by the last input capture 3 event (IC3). When configured as input mode, register CCDAT3 and CCDDAT3 are only readable. When configured as output mode, register CCDAT3 and CCDDAT3 are readable and writable.

12.4.15 Capture/Compare Register 4 (TIMx_CCDAT4)

Offset address: 0x34

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CCDDAT4[15:0]															
rw															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CCDAT4[15:0]															
rw															

Bit Field	Name	Description
31:16	CCDDAT4 [15:0]	Capture/Compare 4 down-counting value, dedicated to center-aligned asymmetric mode ■ CC4 channel can only configured as output: CCDDAT4 contains the value to be compared to the counter TIMx_CNT (only when TIMx_CTRL1.DIR = 1 and in asymmetric mode), signaling on the OC4 output. If the preload feature is not selected in TIMx_CCMOD2.OC4PEN bit, the written value is immediately transferred to the active register. Otherwise, this preloaded value is transferred to the active register only when an update event occurs.
15:0	CCDAT4[15:0]	Capture/Compare 4 value ■ CC4 channel is configured as output: CCDAT4 contains the value to be compared to the counter TIMx_CNT (except when TIMx_CTRL1.DIR = 1 and in asymmetric mode), signaling on the OC4 output. If the preload feature is not selected in TIMx_CCMOD2.OC4PEN bit, the written value is immediately transferred to the active register. Otherwise, this preloaded value is transferred to the active register only when an update event occurs. ■ CC4 channel is configured as input: CCDAT4 contains the counter value transferred by the last input capture 4 event (IC4). When configured as input mode, register CCDAT4 and CCDDAT4 are only readable.

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Bit Field	Name	Description
		When configured as output mode, register CCDAT4 and CCDDAT4 are readable and writable.

12.4.16 Capture/Compare Register 5 (TIMx_CCDAT5)

Offset address: 0x38

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CCDAT5[15:0]															
rw															

Bit Field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained
15:0	CCDAT5[15:0]	Capture/Compare 5 value ■ CC5 channel can only configured as output: CCDAT5 contains the value to be compared with the counter TIMx_CNT, and signal is sent out on the OC5 output. If the preload function is not selected in the TIMx_CCMOD3.OC5PEN bit, the written value is immediately transferred to the active register. Otherwise, this preloaded value is transferred to the active register only when an update event occurs. CC5 is used for comparator blanking.

12.4.17 Capture/Compare Register 6 (TIMx_CCDAT6)

Offset address: 0x3C

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CCDAT6[15:0]															
rw															

Bit Field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained

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Bit Field	Name	Description
15:0	CCDAT6[15:0]	Capture/Compare 6 value ■ CC6 channel can only configured as output: CCDAT6 contains the value to be compared with the counter TIMx_CNT, and signals are sent out on the OC6 output. If the preload function is not selected in the TIMx_CCMOD3.OC6PEN bit, the written value is immediately transferred to the active register. Otherwise, this preloaded value is transferred to the active register only when an update event occurs.

12.4.18 Prescaler (TIMx_PSC)

Offset address: 0x40

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PSC[15:0]															
rw															

Bit Field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained
15:0	PSC[15:0]	Prescaler value Counter clock $f_{CK\_CNT} = f_{CK\_PSC} / (PSC[15:0] + 1)$. The PSC value is loaded into the shadow register of the prescaler each time an update event occurs.

12.4.19 Auto-reload Register (TIMx_AR)

Offset address: 0x44

Reset value: 0x0000 FFFF

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
AR[15:0]															
rw															

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Bit Field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained
15:0	AR[15:0]	Auto-reload value AR contains the value to be loaded into the actual auto-reload register. Refer to section 14.4.1 for details on the update and action of AR. When the value for auto-reload is empty, the counter will not operate.

12.4.20 Counters (TIMx_CNT)

Offset address: 0x48

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CNT[15:0]															
rw															

Bit Field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained
15:0	CNT[15:0]	Counter value

12.4.21 Repeat Count Register (TIMx_REPCNT)

Offset address: 0x4C

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								REPCNT[7:0]							
								rw							

Bit Field	Name	Description
31:8	Reserved	Reserved, the reset value must be maintained
7:0	REPCNT[7:0]	Repetition counter value Repetition counter is used to generate the update event or update the timer registers only after a given number (N+1) cycles of the counter, where N is the value of TIMx_REPCNT.REPCNT.

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Bit Field	Name	Description
		The repetition counter is decremented at each counter overflow in up-counting mode, at each counter underflow in down-counting mode or at each counter overflow and at each counter underflow in center-aligned mode. Setting the TIMx_EVTGEN.UDGN bit will reload the content of TIMx_REPCNT.REPCNT and generate an update event.

12.4.22 Break and Dead-time Registers (TIMx_BKDT)

Offset address: 0x50

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LCKCFG[1:0]		OSSR	OSSI	BKEN	BKP	AOEN	MOEN	DTGN[7:0]							
rw		rw	rw	rw	rw	rw	rw	rw							

Note: AOEN、BKP、BKEN、OSSI、OSSR and DTGN[7:0] bits can all be write protected depending on the LOCK configuration, and it is necessary to configure all of them on the first write to the TIMx_BKDT register.

Bit Field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained
15:14	LCKCFG[1:0]	Lock configuration. This bit provides write protection to prevent software errors. These bits offer a write protection against software errors. 00: – No write protected. 01: – LOCK Level 1 TIMx_BKDT.DTGN、TIMx_BKDT.BKEN、TIMx_BKDT.BKP、TIMx_BKDT.AOEN、TIMx_CTRL2.OIx、TIMx_CTRL2.OIxN、TIMx_AF1 bits enable write protection. 10: – LOCK Level 2 Except for register write protection in LOCK Level 1 mode, TIMx_CCEN.CCxP and TIMx_CCEN.CCxNP (If the corresponding channel is configured in output mode), TIMx_BKDT.OSSR and TIMx_BKDT.OSSI bits also enable write protection 11: – LOCK Level 3 Except for register write protection in LOCK Level 2, TIMx_CCMODx.OCxMD and TIMx_CCMODx.OCxPEN bits (If the corresponding channel is configured in output mode) also enable write protection. *Note: After the system reset, the LCKCFG bit can only be written once. Once written to the TIMx_BKDT register, LCKCFG will be protected until the next reset.*
13	OSSR	Off-state Selection for Run Mode This bit is used when TIMx_BKDT.MOEN=1 and the channel is a complementary output.

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Bit Field	Name	Description
		The OSSR bit does not exist in timer without complementary outputs. 0: When inactive, OC/OCN outputs are disabled (OC/OCN enable output signal = 0) 1: When inactive, OC/OCN outputs are enabled with their inactive level as soon as CCxEN = 1 or CCxNEN = 1. Then, OC/OCN enable output signal = 1 For more details, See Section 12.4.11 capture/compare enable registers (TIMx_CCEN).
12	OSSI	Off-state selection for Idle mode This bit is used when TIMx_BKDT.MOEN=0 and the channels configured as outputs. 0: When inactive, OC/OCN outputs are disabled (OC/OCN enable output signal = 0) 1: When inactive, OC/OCN outputs are forced with their with their idle level as soon as CCxEN = 1 or CCxNEN = 1. Then, OC/OCN enable output signal = 1 For more details, See Section 12.4.11 capture/compare enable registers (TIMx_CCEN).
11	BKEN	Break1 enable 0: Disable break input 1: Enable break input *Note: Any write to this bit requires an APB clock delay to take effect.*
10	BKP	Break1 polarity 0: Low level of the break input is valid 1: High level of the break input is valid *Note: Any write to this bit requires an APB clock delay to take effect.*
9	AOEN	Automatic output enable 0: Only software can set TIMx_BKDT.MOEN; 1: Software sets TIMx_BKDT.MOEN; or if the break input is not active, when the next update event occurs, hardware automatically sets TIMx_BKDT.MOEN.
8	MOEN	Main output enable This bit can be set by software or hardware depending on the TIMx_BKDT.AOEN bit, and is asynchronously cleared to '0' by hardware once the break input is active. It is only valid for channels configured as outputs. 0: OC and OCN outputs are disabled or forced to idle state. 1: OC and OCN outputs are enabled if TIMx_CCEN.CCxEN or TIMx_CCEN.CCxNEN bits are set.For more details, see Section 12.4.11 Capture/Compare enable registers (TIMx_CCEN).
7:0	DTGN[7:0]	Dead-time generator setup These bits define the dead-time duration between inserted complementary outputs. The relationship between the DTGN value and the dead time is as follows: DTGN[7:5]=0xx => DT=DTGN[7:0] $\times T_{dtgn}$， $T_{dtgn} = T_{DTS}$; DTGN[7:5]=10x => DT=(64+DTGN[5:0]) $\times T_{dtgn}$， $T_{dtgn} = 2 \times T_{DTS}$; DTGN[7:5]=110 => DT=(32+DTGN[4:0]) $\times T_{dtgn}$， $T_{dtgn} = 8 \times T_{DTS}$; DTGN[7:5]=111 => DT=(32+DTGN[4:0]) $\times T_{dtgn}$， $T_{dtgn} = 16 \times T_{DTS}$;

12.4.23 Capture/Compare Register 7 (TIMx_CCDAT7)

Offset address: 0x54

Reset value: 0x0000 0000

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CCDAT7[15:0]															
rw															

Bit Field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained
15:0	CCDAT7[15:0]	Capture/Compare 7 value ■ CC7 channel can only configured as output: CCDAT7 contains the value to be compared with the counter TIMx_CNT, and signals are sent out on OC7 output. If the preload function is not selected in the TIMx_CCMOD3.OC7PEN bit, the written value is immediately transferred to the active register. Otherwise, this preloaded value is transferred to the active register only when an update event occurs.

12.4.24 Break Filter Register (TIMx_BKFR)

Offset address: 0x60

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved		THRESH						Reserved	WSIZE						FILTEN
		rw							rw						rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved															

Bit Field	Name	Description
31:30	Reserved	Reserved, the reset value must be maintained
29:24	THRESH[5:0]	Threshold number of sample logic level to be valid, maximum 63: Threshold value for a valid logic level. Within sample window if number of logic high is more than or equal to threshold value, next logic level will be logic high. Same rule applies to logic low. If both number of 1's and 0's inside window are smaller than threshold, filter output stays unchanged. Threshold value should set to more than or equal to half of window value. Recommend threshold range is: **Minimum**: 1 pre-scale clock cycle more than ceiling value of max glitch size (in pre-scale clock cycle) and need to larger than half of window size.

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Bit Field	Name	Description
		for example, if glitch size is 3.2*(pre-scale clock period), threshold should be $\lceil 3.2 \rceil$ = 4 + 1 =5 **Maximum**: floor value of minimum size of valid signal (in pre-scale clock cycle) and need to be smaller than window size. For example, if minimum message size is 3.2*(pre-scale clock period), threshold should be floor (3.2) = 3.
23	Reserved	Reserved, the reset value must be maintained
22:17	WSIZE[5:0]	Window size value for logic level check, maximum 63: Window size decides how many sampled values will take into consideration for getting next logic level. Build-in FIFO is 64 bits with maximum index 63 which can only set window size to be 63.
16	FILTEN	Filter enable 0: Disable filter 1: Enable filter
15:0	Reserved	Reserved, the reset value must be maintained

12.4.25 Alternate Function Option Register 1（TIMx_AF1）

Offset address: 0x7C

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved										IOM4 BRKP	IOM3 BRKP	IOM2 BRKP	IOM4 BRKEN	IOM3 BRKEN	IOM2 BRKEN

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved					COMP1 BRKP	IOM BRKP	Reserved							COMP1 BRKEN	IOM BRKEN
		rw	rw	rw	rw	rw		rw	rw	rw	rw	rw	rw	rw	rw

Bit Field	Name	Description
31:22	Reserved	Reserved, the reset value must be maintained
21	IOM4BRKP	TIMx_BKIN IO4 input polarity 0：TIMx_BKIN IO4 input polarity is not inverted (active low if BKP = 0, active high if BKP = 1) 1：TIMx_BKIN IO4 input polarity is inverted (active high if BKP = 0, active low if BKP = 1)
20	IOM3BRKP	TIMx_BKIN IO3 input polarity 0：TIMx_BKIN IO3 input polarity is not inverted (active low if BKP = 0, active high if BKP = 1) 1：TIMx_BKIN IO3 input polarity is inverted (active high if BKP = 0, active low if BKP = 1)
19	IOM2BRKP	TIMx_BKIN IO2 input polarity 0：TIMx_BKIN IO2 input polarity is not inverted (active low if BKP = 0, active high if BKP =

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		1) 1：TIMx_BKIN IO2 input polarity is inverted (active high if BKP = 0, active low if BKP = 1)
18	IOM4BRKEN	TIMx_BKIN IO4 input enable 0：TIMx_BKIN IO4 input disabled 1：TIMx_BKIN IO4 input enabled
17	IOM3BRKEN	TIMx_BKIN IO3 input enable 0：TIMx_BKIN IO3 input disabled 1：TIMx_BKIN IO3 input enabled
16	IOM2BRKEN	TIMx_BKIN IO2 input enable 0：TIMx_BKIN IO2 input disabled 1：TIMx_BKIN IO2 input enabled
15:11	Reserved	Reserved, the reset value must be maintained
10	COMP1BRKP	tim_brk_comp1 input polarity 0：tim_brk_comp1 input polarity is not inverted (active low if BKP = 0, active high if BKP = 1) 1：tim_brk_comp1 input polarity is inverted (active high if BKP = 0, active low if BKP = 1)
9	IOMBRKP	TIMx_BKIN input polarity 0：TIMx_BKIN input polarity is not inverted (active low if BKP = 0, active high if BKP = 1) 1：TIMx_BKIN input polarity is inverted (active high if BKP = 0, active low if BKP = 1)
8:2	Reserved	Reserved, the reset value must be maintained
1	COMP1BRKEN	tim_brk_comp1 input enable 0：tim_brk_comp1 input disabled 1：tim_brk_comp1 input enabled
0	IOMBRKEN	TIMx_BKIN IO1 input enable 0：TIMx_BKIN IO1 input disabled 1：TIMx_BKIN IO1 input enabled

12.4.26 DMA Control Register (TIMx_DCTRL)

Offset address: 0x94

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved		DBADDR[5:0]						Reserved		DBLEN[5:0]					
					rw								rw		

Bit Field	Name	Description
31:14	Reserved	Reserved, the reset value must be maintained
13:8	DBADDR[5:0]	DMA base address This bit field defines the first address where the DMA accesses the TIMx_DADDR register.

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Bit Field	Name	Description
		When access is done through the TIMx_DADDR first time, this bit-field specifies the address you just access. And then the second access to the TIMx_DADDR, you will access the address of “DMA Base Address + 4” 000000：TIMx_CTRL1, 000001：TIMx_CTRL2, 000010：TIMx_SMCTRL, ... 100101：TIMx_DCTRL
7:6	Reserved	Reserved, the reset value must be maintained
5:0	DBLEN[5:0]	DMA burst length This bit field defines the number DMA will accesses (write/read) TIMx_DADDR register. 000000: 1 time transfer 000001: 2 time transfer 000010: 3 time transfer … 010001: 18 time transfer 100010: 35 time transfer

12.4.27 DMA Transfer For Full Transfer Register (TIMx_DADDR)

Offset address: 0x98

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
BURST[31:16]															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BURST[15:0]															
rw															

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<table>
<tr><th>Bit Field</th><th>Name</th><th>Description</th></tr>
<tr><td>31:0</td><td>BURST[31:0]</td><td>DMA Access Buffer
When a read or write operation is assigned to this register, the register located at the address range (DMA base address + DMA burst length ×4) will be accessed.
DMA base address = The address of TIM_CTRL1 + TIMx_DCTRL. DBADDR * 4；
DMA burst len = TIMx_DCTRL.DBLEN + 1.
Example:
If TIMx_DCTRL.DBLEN = 0x3(4 transfers), TIMx_DCTRL.DBADDR = 0xD (TIMx_CCDAT1), DMA data length = half word, DMA memory address = buffer address in SRAM, DMA peripheral address = TIMx_DADDR address.
When an event occurs, TIMx will send requests to the DMA, and transfer data 4 times.
For the first time, DMA access to the TIMx_ DADDR register will be mapped to access TIMx_CCDAT1 register;
For the second time, DMA access to the TIMx_ DADDR register will be mapped to access TIMx_CCDAT2 register;
… …
For the fourth time, DMA access to the TIMx_ DADDR register will be mapped to access TIMx_CCDAT4 register;</td></tr>
</table>

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13 General-purpose Timer (TIM3)

13.1 General-purpose Timer Introduction

The general-purpose timer (TIM3) is mainly used in the following scenarios: counting the input signal, measuring the pulse width of the input signal and generating the output waveform, etc.

13.2 Main Features of General-purpose Timer

- 16-bit auto-reload counters. (It can realize up-counting, down-counting, up/down counting)
- 16-bit programmable prescaler. (The prescaler factor can be configured with any value between 1 and 65536)
- TIM3 up to 4 channels
- Channel's working modes: PWM output, ouput compare, one-pulse mode output, input capture
- The events that generate the interrupt/DMA are as follows:
  - Update event
  - Trigger event
  - Input capture
  - Output compare
- Timer can be controlled by external signal
- Timer can be linked together internally for timer synchronization or chaining
- Incremental (quadrature) encoder interface: used for tracking motion and resolving rotation direction and position
- Hall sensor interface: used to do three-phase motor control
- Supports capture of internal comparator output signal.

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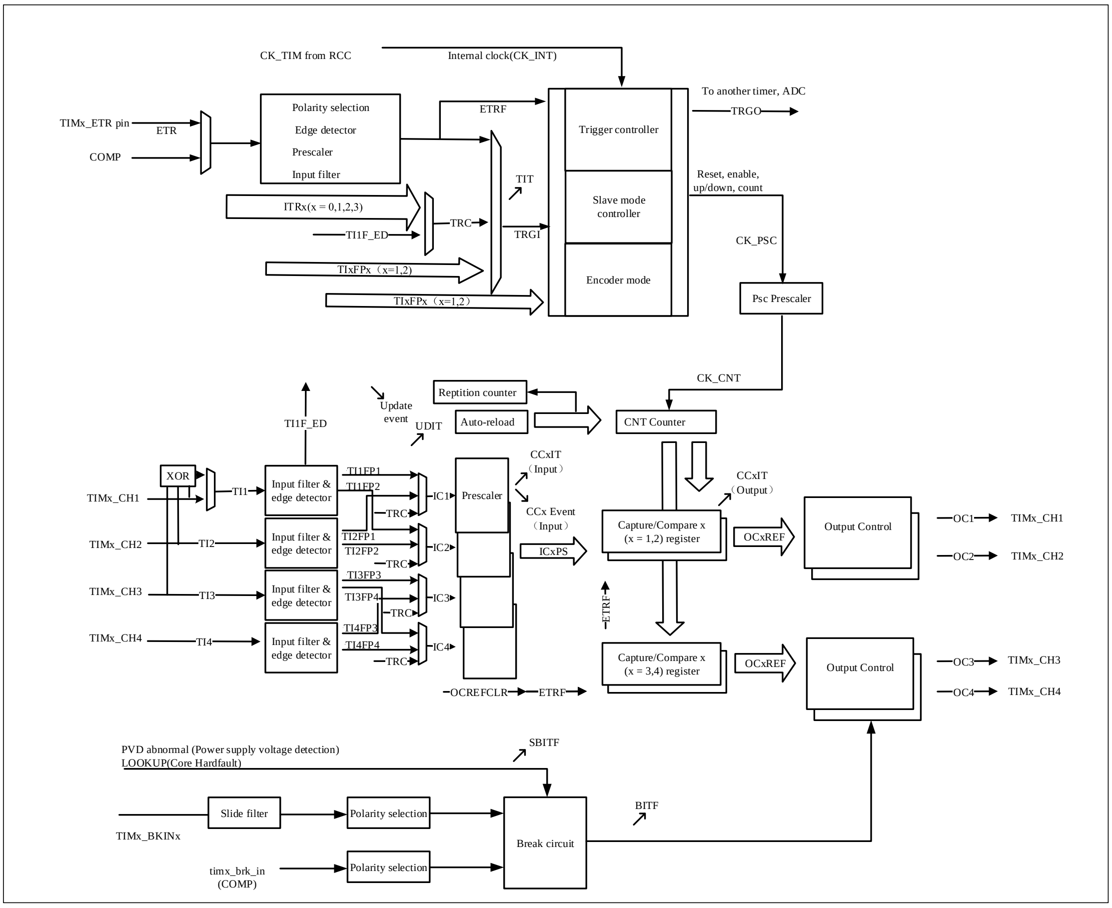
Figure 13-1 Block Diagram of TIM3



↘ *The event* ↗ *Interrupt and DMA output*

The input for capture channel 1 may originate from the IOM or comparator output.

13.3 General-purpose Timer3 Description

13.3.1 Time-base Unit

The time-base unit mainly includes: prescaler, counter and auto-reload. When the time base unit is working, the software can read and write the corresponding registers (TIMx_PSC, TIMx_CNT and TIMx_AR) at any time.

Depending on the setting of the auto-reload preload enable bit (TIMx_CTRL1.ARPEN), the value of the preload register is transferred to the shadow register immediately or at each update event UEV. An update event is generated when the counter reaches the overflow/underflow condition and it can be generated by software when TIMx_CTRL1.UPDIS=0. The counter CK_CNT is valid only when the TIMx_CTRL1.CNTEN bit is set. The counter starts counting one clock cycle after the TIMx_CTRL1.CNTEN bit is set.

13.3.1.1 Prescaler description

The TIMx_PSC register consists of a 16-bit counter that can be used to divide the counter clock frequency by any factor between 1 and 65536. It can be changed on the fly as it is buffered. The prescaler value is only taken into account at the next update event.

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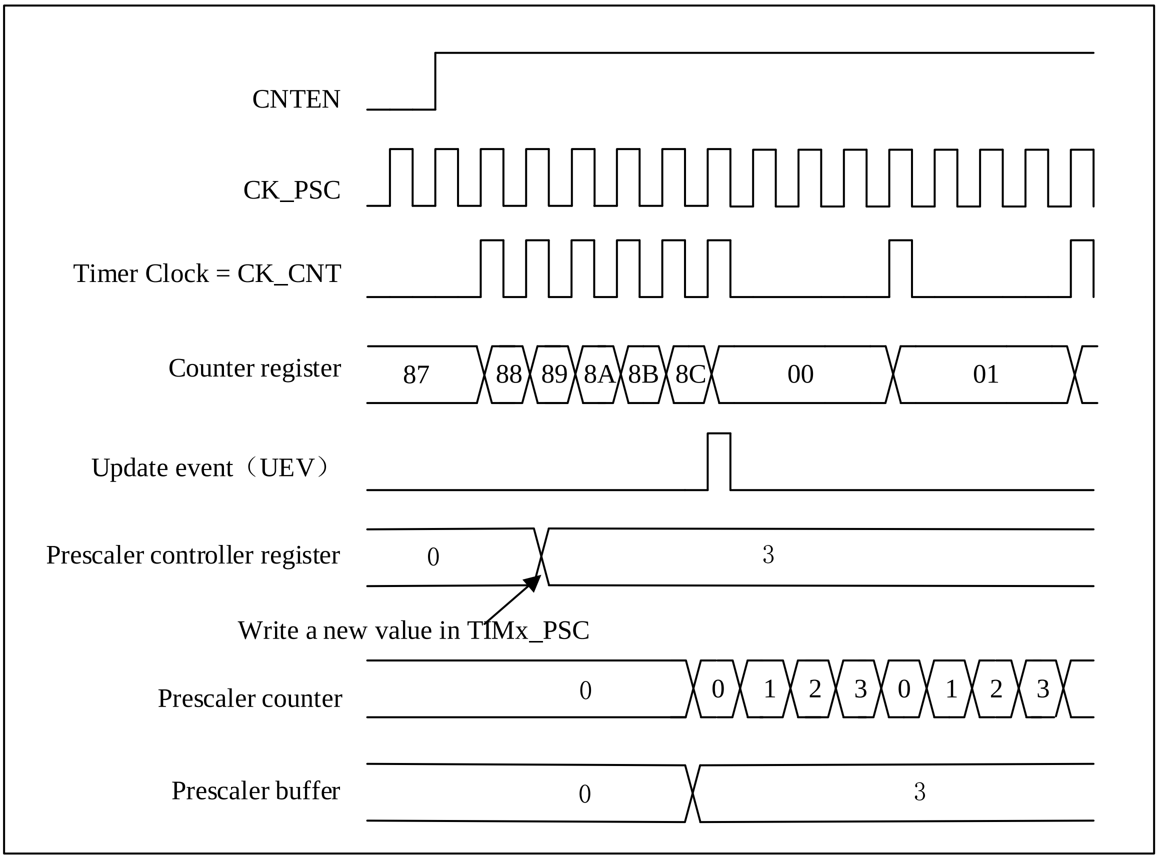
Figure 13-2 Counter Timing Diagram with Prescaler Division Change from 1 to 4



13.3.2 Counter Mode

13.3.2.1 Up-counting mode

In up-counting mode, the counter will count from 0 to the value of the register TIMx_AR, then it resets to 0. And a counter overflow event is generated.

If the TIMx_CTRL1.UPRS bit (select update request) and the TIMx_EVTGEN.UDGN bit are set, an update event (UEV) will generate And TIMx_STS.UDITF will not be set by hardware, therefore, no update interrupts or update DMA requests are generated. This setting is used in scenarios where you want to clear the counter but do not want to generate an update interrupt.

Depending on the update request source is configured in the TIMx_CTRL1.UPRS. When an update event occurs, TIMx_STS.UDITF is set, all registers are updated:

- Update auto-reload shadow registers with preload value (TIMx_AR), when TIMx_CTRL1.ARPEN = 1.
- The prescaler shadow register is reloaded with the preload value (TIMx_PSC).

To avoid updating the shadow registers when new values are written to the preload registers, you can disable the update by setting TIMx_CTRL1.UPDIS=1.

When an update event occurs, the counter will still be cleared and the prescaler counter will also be set to 0 (but the prescaler value will remain unchanged).

The figure below shows some examples of the counter behavior and the update flags for different division factors in

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the up-counting mode.

Figure 13-3 Timing Diagram of Up-counting, The Internal Clock Divider Factor = 2/N

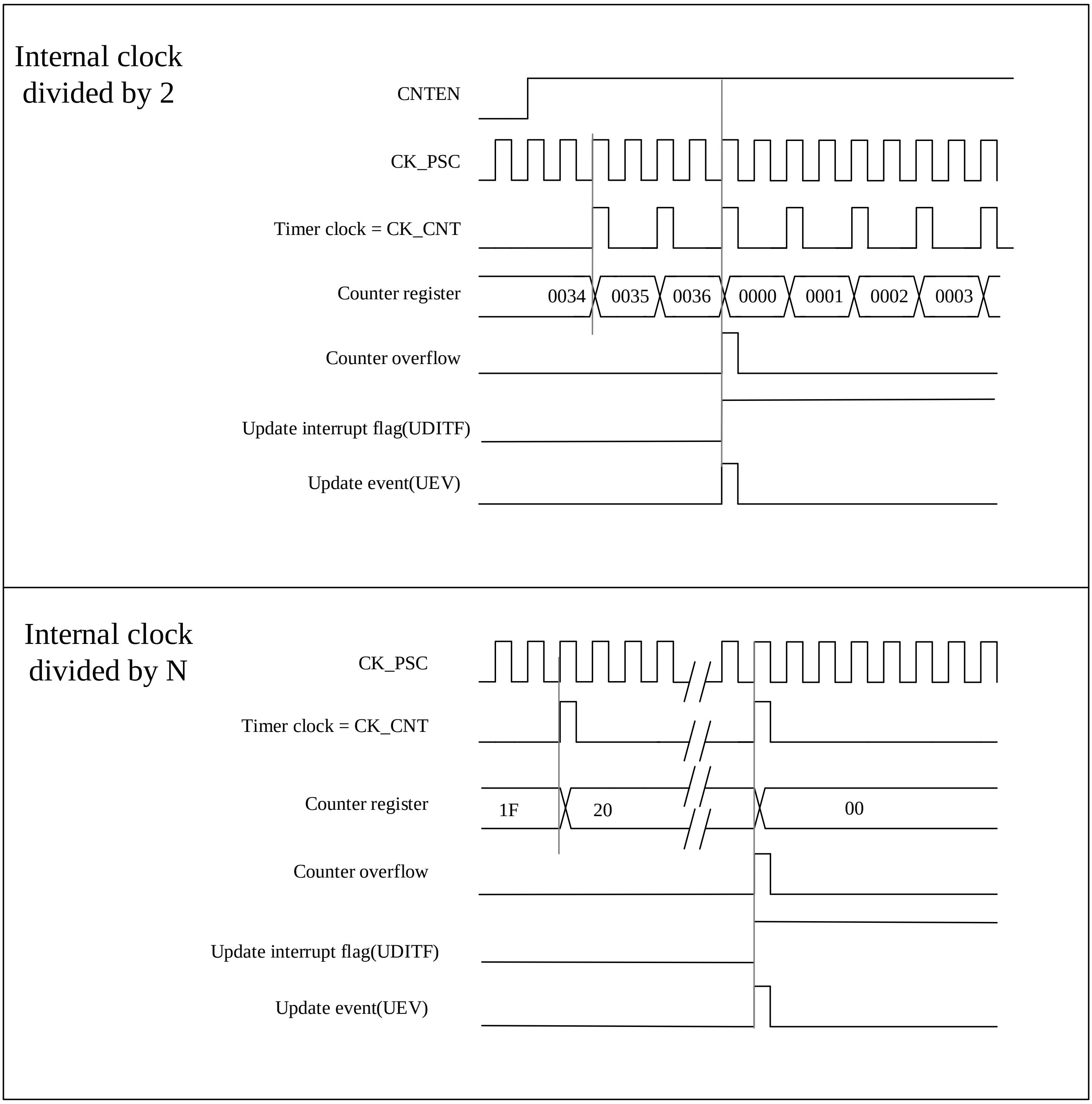

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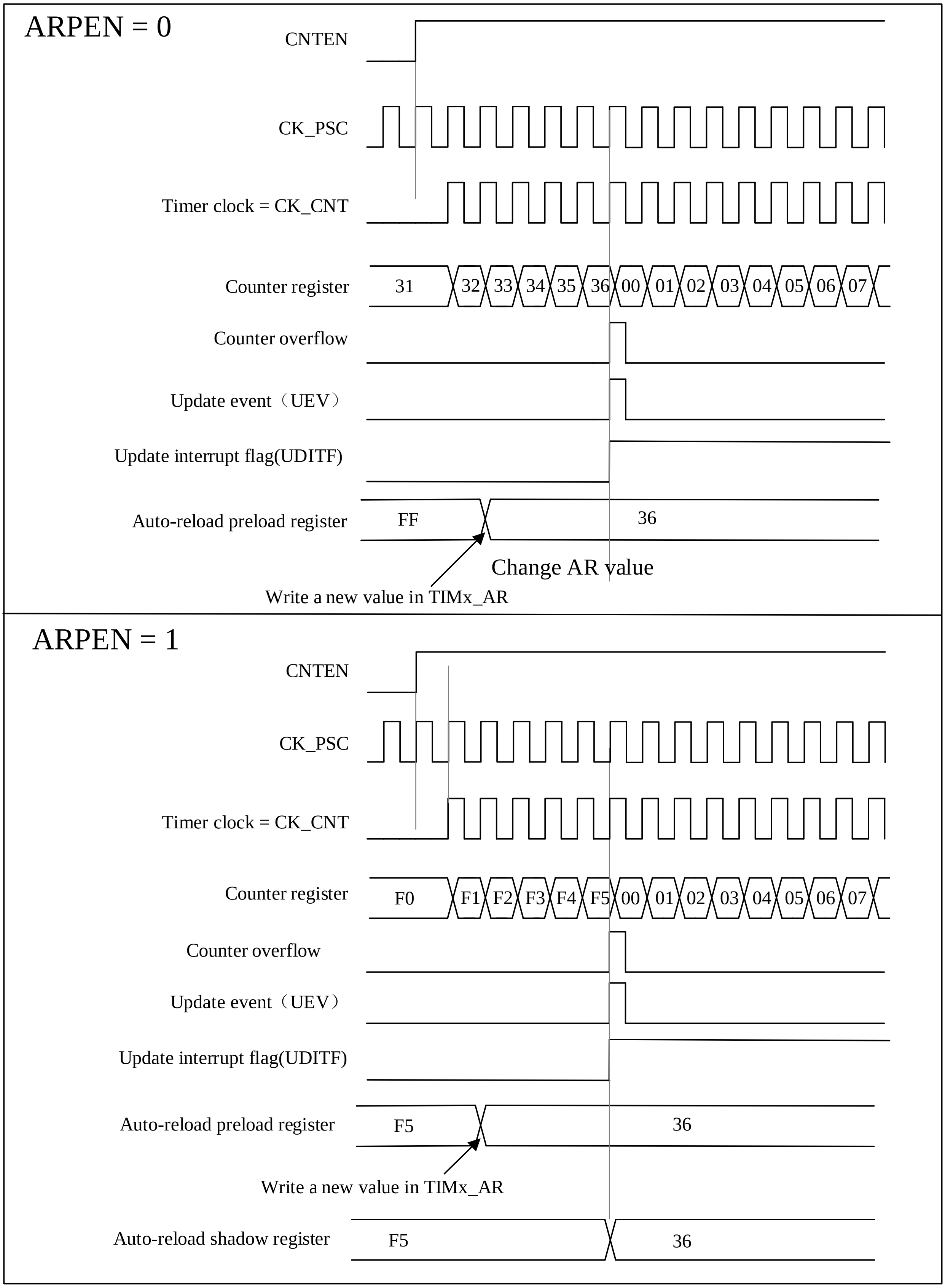
Figure 13-4 Timing Diagram of The Up-counting, Update Event When ARPEN = 0/1



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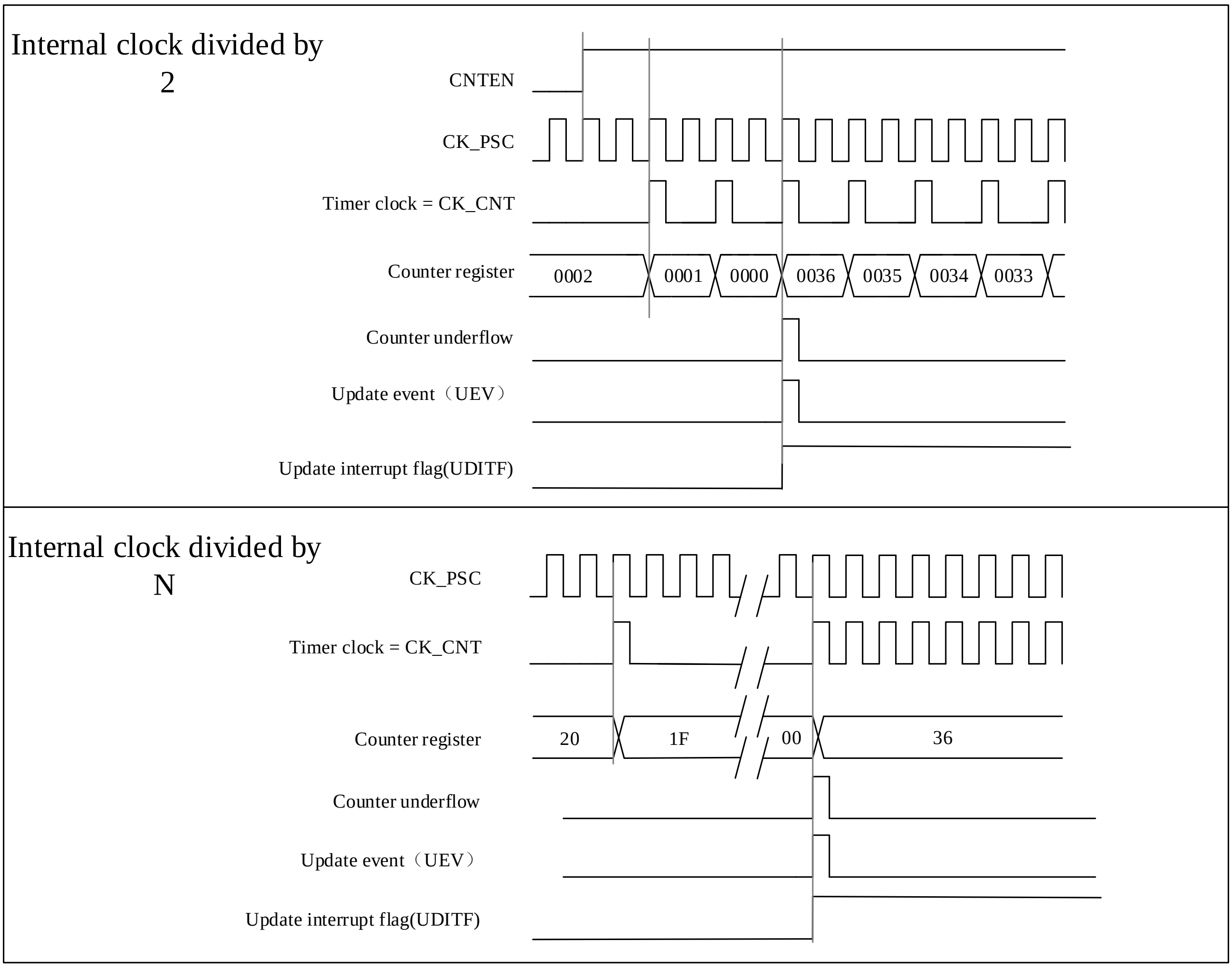
13.3.2.2 Down-counting mode

In down-counting mode, the counter will decrement from the value of the register TIMx_AR to 0, then restart from the auto-reload value and generate a counter underflow event.

The process of configuring update events and updating registers in down-counting mode is the same as in up-counting mode, see Section 14.3.2.1.

The figure below shows some examples of the counter behavior and the update flags for different division factors in the down-counting mode.

Figure 13-5 Timing Diagram of the Down-counting, Internal Clock Divided Factor = 2/N



13.3.2.3 Center-aligned mode

In center-aligned mode, the counter increments from 0 to the value (TIMx_AR) – 1, a counter overflow event is generated. It then counts down from the auto-reload value (TIMx_AR) to 1 and generates a counter underflow event. Then the counter resets to 0 and starts counting up again.

In this mode, the TIMx_CTRL1.DIR direction bits have no effect and the count direction is updated and specified by hardware. Center-aligned mode is valid when the TIMx_CTRL1. CAMSEL bit is not equal to "00".

The update events can be generated each time the counter overflows and each time the counter underflows. Alternatively, an update event can also be generated by setting the TIMx_EVTGEN. UDGN bit (either by software

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or using a slave mode controller). In this case, the counter restarts from 0, as does the prescaler's counter.

Note: if the update source is a counter overflow, auto-reload update before reloading the counter.

Figure 13-6 Timing Diagram of the Center-aligned, Internal Clock Divided Factor = 2/N

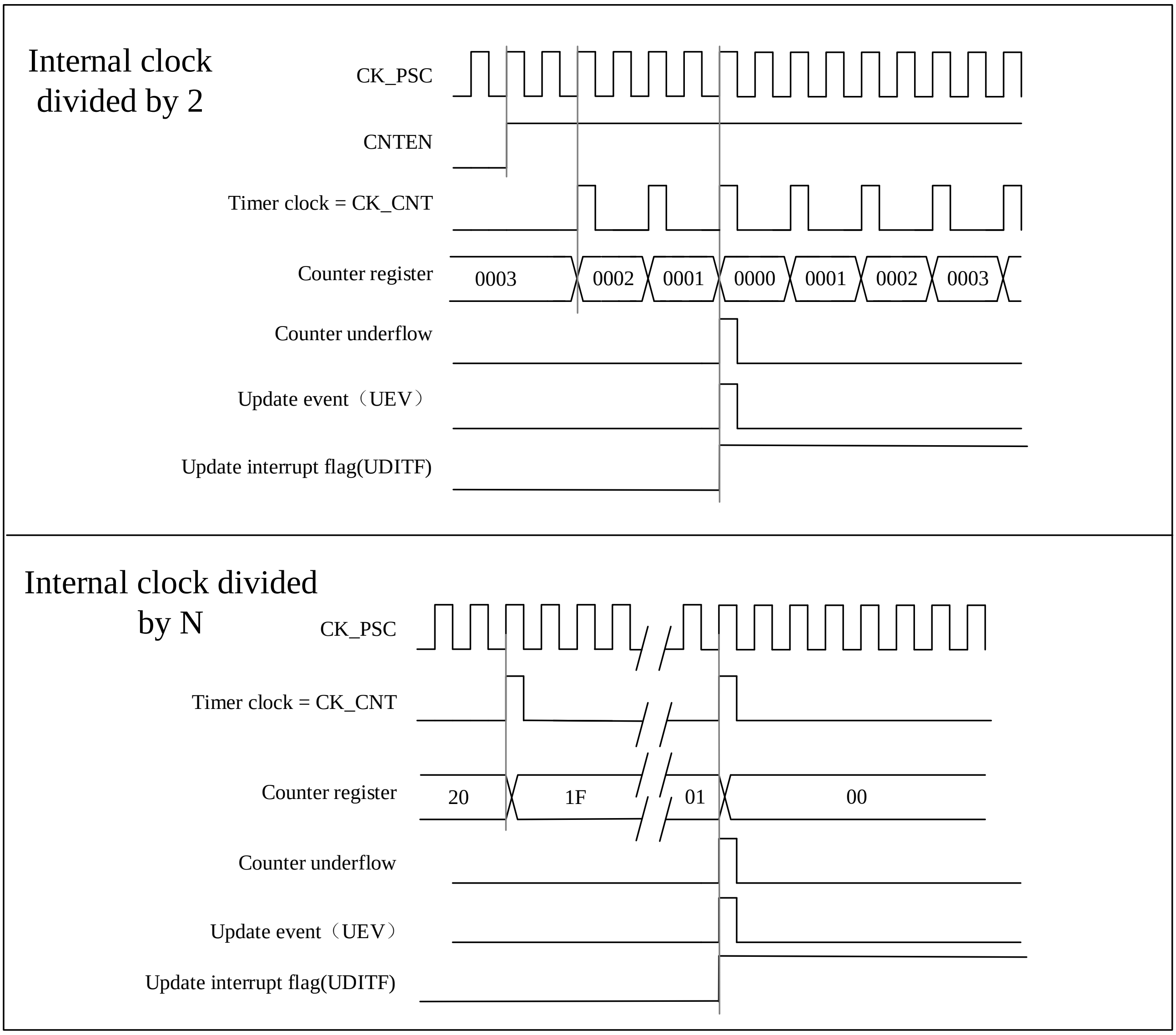

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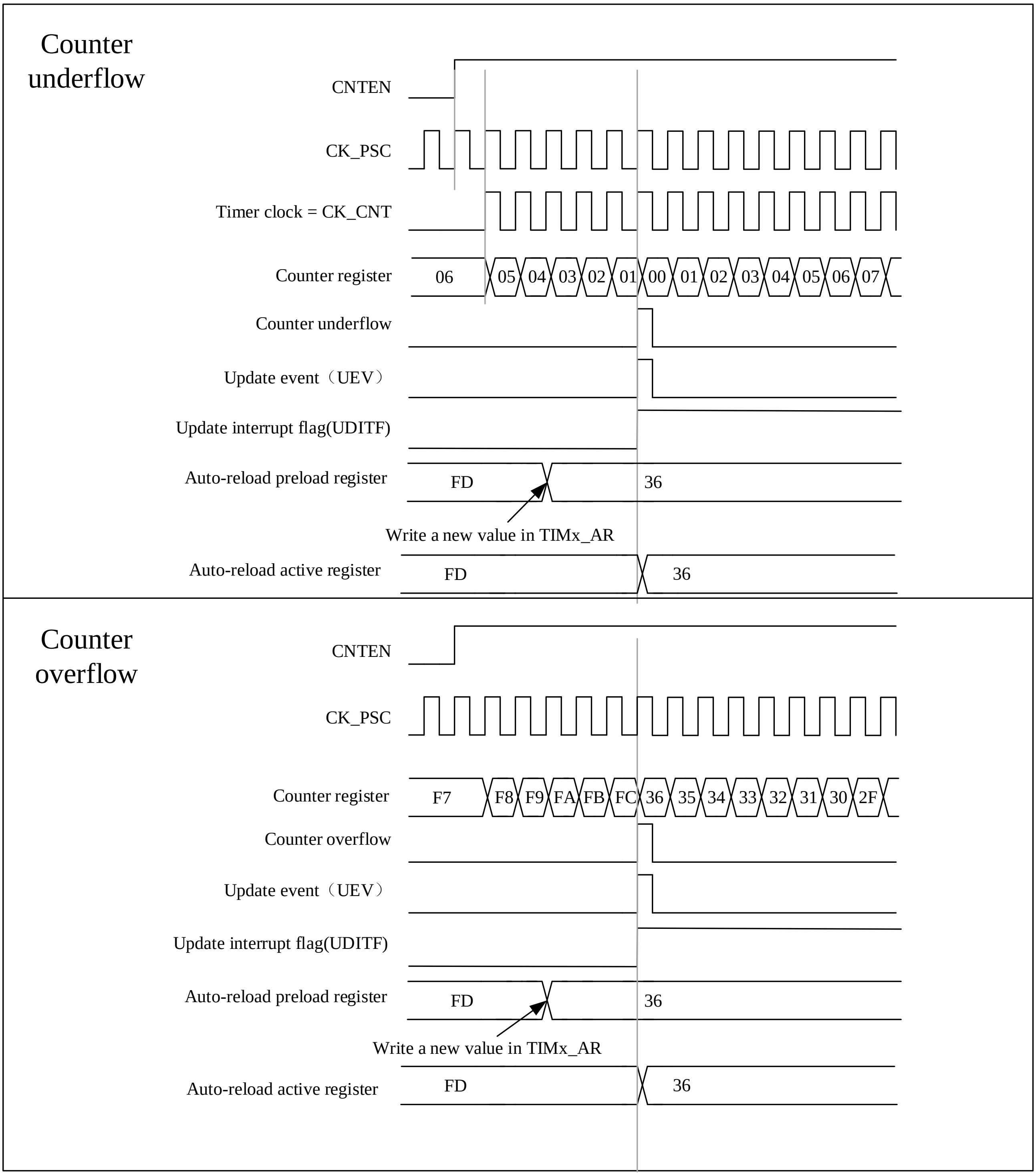
Figure 13-7 A Center-aligned Sequence Diagram That Includes Counter Overflows and Underflows (ARPEN = 1)



13.3.3 Clock Selection

- The internal clock of timers：CK_INT
- Two kinds of external clock mode:
  - External input pin

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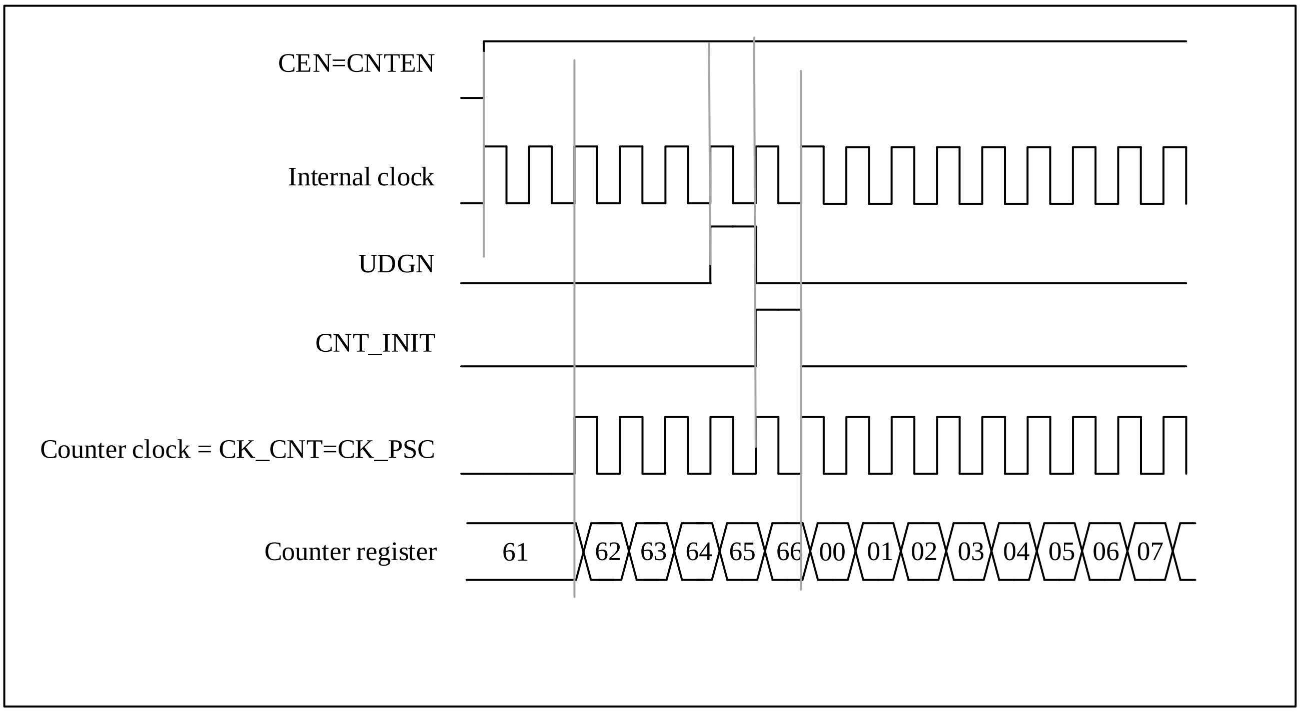
– External trigger input ETR

- Internal trigger input (ITRx) : one timer is used as a prescaler for another timer

13.3.3.1 Internal clock source (CK_INT)

When the TIMx_SMCTRL.SMSEL is equal to “0000”, the slave mode controller is disabled. The three control bits (TIMx_CTRL1.CNTEN、TIMx_CTRL1. DIR、TIMx_EVTGEN. UDGN) can only be changed by software (except TIMx_EVTGEN. UDGN, which remains cleared automatically). It is provided that the TIMx_CTRL1.CNTEN bit is written as' 1 ' by software, the clock source of the prescaler is provided by the internal clock CK_INT.

Figure 13-8 Control Circuit in Normal Mode, Internal Clock Divided by 1



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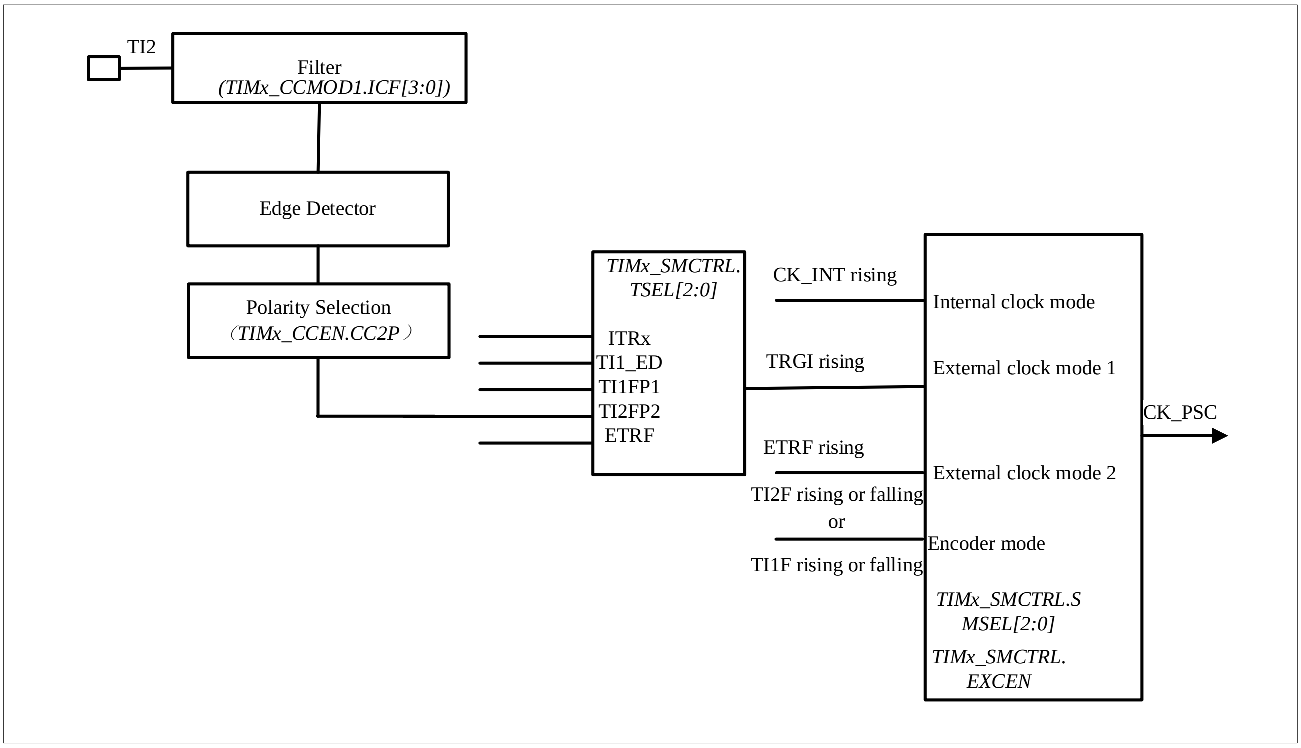
13.3.3.2 External clock source mode 1

Figure 13-9 TI2 External Clock Connection Example



This mode is selected by configuring TIMx_SMCTRL.SMSEL=0111. The counter can be configured to count on the rising or falling edge of the clock at the selected input.

For example, to configure up-counting mode to count on the rising edge of the clock at the T12 input, the configuration steps are as follows:

- Configure TIMx_CCMOD1.CC2SEL equal to ‘01’, CC2 channel is configured as input, IC2 is mapped to TI2
- Configure TIMx_CCEN.CC2P equal to ‘0’, select clock rising edge polarity
- To select input filter bandwidth by configuring TIMx_CCMOD1.IC2F[3:0] (if filter is not needed, keep IC2F bit at ‘0000’)
- Configure TIMx_SMCTRL.SMSEL equal to ‘0111’, select timer external clock mode 1
- Configure TIMx_SMCTRL.TSEL equal to ‘110’, select TI2 as the trigger input source
- Configure TIMx_CTRL1.CNTEN equal to ‘1’ to start the counter

Note：The capture prescaler is not used for triggering, so it does not need to be configured

When the rising edge of the timer clock occurs at TI2=1, the counter counts once and the TIMx_STS .TITF flag is pulled high.

The delay between the rising edge of TI2 and the actual clock of the counter depends on the resynchronization circuit at the input of TI2.

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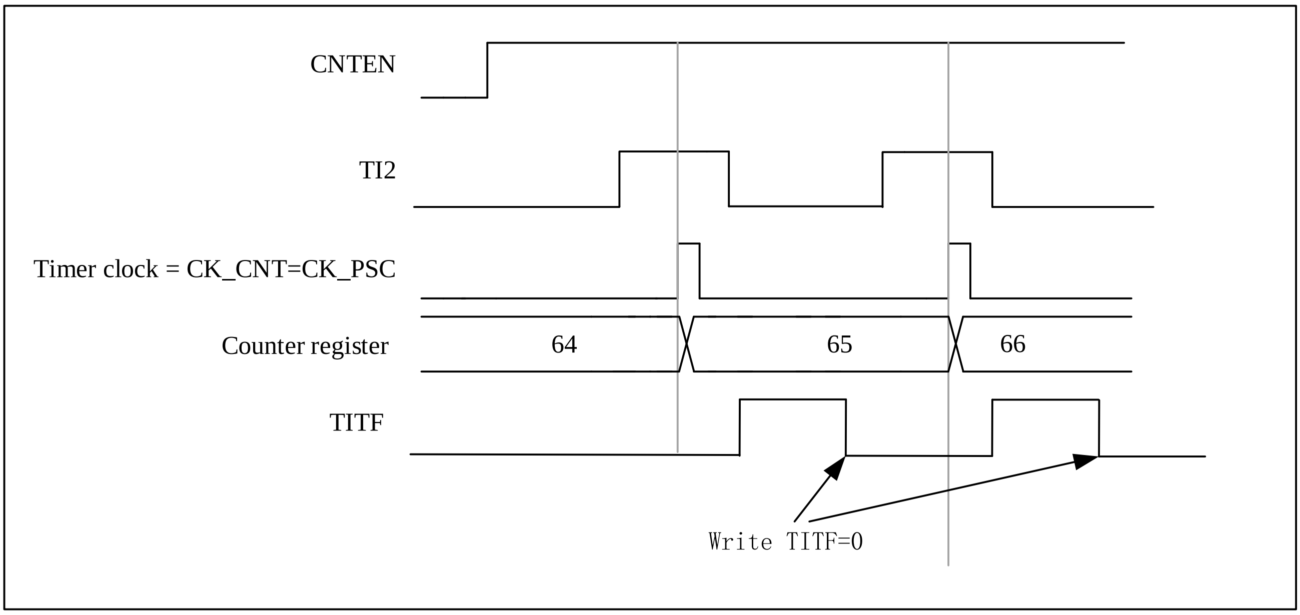
Figure 13-10 Control Circuit in External Clock Mode 1

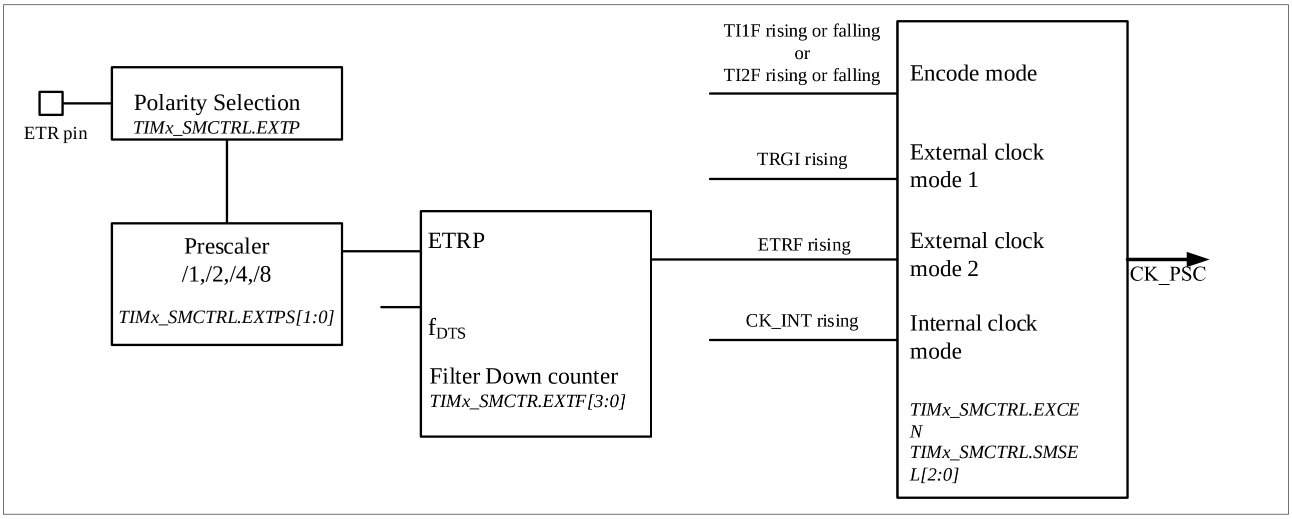


13.3.3.3 External clock source mode 2

This mode is selected by TIMx_SMCTRL .EXCEN equal to 1. The counter can count on every rising or falling edge of the external trigger input ETR.

The following figure is a schematic diagram of the external trigger input module in External clock source mode 2

Figure 13-11 External Trigger Input Block Diagram



For example, use the following configuration steps to make the up counter count every 2 rising edges on ETR.

- Since no filter is needed in this case, make TIMx_SMCTRL .EXTF[3:0] equal to ‘0000’
- Configure the prescaler by making TIMx_SMCTRL.EXTPS[1:0] equal to ‘01’
- Select the polarity on ETR pin by setting TIMx_SMCTRL.EXTP equal to ‘0’, The rising edge of ETR is valid
- External clock mode 2 is selected by setting TIMx_SMCTRL .EXCEN equal to ‘1’

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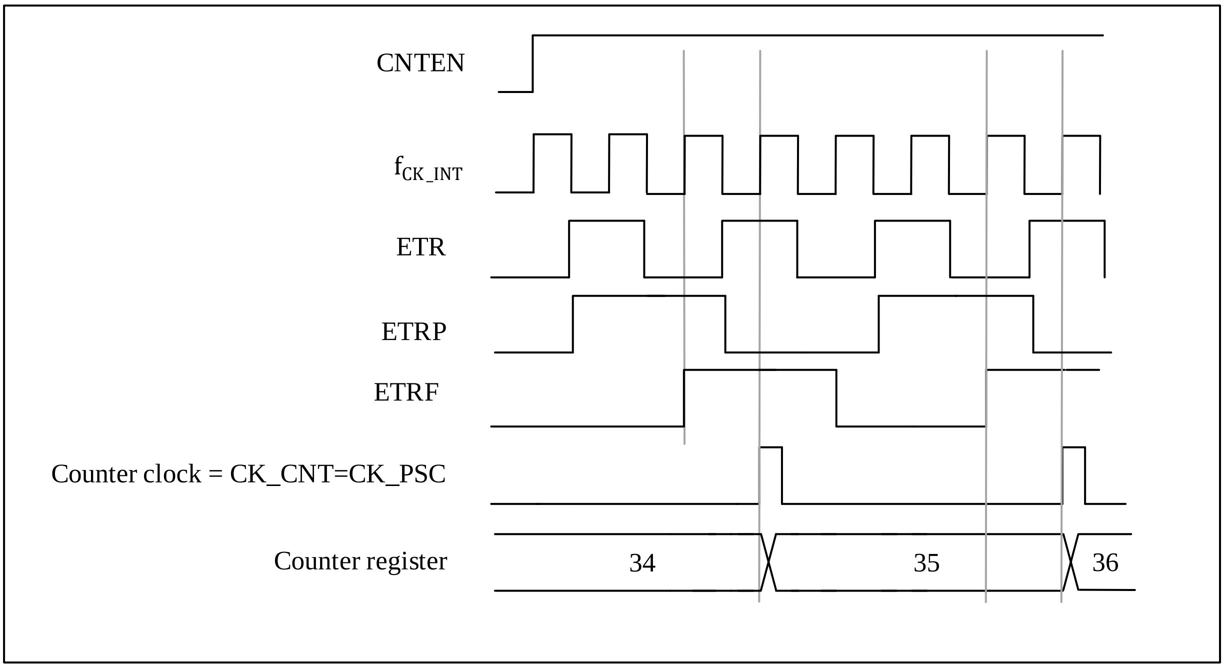
- Turn on the counter by setting TIMx_CTRL1. CNTEN equal to '1'

The counter counts every 2 rising edges of ETR. The delay between the rising edge of ETR and the actual clock to the counter is due to a resynchronization circuit on the ETRP signal.

Figure 13-12 Control Circuit in External Clock Mode 2



13.3.4 Capture/Compare Channels

Capture/Compare channels include Capture/Compare registers and shadow registers. The input section consists of digital filters, multiplexers and prescalers. The output section includes comparators and output controls.

The input signal TIx is sampled and filtered to generate the signal TIxF. A signal (TIxF_rising or TIxF_falling) is then generated by the edge detector of the polarity select function, the polarity of which is selected by the TIMx_CCEN.CCxP bits. This signal can be used as a trigger input for the slave mode controller. At the same time, the signal ICx is sent to the capture register after prescale. The following figure shows a block diagram of a capture/compare channel.

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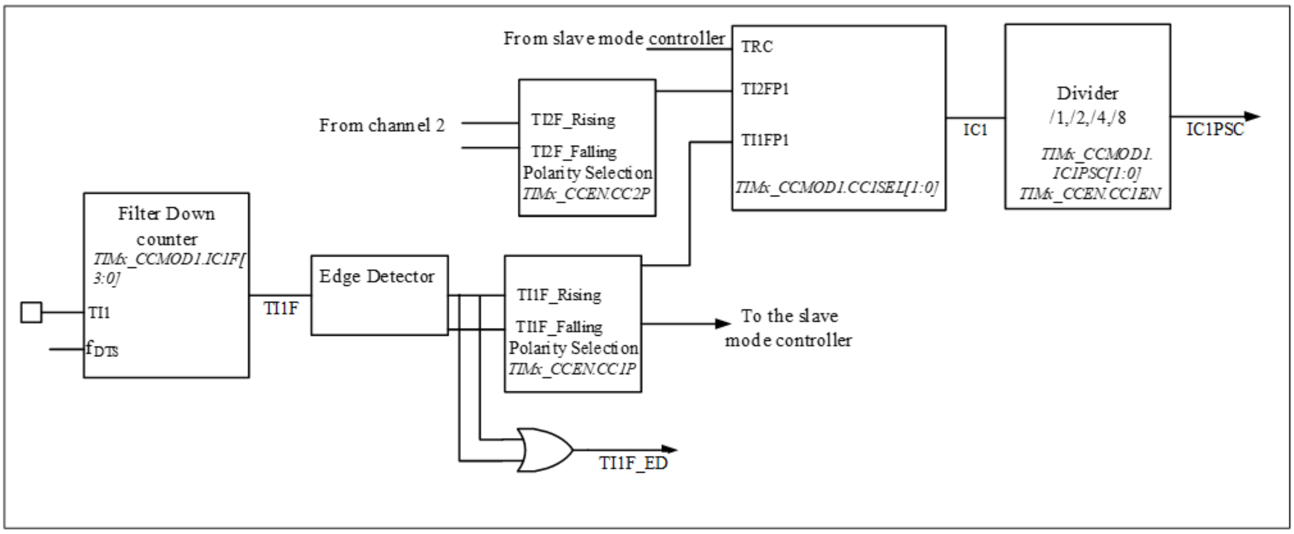
Figure 13-13 Capture/Compare Channel (Example: Channel 1 Input Stage)



The output part generates an intermediate waveform OCxRef (active high) as reference. The polarity acts at the end of the chain.

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Figure 13-14 Capture/Compare Channel 1 Main Circuit

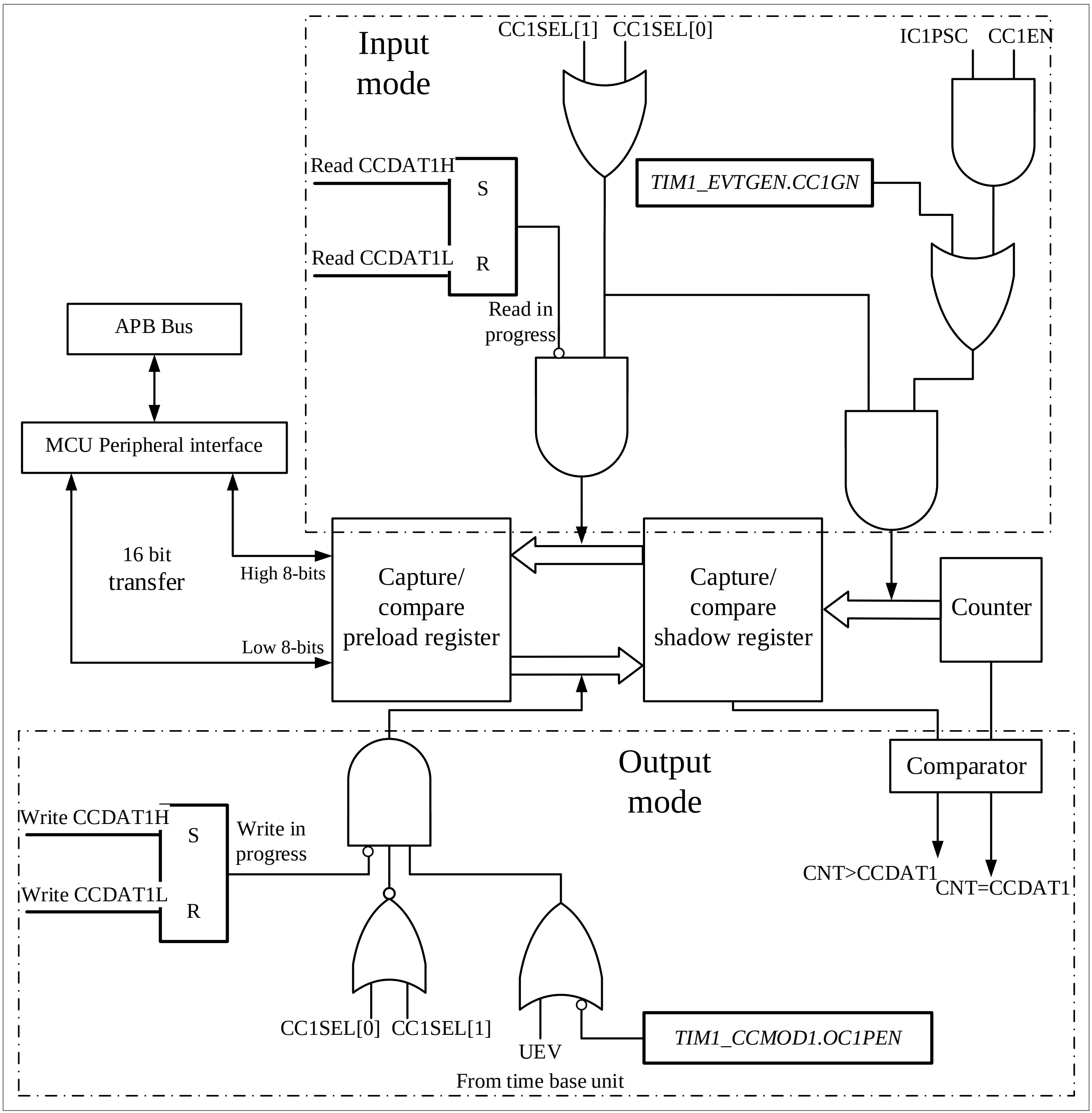

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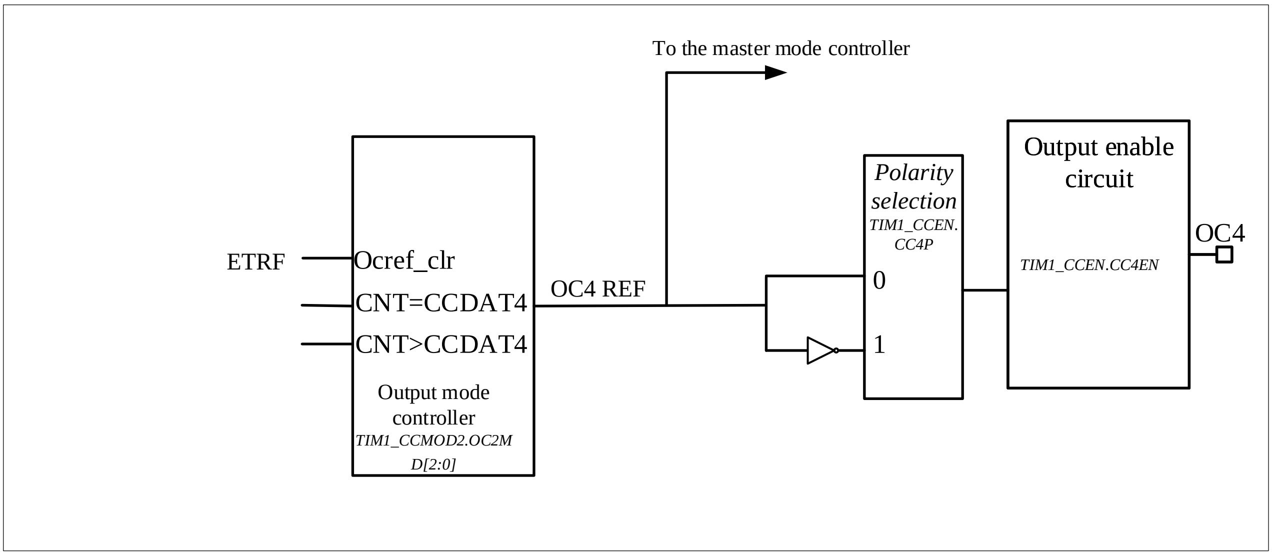
Figure 13-15 Output Part of Channelx (x = 1,2,3,4; Take Channel 4 as an Example)



Reads and writes always access preloaded registers when capturing/comparing. The two specific working processes are as follows:

In capture mode, the capture is actually done in the shadow register, and then the value in the shadow register is copied into the preload register.

In compare mode, as opposed to capture mode, the value of the preload register is copied into the shadow register, which is compared with the counter.

13.3.5 Input Capture Mode

In capture mode, the TIMx_CCDATx registers are used to latch the counter value after the ICx signal detects.

There is a capture interrupt flag TIMx_STS.CCxITF, which can issue an interrupt or DMA request if the corresponding interrupt enable is pulled high.

The TIMx_STS. CCxITF bit is set by hardware when a capture event occurs and is cleared by software or by reading the TIMx_CCDATx register.

The overcapture flag TIMx_STS.CCxOCF is set equal to 1 when the counter value is captured in the TIMx_CCDATx register and TIMx_STS.CC1ITF is already pulled high. Unlike the former, TIMx_STS.CCxOCF is cleared by writing 0 to it.

To achieve a rising edge of the TI1 input to capture the counter value into the TIMx_CCDAT1 register, the configuration flow is as follows:

- To select a valid input:

  Configure TIMx_CCMOD1.CC1SEL to ‘01’. At this time, the input is the CC1 channel, and IC1 is mapped to TI1.

- The duration of the input filter required for programming：

  Define the sampling frequency of the TI1 input and the length of the digital filter by configuring the

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TIMx_CCMODx.ICxF bits. Example: If the input signal jitters up to 5 internal clock cycles, we must choose a filter duration longer than these 5 clock cycles. When 8 consecutive samples (sampled at $f_{TIM4FILTCLK}$ frequency) with the new level are detected, we can validate the transition on TI1. Then configure TIMx_CCMOD1.IC1F to '1xxx'.

- By configuring TIMx_CCEN.CC1P=0, select the rising edge as the valid transition polarity on the TI1 channel.
- Configure the input prescaler. In this example, configure TIMx_CCMOD1.IC1PSC='00' to disable the prescaler because we want to capture every valid transition.
- Enable capture by configuring TIMx_CCEN.CC1EN = '1'.

If you want to enable DMA request, you can configure TIMx_DINTEN.CC1DEN=1.If you want enable related interrupt request, you can configureTIMx_DINTEN.CC1IEN bit=1

13.3.6 PWM Input Mode

There are some differences between PWM input mode and normal input capture mode, including:

- Two ICx signals are mapped to the same TIx input.
- The two ICx signals are active on edges of opposite polarity.
- Select one of two TIxFP signals as trigger input.
- The slave mode controller is configured in reset mode.

For example, the following configuration flow can be used to know the period and duty cycle of the PWM signal on TI1 (It depends on the frequency of CK_INT and the value of the prescaler).

- Configure TIMx_CCMOD1.CC1SEL equal to '01' to select TI1 as valid input for TIMx_CCDAT1
- Configure TIMx_CCEN.CC1P equal to '0' to select the active polarity of filtered timer input 1(TI1FP1), active at the rising edge.
- Configure TIMx_CCMOD1.CC2SEL equal to '10' select TI1 as valid input for TIMx_CCDAT2.
- Configure TIMx_CCEN.CC2P equal to 1 to select the valid polarity of filtered timer input 2(TI1FP2), active at the falling edge.
- Configure TIMx_SMCTRL.TSEL=101 to select Filtered timer input 1 (TI1FP1) as valid trigger input.
- Configure TIMx_SMCTRL.SMSEL=0100 to configure the slave mode controller to reset mode.
- Configure TIMx_CCEN. CC1EN=1 and TIMx_CCEN.CC2EN=1 to enable capture.

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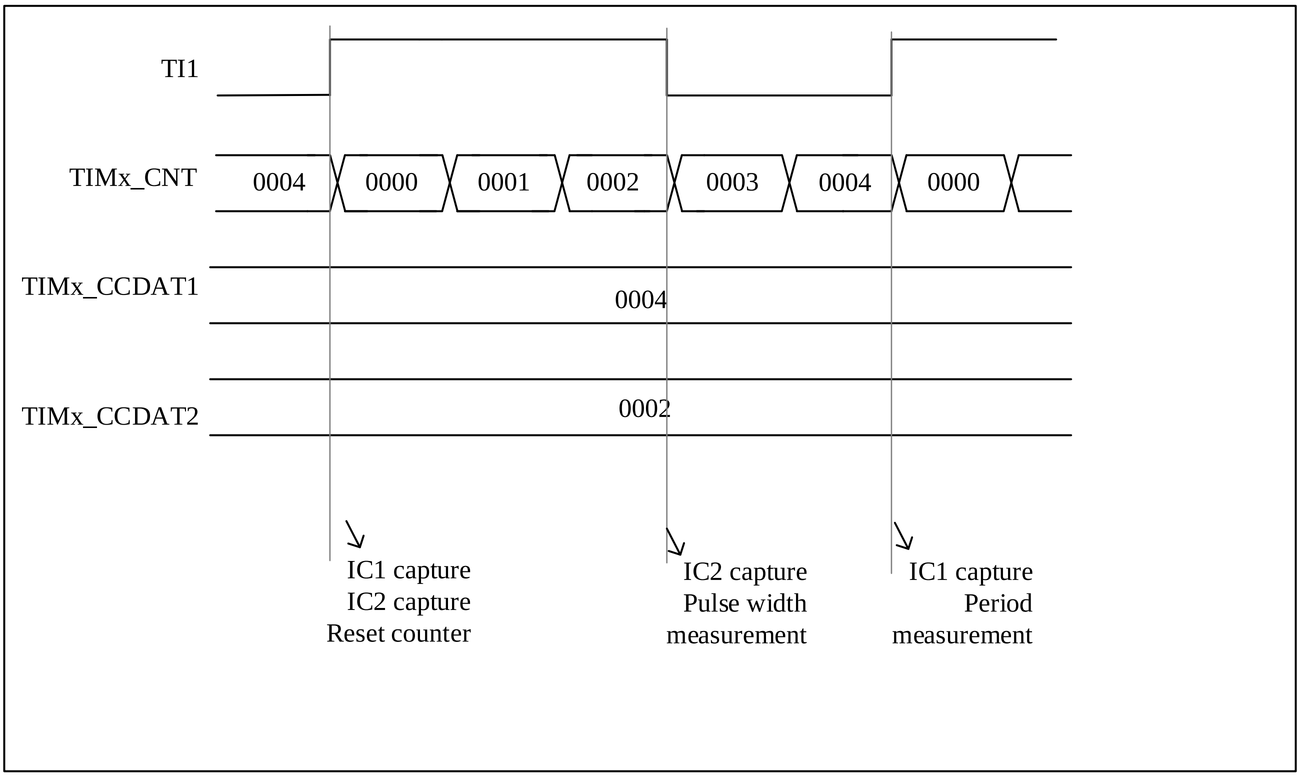
Figure 13-16 PWM Input Mode Timing



Because of only filter timer input 1 (TI1FP1) and filter timer input 2 (TI2FP2) are connected to the slave mode controller, the PWM input mode can only be used with the TIMx_CH1/TIMx_CH2 signals.

13.3.7 Forced Output Mode

Software can force output compare signals to active or inactive level directly, in output mode (TIMx_CCMODx.CCxSEL=00).

User can set TIMx_CCMODx. OCxMD=101 to force the output compare signal to active level. And the OCxREF will be forced high, OCx get opposite value to CCxP polarity bit. On the other hand, user can set TIMx_CCMODx. OCxMD=100 to force the output compare signal to inactive level, the OCxREF will be forced low.

The values of the TIMx_CCDATx shadow register and the counter still comparing with each other in this mode.

The comparison between the output compare register TIMx_CCDATx and the counter TIMx_CNT has no effect on OCxREF. And the flag still can be set. Therefore, the interrupt and DMA requests still can be sent.

13.3.8 Output Compare Mode

User can use this mode to control the output waveform, or to indicate that a period of time has elapsed。

When the capture/compare register and the counter have the same value, the output compare function’s operations are as follow:

- TIMx_CCMODx.OCxMD is for output compare mode, and TIMx_CCEN.CCxP is for output polarity. When the compare matches, if set TIMx_CCMODx.OCxMD=000, the output pin will keep its level; if set

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TIMx_CCMODx.OCxMD=001, the output pin will be set active;if set TIMx_CCMODx.OCxMD=010, the output pin will be set inactive;if set TIMx_CCMODx.OCxMD=011, the output pin will be set to toggle.

- Set TIMx_STS.CCxITF.
- If user set TIMx_DINTEN.CCxIEN, a corresponding interrupt will be generated
- If user set TIMx_DINTEN.CCxDEN and set TIMx_CTRL2.CCDSEL to select DMA request, and DMA request will be sent

User can set TIMx_CCMODx.OCxPEN to choose capture/compare shawdow regisete using capture/compare preload registers (TIMx_CCDATx) or not

The time resolution is one counting period of the counter.

In one pulse mode, the output compare mode can also be used to output a single pulse

Here are the configuration steps for output compare mode:

- First of all, user should select the counter clock.
- Secondly, set TIMx_AR and TIMx_CCDATx with required data.
- If user need to generate an interrupt, set TIMx_DINTEN.CCxIEN.
- Then select the output mode by set TIMx_CCEN.CCxP, TIMx_CCMODx.OCxMD, TIMx_CCEN.CCxEN, etc.
- At last, set TIMx_CTRL1.CNTEN to enable the counter.

User can update the output waveform by setting TIMx_CCDATx at any time, as long as the preload register is not enabled. Otherwise the TIMx_CCDATx shadow register will be updated at the next update event

Here is an example.

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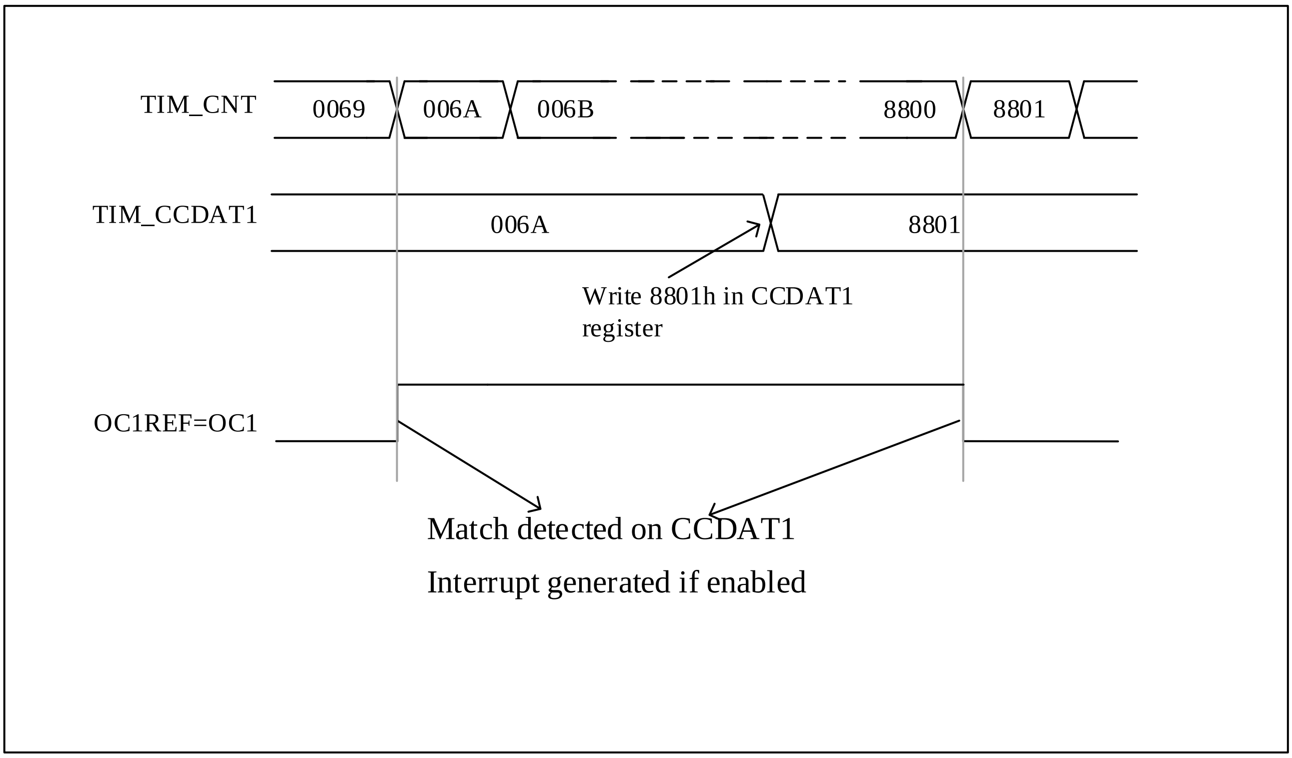
Figure 13-17 Output Compare Mode, Toggle on OC1



13.3.9 PWM Mode

User can use PWM mode to generate a signal whose duty cycle is determined by the value of the TIMx_CCDATx register and whose frequency is determined by the value of the TIMx_AR register. And depends on the value of TIMx_CTRL1.CAMSEL, the TIM can generate PWM signal in edge-aligned mode or center-aligned mode.

User can set PWM mode 1 or PWM mode 2 by setting TIMx_CCMODx. OCxMD=110 or setting TIMx_CCMODx. OCxMD=111. To enable preload register, user must set corresponding TIMx_CCMODx.OCxPEN. And then set TIMx_CTRL1.ARPEN to auto-reload preload register eventually.

User can set polarity of OCx by setting TIMx_CCEN.CCxP.

The values of TIMx_CNT and TIMx_CCDATx are always compared with each other when the TIM is under PWM mode.

Only if an update event occurs, the preload register will transfer to the shadow register. Therefore user must reset all the registers by setting TIMx_EVTGEN.UDGN before the counter starts counting.

13.3.9.1 PWM center-aligned mode

If user set TIMx_CTRL1.CAMSEL equal 01, 10 or 11, the PWM center-aligned mode will be active. The setting of the compare flag depends on the value of TIMx_CTRL1.CAMSEL. There are three kinds of situation that the compare flag is set, only when the counter counts up, only when the counter counts down, or when the counter counts up and counts down. User should not modified TIMx_CTRL1.DIR by software, it is updated by hardware.

Examples of center-aligned PWM waveforms is as follow, and the setting of the waveform are: TIMx_AR=8, PWM mode 1, the compare flag is set when the counter counts down corresponding to TIMx_CTRL1.CAMSEL=01.

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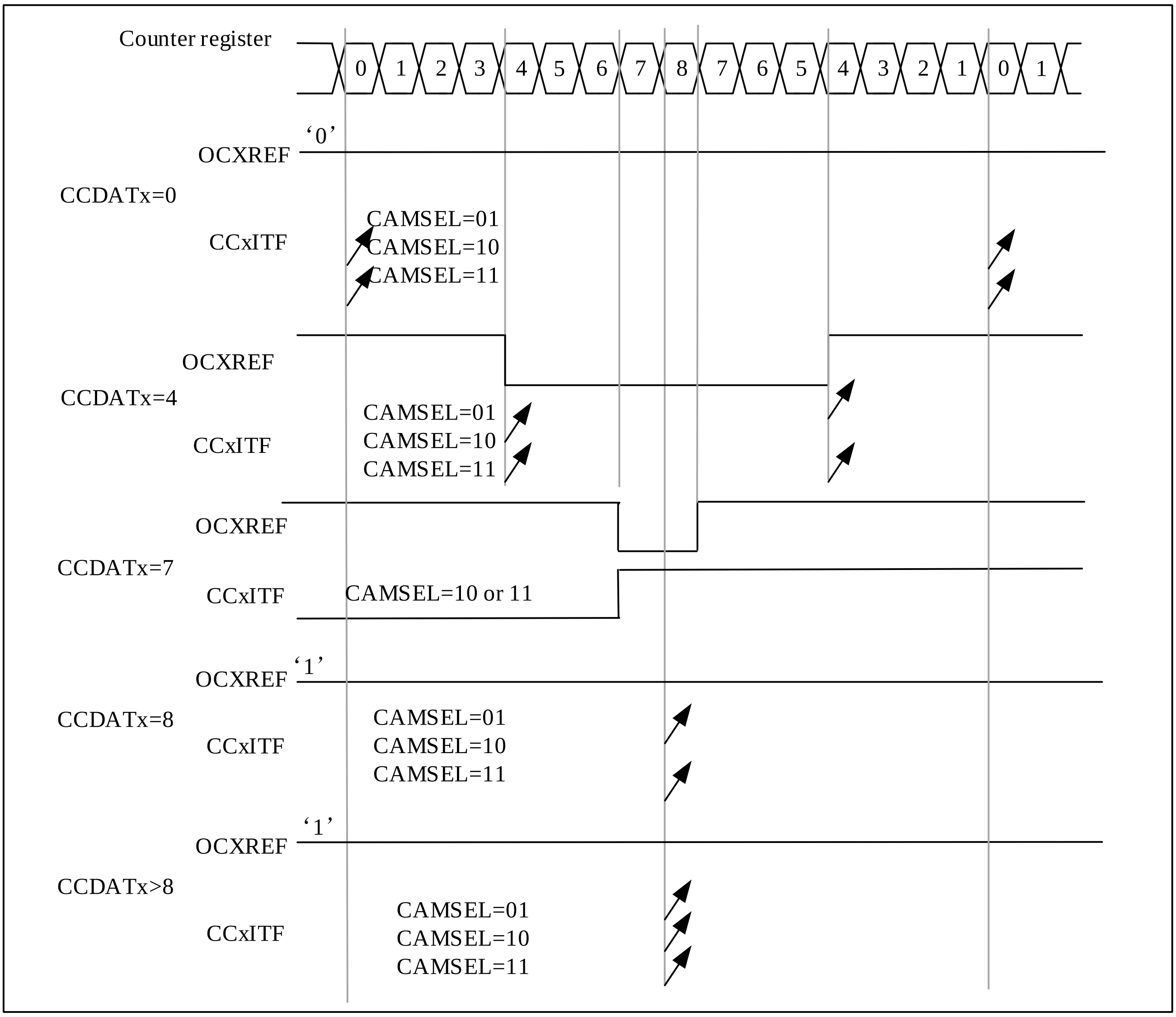
Figure 13-18 Center-aligned PWM Waveform (AR=8)



When using center-aligned mode, users should pay attention to the following considerations:

- It depends on the value of TIMx_CTRL1.DIR that the counter counts up or down. Cautions that the DIR and CAMSEL bits should not be changed at the same time.
- User should not write the counter while running in center-aligned mode, otherwise it will cause unexpected results. Here are some examples:
  - If the value written into the counter is 0 or is the value of TIMx_AR, the direction will be updated but the update event will not be generated.
  - If the value written into the counter is greater than the value of auto-reload, the direction will not be updated
- To be on the safe side, user is suggested setting TIMx_EVTGEN.UDGN to generate an update by software

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before starting the counter, and not writing the counter while it is running.

13.3.9.2 PWM edge-aligned mode

There are two kinds of configuration in edge-aligned mode, up-counting and down-counting.

- **Up-counting**

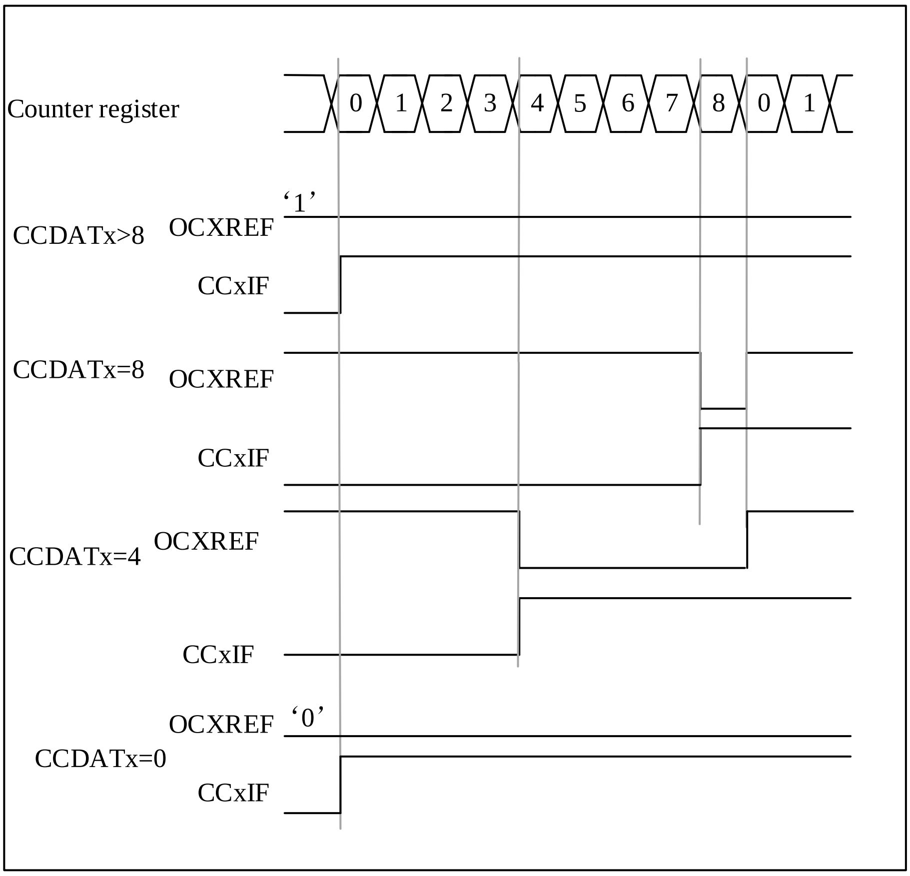
User can set TIMx_CTRL1.DIR=0 to make counter counts up.

Example for PWM mode1：

When TIMx_CNT < TIMx_CCDATx, the reference PWM signal OCxREF is high. Otherwise it will be low. If the compare value in TIMx_CCDATx is greater than the auto-reload value, the OCxREF will remains 1. Conversely, if the compare value is 0, the OCxREF will remains 0.

When TIMx_AR=8, the PWM waveforms are as follow:

Figure 13-19 Edge-aligned PWM Waveform (APR=8)



- **Down-counting**

User can set TIMx_CTRL1.DIR=1 to make counter counts down.
Example for PWM mode1：

When TIMx_CNT > TIMx_CCDATx, the reference PWM signal OCxREF is low. Otherwise it will be high. If the compare value in TIMx_CCDATx is greater than the auto-reload value, the OCxREF will remains 1.

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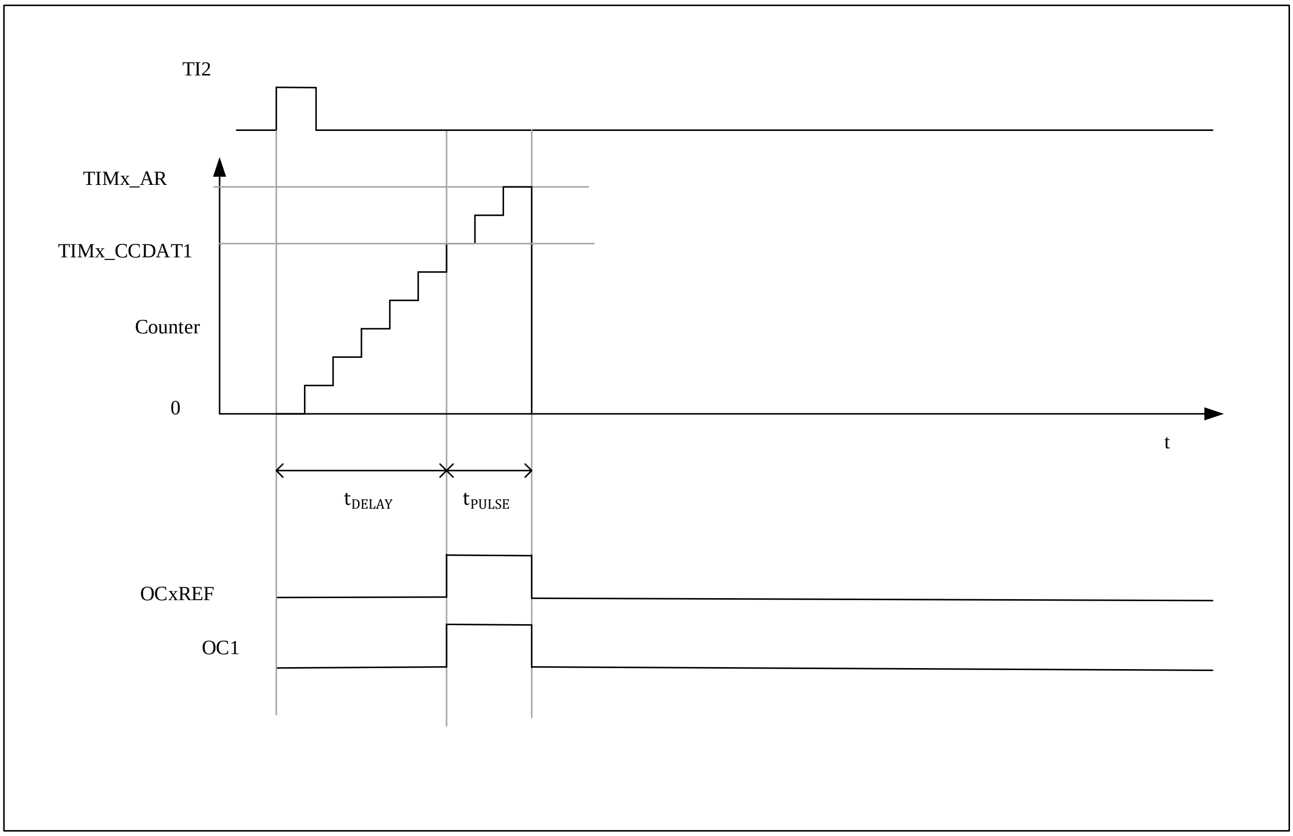
Note: If the nth PWM cycle CCDATx shadow register >= AR value, the shadow register value of CCDATx in the (n+1)th PWM cycle is 0. At the moment when the counter is 0 in the (n+1)th PWM cycle, although the value of the counter = CCDATx shadow register = 0 and OCxREF = '0', no compare event will be generated.

13.3.10 One-pulse Mode

In the one-pulse mode (ONEPM), a trigger signal is received, and a pulse t_{PULSE} with a controllable pulse width is generated after a controllable delay t_{DELAY}. The output mode needs to be configured as output compare mode or PWM mode. After selecting one-pulse mode, the counter will stop counting after the update event UEV is generated

Figure 13-20 Example of One-pulse Mode



The following is an example of a one-pulse mode：

A rising edge trigger is detected from the TI2 input, and a pulse with a width of t_{PULSE} is generated on OC1 after a delay of t_{DELAY}.

1. Counter configuration: count up, counter TIMx_CNT < TIMx_CCDAT1 ≤ TIMx_AR;
2. TI2FP2 is mapped to TI2, TIMx_CCMOD1.CC2SEL=‘01’; TI2FP2 is configured for rising edge detection, TIMx_CCEN.CC2P=‘0’;
3. TI2FP2 acts as the trigger (TRGI) of the slave mode controller and starts the counter, TIMx_SMCTRL.TSEL= ‘110’, TIMx_SMCTRL.SMSEL=‘0110’ (trigger mode);
4. TIMx_CCDAT1 writes the count value to be delayed (t_{DELAY}), TIMx_AR - TIMx_CCDAT1 is the count value

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of the pulse width t_{PULSE};

5. Configure TIMx_CTRL1.ONEPM=1 to enable single pulse mode, configure TIMx_CCMOD1.OC1MD=‘111’ to select PWM2 mode;
6. Wait for an external trigger event on TI2, and a one pulse waveform will be output on OC1;

13.3.10.1 Special case: OCx fast enable

In one-pulse mode, an edge is detected through the TIx input, and triggers the start of the counter to count to the comparison value and then output a pulse. These operations limit the minimum delay t_{DELAY} that can be achieved.

You can set TIMx_CCMODx.OCxFEN=1 to turn on OCx fast enable, after triggering the rising edge, the OCxREF signal will be forced to be converted to the same level as the comparison match occurs immediately, regardless of the comparison result. OCxFEN fast enable only takes effect when the channel mode is configured for PWM1 and PWM2 modes.

13.3.11 Clearing The OCxREF Signal on an External Event

If user set TIMx_CCMODx.OCxCEN=1, high level of tim_ocref_clr_in input can be used to driven the OCxREF signal to low, and the OCxREF signal will remains low, until the next UEV happens. Only output compare and PWM modes can use this function. This cannot be used when it is in forced mode.

For example, to control the current, users can connect the ETR signal to the comparator's output. The operation of ETR is as follows:

- Set TIMx_SMCTRL.EXTPS=00 to disable the external trigger prescaler.
- Set TIMx_SMCTRL.EXCEN=0 to disable the external clock mode 2.
- Set TIMx_SMCTRL.EXTP and TIMx_SMCTRL.EXTF to configure the external trigger polarity and external trigger filter as needed.

Here is an example for the case that when ETRF input becomes high, the behavior of OCxREF signal for different value of OCxCEN. Timer is set to be in PWM mode in this case.

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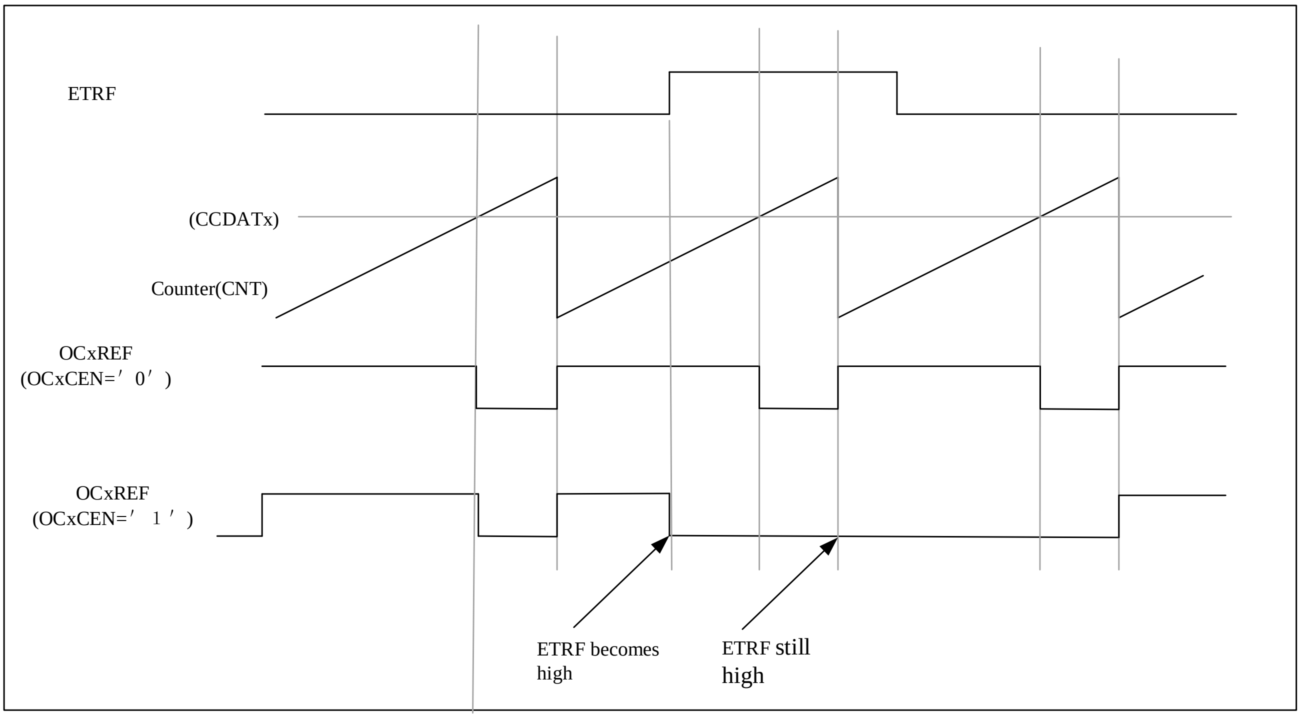
Figure 13-21 Clearing OCxREF of TIMx

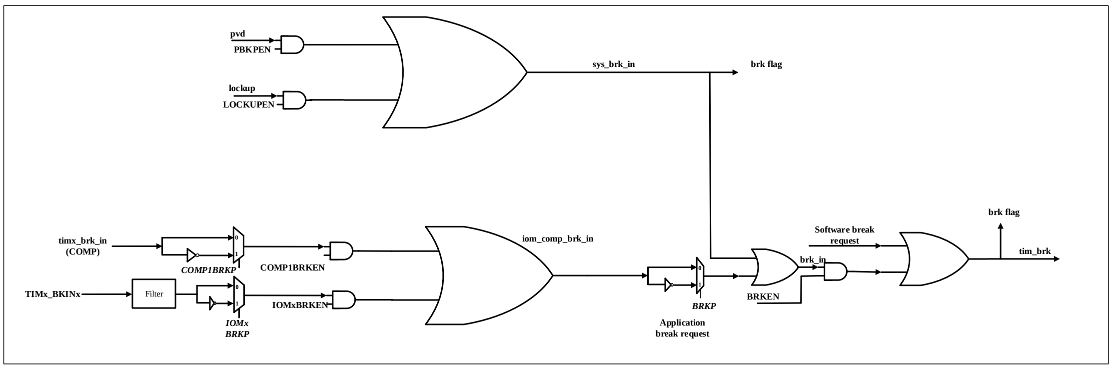


13.3.12 Breaking Function

When utilising the brake function, setting the corresponding control bit will modify the output enable signal and set the OCx output to the OIx level. The TIM3 brake function is only effective for OC3 and OC4; it is ineffective for OC1 and OC2.When multiple breaking signals are enabled, each breaking signal forms an OR logic. There are several signals that may act as sources of breaking.

- Break input pin(4 I/O pins).
- PVD event.
- Core Hardfault event.
- Comparator output signal.
- Software set TIMx_EVTGEN.BGN.

Figure 13-22 Break input



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After reset, the break circuit will be disabled. The MOEN bit will be at a low level. Users can set TIMx_BKDT.BKEN to enable the break function. By setting TIMx_BKDT.BKP, you can select the polarity of the break input signal. Users can simultaneously modify TIMx_BKDT.BKEN and TIMx_BKDT.BKP. After users set TIMx_BKDT.BKEN and TIMx_BKDT.BKP, there is a 1 APB clock cycle delay before it takes effect. Therefore, users need to wait for 1 APB clock cycle before reading back the written value.

The falling edge of MOEN can be asynchronous, so a synchronization circuit is placed between the actual signal and the synchronous control bit. This circuit will introduce a delay between the asynchronous and synchronous signals. When the user sets TIMx_BKDT.MOEN to a low level, a delay needs to be inserted before reading this value. This is because an asynchronous signal is written, but the user is reading a synchronous signal.

The behavior after the break occurs is as follows:

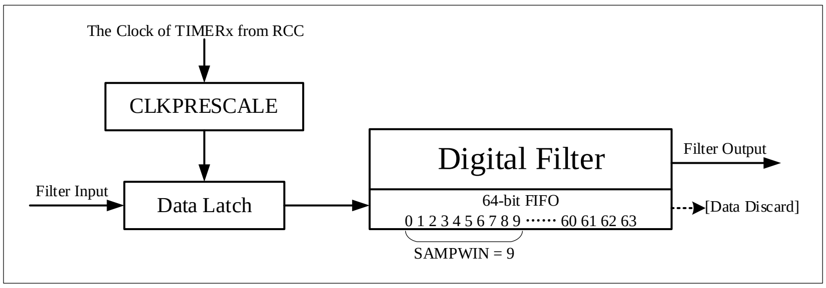
- TIMx_BKDT.MOEN shall be cleared asynchronously, causing the output to immediately enter the idle state (OIx). This shall remain effective even when the MCU oscillator is disabled.
- Once TIMx_BKDT.MOEN=0,the output of each output channel will be driven by the level programmed in TIMx_CTRL2.OIx.
- If TIMx_DINTEN.BIEN=1, an interrupt will be generated when TIMx_STS.BITF=1.
- If the user sets TIMx_BKDT.AOEN, TIMx_BKDT.MOEN will be automatically set on the next UEV occurrence. The user can adjust it using this feature. If the user does not set TIMx_BKDT.AOEN, TIMx_BKDT.MOEN will remain at a low level until set to 1 again. In this case, the user can use it to ensure safety. The user can connect the break input to a thermal sensor, power driver alarm, or other safety components.
- When the break input is active, TIMx_BKDT.MOEN cannot be automatically set or set simultaneously by software, and TIMx_STS.BITF cannot be cleared. This is because the break input is in an active state at the level.

To ensure application safety, the break circuit has write protection functionality and break input-output management. It allows users to freeze certain parameters, such as dead-time duration, OCx/OCxN polarity and disabled state, OCxMD configuration, break enable and polarity. Users can choose one of three protection levels by setting TIMx_BKDT.LCKCFG. However, TIMx_BKDT.LCKCFG can only be written once after MCU reset.

13.3.12.1 Break Filter

The register TIMx_BKFR is described as follows：

Figure 13-23 Sliding filter



- The digital filter samples the brake signal using the RCC's TIMx clock and accumulates the samples in a 64-bit FIFO. It samples data only within the window size defined in TIMx_BKFR.WSIZE [5:0], with a maximum size

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of 64.

- The filter output samples the majority value within the sampling window, which is defined by the threshold in TIMx_BKFR.THRESH [5:0], with a maximum threshold of 63. This value should be equal to or greater than half the window size. If the count of logic 1s and logic 0s within the sampling window is not greater than the threshold, the digital filter will maintain the previous output value.
- RCC_TIMFILTCFG.TIM3FILTCLK[4:0] register determines the sampling rate of the corresponding digital filter. The filter FIFO captures a sample value from the input at each sampling clock.
- If the digital filter is disabled, the filter input is directly output.

13.3.13 Debug Mode

When the microcontroller is in debug mode (the Cortex-M0 core halted), depending on the DBG_CTRL.TIMx_STOP configuration, the TIMx counter can either continue to work normally or stop. For more details, refer to Section 3.3.1.

13.3.14 External Event Triggering LVR Mounting

Users may select an external signal as a trigger to reload the timer value with the current value from the external event counter load register (TIMx_ENCLVR. LVR[31:0]). Different external trigger signals may be selected by setting the desired value in the TIMx_SMCTRL. TSEL[2:0] register. This functionality is enabled via the TIMx_CTRL1.TRGLDCNTEN bit.

Note that when selecting the edge detector with trigger source TI1 (TSEL = “100”), the trigger signal is valid on both rising and falling edges. When selecting other trigger sources (TSEL ≠ “100”), the trigger signal is valid only on rising edges. Users may also configure CCxP=1 or EXTP=1 to select the corresponding trigger signal valid on falling edges.

Note: When enabling the external event (TRGI) trigger to load counter values, if output comparison mode is simultaneously employed, either ETRF or ITRx must be selected as the trigger source (TSEL can only be configured as ‘0xx or 111’).

In the diagram below, the external signal serves as a trigger, activated on its rising edge. Each time a rising edge of the external signal is detected, the timer value is loaded into TIMx_ENCLVR. LVR[31:0] after two TIM_CLK cycles.

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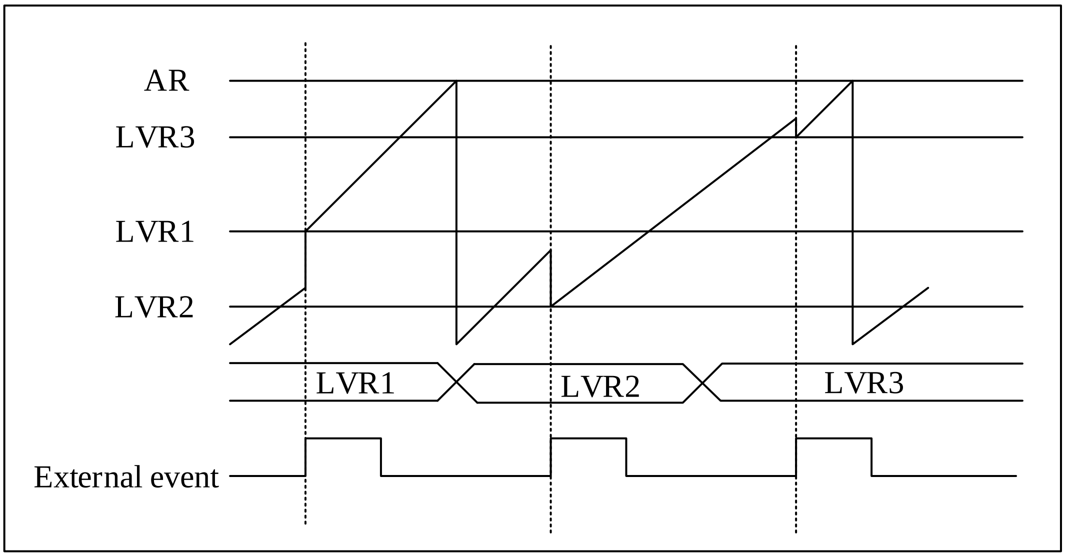
Figure 13-24 CNT counting method when an external event triggers LVR loading



13.3.15 TIMx and External Trigger Synchronization

Same as the advanced timer, refer to Section 12.3.16.

13.3.16 Timer Synchronization

All TIMx timers are internally interconnected to each other. This implementation allows a master timer to provide trigger to reset, start, stop or provide a clock for the other slave timers. The master clock is used for internal counter and can be prescaled. Below figure shows a block diagram of timer interconnection. The synchronization function does not support dynamic change of the connection. User should configure and enable the slave timer before enabling the master timer's trigger or clock.

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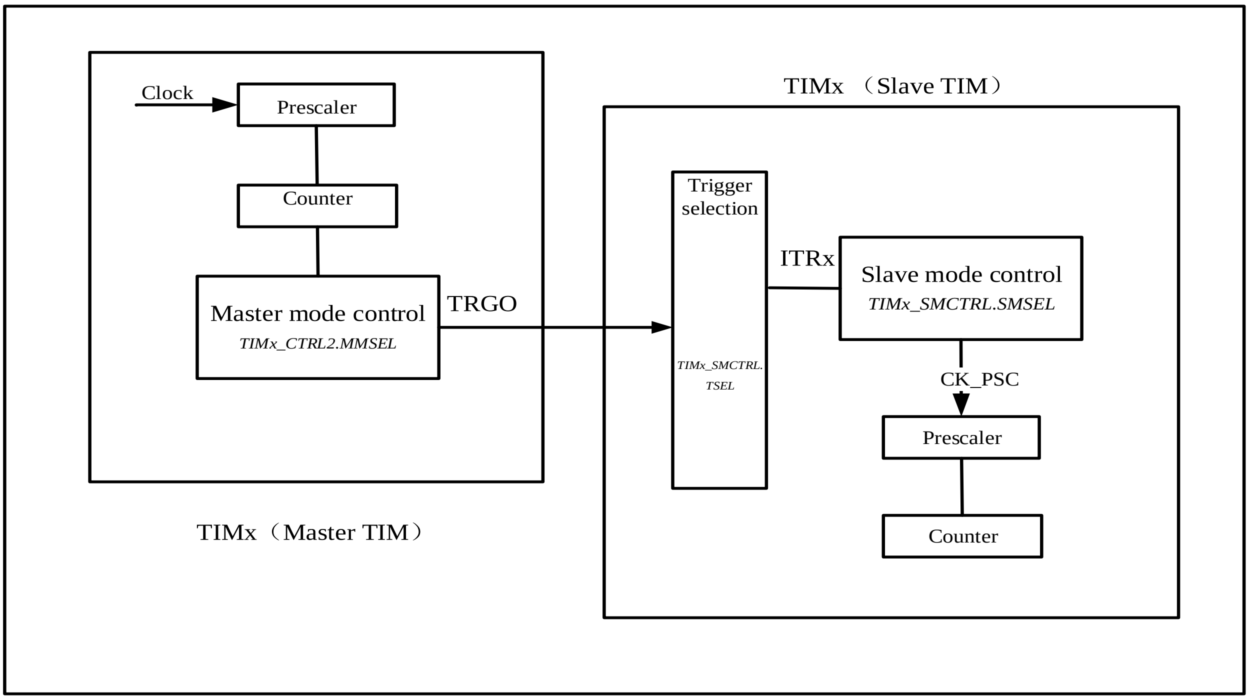
Figure 13-25 Master/Slave Timer Connection



13.3.16.1 Master timer as a prescaler for another timer

TIM1 acts as the prescaler for TIM3. TIM1 is master timer, and TIM3 is slave timer.

User needs to do the following steps for this configuration.

- Set TIM1_CTRL2.MMSEL='010' to use the update event of TIM1 as trigger output.
- Configure TIM3_SMCTRL.TSEL= '000' to connect the TRGO of TIM1 to TIM3.
- Configure TIM3_SMCTRL.SMSEL = '0111' so that the slave mode controller will be configured in external clock mode 1.
- Start TIM3 by setting TIM3_CTRL1. CNTEN = '1'.
- Start TIM1 by setting TIM1_CTRL1. CNTEN = '1'.

Note: If user select OCx as the trigger output of TIM1 by configuring MMSEL = '1xx', OCx rising edge will be used to drive TIM3.

13.3.16.2 Master timer to enable another timer

In this example, TIM3 is enabled by the output compare of TIM1. TIM3 counter will start to count after the OC1REF output from TIM1 is high. Both counters are clocked based on CK_INT via a prescaler divide by 3 is performed ($f_{CK\_CNT} = f_{CK\_INT}/3$).

The configuration steps are shown as below。

- Set TIM1_CTRL2.MMSEL='100' to use the OC1REF of TIM1 as trigger output.
- Configure TIM1_CCMOD1 register to configure the OC1REF output waveform.

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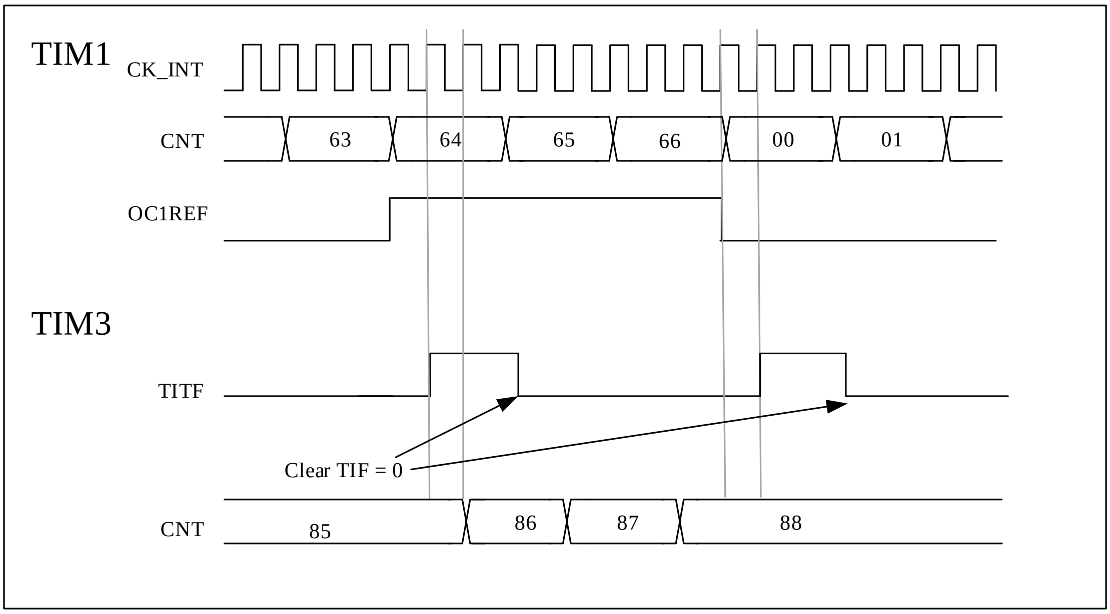
- Set TIM3_SMCTRL.TSEL = ‘000’ to connect TIM1 trigger output to TIM3.
- Set TIM3_SMCTRL.SMSEL= ‘0101’ to set TIM3 to gated mode.
- Set TIM3_CTRL1.CNTEN= ‘1’ to start TIM3.
- Set TIM1_CTRL1.CNTEN= ‘1’ to start TIM1.

Note: The TIM3 clock is not synchronized with the TIM1 clock, this mode only affects the TIM3 counter enable signal.

Figure 13-26 TIM3 Gated by OC1REF of TIM1



In the next example, it sets the enable of TIM3 with enable signal of TIM1. Set TIM1.CTRL1.CNTEN = ‘0’ to stop TIM1. TIM3 counts on the divided internal clock only when TIM1 is enable. Both counters are clocked based on CK_INT via a prescaler divide by 3 is performed ($f_{CK\_CNT} = f_{CK\_INT}/3$).

The configuration steps are shown as below:

- Set TIM1_CTRL2.MMSEL=’001’ to use the enable signal of TIM1 as trigger output.
- Set TIM3_SMCTRL.TSEL = ‘000’ to configure TIM3 to get the trigger input from TIM1.
- Set TIM3_SMCTRL.SMSEL = ‘0101’ to configure TIM3 in gated mode.
- Set TIM3_CTRL1.CNTEN= ‘1’ to start TIM3.
- Set TIM1_CTRL1.CNTEN= ‘1’ to start TIM1.
- Set TIM1_CTRL1.CNTEN= ‘0’ to stop TIM1.

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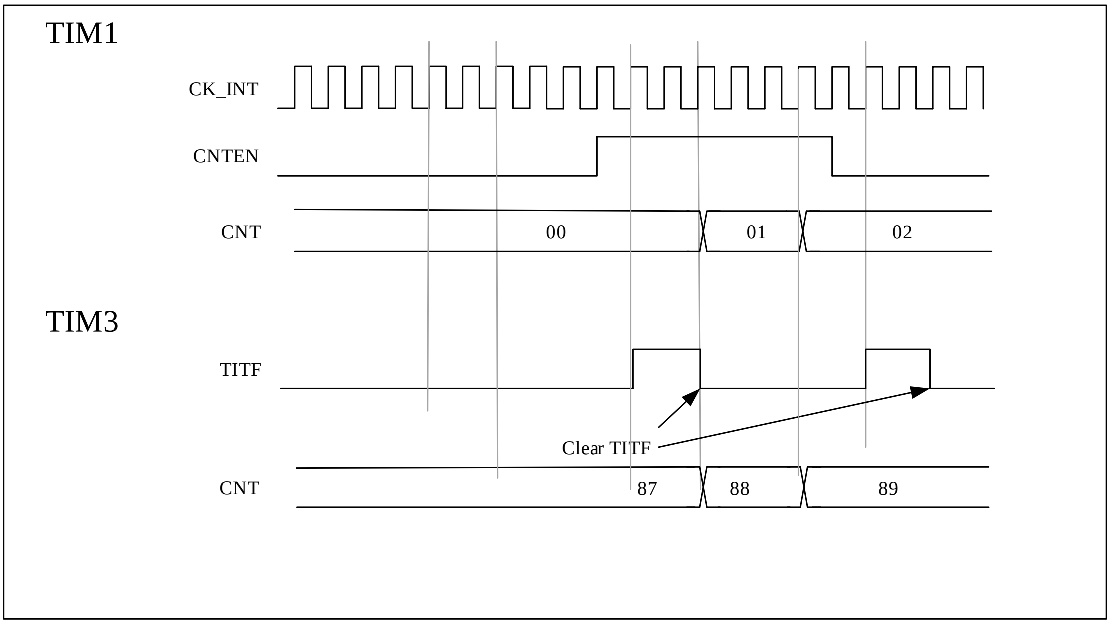
Figure 13-27 TIM3 Gated by Enable Signal of TIM1



13.3.16.3 Master timer to start another timer

In this example, we can use update event as trigger source. TIM1 is master, TIM3 is slave.

The configuration steps are shown as below:

- Set TIM1_CTRL2.MMSEL=' 010' to use the update event of TIM1 as trigger output.
- Configure TIM1_AR register to set the output period.
- Set TIM3_SMCTRL .TSEL= '000' to connect TIM1 trigger output to TIM3.
- Set TIM3_SMCTRL. SMSEL = '0110' to set TIM3 to trigger mode.
- Set TIM1_CTRL1.CNTEN=1 to start TIM1.

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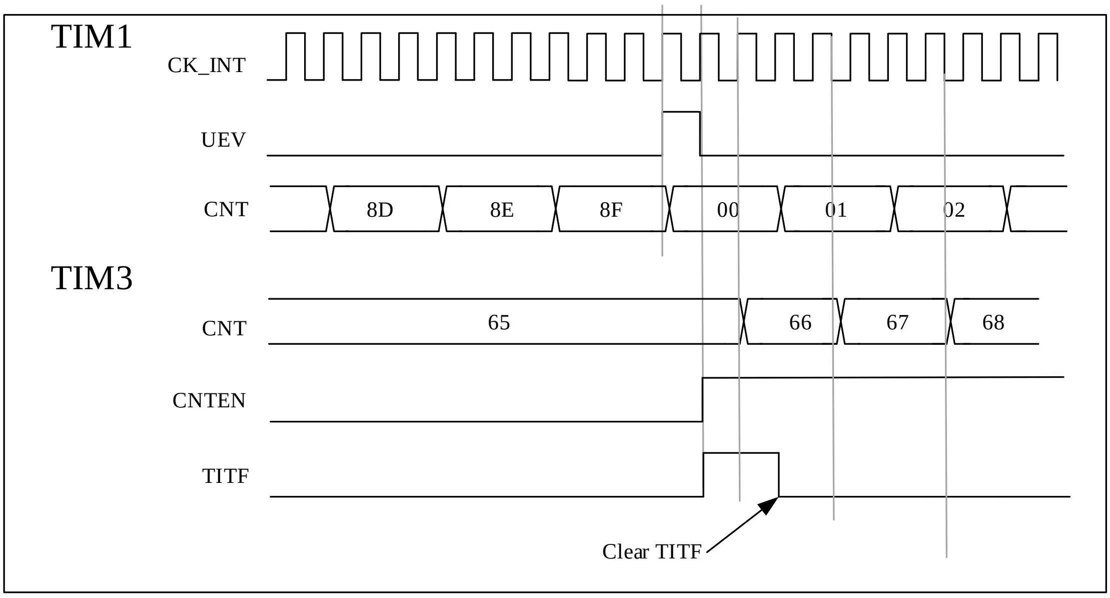
Figure 13-28 Trigger TIM3 with an Update of TIM1



13.3.16.4 Start 2 timers synchronously using an external trigger

In this example, TIM1 is enabled when TIM1's TI1 input rises, and TIM3 is enabled when TIM1 is enabled. To ensure the alignment of counters, TIM1 must be configured in master/slave mode. For TI1, TIM1 is the slave; for TIM3, TIM1 is the master.

The configuration steps are shown as below:

- Set TIM1.MMSEL = '001' to use the enable signal as trigger output.
- Set TIM1_SMCTRL.TSEL = '100' to configure the TIM1 to slave mode and receive the trigger input of TI1.
- Set TIM1_SMCTRL.SMSEL = '0110' to configure TIM1 to trigger mode.
- Set TIM1_SMCTRL.MSMD = '1' to configure TIM1 to master/slave mode.
- Set TIM3_SMCTRL.TSEL = '000' to connect TIM1 trigger output to TIM3.
- Set TIM3_SMCTRL.SMSEL = '0110' to configure TIM3 to trigger mode.

When TI1 rising edge arrives, both timers start counting synchronously according to the internal clock, and both TITF flags are set simultaneously.

Note: The following figure shows a delay between CNTEN and CK_PSC of TIM1 in master/slave mode.

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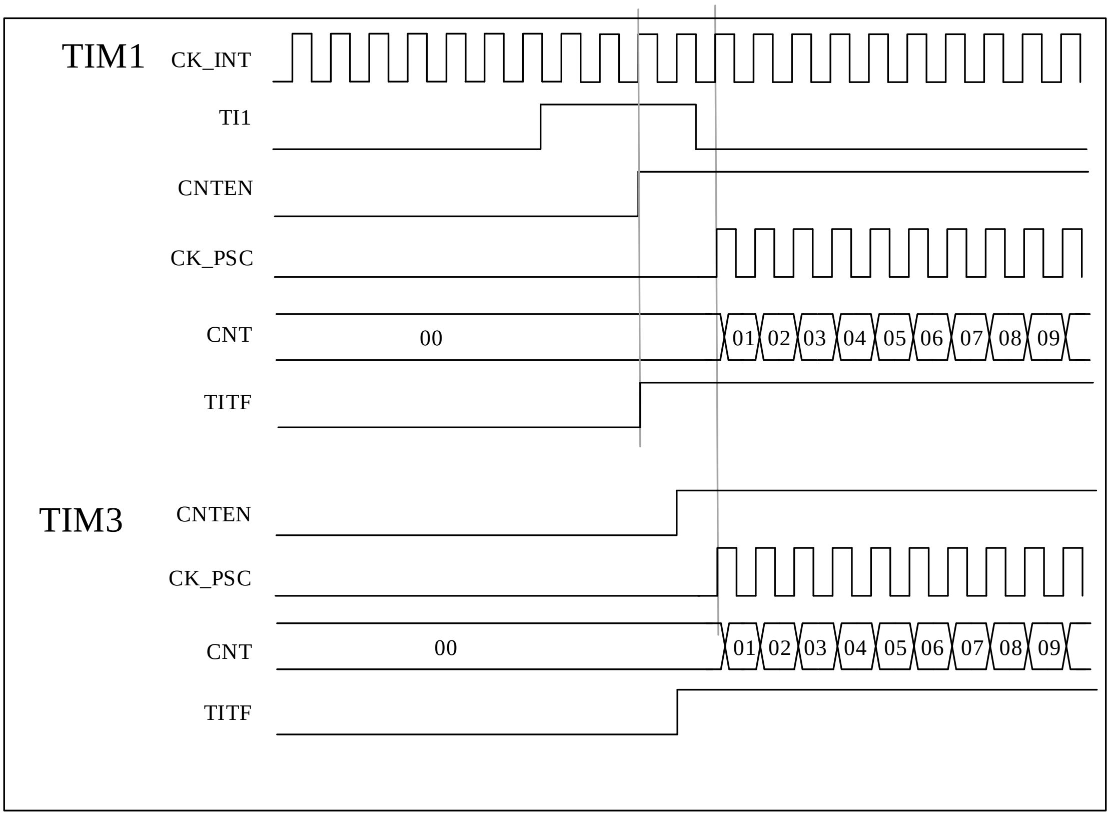
Figure 13-29 Triggers TIM1 and TIM3 Using the TI1 Input of TIM1



13.3.17 Encoder Interface Mode

The encoder uses two inputs TI1 and TI2 as an interface. And the counter counts on every edge change on TI1FP1 or TI2FP2. The counting direction is automatically controlled by hardware TIMx_CTRL1.DIR. There are three types of encoder counting modes:

- Encode Mode 1: The counter only counts on the edge of TI1, TIMx_SMCTRL.SMSEL = ‘0001’;
- Encode Mode 2: The counter only counts on the edge of TI2, TIMx_SMCTRL.SMSEL =’0010’;
- Encode Mode 3: The counter counts on both TI1 and TI2 edges, TIMx_SMCTRL.SMSEL = ‘0011’;

The encoder interface is equivalent to using an external clock with direction selection, and the counter only counts continuously between 0 and the auto-reload value (TIMx_AR.AR [15:0]). Therefore, it is necessary to configure the auto-reload register TIMx_AR in advance.

Note: Encoder mode and external clock mode 2 are not compatible and must not be selected together.

The relationship between the counting direction and the encoder signal is shown in following table:

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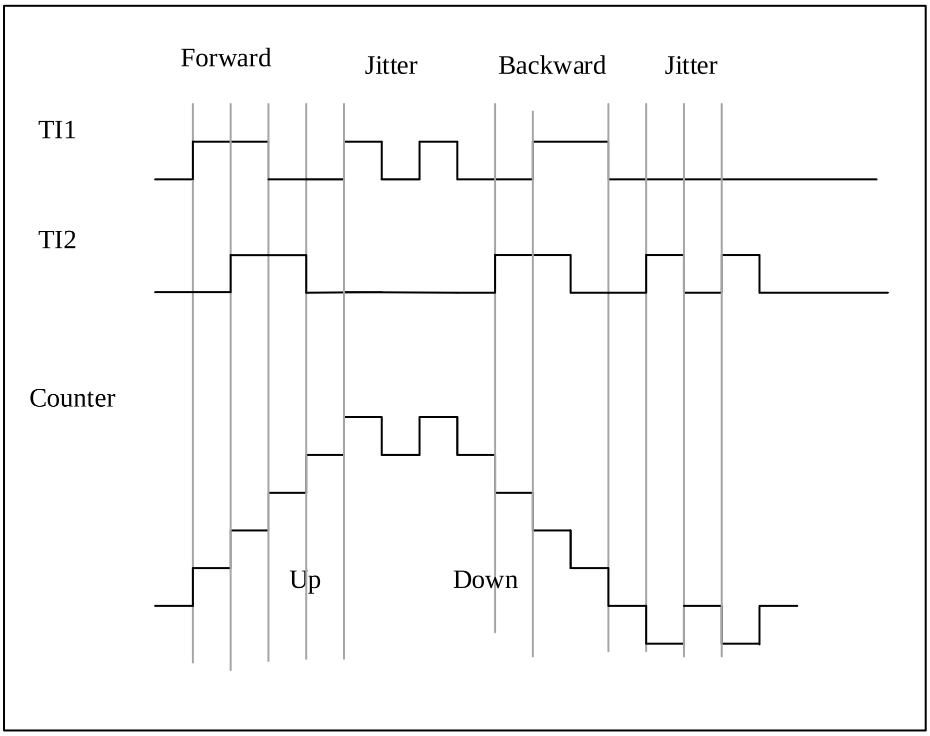
Table 13-1 The Relationship between the Counting Direction and the Encoder Signal

Active Edge	Relative Signal Level（TI1FP1 for TI2, TI2FP2 for TI1）	TI1FP1 Signal		TI2FP2 Signal	
		Rising	Falling	Rising	Falling
Counting only at TI1	High	Counting down	Counting up	Don't count	Don't count
	Low	Counting up	Counting down	Don't count	Don't count
Counting only at TI2	High	Don't count	Don't count	Counting up	Counting down
	Low	Don't count	Don't count	Counting down	Counting up
Counting on TI1 and TI2	High	Counting down	Counting up	Counting up	Counting down
	Low	Counting up	Counting down	Counting down	Counting up

Here is an example of an encoder with dual edges triggering selected to suppress input jitter：

1. IC1FP1 is mapped to TI1(TIMx_CCMOD1.CC1SEL=‘01’), IC1FP1 is not inverted(TIMx_CCEN.CC1P=‘0’);
2. IC1FP2 is mapped to TI2(TIMx_CCMOD2.CC2SEL=‘01’), IC2FP2 is not inverted(TIMx_CCEN.CC2P=‘0’);
3. The input is valid on both rising and falling edges(TIMx_SMCTRL.SMSEL=‘0011’);
4. Enable counter TIMx_CTRL1.CNTEN=‘1’;

Figure 13-30 Example of Counter Operation in Encoder Interface Mode



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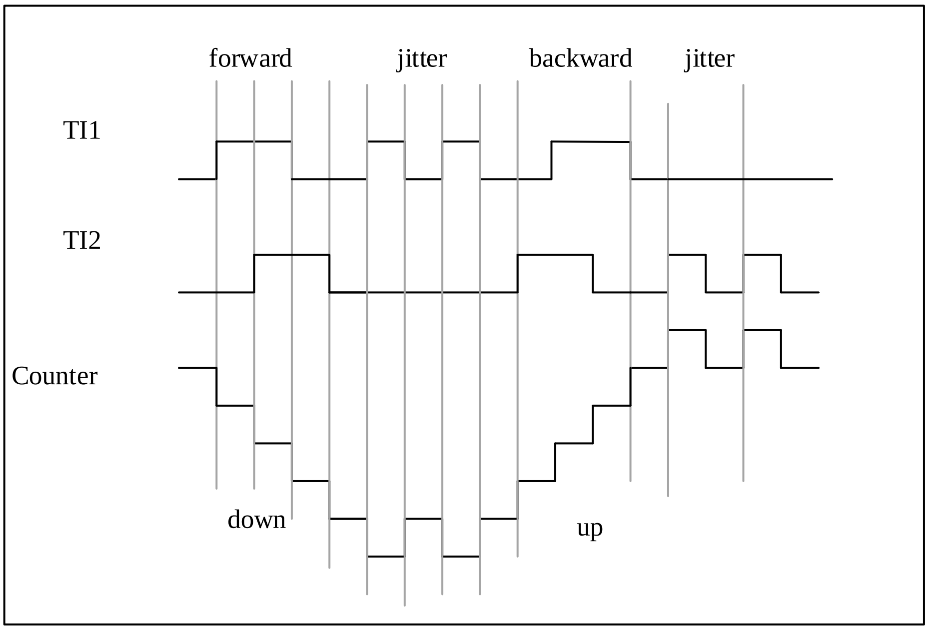
The following figure shows the example of counter behavior when IC1FP1 polarity is inverted (CC1P='1', other configurations are the same as above)

Figure 13-31 Encoder Interface Mode Example with IC1FP1 Polarity Inverted



13.3.18 Interfacing with Hall Sensor

Please refer to Section 12.3.21.

13.4 TIMx Register Description (x=3)

For abbreviations used in the registers, please refer to Section 1.1.

These peripheral registers can be operated as half-word (16 bits) or word (32 bits).

13.4.1 Register Overview

Table 13-2 Register Overview

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
000h	TIM_CTRL1	TRGRSTCNTEN	Reserve														C1SEL	Reserve		CLRSEL	Reserve	PBKPEN	LBKPEN	ARPEN	ONEPM	Reserve		UPDIS	UPRS	CAMSEL[1:0]		DIR	CNTEN
004h	TIM_CTRL2	Reserve												T1SEL	Reserve	CCDSEL	Reserve		MMSEL[2:0]			Reserve					OI4	Reserve	OI3	Reserve			
008h	TIM_STS	Reserve				IOMBITF	Reserve			COMPBITF	PBKPITF	LBKPITF	Reserve	BITF	TITF	Reserve	UDITF	Reserve				CC4OCF	CC3OCF	CC2OCF	CC1OCF	Reserve				CC4ITF	CC3ITF	CC2ITF	CC1ITF

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00Ch	TIM_EVTGEN	Reserve	BGN	TGN	Reserve	UDGN	Reserve	CC4GN	CC3GN	CC2GN	CC1GN							
010h	TIM_SMCTRL	Reserve	MSMD	EXTF[3:0]	EXTP	EXCEN	EXTPS[1:0]	SMSEL[3:0]	Reserve	TSEL[2:0]								
014h	TIM_DINTEN	Reserve	TDEN	Reserve	UDEN	BIEN	TIEN	UIEN	Reserve	CC4DEN	CC3DEN	CC2DEN	CC1DEN	Reserve	CC4IEN	CC3IEN	CC2IEN	CC1IEN
018h	TIM_CCMOD1_OUT	Reserve	OC2MD[2:0]	OC2CEN	OC2FEN	OC2PEN	CC2SEL[1:0]	OC1MD[2:0]	OC1CEN	OC2FEN	OC1PEN	CC1SEL[1:0]						
	TIM_CCMOD1_IN	Reserve	IC2F[3:0]	IC2PSC[1:0]	CC2SEL[1:0]	IC1F[3:0]	IC1PSC[1:0]	CC1SEL[1:0]										
01Ch	TIM_CCMOD2_OUT	Reserve	OC4MD[2:0]	OC4CEN	OC4FEN	OC4PEN	CC4SEL[1:0]	OC3MD[2:0]	OC3CEN	OC3FEN	OC3PEN	CC3SEL[1:0]						
	TIM_CCMOD2_IN	Reserve	IC4F[3:0]	IC4PSC[1:0]	CC4SEL[1:0]	IC3F[3:0]	IC3PSC[1:0]	CC3SEL[1:0]										
024h	TIM_CCEN	Reserve	CC4P	CC4EN	Reserve	CC3P	CC3EN	Reserve	CC2P	CC2EN	Reserve	CC1P	CC1EN	Reserve				
028h	TIM_CCDAT1	Reserve	CCDAT1[15:0]															
02Ch	TIM_CCDAT2	Reserve	CCDAT2[15:0]															
030h	TIM_CCDAT3	Reserve	CCDAT3[15:0]															
034h	TIM_CCDAT4	Reserve	CCDAT4[15:0]															
040h	TIM_PSC	Reserve	PSC[15:0]															
044h	TIM_AR	Reserve	AR[15:0]															
048h	TIM_CNT	Reserve	CNT[15:0]															
04Ch	TIM_REPCNT	Reserve	REPCNT[7:0]															
050h	TIM_BKDT	Reserve	LCKCFG[1:0]	Reserve	BKEN	BKP	AOEN	MOEN	Reserve									
060h	TIM_BKFR	Reserve	THRESH[5:0]	Reserve	WSIZE[5:0]	FILTEN	Reserve											
07Ch	TIM_AF1	Reserve	IOM4BRKP	IOM3BRKP	IOM2BRKP	IOM4BRKEN	IOM3BRKEN	IOM2BRKEN	Reserve	COMP1BRKP	IOM1BRKP	Reserve	COMP1BRKEN	IOMBRKEN				
090h	TIM_ENCLVR	Reserve	LVR[15:0]															
094h	TIM_DCTRL	Reserve	DBADDR[5:0]	Reserve	DBLEN[5:0]													
098h	TIM_DADDR	BURST[31:0]																

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13.4.2 Control Register 1 (TIMx_CTRL1)

Offset address：0x00

Reset value：0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TRGLDCNTEN	Reserved														C1SEL
rw															rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved		CLRSEL	Reserved	PBKPEN	LBKPEN	ARPEN	ONEPM	Reserved		UPDIS	UPRS	CAMSEL[1:0]		DIR	CNTEN
		rw		rw	rw	rw	rw			rw	rw	rw		rw	rw

Bit Field	Name	Description
31	TRGLDCNTEN	The TRGI effective event trigger counter is loaded with the LVR value to enable it. Upon detection of a TRGI event (as determined by the TIMx_SMCTRL.TSEL[2:0] register), the counter shall be loaded with the TIMx_ENCLVR .LVR value. 0: TRGI valid events cannot trigger counter loading with LVR values 1: TRGI valid events can trigger counter loading with LVR values
30:17	Reserved	Reserved, the reset value must be maintained
16	C1SEL	Channel 1 Selection 0: Select the external CH1 (from IOM) signal. 1: Select internal CH1 (from COMP) signal.
15:14	Reserved	Reserved, the reset value must be maintained
13	CLRSEL	OcxRef Clear Selection 0: Select the external Ocxclr (ETR) signal 1: Select the internal Ocxclr (from COMP) signal
12	Reserved	Reserved, the reset value must be maintained
11	PBKPEN	PVD break Enable 0: Disable 1: Enable
10	LBKPEN	LockUp break Enable（Core Hardfault） 0: Disable 1: Enable
9	ARPEN	Auto-reload preload enable 0: Shadow register disable for TIMx_AR register 1: Shadow register enable for TIMx_AR register
8	ONEPM	One-pulse mode 0: Disable one-pulse mode, the counter counts are not affected when an update event occurs。 1: Enable one-pulse mode, the counter stops counting when the next update event occurs
7:6	Reserved	Reserved, the reset value must be maintained

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Bit Field	Name	Description
5	UPDIS	Update disable This bit is used to enable/disable the Update event (UEV) events generation by software. 0: Enable UEV. And UEV will be generated if one of following condition been fulfilled: – Counter overflow/underflow – The TIMx_EVTGEN.UDGN bit is set – Update generation from the slave mode controller Shadow registers will update with preload value. 1: UEV disabled. No update event is generated, and the shadow registers (AR, PSC, and CCDATx) keep their values. If the TIMx_EVTGEN.UDGN bit is set or a hardware reset is issued by the slave mode controller, the counter and prescaler are reinitialized.
4	UPRS	Update request source This bit is used to select the UEV event sources by software. 0: If update interrupt or DMA request is enabled, any of the following events will generate an update interrupt or DMA request – Counter overflow/underflow – TIMx_EVTGEN.UDGN bit is set – Update generation from the slave mode controller 1: If update interrupt or DMA request is enabled, only counter overflow/underflow will generate update interrupt or DMA request
3:2	CAMSEL[1:0]	Center-aligned mode selection 00: Edge-aligned mode. TIMx_CTRL1.DIR specifies up-counting or down-counting。 01: Center-aligned mode 1. The counter counts in center-aligned mode, and the output compare interrupt flag bit is set to 1 when down-counting。 10: Center-aligned mode 2. The counter counts in center-aligned mode, and the output compare interrupt flag bit is set to 1 when up-counting。 11: Center-aligned mode 3. The counter counts in center-aligned mode, and the output compare interrupt flag bit is set to 1 when up-counting or down-counting。 *Note: Switching from edge-aligned mode to center-aligned mode is not allowed when the counter is still enabled (TIMx_CTRL1.CNTEN = 1)*
1	DIR	Direction 0: Up-counting 1: Down-counting *Note: This bit is read-only when the counter is configured in center-aligned mode or encoder mode.*
0	CNTEN	Counter enable 0: Disable counter 1: Enable counter *Note: external clock, gating mode and encoder mode can only work after TIMx_CTRL1.CNTEN bit is set in the software. Trigger mode can automatically set TIMx_CTRL1.CNTEN bit by hardware.*

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Bit Field	Name	Description
		Note: After setting the CNTEN bit in the software, it is necessary to wait for at least two TIMx_CLK cycles for the CNTEN synchronisation from TIMx_PCLK to TIMx_CLK to take effect.

13.4.3 Control Register 2 (TIMx_CTRL2)

Offset address: 0x04

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved												TI1SEL	Reserved	CCDSEL	Reserved
												rw		rw	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MMSEL[3:0]				Reserved					OI4	Reserved	OI3	Reserved			
rw									rw		rw				

Bit Field	Name	Description
31:20	Reserved	Reserved, the reset value must be maintained
19	TI1SEL	TI1 selection 0: TIMx_CH1 pin connected to TI1 input; 1: TIMx_CH1, TIMx_CH2, and TIMx_CH3 pins are XOR connected to the TI1 input.
18	Reserved	Reserved, the reset value must be maintained
17	CCDSEL	Capture/compare DMA selection 0: When a CCx event occurs, a DMA request for CCx is sent； 1: When an update event occurs, a DMA request for CCx is sent.
16	Reserved	Reserved, the reset value must be maintained
15:12	MMSEL[3:0]	Master Mode Selection These 4 bits (TIMx_CTRL2. MMSEL [3:0]) are used to select the synchronization information (TRGO) sent to the slave timer in the master mode. Possible combinations are as follows： x000: Reset –When the TIMx_EVTGEN.UDGN is set or a reset is generated by the slave mode controller, a TRGO pulse occurs. And in the later case, the signal on TRGO is delayed compared to the actual reset. x001: Enable - The TIMx_CTRL1.CNTEN bit is used as the trigger output (TRGO). Sometimes you need to start multiple timers at the same time or enable slave timer for a period of time. The counter enable signal is set when TIMx_CTRL1.CNTEN bit is set or the trigger input in gated mode is high. When the counter enable signal is controlled by the trigger input, there is a delay on TRGO except if the master/slave mode is selected (see the description of the TIMx_SMCTRL.MSMD bit). x010: Update - The update event is selected as the trigger output (TRGO). For example, a master timer clock can be used as a slave timer prescaler.

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Bit Field	Name	Description
		x011: Compare pulse - Triggers the output to send a positive pulse (TRGO) when the TIMx_STS.CC1ITF is to be set (even if it is already high), when a capture or a comparison succeeds. x100: Compare - OC1REF signal is used as the trigger output (TRGO). x101: Compare - OC2REF signal is used as the trigger output (TRGO). x110: Compare - OC3REF signal is used as the trigger output (TRGO). x111: Compare - OC4REF signal is used as the trigger output (TRGO)
11:7	Reserved	Reserved, the reset value must be maintained
6	OI4	Output Idle state 4 0: When TIMx_BKDT.MOEN = 0, if OC4 is implemented, after dead-time OC4 = 0 1: When TIMx_BKDT.MOEN = 0, if OC4 is implemented, after dead-time OC4 = 1 *Note: Once TIMx_BKDT.LCKCFG level 1, 2, or 3 has been set, this bit cannot be modified.*
5	Reserved	Reserved, the reset value must be maintained
4	OI3	Output Idle state 3 0: When TIMx_BKDT.MOEN = 0, if OC3 is implemented, after dead-time OC3 = 0 1: When TIMx_BKDT.MOEN = 0, if OC3 is implemented, after dead-time OC3 = 1 *Note: Once TIMx_BKDT.LCKCFG level 1, 2, or 3 has been set, this bit cannot be modified.*
3:0	Reserved	Reserved, the reset value must be maintained

13.4.4 Status Registers (TIMx_STS)

Offset address: 0x08

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved				IOMBITF	Reserved			COMPBITF	PBKPITF	LBKPITF	Reserved	BITF	TITF	Reserved	UDITF
				rc_w0				rc_w0	rc_w0	rc_w0		rc_w0	rc_w0		rc_w0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved				CC4OCF	CC3OCF	CC2OCF	CC1OCF	Reserved				CC4ITF	CC3ITF	CC2ITF	CC1ITF
				rc_w0	rc_w0	rc_w0	rc_w0					rc_w0	rc_w0	rc_w0	rc_w0

Bit Field	Name	Description
31:28	Reserved	Reserved, the reset value must be maintained
27	IOMBITF	IOM Break interrupt flag Once the IOM Break input is active, it is set to '1' by hardware. If the IOM Break input is inactive, this bit can be cleared to '0' by software. 0: No break event generated; 1: Valid level detected on IOM Break input;
26:24	Reserved	Reserved, the reset value must be maintained
23	COMPBITF	COMP Break interrupt flag Once the COMP Break input is active, it is set to '1' by hardware. If the COMP Break input is inactive, this bit can be cleared to '0' by software.

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Bit Field	Name	Description
		0: No break event generated; 1: Valid level detected on COMP Break input;
22	PBKPITF	PVD Break interrupt flag Once the PVD Break input is active, it is set to '1' by hardware. If the PVD Break input is inactive, this bit can be cleared to '0' by software. 0: No break event generated; 1: Valid level detected on PVD Break input;
21	LBKPITF	Lockup Break interrupt flag Once the Lockup Break input is active, it is set to '1' by hardware. If the Lockup Break input is inactive, this bit can be cleared to '0' by software. 0: No break event generated; 1: Valid level detected on Lockup Break input;
20	Reserved	Reserved, the reset value must be maintained
19	BITF	Break interrupt flag Once the Break input is active, it is set to '1' by hardware. If the Break input is inactive, this bit can be cleared to '0' by software. 0: No break event generated; 1: Valid level detected on Break input;
18	TITF	Trigger interrupt flag This bit is set by hardware when an active edge is detected on the TRGI input when the slave mode controller is in a mode other than gated. This bit is set by hardware when any edge in gated mode is detected. This bit is cleared by software. 0: No trigger event occurred； 1: Trigger interrupt occurred.
17	Reserved	Reserved, the reset value must be maintained
16	UDITF	Update interrupt flag This bit is set by hardware when an update event occurs under the following conditions： –When TIMx_CTRL1.UPDIS = 0, and repetition counter value overflow or underflow (when repetition counter equal to 0 an update event is generated). – When TIMx_CTRL1.UPRS = 0, TIMx_CTRL1.UPDIS = 0, and set the TIMx_EVTGEN.UDGN bit by software to reinitialize the CNT. –When TIMx_CTRL1.UPRS = 0, TIMx_CTRL1.UPDIS = 0, and the counter CNT is reinitialized by the trigger event. (See TIMx_SMCTRL Register description) This bit is cleared by software. 0: No update event occurred 1: Update interrupt occurred
15:12	Reserved	Reserved, the reset value must be maintained
11	CC4OCF	Capture/Compare 4 overcapture flag See TIMx_STS.CC1OCF description.
10	CC3OCF	Capture/Compare 3 overcapture flag See TIMx_STS.CC1OCF description.
9	CC2OCF	Capture/Compare 2 overcapture flag See TIMx_STS.CC1OCF description.

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Bit Field	Name	Description
8	CC1OCF	Capture/Compare 1 overcapture flag This bit is set by hardware only when the corresponding channel is configured in input capture mode. Cleared by software writing 0. 0: No overcapture occurred; 1: TIMx_STS.CC1ITF was already set when the value of the counter has been captured in the TIMx_CCDAT1 register.
7:4	Reserved	Reserved, the reset value must be maintained.
3	CC4ITF	Capture/Compare 4 interrupt flag See TIMx_STS.CC1ITF description.
2	CC3ITF	Capture/Compare 3 interrupt flag See TIMx_STS.CC1ITF description.
1	CC2ITF	Capture/Compare 2 interrupt flag See TIMx_STS.CC1ITF description.
0	CC1ITF	Capture/Compare 1 interrupt flag **When the corresponding channel of CC1 is in output mode:** Except in center-aligned mode, this bit is set by hardware when the counter value is the same as the compare value (see TIMx_CTRL1.CAMSEL bit description). This bit is cleared by software. 0: No match occurred. 1: The value of TIMx_CNT is the same as the value of TIMx_CCDAT1. When the value of TIMx_CCDAT1 is greater than the value of TIMx_AR, the TIMx_STS.CC1ITF bit will go high if the counter overflows (in up-counting and up/down-counting modes) and underflows in down-counting mode. **When the corresponding channel of CC1 is in input mode:** This bit is set by hardware when the capture event occurs. This bit is cleared by software or by reading TIMx_CCDAT1. 0: No input capture occurred. 1: Input capture occurred. Counter value has captured in the TIMx_CCDAT1. An edge with the same polarity as selected has been detected on IC1.

13.4.5 Event Generation Registers (TIMx_EVTGEN)

Offset address: 0x0C

Reset values: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved					TGN	Reserved	UDGN	Reserved				CC4GN	CC3GN	CC2GN	CC1GN
					w		w					w	w	w	w

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Bit Field	Name	Description
31:11	Reserved	Reserved, the reset value must be maintained
10	TGN	Trigger generation This bit can generate a trigger event when set by software. And at this time TIMx_STS.TITF = 1, if the corresponding interrupt and DMA are enabled, the corresponding interrupt and DMA will be generated. This bit is automatically cleared by hardware. 0: No action No action 1: Generated a trigger event
9	Reserved	Reserved, the reset value must be maintained
8	UDGN	Update generation This bit can generate an update event when set by software. And at this time the counter will be reinitialized, the prescaler counter will be cleared, the counter will be cleared in center-aligned or up-counting mode, but take TIMx_AR in down-counting mode the value of the register. This bit is automatically cleared by hardware. 0: No action 1: Generated an update event
7:4	Reserved	Reserved, the reset value must be maintained
3	CC4GN	Capture/Compare 4 generation See TIMx_EVTGEN.CC1GN description.
2	CC3GN	Capture/Compare 3 generation See TIMx_EVTGEN.CC1GN description.
1	CC2GN	Capture/Compare 2 generation See TIMx_EVTGEN.CC1GN description.
0	CC1GN	Capture/Compare 1 generation This bit can generate a capture/compare event when set by software. This bit is automatically cleared by hardware. **When the corresponding channel of CC1 is in output mode:** The TIMx_STS.CC1ITF flag will be pulled high, if the corresponding interrupt and DMA are enabled, the corresponding interrupt and DMA will be generated. **When the corresponding channel of CC1 is in input mode:** TIMx_CCDAT1 will capture the current counter value, and the TIMx_STS.CC1ITF flag will be pulled high, if the corresponding interrupt and DMA are enabled, the corresponding interrupt and DMA will be generated. If The IMx_STS.CC1ITF is already pulled high, pull TIMx_STS.CC1OCF high. 0: No action 1: Generated a CC1 capture/compare event

13.4.6 Slave Mode Control Register (TIMx_SMCTRL)

Offset address: 0x10

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															MSMD

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															rw
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EXTF[3:0]				EXTP	EXCEN	EXTPS[1:0]		Reserved	SMSEL[2:0]			Reserved	TSEL[2:0]		
rw				rw	rw	rw			rw				rw		

Bit Field	Name	Description
31:17	Reserved	Reserved, the reset value must be maintained
16	MSMD	Master/slave mode 0: No effect; 1: The event on the trigger input (TRGI) is delayed to allow perfect synchronization between the current timer (via TRGO) and its slave timers. This is very useful for cases where multiple timers need to be synchronized to a single external event.
15:12	EXTF[3:0]	External trigger filter These bits define the length of the ETRP digital filter (the RCC_TIMFILTCFG.TIM3FILTCLK[4:0] register determines the sampling frequency of the corresponding digital filter). The digital filter consists of an event counter which generates an output transition after recording N events: 0000：No filter, sampled using TIM's internal operating clock 0001：N=1 0010：N=2 0011：N=3 0100：N=4 0101：N=5 0110：N=6 0111：N=7 1xxx：N=8
11	EXTP	External trigger polarity This bit is used to select whether the trigger operation is to use tim_etr_in or the inversion of tim_etr_in. 0: tim_etr_in active at high level or rising edge. 1: tim_etr_in active at low level or falling edge.
10	EXCEN	External clock enable This bit is used to enable external clock mode 2, and the counter is driven by any active edge on the ETRF signal in this mode. 0: External clock mode 2 disable. 1: External clock mode 2 enable. *Note1: When external clock mode 1 and external clock mode 2 are enabled at the same time, the input of the external clock is ETRF.* *Note2: The following slave modes can be used simultaneously with external clock mode 2: reset mode, gated mode and trigger mode; However, TRGI cannot connect to ETRF (TIMx_SMCTRL.TSEL ≠ '111').*

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Bit Field	Name	Description
		Note3: Setting the TIMx_SMCTRL.EXCEN bit has the same effect as selecting external clock mode 1 and connecting TRGI to ETRF (TIMx_SMCTRL.SMSEL = 0111 and TIMx_SMCTRL.TSEL = 111).
9:8	EXTPS[1:0]	External trigger prescaler The frequency of the external trigger signal ETRP must be at most 1/4 of TIMxCLK frequency. When a faster external clock is input, a prescaler can be used to reduce the frequency of ETRP. 00: Prescaler disable 01: ETRP frequency divided by 2 10: ETRP frequency divided by 4 11: ETRP frequency divided by 8
7:4	SMSEL[2:0]	Slave mode selection When an external signal is selected, the active edge of the trigger signal (TRGI) is linked to the selected external input polarity (see input control register and control register description) 0000: Disable slave mode. If TIMx_CTRL1.CNTEN = 1, the prescaler is driven directly by the internal clock. 0001: Encoder mode 1. According to the level of TI2FP2, the counter up-counting or down-counting on the edge of TI1FP1。 0010: Encoder mode 2. According to the level of TI1FP1, the counter up-counting or down-counting on the edge of TI2FP2. 0011: Encoder mode 3. According to the input level of another signal, the counter up-counting or down-counting on the edges of TI2FP1 and TI2FP2 0100: Reset mode. On the rising edge of the selected trigger input (TRGI), the counter is reinitialized and the shadow register is updated 0101: Gated mode. When the trigger input (TRGI) is high, the clock of the counter is enabled. Once the trigger input becomes low, the counter stops counting, but is not reset. In this mode, the start and stop of the counter are controlled 0110: Trigger mode. When a rising edge occurs on the trigger input (TRGI), the counter is started but not reset. In this mode, only the start of the counter is controlled. 0111: External clock mode 1. The counter is clocked by the rising edge of the selected trigger input (TRGI). 1000~1101：Reserved. 1110: Combined Reset + Trigger Mode - The counter starts (and resets) on the rising edge of the trigger input TRGI, only the start of the counter is controlled. 1111：Reserved. *Note: Do not use gated mode if TI1F_ED is selected as the trigger input (TIMx_SMCTRL.TSEL=100). This is because TI1F_ED outputs a pulse for each TI1F transition, whereas gated mode checks the level of the triggered input.*
3	Reserved	Reserved, the reset value must be maintained
2:0	TSEL[2:0]	Trigger selection These 3 bits are used to select the trigger input of the synchronous counter. 000: Internal trigger 0 (ITR0) 100: Edge detector for TI1 (TI1F_ED) 001: Internal trigger 1 (ITR1) 101: Filtered timer input 1 (TI1FP1)

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Bit Field	Name	Description
		010: Internal trigger 2 (ITR2) 110: Filtered timer input 2 (TI2FP2) 011: Internal trigger 3 (ITR3) 111: External trigger input (ETRF) For further details regarding ITRx, see Table 14-5. *Note: These bits must be changed only when not in use (e. g. TIMx_SMCTRL.SMSEL=0000) to avoid false edge detection at the transition.* *Note: When enabling the external event (TRGI) trigger to load counter values, if output comparison mode is simultaneously employed, either ETRF or ITRx must be selected as the trigger source.*

Table 13-3 TIMx Internal Trigger Connection

Slave timer	ITR0 (TSEL = 000)	ITR1 (TSEL = 001)	ITR2 (TSEL = 010)	ITR3 (TSEL = 011)
TIM1	TIM3	NA	NA	NA
TIM3	TIM1	NA	NA	NA
TIM4	NA	NA	NA	NA

13.4.7 DMA/Interrupt Enable Registers (TIMx_DINTEN)

Offset address: 0x14

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved										TDEN	Reserved	UDEN	BIEN	TIEN	UIEN
										rw		rw		rw	rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved				CC4DEN	CC3DEN	CC2DEN	CC1DEN	Reserved				CC4IEN	CC3IEN	CC2IEN	CC1IEN
				rw	rw	rw	rw					rw	rw	rw	rw

Bit Field	Name	Description
31:22	Reserved	Reserved, the reset value must be maintained
21	TDEN	Trigger DMA request enable 0: Disable trigger DMA request. 1: Enable trigger DMA request
20	Reserved	Reserved, the reset value must be maintained
19	UDEN	Update DMA request enable 0: Disable update DMA request. 1: Enable update DMA request
18	BIEN	Break interrupt enable 0: Disable break interrupt 1: Enable break interrupt
17	TIEN	Trigger interrupt enable

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Bit Field	Name	Description
		0: Disable trigger interrupt 1: Enable trigger interrupt
16	UIEN	Update interrupt enable 0: Disable update interrupt 1: Enables update interrupt
15:12	Reserved	Reserved, the reset value must be maintained
11	CC4DEN	Capture/Compare 4 DMA request enable 0: Disable capture/compare 4 DMA request 1: Enable capture/compare 4 DMA request
10	CC3DEN	Capture/Compare 3 DMA request enable 0: Disable capture/compare 3 DMA request 1: Enable capture/compare 3 DMA request
9	CC2DEN	Capture/Compare 2 DMA request enable 0: Disable capture/compare 2 DMA request 1: Enable capture/compare 2 DMA request
8	CC1DEN	Capture/Compare 1 DMA request enable 0: Disable capture/compare 1 DMA request 1: Enable capture/compare 1 DMA request
7:4	Reserved	Reserved, the reset value must be maintained
3	CC4IEN	Capture/Compare 4 interrupt enable 0: Disable capture/compare 4 interrupt 1: Enable capture/compare 4 interrupt
2	CC3IEN	Capture/Compare 3 interrupt enable 0: Disable capture/compare 3 interrupt 1: Enable capture/compare 3 interrupts
1	CC2IEN	Capture/Compare 2 interrupt enable 0: Disable capture/compare 2 interrupt 1: Enables capture/compare 2 interrupts
0	CC1IEN	Capture/Compare 1 interrupt enable 0: Disable capture/compare 1 interrupt 1: Enables capture/comparing 1 interrupt

13.4.8 Capture/Compare Mode Register 1 (TIMx_CCMOD1)

Offset address: 0x18

Reset value: 0x0000 0000

Channels can be used for input (capture mode) or output (compare mode), and the direction of the channel is defined by the corresponding CCxSEL bit. The other bits of the register act differently in input and output modes. OCx describes the function of a channel in output mode, ICx describes the function of a channel in input mode. Hence, please note that the same bit can have different meanings for output mode and for input mode.

Output compare mode:

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

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Reserved

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OC2MD[2:0]			OC2CEN	OC2FEN	OC2PEN	CC2SEL[1:0]		OC1MD[2:0]			OC1CEN	OC1FEN	OC1PEN	CC1SEL[1:0]	
rw			rw	rw	rw	rw		rw			rw	rw	rw	rw	

Bit Field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained
15:13	OC2MD[2:0]	Output Compare 2 mode
12	OC2CEN	Output Compare 2 clear enable
11	OC2FEN	Output Compare 2 fast enable
10	OC2PEN	Output Compare 2 preload enable
9:8	CC2SEL[1:0]	Capture/Compare 2 selection These bits are used to select the input/output and input mapping of the channel 00: CC2 channel is configured as output. 01: CC2 channel is configured as input, IC2 is mapped on TI2 10: CC2 channel is configured as input, IC2 is mapped on TI1 11: CC2 channel is configured as input, IC2 is mapped on TRC. This mode is only active when the internal trigger input is selected by TIMx_SMCTRL.TSEL. *Note: CC2SEL is writable only when the channel is off (TIMx_CCEN.CC2EN = 0).*
7:5	OC1MD[2:0]	Output Compare 1 mode These bits are used to manage the output reference signal OC1REF, which determines the values of OC1 and OC1N, and is valid at high levels, while the active levels of OC1 and OC1N depend on the TIMx_CCEN.CC1P and TIMx_CCEN.CC1NP bits. 000: Frozen. Comparison between TIMx_CCDAT1 register and counter TIMx_CNT has no effect on OC1REF signal. 001: Set channel 1 to the active level on match. When TIMx_CCDAT1 = TIMx_CNT, OC1REF signal will be forced high. 010: Set channel 1 as inactive level on match. When TIMx_CCDAT1 = TIMx_CNT, OC1REF signal will be forced low. 011: Toggle. When TIMx_CCDAT1 = TIMx_CNT, OC1REF signal will be toggled. 100: Force to inactive level. OC1REF signal is forced low. 101: Force to active level. OC1REF signal is forced high. 110: PWM mode 1 - In up-counting mode, if TIMx_CNT < TIMx_CCDAT1, OC1REF signal of channel 1 is high, otherwise it is low. In down-counting mode, if TIMx_CNT > TIMx_CCDAT1, OC1REF signal of channel 1 is low, otherwise it is high. 111: PWM mode 2 - In up-counting mode, if TIMx_CNT < TIMx_CCDAT1, OC1REF signal of channel 1 is low, otherwise it is high. In down-counting mode, if TIMx_CNT > TIMx_CCDAT1, OC1REF signal of channel 1 is high, otherwise it is low. *Note 1: In PWM mode 1 or PWM mode 2, the OC1REF level changes only when the comparison result changes or when the output compare mode is switched from frozen mode to PWM mode.*
4	OC1CEN	Output Compare 1 clear enable

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Bit Field	Name	Description
		0: OC1REF is not affected by tim_ocref_clr_in input level. 1: OC1REF is cleared immediately when the tim_ocref_clr_in input level is detected as high (the source of tim_ocref_clr_in is controlled by TIMx_CTRL1.CLRSEL).
3	OC1FEN	Output Compare 1 fast enable This bit is used to speed up the response of the CC output to the trigger input event. 0: CC1 behaves normally depending on the counter and CCDAT1 values, even if the trigger is ON. The minimum delay for activating CC1 output when an edge occurs on the trigger input is 5 clock cycles 1: An active edge of the trigger input acts like a comparison match on CC1 output. Therefore, OC is set to the comparison level regardless of the comparison result. The delay time for sampling the trigger input and activating the CC1 output is reduced to 3 clock cycles. OCxFEN only works if the channel is configured in PWM1 or PWM2 mode.
2	OC1PEN	Output Compare 1 preload enable 0: Disable preload function of TIMx_CCDAT1 register. Supports write operations to TIMx_CCDAT1 register at any time, and the written value is effective immediately. 1: Enable preload function of TIMx_CCDAT1 register. Only read and write operations to preload registers. When an update event occurs, the value of TIMx_CCDAT1 is loaded into the active register. *Note 1: Only when TIMx_CTRL1.ONEPM = 1(In one-pulse mode), PWM mode can be used without verifying the preload register, otherwise no other behavior can be predicted.*
1:0	CC1SEL[1:0]	Capture/Compare 1 selection These bits are used to select the input/output and input mapping of the channel 00: CC1 channel is configured as output. 01: CC1 channel is configured as input, IC1 is mapped on TI1. 10: CC1 channel is configured as input, IC1 is mapped on TI2 11: CC1 channels are configured as inputs and IC1 is mapped to TRC. This mode is only active when the internal trigger input is selected by TIMx_SMCTRL.TSEL. *Note: CC1SEL is writable only when the channel is off (TIMx_CCEN.CC1EN = 0).*

Iutput capture mode:

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IC2F[3:0]				IC2PSC[1:0]		CC2SEL[1:0]		IC1F[3:0]				IC1PSC[1:0]		CC1SEL[1:0]	
rw				rw		rw		rw				rw		rw	

Bit Field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained
15:12	IC2F[3:0]	Input capture 2 filter
11:10	IC2PSC[1:0]	Input capture 2 prescaler

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Bit Field	Name	Description
9:8	CC2SEL[1:0]	Capture/Compare 2 selection These bits are used to select the input/output and input mapping of the channel: 00: CC2 channel is configured as output 01: CC2 channel is configured as input, IC2 is mapped on TI2 10: CC2 channel is configured as input, IC2 is mapped on TI1 11: CC2 channel is configured as input, IC2 is mapped on TRC. This mode is only active when the internal trigger input is selected by TIMx_SMCTRL.TSEL. *Note: CC2SEL is writable only when the channel is off (TIMx_CCEN.CC2EN = 0).*
7:4	IC1F[3:0]	Input capture 1 filter These bits define the length of the ETRP digital filter (the RCC_TIMFILTCFG.TIM3FILTCLK[4:0] register determines the sampling frequency of the corresponding digital filter). The digital filter consists of an event counter which generates an output transition after recording N events: 0000：No filter, sampled using TIM's internal operating clock 0001：N=1 0010：N=2 0011：N=3 0100：N=4 0101：N=5 0110：N=6 0111：N=7 1xxx：N=8
3:2	IC1PSC[1:0]	Input capture 1 prescaler These bits are used to select the ratio of the prescaler for IC1 (CC1 input). When TIMx_CCEN.CC1EN = 0, the prescaler will be reset. 00: No prescaler, capture is done each time an edge is detected on the capture input 01: Capture is done once every 2 events 10: Capture is done once every 4 events 11: Capture is done once every 8 events
1:0	CC1SEL[1:0]	Capture/Compare 1 Selection These bits are used to select the input/output and input mapping of the channel 00: CC1 channel is configured as output 01: CC1 channel is configured as input, IC1 is mapped on TI1 10: CC1 channel is configured as input, IC1 is mapped on TI2 11: CC1 channel is configured as input, IC1 is mapped to TRC. This mode is only active when the internal trigger input is selected by TIMx_SMCTRL.TSEL. *Note: CC1SEL is writable only when the channel is off (TIMx_CCEN.CC1EN = 0).*

13.4.9 Capture/Compare Mode Register 2 (TIMx_CCMOD2)

Offset address: 0x1C

Reset value: 0x0000 0000

See the description of the CCMOD1 register above

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Output comparison mode:

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Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OC4MD[2:0]			OC4CEN	OC4FEN	OC4PEN	CC4SEL[1:0]		OC3MD[2:0]			OC3CEN	OC3FEN	OC3PEN	CC3SEL[1:0]	
rw			rw	rw	rw	rw		rw			rw	rw	rw	rw	

Bit Field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained
15:13	OC4MD[2:0]	Output compare 4 mode
12	OC4CEN	Output compare 4 clear enable
11	OC4FEN	Output compare 4 fast enable
10	OC4PEN	Output compare 4 preload enable
9:8	CC4SEL[1:0]	Capture/Compare 4 selection These bits are used to select the input/output and input mapping of the channel 00: CC4 channel is configured as output 01: CC4 channel is configured as input, IC4 is mapped on TI4 10: CC4 channel is configured as input, IC4 is mapped on TI3 11: CC4 channel is configured as input, IC4 is mapped on TRC. This mode is only active when the internal trigger input is selected by TIMx_SMCTRL.TSEL. *Note: CC4SEL is writable only when the channel is off (TIMx_CCEN.CC4EN = 0).*
7:5	OC3MD[2:0]	Output compare 3 mode
4	OC3CEN	Output compare 3 clear enable
3	OC3FEN	Output compare 3 fast enable
2	OC3PEN	Output compare 3 preload enable
1:0	CC3SEL[1:0]	Capture/Compare 3 selection These bits are used to select the input/output and input mapping of the channel 00: CC3 channel is configured as output 01: CC3 channel is configured as input, IC3 is mapped to TI3 10: CC3 channel is configured as input, IC3 is mapped on TI4 11: CC3 channel is configured as input, IC3 is mapped to TRC. This mode is only active when the internal trigger input is selected by TIMx_SMCTRL.TSEL. *Note: CC3SEL is writable only when the channel is off (TIMx_CCEN.CC3EN = 0).*

Input capture mode:

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

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15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IC4F[3:0]				IC4PSC[1:0]		CC4SEL[1:0]		IC3F[3:0]				IC3PSC[1:0]		CC3SEL[1:0]	

Bit Field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained
15:12	IC4F[3:0]	Input capture 4 filter
11:10	IC4PSC[1:0]	Input capture 4 prescaler
9:8	CC4SEL[1:0]	Capture/Compare 4 selection These bits are used to select the input/output and input mapping of the channel 00: CC4 channel is configured as output 01: CC4 channel is configured as input, IC4 is mapped on TI4 10: CC4 channel is configured as input, IC4 is mapped on TI3 11: CC4 channel is configured as input, IC4 is mapped on TRC. This mode is only active when the internal trigger input is selected by TIMx_SMCTRL.TSEL. *Note: CC4SEL is writable only when the channel is off (TIMx_CCEN.CC4EN = 0).*
7:4	IC3F[3:0]	Input capture 3 filter
3:2	IC3PSC[1:0]	Input capture 3 prescaler
1:0	CC3SEL[1:0]	Capture/compare 3 selection These bits are used to select the input/output and input mapping of the channel 00: CC3 channel is configured as output 01: CC3 channel is configured as input, IC3 is mapped to TI3 10: CC3 channel is configured as input, IC3 is mapped on TI4 11: CC3 channel is configured as input, IC3 is mapped to TRC. This mode is only active when the internal trigger input is selected by TIMx_SMCTRL.TSEL. *Note: CC3SEL is writable only when the channel is off (TIMx_CCEN.CC3EN = 0).*

13.4.10 Capture/Compare Enable Registers (TIMx_CCEN)

Offset address: 0x24

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CC4P	CC4EN	Reserved		CC3P	CC3EN	Reserved		CC2P	CC2EN	Reserved		CC1P	CC1EN	Reserved	
rw	rw			rw	rw			rw	rw			rw	rw		

Bit Field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained.
15	CC4P	Capture/Compare 4 output polarity See TIMx_CCEN.CC1P description.
14	CC4EN	Capture/Compare 4 output enable

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Bit Field	Name	Description
		See TIMx_CCEN.CC1EN description.
13:12	Reserved	Reserved, the reset value must be maintained.
11	CC3P	Capture/Compare 3 output polarity See TIMx_CCEN.CC1P description.
10	CC3EN	Capture/Compare 3 output enabl） See TIMx_CCEN.CC1EN description.
9:8	Reserved	Reserved, the reset value must be maintained.
7	CC2P	Capture/Compare 2 output polarity See TIMx_CCEN.CC1P description.
6	CC2EN	Capture/Compare 2 output enable See TIMx_CCEN.CC1EN description.
5:4	Reserved	Reserved, the reset value must be maintained.
3	CC1P	Capture/Compare 1 output polarity **When the corresponding channel of CC1 is in output mode:** 0: OC1 active high 1: OC1 active low **When the corresponding channel of CC1 is in input mode:** At this time, this bit is used to select whether IC1 or the inverse signal of IC1 is used as the trigger or capture signal. 0: non-inverted: Capture action occurs when IC1 generates a rising edge. When used as external trigger, IC1 is non-inverted. 1: inverted: Capture action occurs when IC1 generates a falling edge. When used as external trigger, IC1 is inverted.
2	CC1EN	Capture/Compare 1 output enable **When the corresponding channel of CC1 is in output mode:** 0: Disable - Disable output OC1 signal. Therefore, the output level of OC1 depends on the values of MOEN, OSSI, OSSR, OI1, OI1N, and CC1NEN bits. 1: Enable - Enable output OC1 signal. The OC1 signal is output to the corresponding output pin, and its output level depends on the values of the MOEN, OSSI, OSSR, OI1, OI1N, and CC1NEN bits. **When the corresponding channel of CC1 is in input mode:** At this time, this bit is used to disable/enable the capture function. 0: Disable capture 1: Enable capture
1:0	Reserved	Reserved, the reset value must be maintained.

Table 13-4 Output Control Bits of Standard OCx Channel

CCxEN	OCx Output Status
0	Disable output (OCx=0)
1	OCx = OCxREF + polarity

Note: The state of external I/O pins connected to standard OCx channels depends on the OCx channel state and GPIO and AFIO registers.

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13.4.11 Capture/Compare Register 1 (TIMx_CCDAT1)

Offset address: 0x28

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CCDAT1[15:0]															
rw															

Bit Field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained.
15:0	CCDAT1[15:0]	Capture/Compare 1 value CC1 channel is configured as output: CCDAT1 contains the value to be compared to the counter TIMx_CNT, signaling on the OC1 output. If the preload feature is not selected in TIMx_CCMOD1.OC1PEN bit, the written value is immediately transferred to the active register. Otherwise, this preloaded value is transferred to the active register only when an update event occurs. CC1 channel is configured as input: CCDAT1 contains the counter value transferred by the last input capture 1 event (IC1). When configured as input mode, register CCDAT1 is only readable. When configured as output mode, register CCDAT1 is readable and writable.

13.4.12 Capture/Compare Register 2 (TIMx_CCDAT2)

Offset address: 0x2C

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CCDAT2[15:0]															
rw															

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Bit Field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained.
15:0	CCDAT2[15:0]	Capture/Compare 2 value CC2 channel is configured as output: CCDAT2 contains the value to be compared to the counter TIMx_CNT, signaling on the OC2 output. If the preload feature is not selected in TIMx_CCMOD1.OC2PEN bit, the written value is immediately transferred to the active register. Otherwise, this preloaded value is transferred to the active register only when an update event occurs. CC2 channel is configured as input: CCDAT2 contains the counter value transferred by the last input capture 2 event (IC2). When configured as input mode, register CCDAT2 is only readable. When configured as output mode, register CCDAT2 is readable and writable.

13.4.13 Capture/Compare Register 3 (TIMx_CCDAT3)

Offset address: 0x30

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CCDAT3[15:0]															
rw															

Bit Field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained.
15:0	CCDAT3[15:0]	Capture/Compare 3 value CC3 channel is configured as output: CCDAT3 contains the value to be compared to the counter TIMx_CNT, signaling on the OC3 output. If the preload feature is not selected in TIMx_CCMOD2.OC3PEN bit, the written value is immediately transferred to the active register. Otherwise, this preloaded value is transferred to the active register only when an update event occurs. CC3 channel is configured as input: CCDAT3 contains the counter value transferred by the last input capture 3 event (IC3). When configured as input mode, register CCDAT3 is only readable. When configured as output mode, register CCDAT3 is readable and writable.

13.4.14 Capture/Compare Register 4 (TIMx_CCDAT4)

Offset address: 0x34

Reset value: 0x0000 0000

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CCDAT4[15:0]															
rw															

Bit Field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained.
15:0	CCDAT4[15:0]	Capture/Compare 4 value CC4 channel is configured as output: CCDAT4 contains the value to be compared to the counter TIMx_CNT, signaling on the OC4 output. If the preload feature is not selected in TIMx_CCMOD2.OC4PEN bit, the written value is immediately transferred to the active register. Otherwise, this preloaded value is transferred to the active register only when an update event occurs. CC4 channel is configured as input: CCDAT4 contains the counter value transferred by the last input capture 4 event (IC4). When configured as input mode, register CCDAT4 is only readable. When configured as output mode, register CCDAT4 is readable and writable.

13.4.15 Prescaler (TIMx_PSC)

Offset address: 0x40

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PSC[15:0]															
rw															

Bit Field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained.
15:0	PSC[15:0]	Prescaler value Counter clock $f_{CK\_CNT} = f_{CK\_PSC}/$ (PSC [15:0] +1). Each time an update event occurs, the PSC value is loaded into the active prescaler register.

13.4.16 Auto-reload Register (TIMx_AR)

Offset address: 0x44

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Reset value: 0x0000 FFFF

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
AR[15:0]															
rw															

Bit Field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained.
15:0	AR[15:0]	Auto-reload value These bits define the value that will be loaded into the actual auto-reload register. See Section 14.4.1 for more details. When the TIMx_AR.AR [15:0] value is null, the counter does not work.

13.4.17 Counters (TIMx_CNT)

Offset address: 0x48

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CNT[15:0]															
rw															

Bit Field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained.
15:0	CNT[15:0]	Counter value

13.4.18 Break and Dead-time Registers (TIMx_BKDT)

Offset address: 0x50

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LCKCFG[1:0]		Reserved		BKEN	BKP	AOEN	MOEN	Reserved							
rw		rw	rw	rw	rw	rw	rw	rw							

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Note: AOEN、BKP、BKEN、OSSI、OSSR and DTGN[7:0] bits can all be write protected depending on the LOCK configuration, and it is necessary to configure all of them on the first write to the TIMx_BKDT register.

Bit Field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained
15:14	LCKCFG[1:0]	Lock configuration. This bit provides write protection to prevent software errors. These bits offer a write protection against software errors. 00: – No write protected. 01: – LOCK Level 1 TIMx_BKDT.DTGN、TIMx_BKDT.BKEN、TIMx_BKDT.BKP、TIMx_BKDT.AOEN、TIMx_CTRL2.OIx、TIMx_CTRL2.OIxN、TIMx_AF1 bits enable write protection. 10: – LOCK Level 2 Except for register write protection in LOCK Level 1 mode, TIMx_CCEN.CCxP and TIMx_CCEN.CCxNP (If the corresponding channel is configured in output mode), TIMx_BKDT.OSSR and TIMx_BKDT.OSSI bits also enable write protection 11: – LOCK Level 3 Except for register write protection in LOCK Level 2, TIMx_CCMODx.OCxMD and TIMx_CCMODx.OCxPEN bits (If the corresponding channel is configured in output mode) also enable write protection. *Note: After the system reset, the LCKCFG bit can only be written once. Once written to the TIMx_BKDT register, LCKCFG will be protected until the next reset.*
13:12	Reserved	Reserved, the reset value must be maintained
11	BKEN	Break1 enable 0: Disable break input 1: Enable break input *Note: Any write to this bit requires an APB clock delay to take effect.*
10	BKP	Break polarity 0: Low level of the break input is valid 1: High level of the break input is valid *Note: Any write to this bit requires an APB clock delay to take effect.*
9	AOEN	Automatic output enable 0: Only software can set TIMx_BKDT.MOEN; 1: Software sets TIMx_BKDT.MOEN; or if the break input is not active, when the next update event occurs, hardware automatically sets TIMx_BKDT.MOEN.
8	MOEN	Main output enable This bit can be set by software or hardware depending on the TIMx_BKDT.AOEN bit, and is asynchronously cleared to '0' by hardware once the break input is active. It is only effective for channels 3 and 4 configured as outputs; it is ineffective for channels 1 and 2. 0: OC and OCN outputs are disabled or forced to idle state. 1: OC and OCN outputs are enabled if TIMx_CCEN.CCxEN or TIMx_CCEN.CCxNEN bits are set.For more details, see Section 12.4.11 Capture/Compare enable registers (TIMx_CCEN).

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Bit Field	Name	Description
7:0	Reserved	Reserved, the reset value must be maintained

13.4.19 Break Filter Register（TIMx_BKFR）

Offset address: 0x60

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved		THRESH						Reserved	WSIZE						FILTEN
		rw							rw						rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved															

Bit field	Name	Description
31:30	Reserved	Reserved, the reset value must be maintained
29:24	THRESH[5:0]	Threshold number of sample logic level to be valid, maximum 63: Threshold value for a valid logic level. Within sample window if number of logic high is more than or equal to threshold value, next logic level will be logic high. Same rule applies to logic low. If both number of 1's and 0's inside window are smaller than threshold, filter output stays unchanged. Threshold value should set to more than or equal to half of window value. Recommend threshold range is: **Minimum**: 1 pre-scale clock cycle more than ceiling value of max glitch size (in pre-scale clock cycle) and need to larger than half of window size. for example, if glitch size is 3.2*(pre-scale clock period), threshold should be $\lceil 3.2 \rceil$ = 4 + 1 =5 **Maximum**: floor value of minimum size of valid signal (in pre-scale clock cycle) and need to be smaller than window size. For example, if minimum message size is 3.2*(pre-scale clock period), threshold should be floor (3.2) = 3.
23	Reserved	Reserved, the reset value must be maintained
22:17	WSIZE[5:0]	Window size value for logic level check, maximum 63: Window size decides how many sampled values will take into consideration for getting next logic level. Build-in FIFO is 64 bits with maximum index 63 which can only set window size to be 63.
16	FILTEN	Filter enable 0: Disable filter 1: Enable filter
15:0	Reserved	Reserved, the reset value must be maintained

13.4.20 Alternate Function Option Register 1（TIMx_AF1）

Offset address: 0x7C

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Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved										IOM4 B.RKP	IOM3 BRKP	IOM2 BRKP	IOM4 BRKEN	IOM3 BRKEN	IOM2 BRKEN

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved					COMP1 BRKP	IOM BRKP	Reserved							COMP1 BRKEN	IOM BRKEN
		rw	rw	rw	rw	rw		rw	rw	rw	rw	rw	rw	rw	rw

Bit Field	Name	Description
31:22	Reserved	Reserved, the reset value must be maintained
21	IOM4BRKP	TIMx_BKIN IO4 input polarity 0：TIMx_BKIN IO4 input polarity is not inverted (active low if BKP = 0, active high if BKP = 1) 1：TIMx_BKIN IO4 input polarity is inverted (active high if BKP = 0, active low if BKP = 1)
20	IOM3BRKP	TIMx_BKIN IO3 input polarity 0：TIMx_BKIN IO3 input polarity is not inverted (active low if BKP = 0, active high if BKP = 1) 1：TIMx_BKIN IO3 input polarity is inverted (active high if BKP = 0, active low if BKP = 1)
19	IOM2BRKP	TIMx_BKIN IO2 input polarity 0：TIMx_BKIN IO2 input polarity is not inverted (active low if BKP = 0, active high if BKP = 1) 1：TIMx_BKIN IO2 input polarity is inverted (active high if BKP = 0, active low if BKP = 1)
18	IOM4BRKEN	TIMx_BKIN IO4 input enable 0：TIMx_BKIN IO4 input disabled 1：TIMx_BKIN IO4 input enabled
17	IOM3BRKEN	TIMx_BKIN IO3 input enable 0：TIMx_BKIN IO3 input disabled 1：TIMx_BKIN IO3 input enabled
16	IOM2BRKEN	TIMx_BKIN IO2 input enable 0：TIMx_BKIN IO2 input disabled 1：TIMx_BKIN IO2 input enabled
15:11	Reserved	Reserved, the reset value must be maintained
10	COMP1BRKP	tim_brk_comp1 input polarity 0：tim_brk_comp1 input polarity is not inverted (active low if BKP = 0, active high if BKP = 1) 1：tim_brk_comp1 input polarity is inverted (active high if BKP = 0, active low if BKP = 1)
9	IOMBRKP	TIMx_BKIN input polarity 0：TIMx_BKIN input polarity is not inverted (active low if BKP = 0, active high if BKP = 1) 1：TIMx_BKIN input polarity is inverted (active high if BKP = 0, active low if BKP = 1)
8:2	Reserved	Reserved, the reset value must be maintained
1	COMP1BRKEN	tim_brk_comp1 input enable 0：tim_brk_comp1 input disabled

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		1：tim_brk_comp1 input enabled
0	IOMBRKEN	TIMx_BKIN IO1 input enable 0：TIMx_BKIN IO1 input disabled 1：TIMx_BKIN IO1 input enabled

13.4.21 External Event Counter Load Value Register（TIMx_ENCLVR）

Offset address: 0x90

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserve															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LVR[15:0]															
rw															

Bit Field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained
15:0	LVR[15:0]	An external event (TI3) triggers the counter load value. Upon detection of a valid TI3 event (selectable as active-high, active-low, rising edge, or falling edge, depending on the TIMx_ENCMCTRL.C3LDCNTSEL[1:0] register), the counter shall be loaded with the LVR value.

13.4.22 DMA Control Register (TIMx_DCTRL)

Offset address: 0x94

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved		DBADDR[5:0]						Reserved		DBLEN[5:0]					
		rw								rw					

Bit Field	Name	Description
31:14	Reserved	Reserved, the reset value must be maintained

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Bit Field	Name	Description
13:8	DBADDR[5:0]	DMA base address This bit field defines the first address where the DMA accesses the TIMx_DADDR register. When access is done through the TIMx_DADDR first time, this bit-field specifies the address you just access. And then the second access to the TIMx_DADDR, you will access the address of "DMA Base Address + 4" 000000：TIMx_CTRL1, 000001：TIMx_CTRL2, 000010：TIMx_SMCTRL, ... 100101：TIMx_DCTRL
7:6	Reserved	Reserved, the reset value must be maintained
5:0	DBLEN[5:0]	DMA burst length This bit field defines the number DMA will accesses (write/read) TIMx_DADDR register. 000000: 1 time transfer 000001: 2 time transfer 000010: 3 time transfer … 010001: 18 time transfer 100010: 35 time transfer

13.4.23 DMA Transfer For Full Transfer Register (TIMx_DADDR)

Offset address: 0x98

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
BURST[31:16]															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BURST[15:0]															
rw															

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Bit Field	Name	Description
31:0	BURST[31:0]	DMA Access Buffer When a read or write operation is assigned to this register, the register located at the address range (DMA base address + DMA burst length ×4) will be accessed. DMA base address = The address of TIM_CTRL1 + TIMx_DCTRL. DBADDR * 4； DMA burst len = TIMx_DCTRL.DBLEN + 1. Example: If TIMx_DCTRL.DBLEN = 0x3(4 transfers), TIMx_DCTRL.DBADDR = 0xD (TIMx_CCDAT1), DMA data length = half word, DMA memory address = buffer address in SRAM, DMA peripheral address = TIMx_DADDR address. When an event occurs, TIMx will send requests to the DMA, and transfer data 4 times. For the first time, DMA access to the TIMx_ DADDR register will be mapped to access TIMx_CCDAT1 register; For the second time, DMA access to the TIMx_ DADDR register will be mapped to access TIMx_CCDAT2 register; … … For the fourth time, DMA access to the TIMx_ DADDR register will be mapped to access TIMx_CCDAT4 register;

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14 General-purpose Timer (TIM4)

14.1 General-purpose Timer Introduction

The general-purpose timer (TIM4) is mainly used in the following scenarios: counting the input signal, measuring the pulse width of the input signal and generating the output waveform, etc.

14.2 Main Features of General-purpose Timer

- 16-bit auto-reload counters. (It can realize up-counting, down-counting, up/down counting)
- 16-bit programmable prescaler. (The prescaler factor can be configured with any value between 1 and 65536)
- TIM4 up to 3 channels
- Channel's working modes: PWM output, ouput compare, one-pulse mode output, input capture
- The events that generate the interrupt/DMA are as follows:
  - Update event
  - Trigger event
  - Input capture
  - Output compare
- Timer can be controlled by external signal
- Timers can be linked together internally for timer synchronization or chaining
- Incremental (quadrature) encoder interface: Pulse + symbol used for tracking motion and resolving rotation direction and position
- Hall sensor interface: used to do three-phase motor control
- Supports capture of internal comparator output signal.

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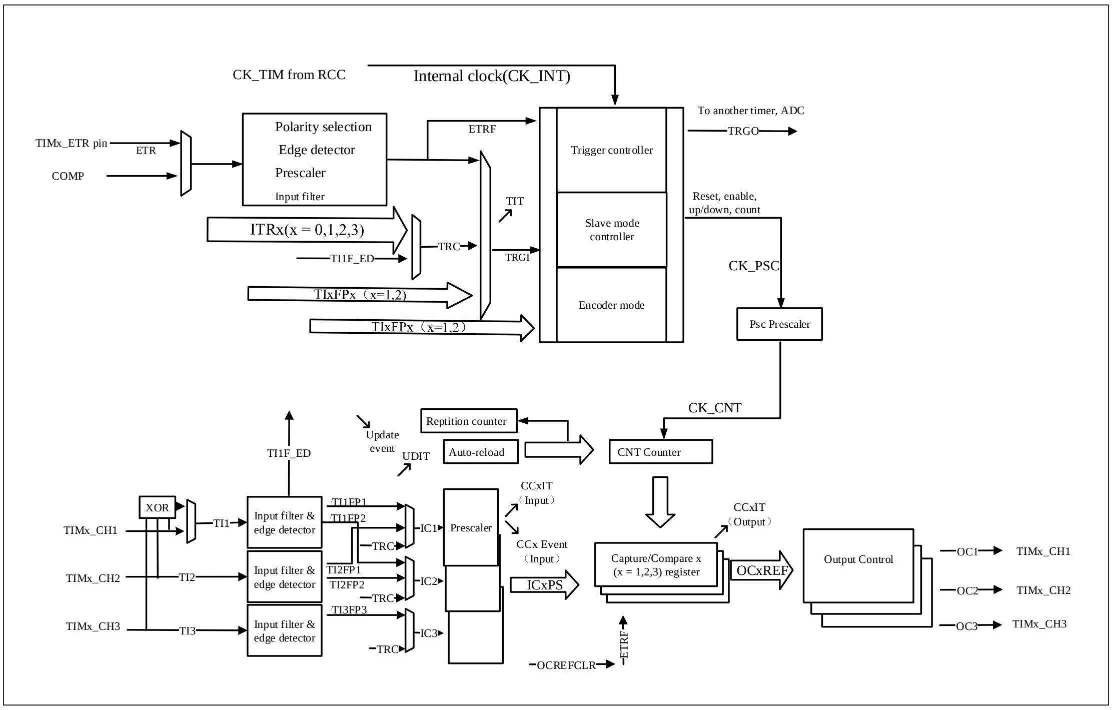
Figure 14-1 Block Diagram of TIM4



↘ *The event* ↗ *Interrupt and DMA output*

The input for capture channel 1 may originate from the IOM or comparator output.

14.3 General-purpose Timer3 Description

14.3.1 Time-base Unit

The time-base unit mainly includes: prescaler, counter and auto-reload. When the time base unit is working, the software can read and write the corresponding registers (TIMx_PSC, TIMx_CNT and TIMx_AR) at any time.

Depending on the setting of the auto-reload preload enable bit (TIMx_CTRL1.ARPEN), the value of the preload register is transferred to the shadow register immediately or at each update event UEV. An update event is generated when the counter reaches the overflow/underflow condition and it can be generated by software when TIMx_CTRL1.UPDIS=0. The counter CK_CNT is valid only when the TIMx_CTRL1.CNTEN bit is set. The counter starts counting one clock cycle after the TIMx_CTRL1.CNTEN bit is set.

14.3.1.1 **Prescaler description**

The TIMx_PSC register consists of a 16-bit counter that can be used to divide the counter clock frequency by any factor between 1 and 65536. It can be changed on the fly as it is buffered. The prescaler value is only taken into account at the next update event.

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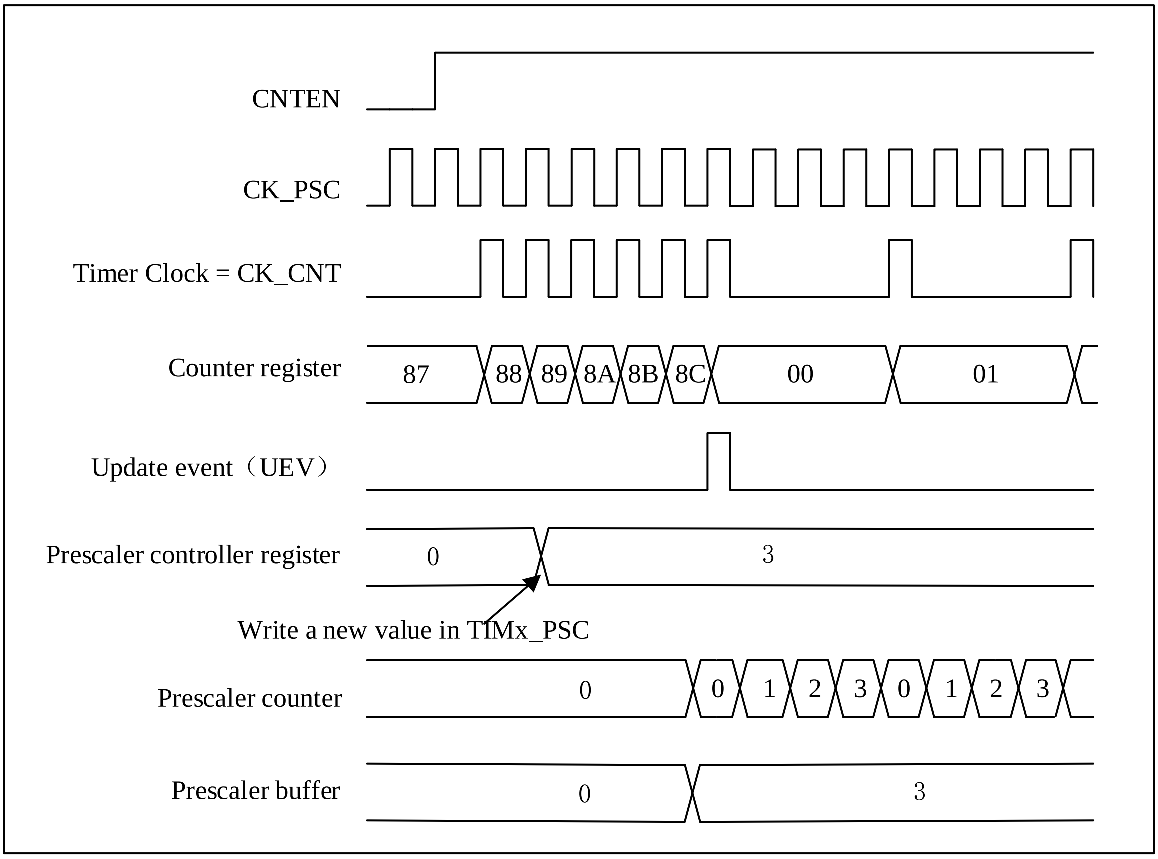
Figure 14-2 Counter Timing Diagram with Prescaler Division Change from 1 to 4



14.3.2 Counter Mode

14.3.2.1 Up-counting mode

In up-counting mode, the counter will count from 0 to the value of the register TIMx_AR, then it resets to 0. And a counter overflow event is generated.

If the TIMx_CTRL1.UPRS bit (select update request) and the TIMx_EVTGEN.UDGN bit are set, an update event (UEV) will generate And TIMx_STS.UDITF will not be set by hardware, therefore, no update interrupts or update DMA requests are generated. This setting is used in scenarios where you want to clear the counter but do not want to generate an update interrupt.

Depending on the update request source is configured in the TIMx_CTRL1.UPRS. When an update event occurs, TIMx_STS.UDITF is set, all registers are updated:

- Update auto-reload shadow registers with preload value (TIMx_AR), when TIMx_CTRL1.ARPEN = 1.
- The prescaler shadow register is reloaded with the preload value (TIMx_PSC).

To avoid updating the shadow registers when new values are written to the preload registers, you can disable the update by setting TIMx_CTRL1.UPDIS=1.

When an update event occurs, the counter will still be cleared and the prescaler counter will also be set to 0 (but the prescaler value will remain unchanged).

The figure below shows some examples of the counter behavior and the update flags for different division factors in

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the up-counting mode.

Figure 14-3 Timing Diagram of Up-counting, The Internal Clock Divider Factor = 2/N

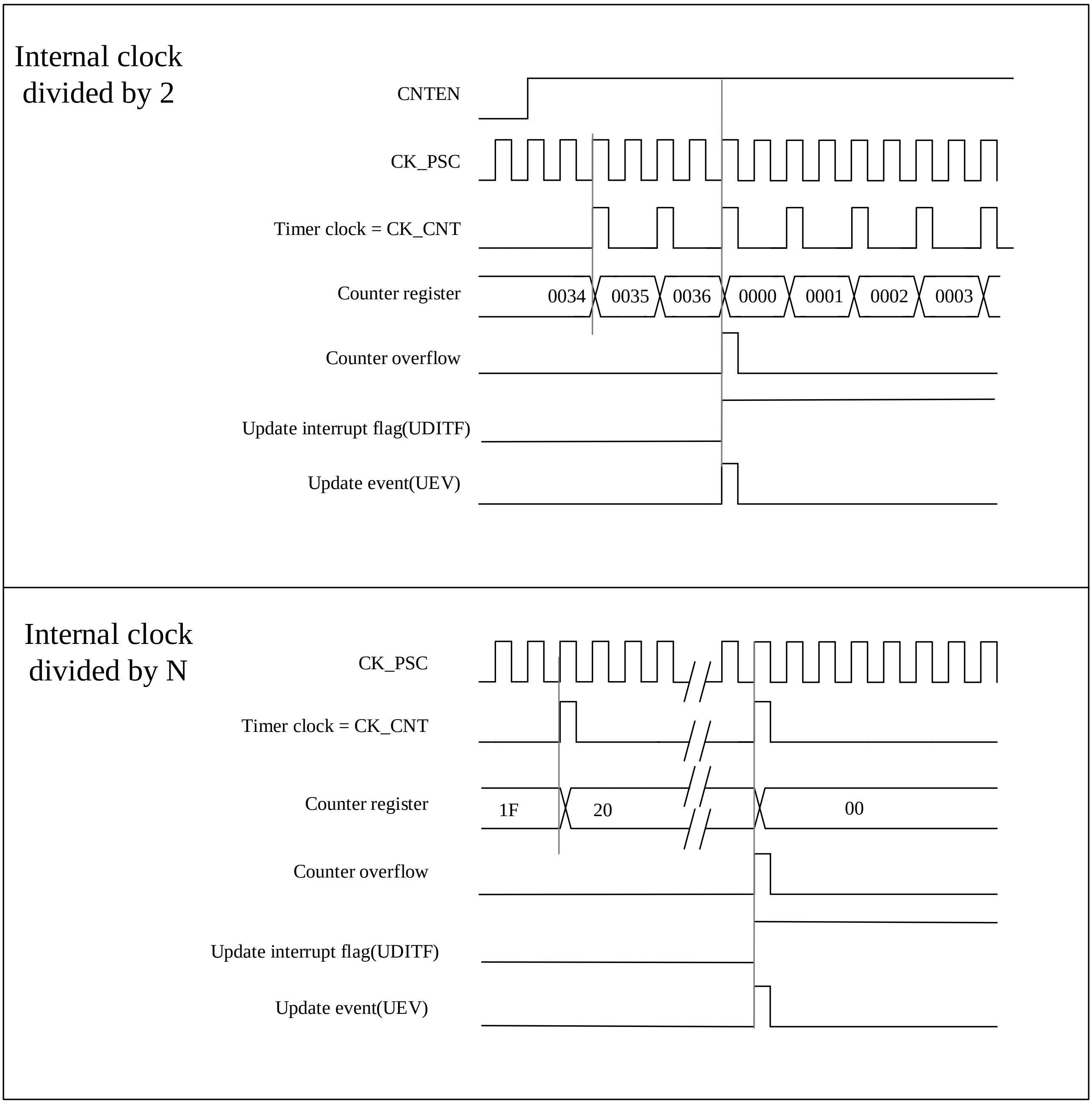

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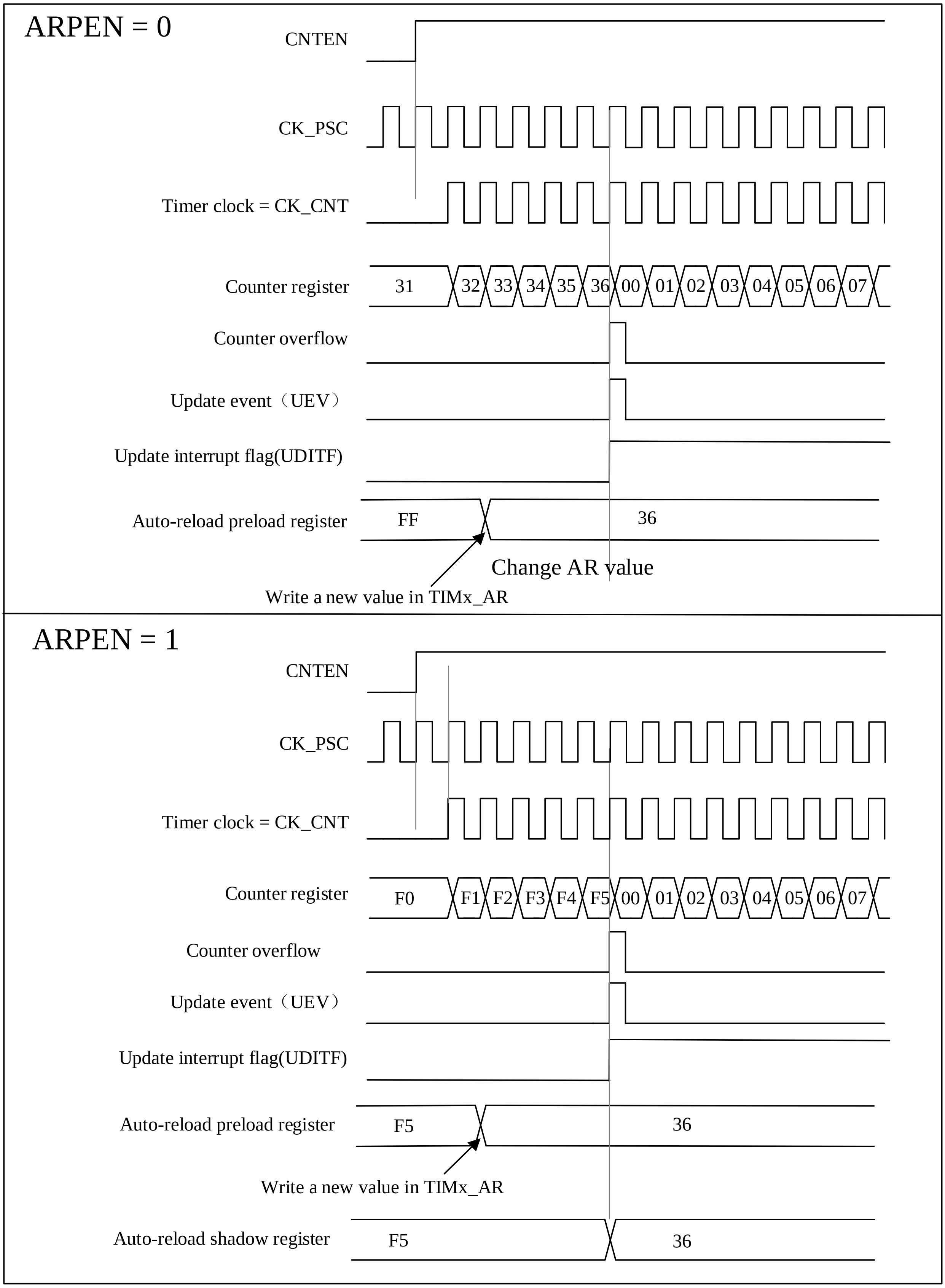
Figure 14-4 Timing Diagram of The Up-counting, Update Event When ARPEN = 0/1



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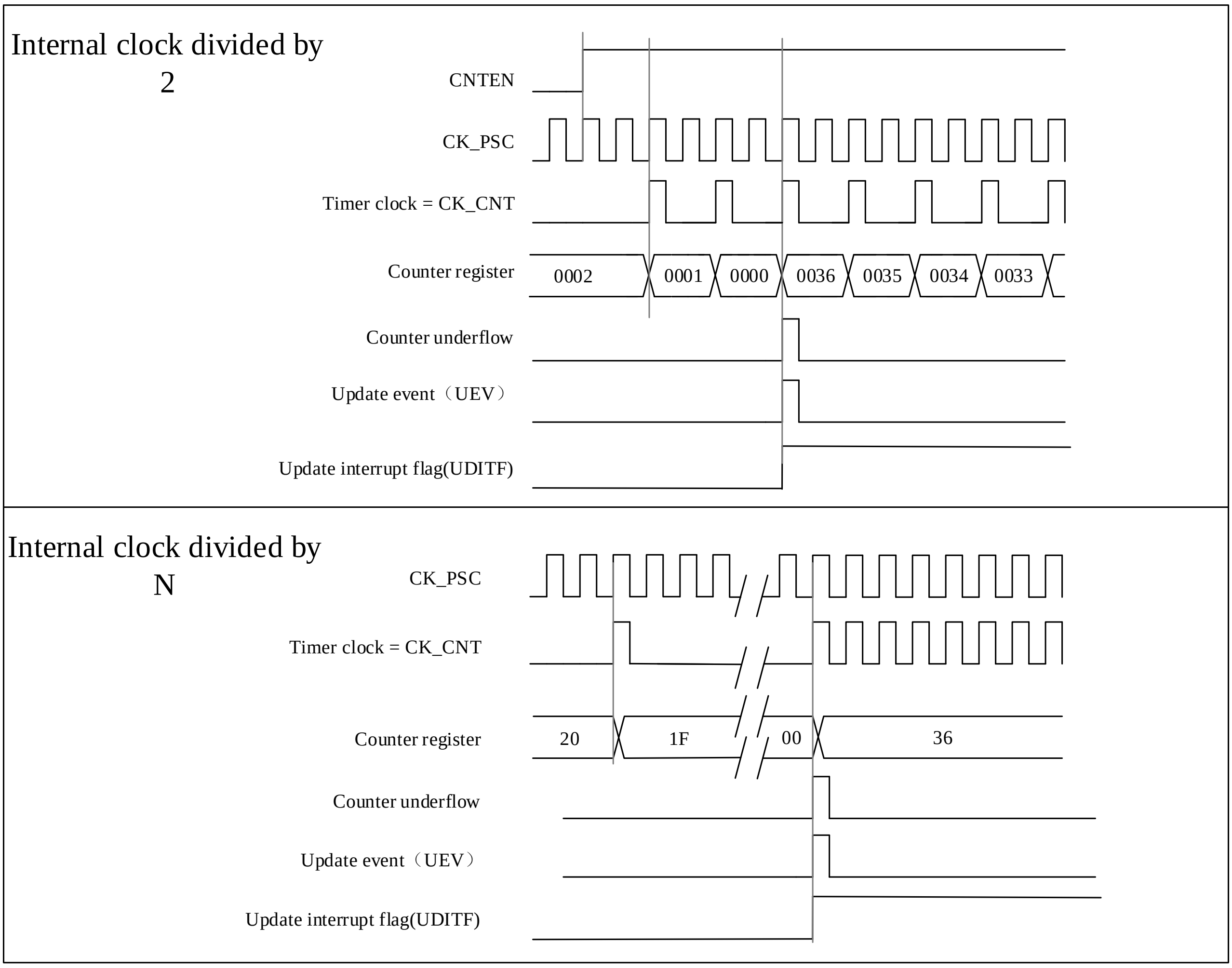
14.3.2.2 Down-counting mode

In down-counting mode, the counter will decrement from the value of the register TIMx_AR to 0, then restart from the auto-reload value and generate a counter underflow event.

The process of configuring update events and updating registers in down-counting mode is the same as in up-counting mode, see Section 14.3.2.1.

The figure below shows some examples of the counter behavior and the update flags for different division factors in the down-counting mode.

Figure 14-5 Timing Diagram of the Down-counting, Internal Clock Divided Factor = 2/N



14.3.2.3 Center-aligned mode

In center-aligned mode, the counter increments from 0 to the value (TIMx_AR) – 1, a counter overflow event is generated. It then counts down from the auto-reload value (TIMx_AR) to 1 and generates a counter underflow event. Then the counter resets to 0 and starts counting up again.

In this mode, the TIMx_CTRL1.DIR direction bits have no effect and the count direction is updated and specified by hardware. Center-aligned mode is valid when the TIMx_CTRL1. CAMSEL bit is not equal to "00".

The update events can be generated each time the counter overflows and each time the counter underflows. Alternatively, an update event can also be generated by setting the TIMx_EVTGEN. UDGN bit (either by software

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or using a slave mode controller). In this case, the counter restarts from 0, as does the prescaler's counter.

Note: if the update source is a counter overflow, auto-reload update before reloading the counter.

Figure 14-6 Timing Diagram of the Center-aligned, Internal Clock Divided Factor = 2/N

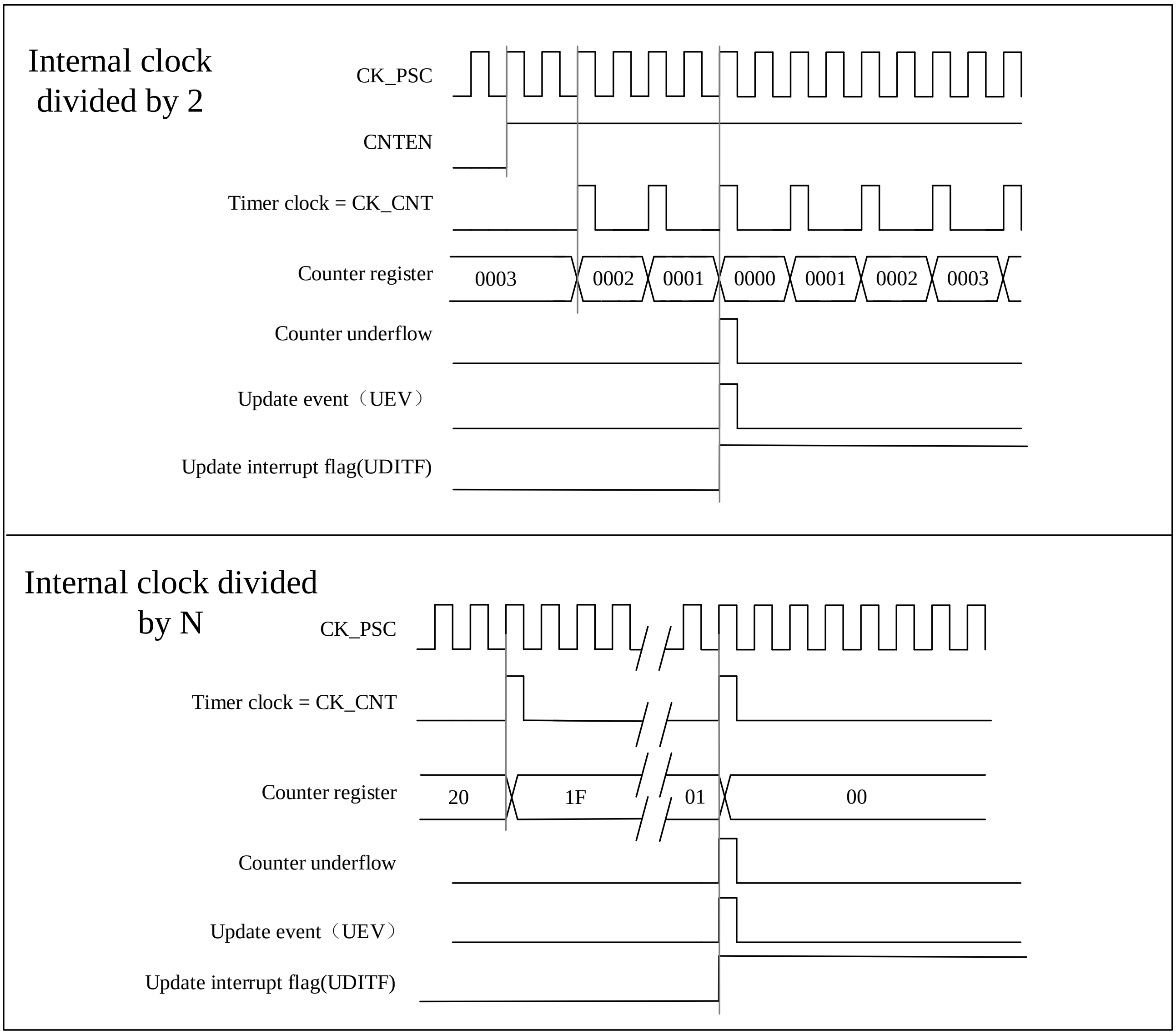

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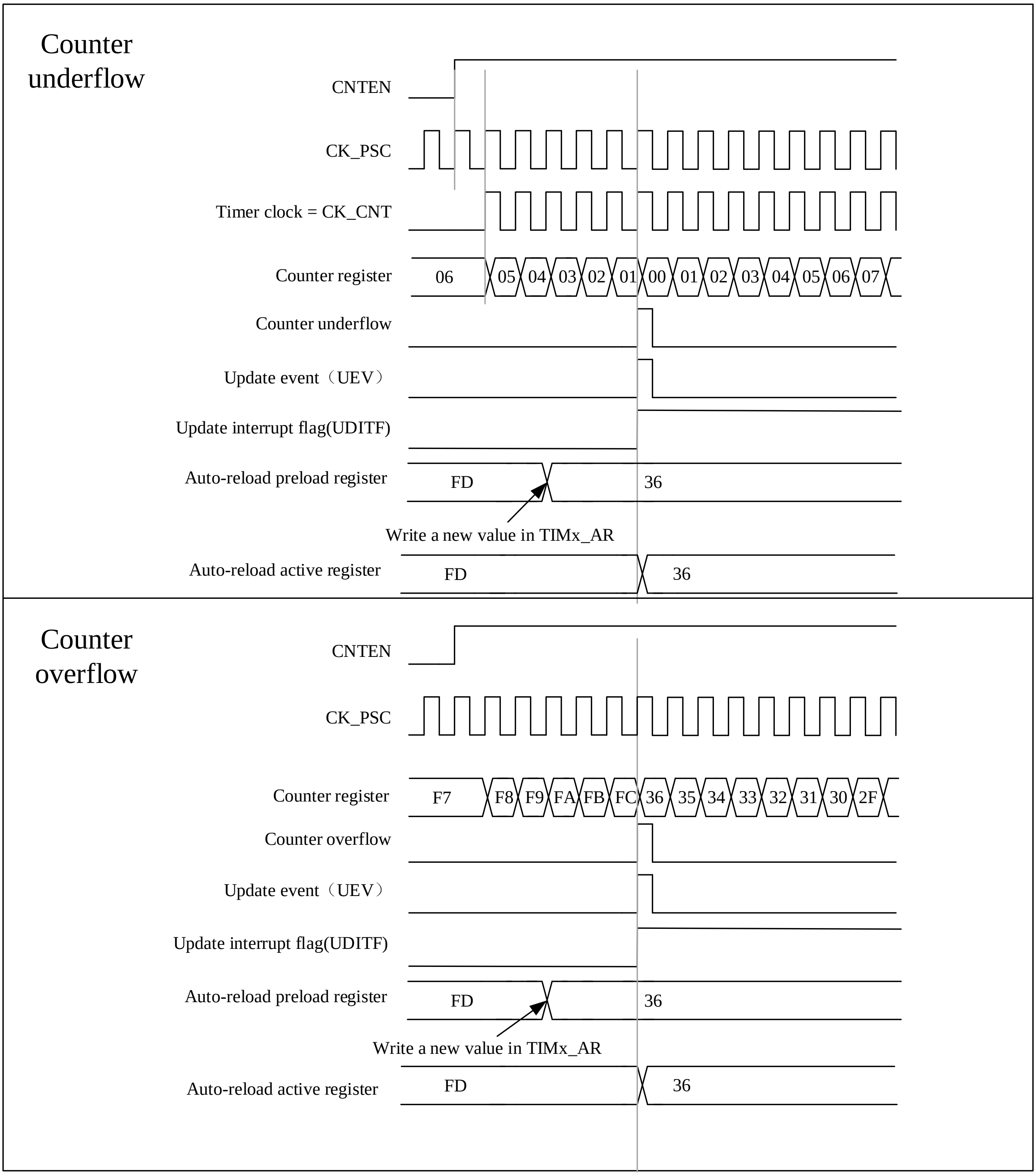
Figure 14-7 A Center-aligned Sequence Diagram That Includes Counter Overflows and Underflows (ARPEN = 1)



14.3.3 Clock Selection

- The internal clock of timers：CK_INT
- Two kinds of external clock mode:
  - External input pin

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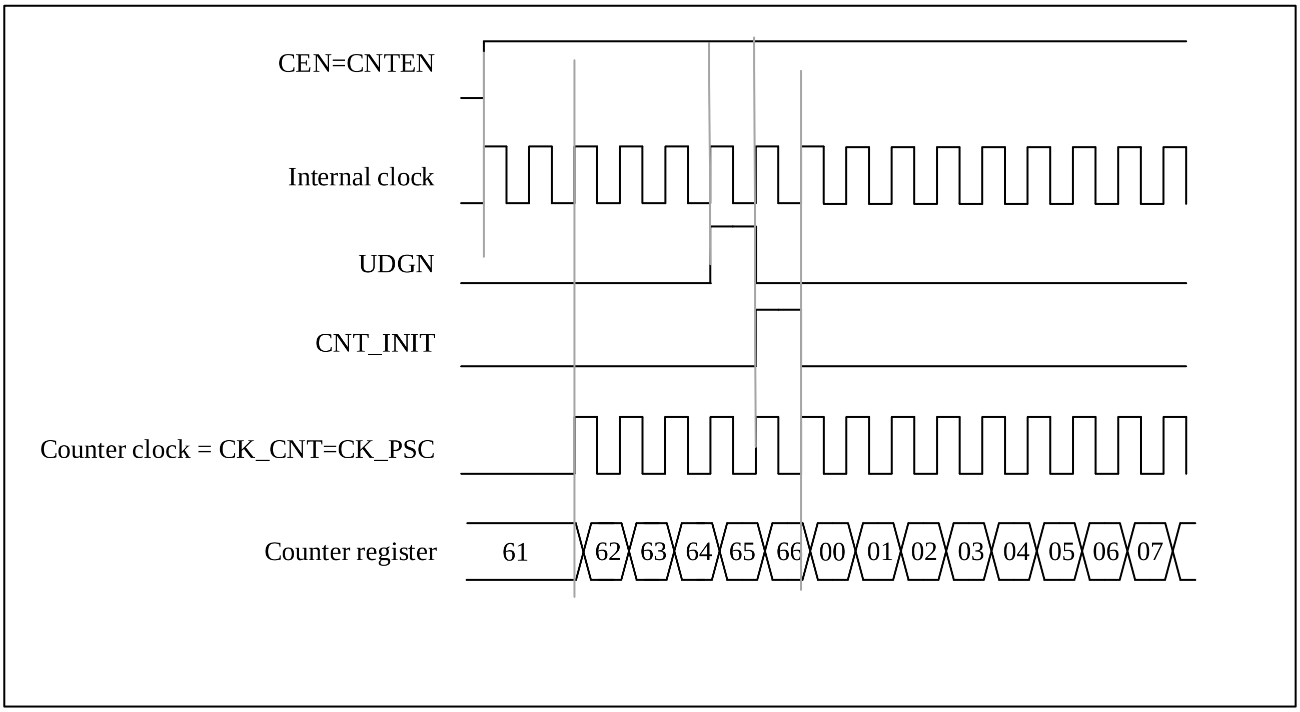
– External trigger input ETR

- Internal trigger input (ITRx) : one timer is used as a prescaler for another timer

14.3.3.1 Internal clock source (CK_INT)

When the TIMx_SMCTRL.SMSEL is equal to “0000”, the slave mode controller is disabled. The three control bits (TIMx_CTRL1.CNTEN、TIMx_CTRL1. DIR、TIMx_EVTGEN. UDGN) can only be changed by software (except TIMx_EVTGEN. UDGN, which remains cleared automatically). It is provided that the TIMx_CTRL1.CNTEN bit is written as' 1 ' by software, the clock source of the prescaler is provided by the internal clock CK_INT.

Figure 14-8 Control Circuit in Normal Mode, Internal Clock Divided by 1



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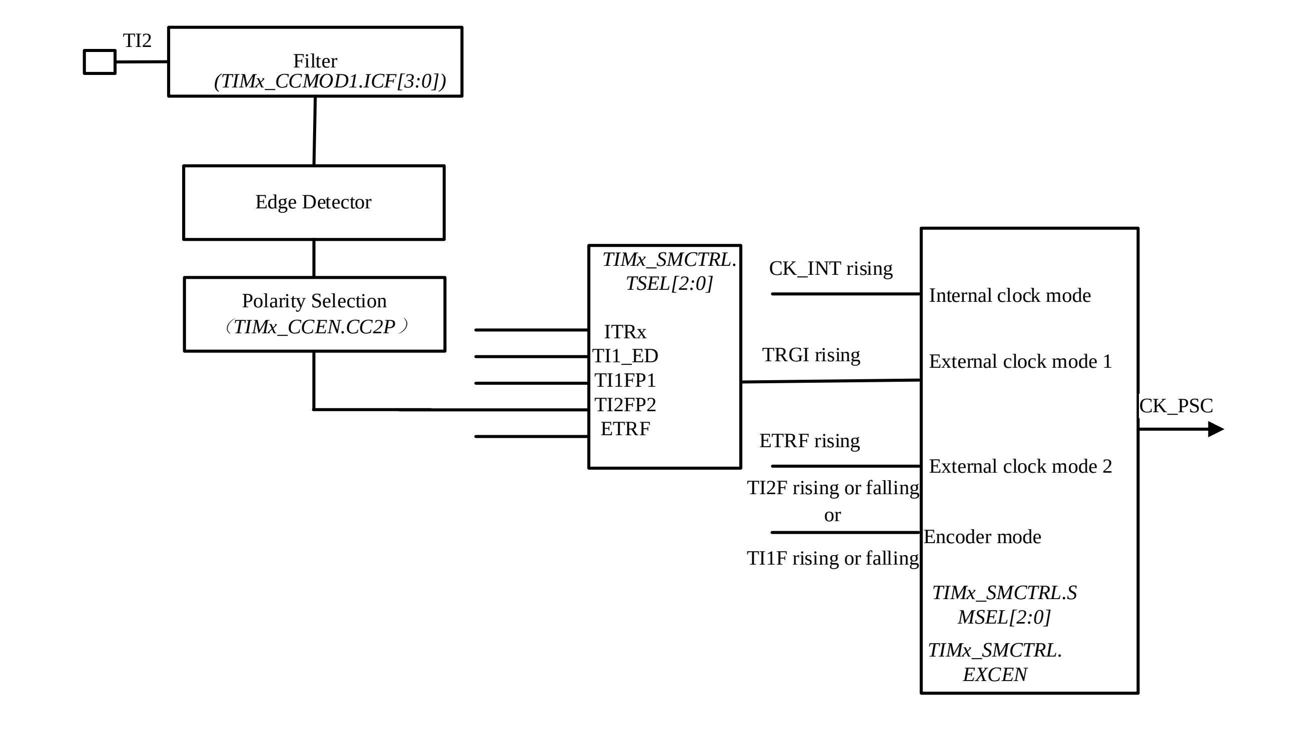
14.3.3.2 External clock source mode 1

Figure 14-9 TI2 External Clock Connection Example



This mode is selected by configuring TIMx_SMCTRL.SMSEL=0111. The counter can be configured to count on the rising or falling edge of the clock at the selected input.

For example, to configure up-counting mode to count on the rising edge of the clock at the T12 input, the configuration steps are as follows:

- Configure TIMx_CCMOD1.CC2SEL equal to ‘01’, CC2 channel is configured as input, IC2 is mapped to TI2
- Configure TIMx_CCEN.CC2P equal to ‘0’, select clock rising edge polarity
- To select input filter bandwidth by configuring TIMx_CCMOD1.IC2F[3:0] (if filter is not needed, keep IC2F bit at ‘0000’)
- Configure TIMx_SMCTRL.SMSEL equal to ‘0111’, select timer external clock mode 1
- Configure TIMx_SMCTRL.TSEL equal to ‘110’, select TI2 as the trigger input source
- Configure TIMx_CTRL1.CNTEN equal to ‘1’ to start the counter

Note：The capture prescaler is not used for triggering, so it does not need to be configured

When the rising edge of the timer clock occurs at TI2=1, the counter counts once and the TIMx_STS .TITF flag is pulled high.

The delay between the rising edge of TI2 and the actual clock of the counter depends on the resynchronization circuit at the input of TI2.

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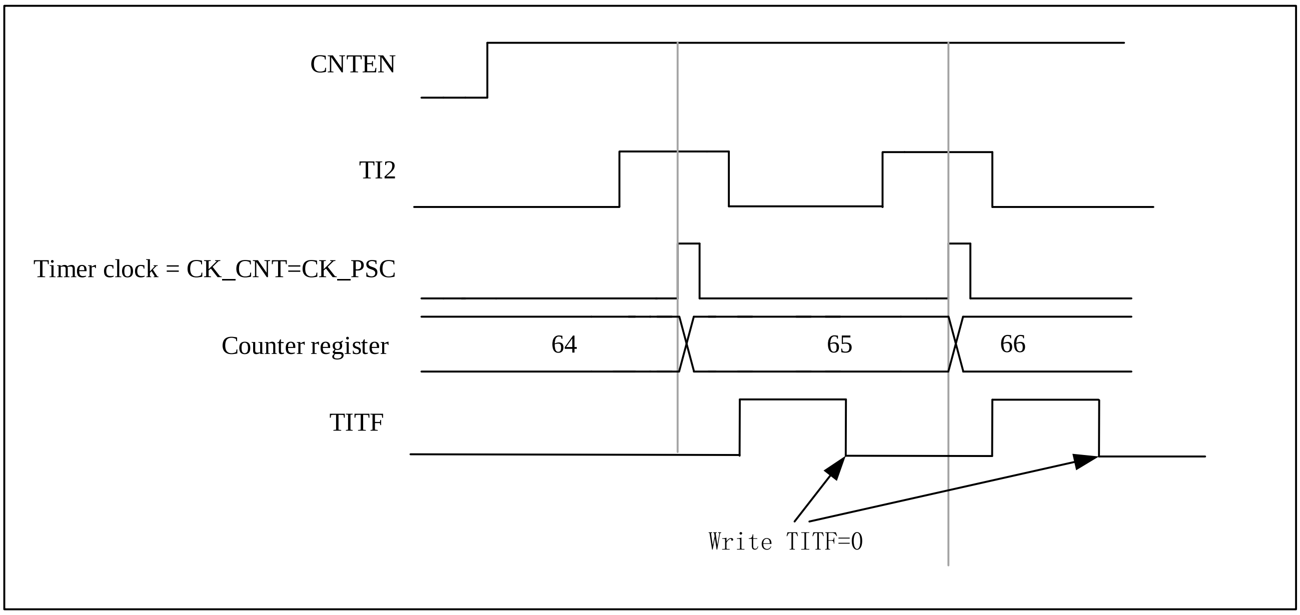
Figure 14-10 Control Circuit in External Clock Mode 1

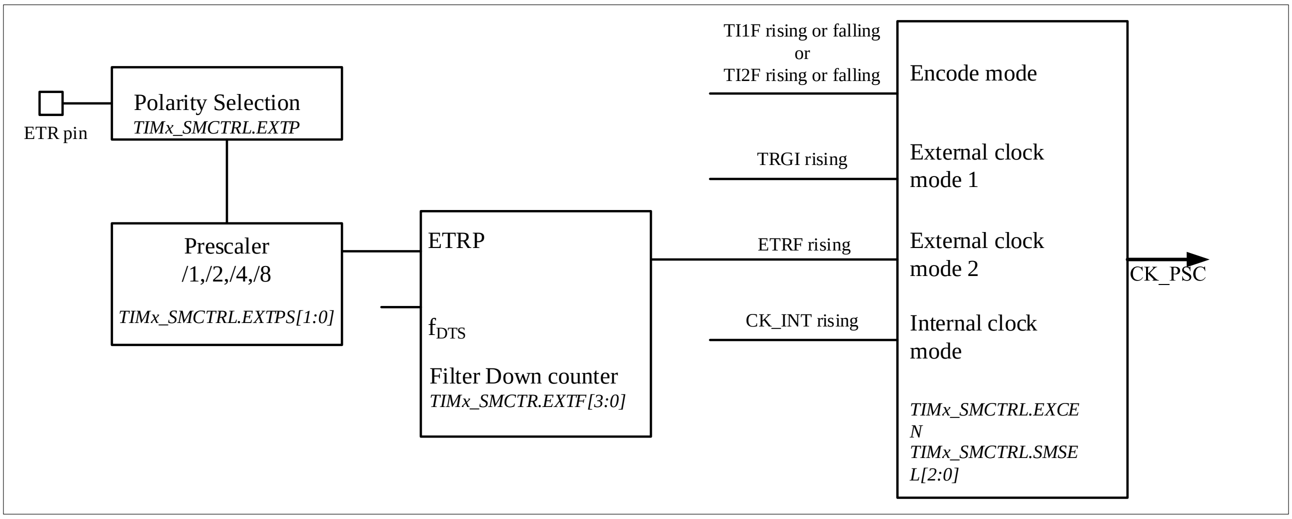


14.3.3.3 External clock source mode 2

This mode is selected by TIMx_SMCTRL .EXCEN equal to 1. The counter can count on every rising or falling edge of the external trigger input ETR.

The following figure is a schematic diagram of the external trigger input module in External clock source mode 2

Figure 14-11 External Trigger Input Block Diagram



For example, use the following configuration steps to make the up counter count every 2 rising edges on ETR.

- Since no filter is needed in this case, make TIMx_SMCTRL .EXTF[3:0] equal to '0000'
- Configure the prescaler by making TIMx_SMCTRL.EXTPS[1:0] equal to '01'
- Select the polarity on ETR pin by setting TIMx_SMCTRL.EXTP equal to '0', The rising edge of ETR is valid
- External clock mode 2 is selected by setting TIMx_SMCTRL .EXCEN equal to '1'

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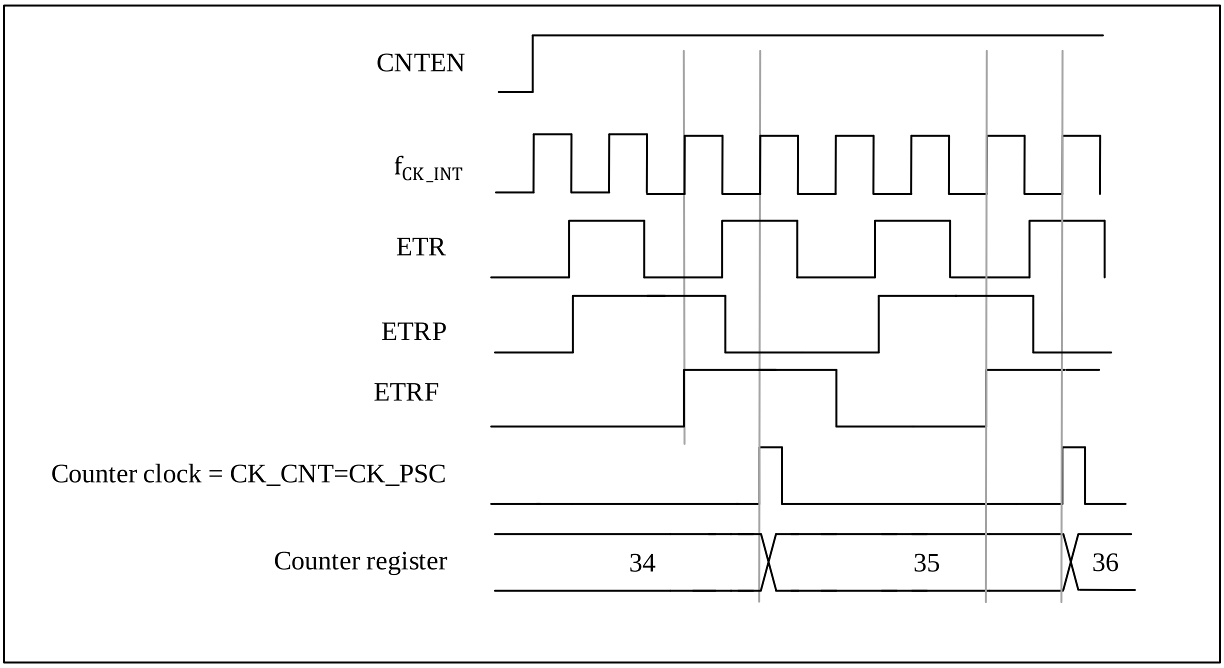
- Turn on the counter by setting TIMx_CTRL1. CNTEN equal to '1'

The counter counts every 2 rising edges of ETR. The delay between the rising edge of ETR and the actual clock to the counter is due to a resynchronization circuit on the ETRP signal.

Figure 14-12 Control Circuit in External Clock Mode 2



14.3.4 Capture/Compare Channels

Capture/Compare channels include Capture/Compare registers and shadow registers. The input section consists of digital filters, multiplexers and prescalers. The output section includes comparators and output controls.

The input signal TIx is sampled and filtered to generate the signal TIxF. A signal (TIxF_rising or TIxF_falling) is then generated by the edge detector of the polarity select function, the polarity of which is selected by the TIMx_CCEN.CCxP bits. This signal can be used as a trigger input for the slave mode controller. At the same time, the signal ICx is sent to the capture register after prescale. The following figure shows a block diagram of a capture/compare channel.

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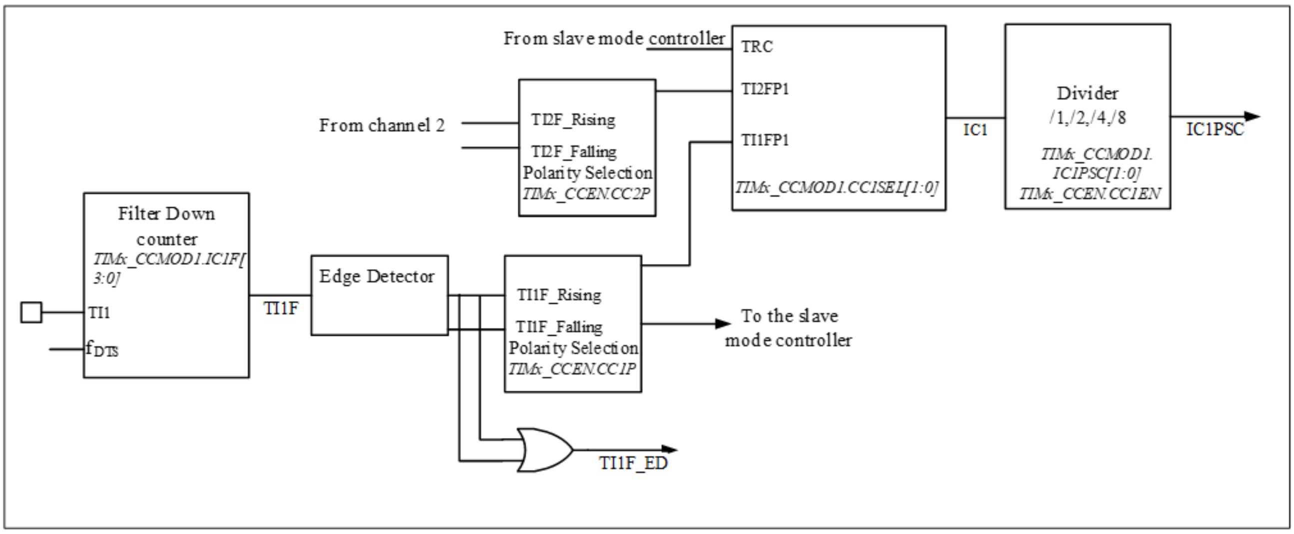
Figure 14-13 Capture/Compare Channel (Example: Channel 1 Input Stage)



The output part generates an intermediate waveform OCxRef (active high) as reference. The polarity acts at the end of the chain.

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Figure 14-14 Capture/Compare Channel 1 Main Circuit

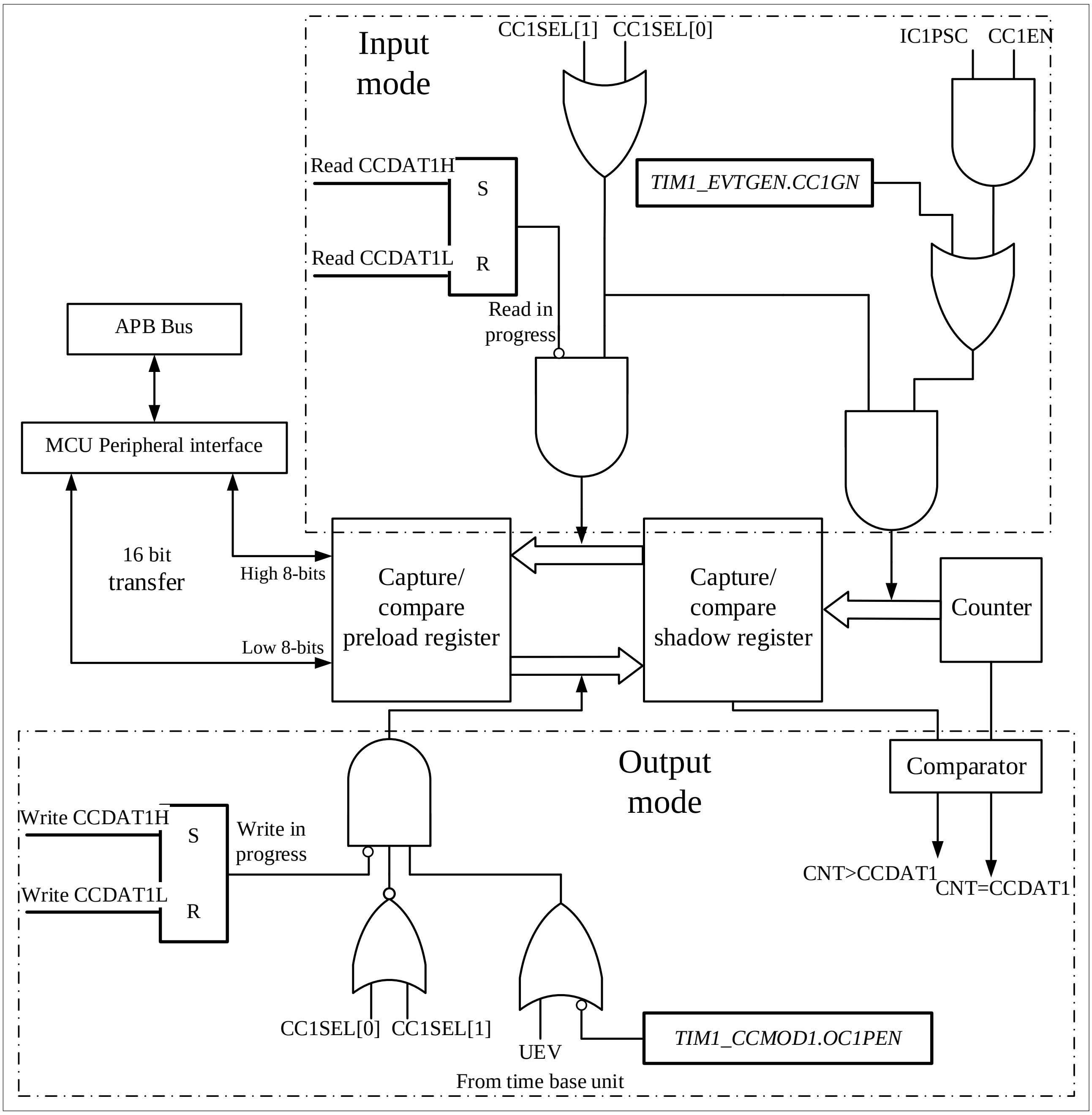

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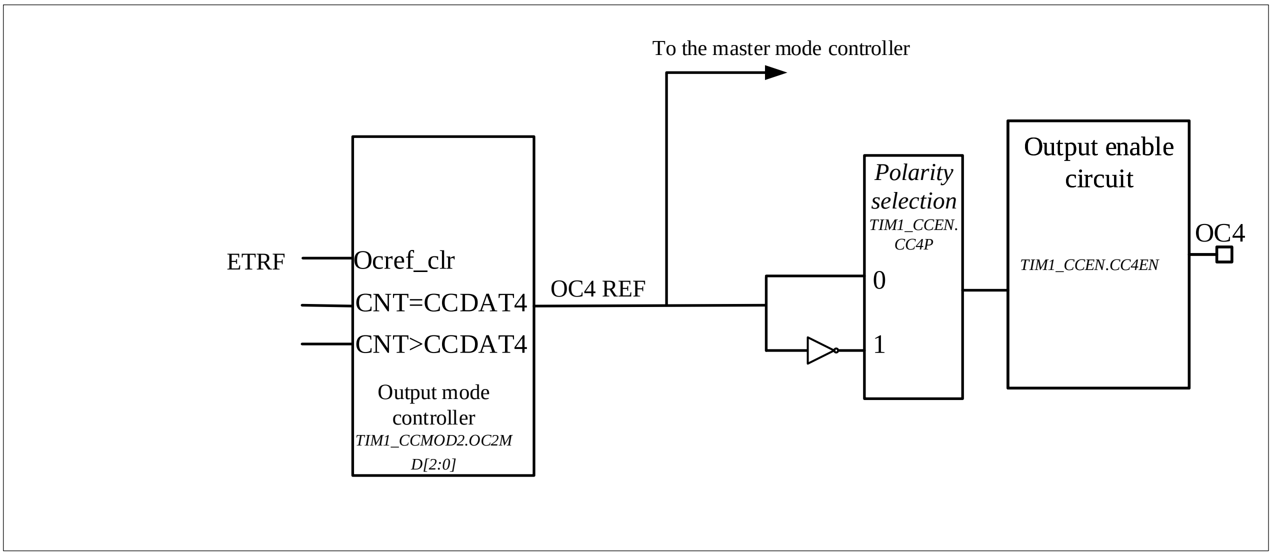
Figure 14-15 Output Part of Channelx (x = 1,2,3,4; Take Channel 4 as an Example)



Reads and writes always access preloaded registers when capturing/comparing. The two specific working processes are as follows:

In capture mode, the capture is actually done in the shadow register, and then the value in the shadow register is copied into the preload register.

In compare mode, as opposed to capture mode, the value of the preload register is copied into the shadow register, which is compared with the counter.

14.3.5 Input Capture Mode

In capture mode, the TIMx_CCDATx registers are used to latch the counter value after the ICx signal detects.

There is a capture interrupt flag TIMx_STS.CCxITF, which can issue an interrupt or DMA request if the corresponding interrupt enable is pulled high.

The TIMx_STS. CCxITF bit is set by hardware when a capture event occurs and is cleared by software or by reading the TIMx_CCDATx register.

The overcapture flag TIMx_STS.CCxOCF is set equal to 1 when the counter value is captured in the TIMx_CCDATx register and TIMx_STS.CC1ITF is already pulled high. Unlike the former, TIMx_STS.CCxOCF is cleared by writing 0 to it.

To achieve a rising edge of the TI1 input to capture the counter value into the TIMx_CCDAT1 register, the configuration flow is as follows:

- To select a valid input:

  Configure TIMx_CCMOD1.CC1SEL to ‘01’. At this time, the input is the CC1 channel, and IC1 is mapped to TI1.

- The duration of the input filter required for programming：

  Define the sampling frequency of the TI1 input and the length of the digital filter by configuring the

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TIMx_CCMODx.ICxF bits. Example: If the input signal jitters up to 5 internal clock cycles, we must choose a filter duration longer than these 5 clock cycles. When 8 consecutive samples (sampled at $f_{TIM4FILTCLK}$ frequency) with the new level are detected, we can validate the transition on TI1. Then configure TIMx_CCMOD1.IC1F to ‘1xxx’.

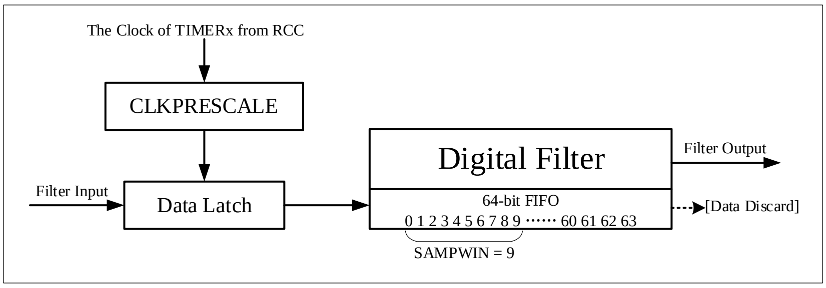
- By configuring TIMx_CCEN.CC1P=0, select the rising edge as the valid transition polarity on the TI1 channel.
- Configure the input prescaler. In this example, configure TIMx_CCMOD1.IC1PSC=‘00’ to disable the prescaler because we want to capture every valid transition.
- Enable capture by configuring TIMx_CCEN.CC1EN = ‘1’.

If you want to enable DMA request, you can configure TIMx_DINTEN.CC1DEN=1.If you want enable related interrupt request, you can configureTIMx_DINTEN.CC1IEN bit=1

14.3.5.1 Channel Input Filtering

The register TIMx_CxFILT (x=1, 2, 3, 4) is described as follows:

Figure 14-16 Sliding Filtering



- Digital filters sample the channel input signal using the RCC's TIMx clock and accumulate the samples in a 64-bit FIFO. Only data sampled within the window size defined in TIMx_CxFILT.WSIZE [5:0] is considered, with a maximum window size of 64.
- The filter outputs the majority value within the sampling window, which is defined by the threshold in TIMx_CxFILT.THRESH [5:0], with a maximum threshold of 63. This value should be equal to or greater than half the window size. If the counts of logic 1 and logic 0 within the sampling window are not greater than the threshold, the digital filter maintains the previous output value.
- RCC_TIMFILTCFG.TIM4FILTCLK[4:0] register determines the sampling rate of the corresponding digital filter. The filter FIFO captures a sample value from the input at each sampling clock.
- If the digital filter is disabled, the filter input is directly output.

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14.3.6 PWM Input Mode

There are some differences between PWM input mode and normal input capture mode, including:

- Two ICx signals are mapped to the same TIx input.
- The two ICx signals are active on edges of opposite polarity.
- Select one of two TIxFP signals as trigger input.
- The slave mode controller is configured in reset mode.

For example, the following configuration flow can be used to know the period and duty cycle of the PWM signal on TI1 (It depends on the frequency of CK_INT and the value of the prescaler).

- Configure TIMx_CCMOD1.CC1SEL equal to '01' to select TI1 as valid input for TIMx_CCDAT1
- Configure TIMx_CCEN.CC1P equal to '0' to select the active polarity of filtered timer input 1(TI1FP1), active at the rising edge.
- Configure TIMx_CCMOD1.CC2SEL equal to '10' select TI1 as valid input for TIMx_CCDAT2.
- Configure TIMx_CCEN.CC2P equal to 1 to select the valid polarity of filtered timer input 2(TI1FP2), active at the falling edge.
- Configure TIMx_SMCTRL.TSEL=101 to select Filtered timer input 1 (TI1FP1) as valid trigger input.
- Configure TIMx_SMCTRL.SMSEL=0100 to configure the slave mode controller to reset mode.
- Configure TIMx_CCEN. CC1EN=1 and TIMx_CCEN.CC2EN=1 to enable capture.

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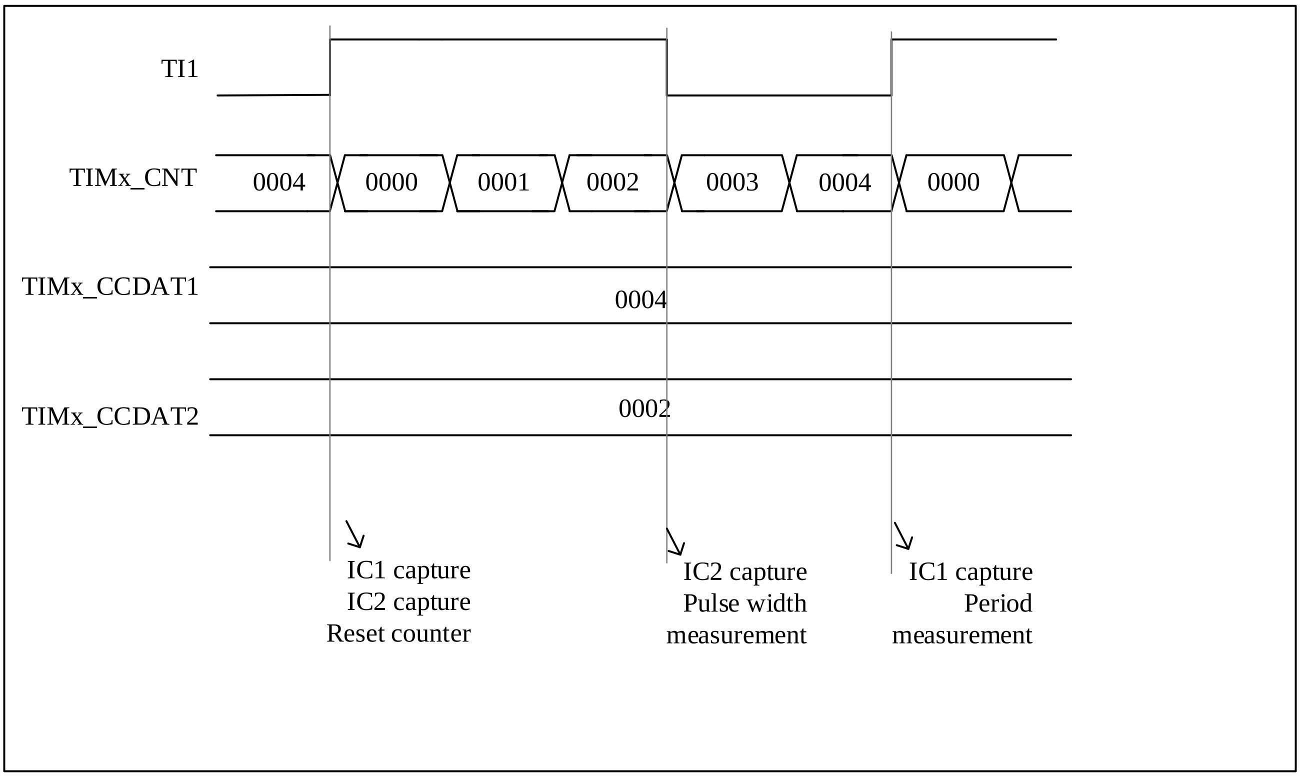
Figure 14-17 PWM Input Mode Timing



Because of only filter timer input 1 (TI1FP1) and filter timer input 2 (TI2FP2) are connected to the slave mode controller, the PWM input mode can only be used with the TIMx_CH1/TIMx_CH2 signals.

14.3.7 Forced Output Mode

Software can force output compare signals to active or inactive level directly, in output mode (TIMx_CCMODx.CCxSEL=00).

User can set TIMx_CCMODx. OCxMD=101 to force the output compare signal to active level. And the OCxREF will be forced high, OCx get opposite value to CCxP polarity bit. On the other hand, user can set TIMx_CCMODx. OCxMD=100 to force the output compare signal to inactive level, the OCxREF will be forced low.

The values of the TIMx_CCDATx shadow register and the counter still comparing with each other in this mode.

The comparison between the output compare register TIMx_CCDATx and the counter TIMx_CNT has no effect on OCxREF. And the flag still can be set. Therefore, the interrupt and DMA requests still can be sent.

14.3.8 Output Compare Mode

User can use this mode to control the output waveform, or to indicate that a period of time has elapsed。

When the capture/compare register and the counter have the same value, the output compare function's operations are as follow:

- TIMx_CCMODx.OCxMD is for output compare mode, and TIMx_CCEN.CCxP is for output polarity. When the compare matches, if set TIMx_CCMODx.OCxMD=000, the output pin will keep its level; if set

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TIMx_CCMODx.OCxMD=001, the output pin will be set active;if set TIMx_CCMODx.OCxMD=010, the output pin will be set inactive;if set TIMx_CCMODx.OCxMD=011, the output pin will be set to toggle.

- Set TIMx_STS.CCxITF.
- If user set TIMx_DINTEN.CCxIEN, a corresponding interrupt will be generated
- If user set TIMx_DINTEN.CCxDEN and set TIMx_CTRL2.CCDSEL to select DMA request, and DMA request will be sent

User can set TIMx_CCMODx.OCxPEN to choose capture/compare shawdow regisete using capture/compare preload registers (TIMx_CCDATx) or not

The time resolution is one counting period of the counter.

In one pulse mode, the output compare mode can also be used to output a single pulse

Here are the configuration steps for output compare mode:

- First of all, user should select the counter clock.
- Secondly, set TIMx_AR and TIMx_CCDATx with required data.
- If user need to generate an interrupt, set TIMx_DINTEN.CCxIEN.
- Then select the output mode by set TIMx_CCEN.CCxP, TIMx_CCMODx.OCxMD, TIMx_CCEN.CCxEN, etc.
- At last, set TIMx_CTRL1.CNTEN to enable the counter.

User can update the output waveform by setting TIMx_CCDATx at any time, as long as the preload register is not enabled. Otherwise the TIMx_CCDATx shadow register will be updated at the next update event

Here is an example.

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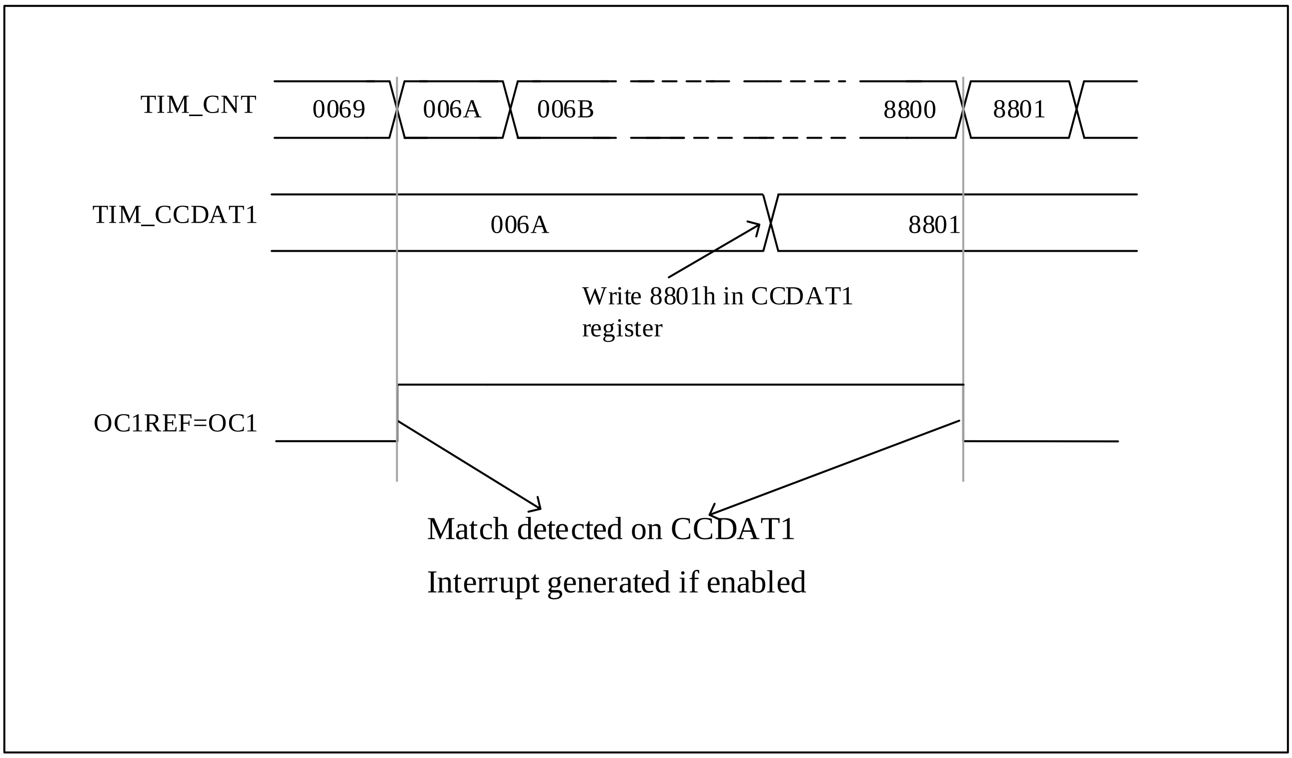
Figure 14-18 Output Compare Mode, Toggle on OC1



14.3.9 PWM Mode

User can use PWM mode to generate a signal whose duty cycle is determined by the value of the TIMx_CCDATx register and whose frequency is determined by the value of the TIMx_AR register. And depends on the value of TIMx_CTRL1.CAMSEL, the TIM can generate PWM signal in edge-aligned mode or center-aligned mode.

User can set PWM mode 1 or PWM mode 2 by setting TIMx_CCMODx. OCxMD=110 or setting TIMx_CCMODx. OCxMD=111. To enable preload register, user must set corresponding TIMx_CCMODx.OCxPEN. And then set TIMx_CTRL1.ARPEN to auto-reload preload register eventually.

User can set polarity of OCx by setting TIMx_CCEN.CCxP.

The values of TIMx_CNT and TIMx_CCDATx are always compared with each other when the TIM is under PWM mode.

Only if an update event occurs, the preload register will transfer to the shadow register. Therefore user must reset all the registers by setting TIMx_EVTGEN.UDGN before the counter starts counting.

14.3.9.1 PWM center-aligned mode

If user set TIMx_CTRL1.CAMSEL equal 01, 10 or 11, the PWM center-aligned mode will be active. The setting of the compare flag depends on the value of TIMx_CTRL1.CAMSEL. There are three kinds of situation that the compare flag is set, only when the counter counts up, only when the counter counts down, or when the counter counts up and counts down. User should not modified TIMx_CTRL1.DIR by software, it is updated by hardware.

Examples of center-aligned PWM waveforms is as follow, and the setting of the waveform are: TIMx_AR=8, PWM mode 1, the compare flag is set when the counter counts down corresponding to TIMx_CTRL1.CAMSEL=01.

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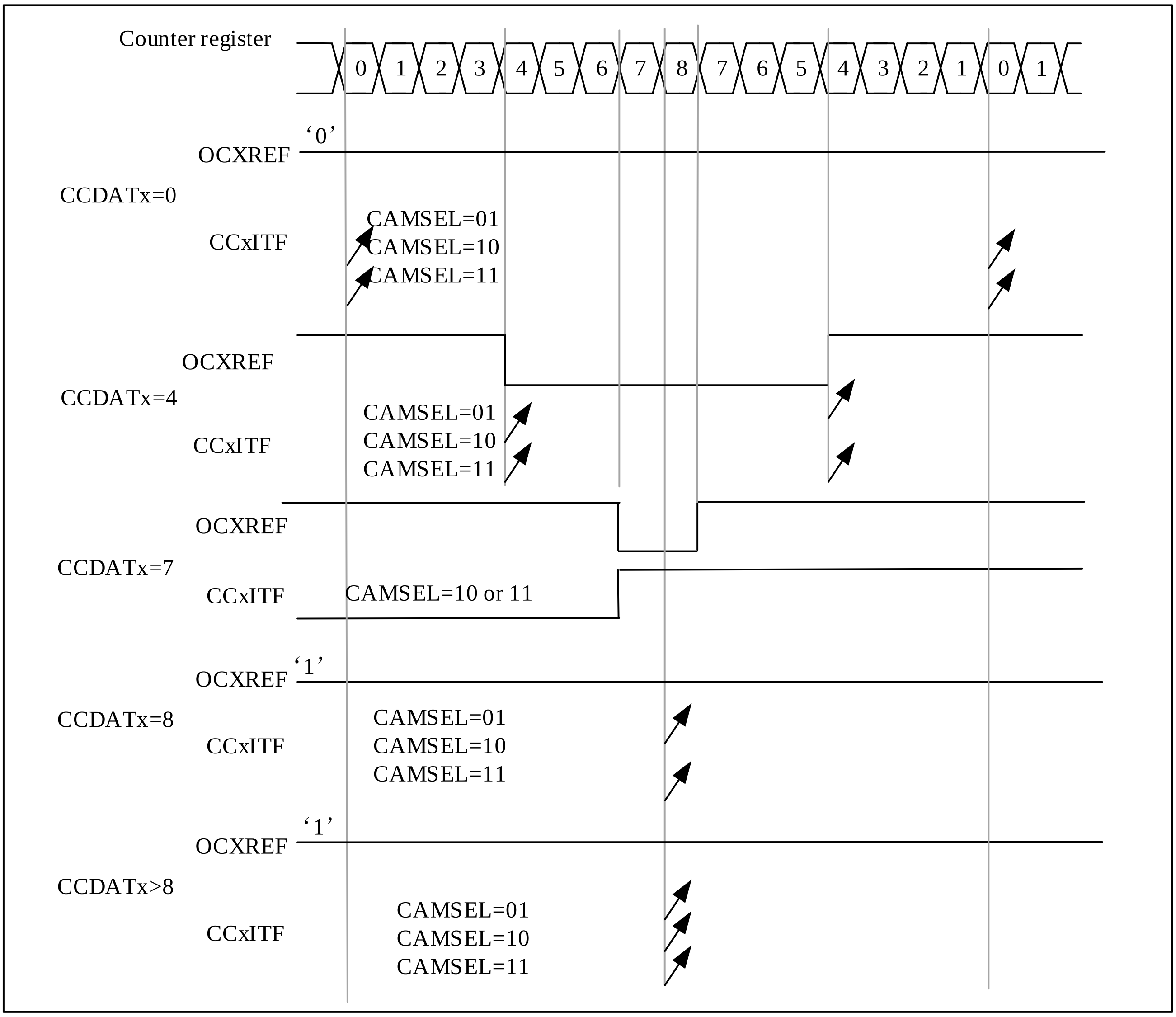
Figure 14-19 Center-aligned PWM Waveform (AR=8)



When using center-aligned mode, users should pay attention to the following considerations:

- It depends on the value of TIMx_CTRL1.DIR that the counter counts up or down. Cautions that the DIR and CAMSEL bits should not be changed at the same time.
- User should not write the counter while running in center-aligned mode, otherwise it will cause unexpected results. Here are some examples:
  - If the value written into the counter is 0 or is the value of TIMx_AR, the direction will be updated but the update event will not be generated.
  - If the value written into the counter is greater than the value of auto-reload, the direction will not be updated
- To be on the safe side, user is suggested setting TIMx_EVTGEN.UDGN to generate an update by software

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before starting the counter, and not writing the counter while it is running.

14.3.9.2 PWM edge-aligned mode

There are two kinds of configuration in edge-aligned mode, up-counting and down-counting.

- **Up-counting**

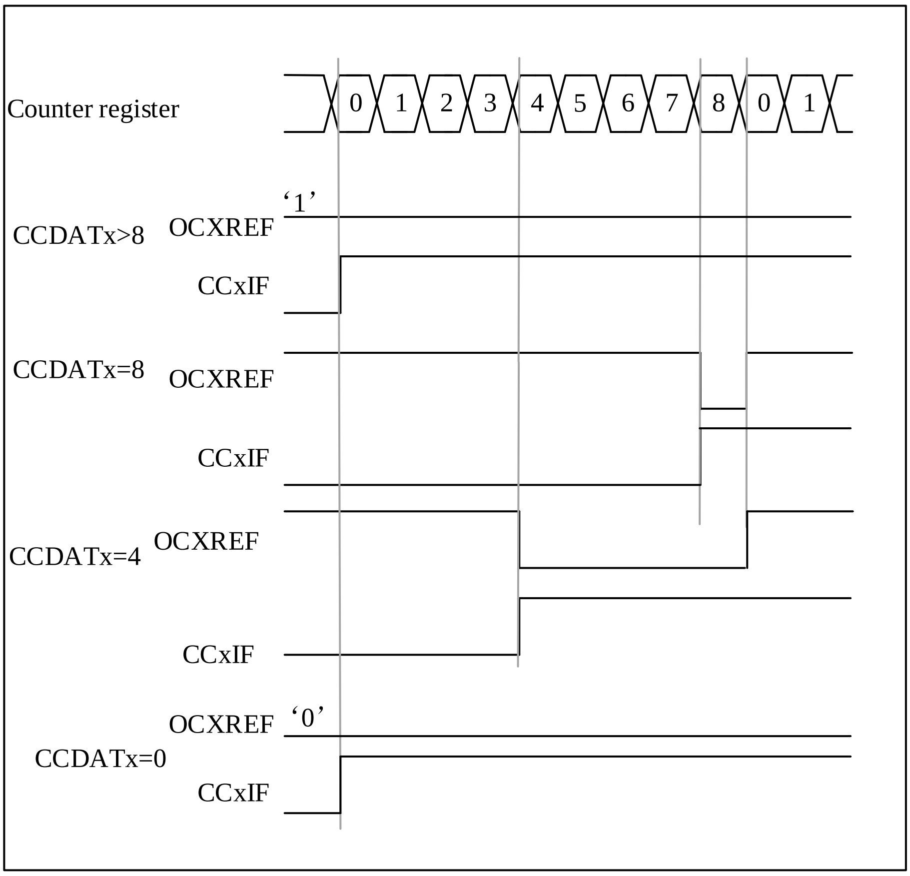
User can set TIMx_CTRL1.DIR=0 to make counter counts up.

Example for PWM mode1：

When TIMx_CNT < TIMx_CCDATx, the reference PWM signal OCxREF is high. Otherwise it will be low. If the compare value in TIMx_CCDATx is greater than the auto-reload value, the OCxREF will remains 1. Conversely, if the compare value is 0, the OCxREF will remains 0.

When TIMx_AR=8, the PWM waveforms are as follow:

Figure 14-20 Edge-aligned PWM Waveform (APR=8)



- **Down-counting**

User can set TIMx_CTRL1.DIR=1 to make counter counts down.
Example for PWM mode1：

When TIMx_CNT > TIMx_CCDATx, the reference PWM signal OCxREF is low. Otherwise it will be high. If the compare value in TIMx_CCDATx is greater than the auto-reload value, the OCxREF will remains 1.

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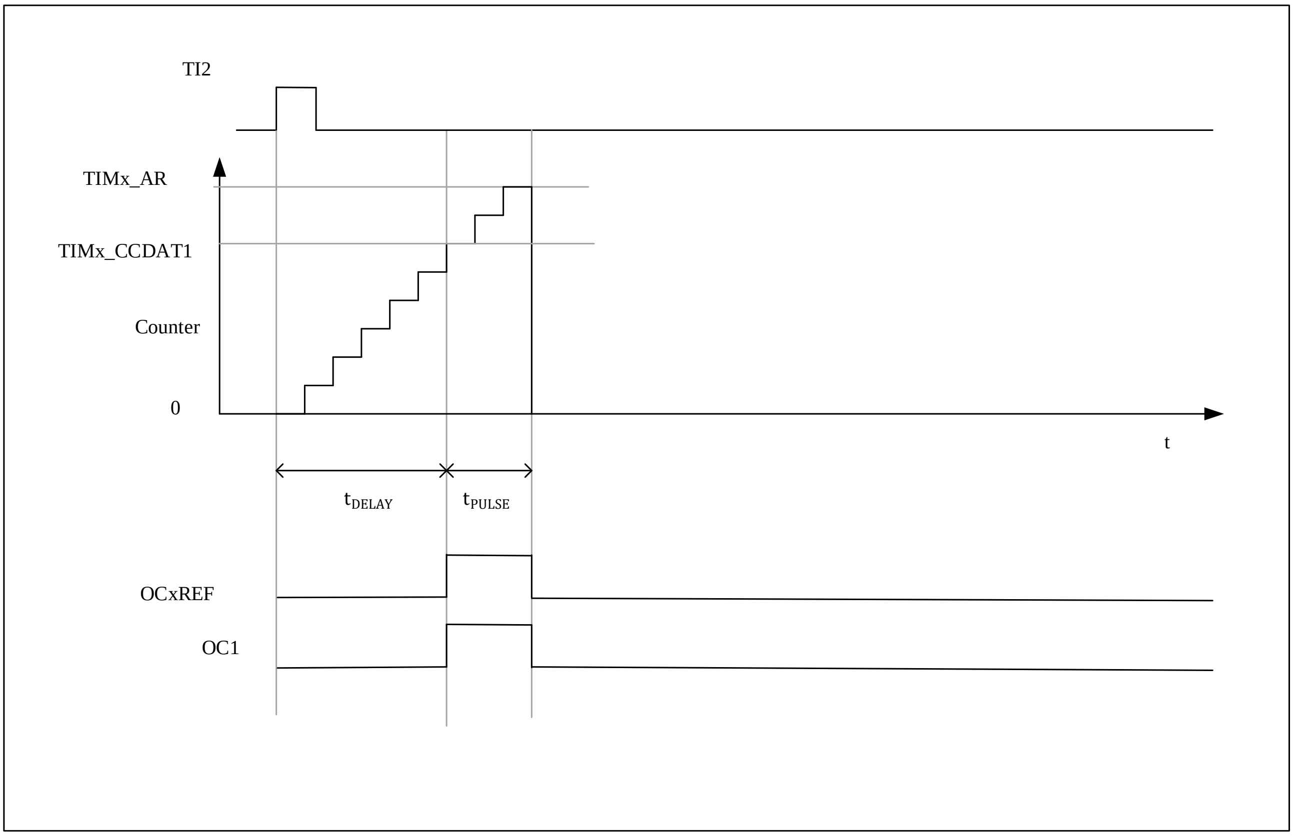
Note: If the nth PWM cycle CCDATx shadow register >= AR value, the shadow register value of CCDATx in the (n+1)th PWM cycle is 0. At the moment when the counter is 0 in the (n+1)th PWM cycle, although the value of the counter = CCDATx shadow register = 0 and OCxREF = '0', no compare event will be generated.

14.3.10 One-pulse Mode

In the one-pulse mode (ONEPM), a trigger signal is received, and a pulse t_{PULSE} with a controllable pulse width is generated after a controllable delay t_{DELAY}. The output mode needs to be configured as output compare mode or PWM mode. After selecting one-pulse mode, the counter will stop counting after the update event UEV is generated

Figure 14-21 Example of One-pulse Mode



The following is an example of a one-pulse mode：

A rising edge trigger is detected from the TI2 input, and a pulse with a width of t_{PULSE} is generated on OC1 after a delay of t_{DELAY}.

7. Counter configuration: count up, counter TIMx_CNT < TIMx_CCDAT1 ≤ TIMx_AR;
8. TI2FP2 is mapped to TI2, TIMx_CCMOD1.CC2SEL=‘01’; TI2FP2 is configured for rising edge detection, TIMx_CCEN.CC2P=‘0’;
9. TI2FP2 acts as the trigger (TRGI) of the slave mode controller and starts the counter, TIMx_SMCTRL.TSEL= ‘110’, TIMx_SMCTRL.SMSEL=‘0110’ (trigger mode);
10. TIMx_CCDAT1 writes the count value to be delayed (t_{DELAY}), TIMx_AR - TIMx_CCDAT1 is the count value

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of the pulse width t_{PULSE};

11. Configure TIMx_CTRL1.ONEPM=1 to enable single pulse mode, configure TIMx_CCMOD1.OC1MD='111' to select PWM2 mode;
12. Wait for an external trigger event on TI2, and a one pulse waveform will be output on OC1;

14.3.10.1 Special case: OCx fast enable

In one-pulse mode, an edge is detected through the TIx input, and triggers the start of the counter to count to the comparison value and then output a pulse. These operations limit the minimum delay t_{DELAY} that can be achieved.

You can set TIMx_CCMODx.OCxFEN=1 to turn on OCx fast enable, after triggering the rising edge, the OCxREF signal will be forced to be converted to the same level as the comparison match occurs immediately, regardless of the comparison result. OCxFEN fast enable only takes effect when the channel mode is configured for PWM1 and PWM2 modes.

14.3.11 Clearing The OCxREF Signal on an External Event

If user set TIMx_CCMODx.OCxCEN=1, high level of tim_ocref_clr_in input can be used to driven the OCxREF signal to low, and the OCxREF signal will remains low, until the next UEV happens. Only output compare and PWM modes can use this function. This cannot be used when it is in forced mode.

For example, to control the current, users can connect the ETR signal to the comparator's output. The operation of ETR is as follows:

- Set TIMx_SMCTRL.EXTPS=00 to disable the external trigger prescaler.
- Set TIMx_SMCTRL.EXCEN=0 to disable the external clock mode 2.
- Set TIMx_SMCTRL.EXTP and TIMx_SMCTRL.EXTF to configure the external trigger polarity and external trigger filter as needed.

Here is an example for the case that when ETRF input becomes high, the behavior of OCxREF signal for different value of OCxCEN. Timer is set to be in PWM mode in this case.

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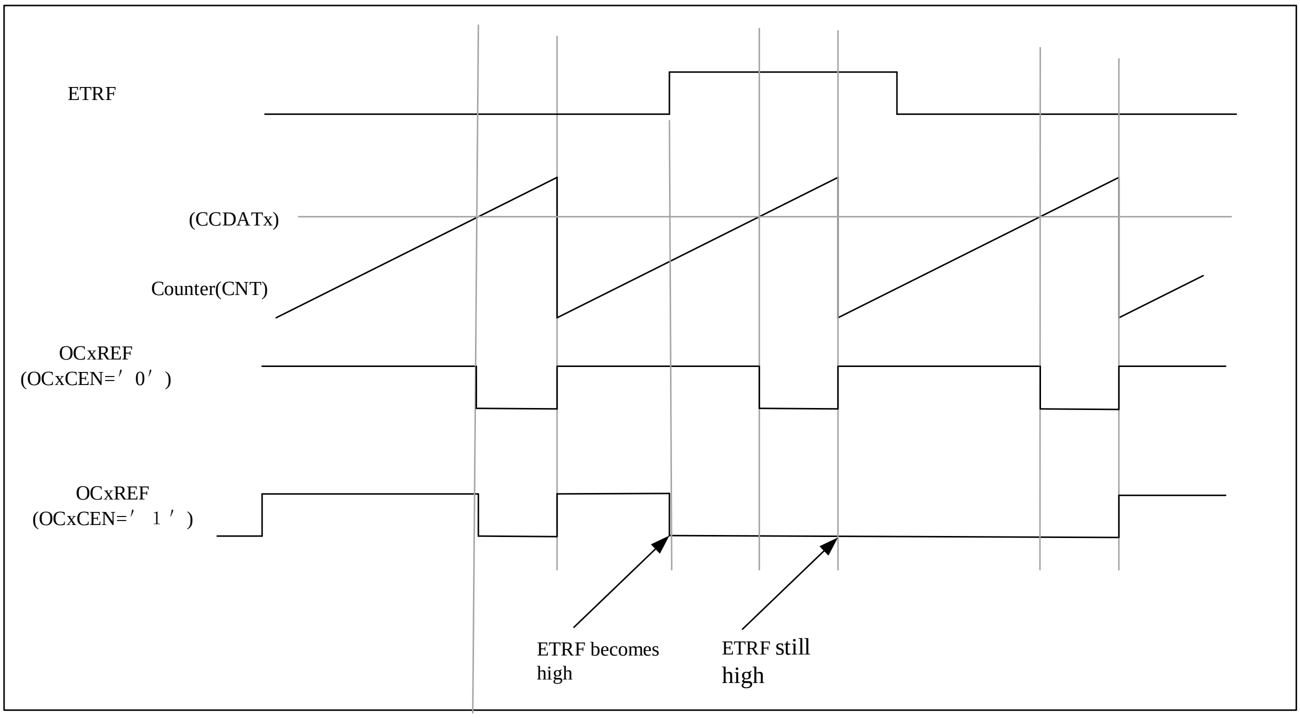
Figure 14-22 Clearing OCxREF of TIMx



14.3.12 Debug Mode

When the microcontroller is in debug mode (the Cortex-M0 core halted), depending on the DBG_CTRL.TIMx_STOP configuration, the TIMx counter can either continue to work normally or stop. For more details, refer to Section 3.3.1.

14.3.13 TI3 Event Trigger Function

14.3.13.1 Event Triggered Loading

Users may employ the input signal TI3 on channel 3 as a trigger to reload the timer value using the current value from the external event counter load register (TIMx_ENCLVR. LVR[31:0]). This functionality is enabled via the TIMx_ENCMCTRL. C3LDCNTEN bit. When the TI3 valid event triggers a load, the TI3 valid event trigger counter load to LVR value interrupt can be enabled via TIMx_DINTEN.C3LDCNTIEN.

Note that the TI3 trigger signal may be edge-sensitive or level-sensitive; users may configure this via TIMx_ENCMCTRL.C3LDCNTSEL[1:0].

As illustrated below, the external signal serves as a trigger, activated upon its rising edge. Each time a rising edge of the external signal is detected, the timer value is loaded into TIMx_ENCLVR. LVR[31:0]. The synchronisation delay for the external event is not depicted in the diagram; actual external events will incorporate a delay.

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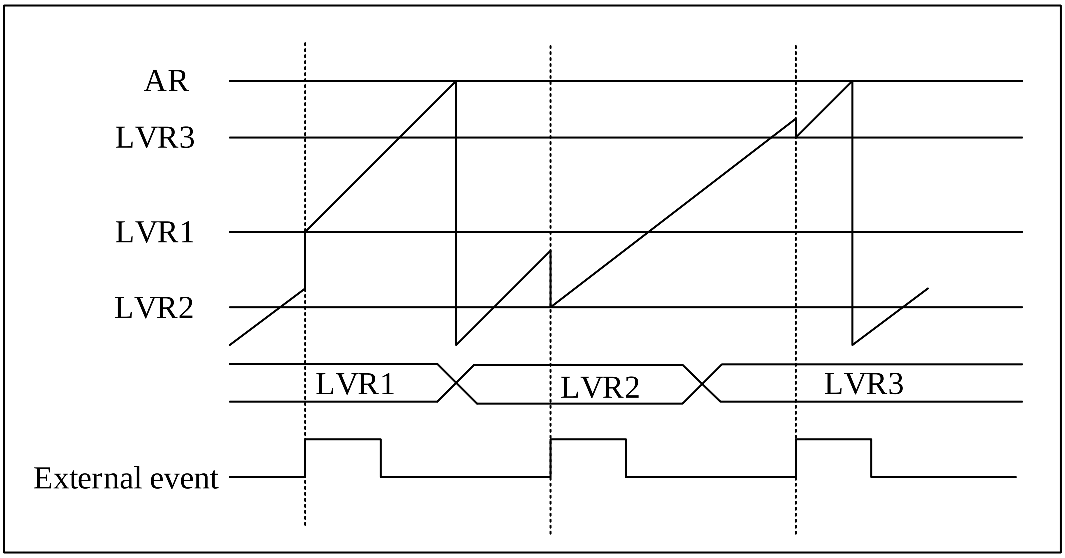
Figure 14-23 External event triggers loading



14.3.13.2 TI3 Event Trigger Capture Interpolation

Upon detection of the valid edge of the TI3 event.

(When TIMx_ENCMCTRL.C3LDCNTSEL[1:0]=2'bx0, the rising edge is active; When TIMx_ENCMCTRL.C3LDCNTSEL[1:0]=2'bx1, the falling edge is active.) TIMx_ENCDAT will record the absolute value of the difference between the current counter value and the TIMx_ENCLVR .LVR value.

TIMx_ENCDAT.ENCDAT= | TIMx_CNT.CNT-TIMx_ENCLVR .LVR | .

Concurrently, TIMx_ENCMCTRL.ENCDATS will record the sign of the difference between the current counter value and the LVR value. For example, if ENCDATS equals 0, this indicates that ENCDAT is positive, meaning TIMx_CNT.CNT - TIMx_ENCLVR.LVR is greater than or equal to 0; if ENCDATS equals 1, this indicates that ENCDAT is negative, meaning TIMx_CNT.CNT - TIMx_ENCLVR.LVR is less than 0.

14.3.14 TIMx and External Trigger Synchronization

Same as the advanced timer, refer to Section 12.3.16

14.3.15 Timer Synchronization

All TIM timers are internally interconnected for timer synchronisation or linking. For further details, refer to Section 13.3.16.

14.3.16 Encoder Interface Mode

14.3.16.1 Orthogonal Coding Mode

The encoder uses two inputs TI1 and TI2 as an interface. And the counter counts on every edge change on TI1FP1 or TI2FP2. The counting direction is automatically controlled by hardware TIMx_CTRL1.DIR. There are five types of quadrature encoder counting modes:

- Encode Mode 1: The counter only counts on the edge of TI1, TIMx_SMCTRL.SMSEL = ‘0001’ or

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TIMx_ENCMCTRL.ENCMD = ‘0001’;

- Encode Mode 2: The counter only counts on the edge of TI2, TIMx_SMCTRL.SMSEL =’0010’ or TIMx_ENCMCTRL.ENCMD = ‘0010’;
- Encode Mode 3: The counter counts on both TI1 and TI2 edges, TIMx_SMCTRL.SMSEL = ‘0011’ or TIMx_ENCMCTRL.ENCMD = ‘0011’;
- Encoder Mode 4: When T2 is high, the counter increments only on the edge of TI1, provided either TIMx_SMCTRL.SMSEL = “1001” or TIMx_ENCMCTRL.ENCMD = “0100”;
- Encoder Mode 5: When T1 is high, the counter only increments on the edge of TI2, with TIMx_SMCTRL.SMSEL = “1010” or TIMx_ENCMCTRL.ENCMD = “0101”;

The encoder interface is equivalent to using an external clock with direction selection, and the counter only counts continuously between 0 and the auto-reload value (TIMx_AR.AR [15:0]). Therefore, it is necessary to configure the auto-reload register TIMx_AR in advance.

Note: Encoder mode and external clock mode 2 are not compatible and must not be selected together.

The relationship between the counting direction and the encoder signal is shown in following table:

Table 14-1 The Relationship between the Counting Direction and the Encoder Signal（CC1P=CC2P=0）

Effective edge	SMSEL[3:0] OR ENCMD[3:0]	Relative signal levels (TI1FP1 corresponds to TI2, TI2FP2 corresponds to TI1)	TI1FP1 Signal		TI2FP2 Signal	
			Rise	Fall	Rise	Fall
Counted only at TI1	SMSEL = 0001 or ENCMD = 0001	High	count down	count up	Not counted	Not counted
		Low	count up	count down	Not counted	Not counted
Counted only at TI2	SMSEL =0010 or ENCMD = 0010	High	Not counted	Not counted	count up	count down
		Low	Not counted	Not counted	count down	count up
Counting on TI1 and TI2	SMSEL =0011 or ENCMD = 0011	High	count down	count up	count up	count down
		Low	count up	count down	count down	count up
Counts only at TI1	SMSEL =1001 or	High	count down	count up	Not counted	Not counted

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Effective edge	SMSEL[3:0] OR ENCMD[3:0]	Relative signal levels (TI1FP1 corresponds to TI2, TI2FP2 corresponds to TI1)	TI1FP1 Signal		TI2FP2 Signal	
			Rise	Fall	Rise	Fall
and T2 is high	ENCMD = 0100	Low	Not counted	Not counted	Not counted	Not counted
Counts only at TI2 and T1 is high	SMSEL =1010 or ENCMD= 0101	High	Not counted	Not counted	count up	count down
		Low	Not counted	Not counted	Not counted	Not counted

The counter value changes as follows in each mode:

Figure 14-24 The encoder only counts at TI1

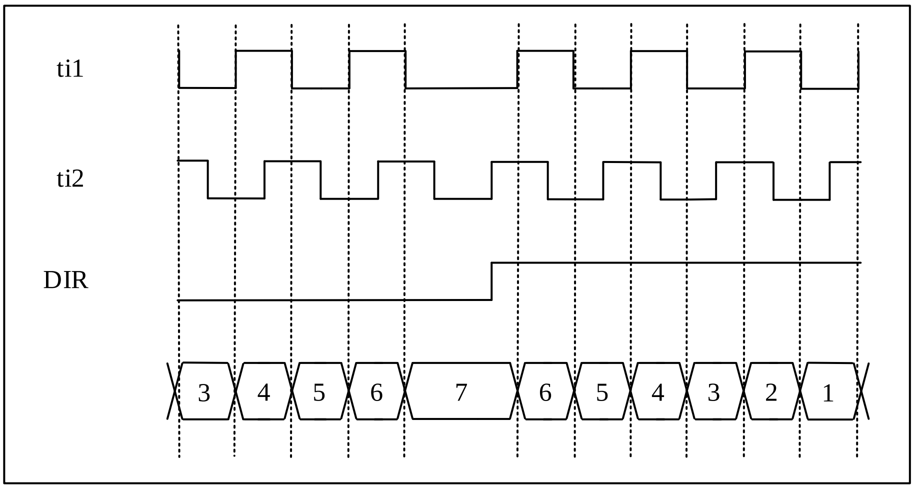

Figure 14-25 Encoder Counts Only at TI2

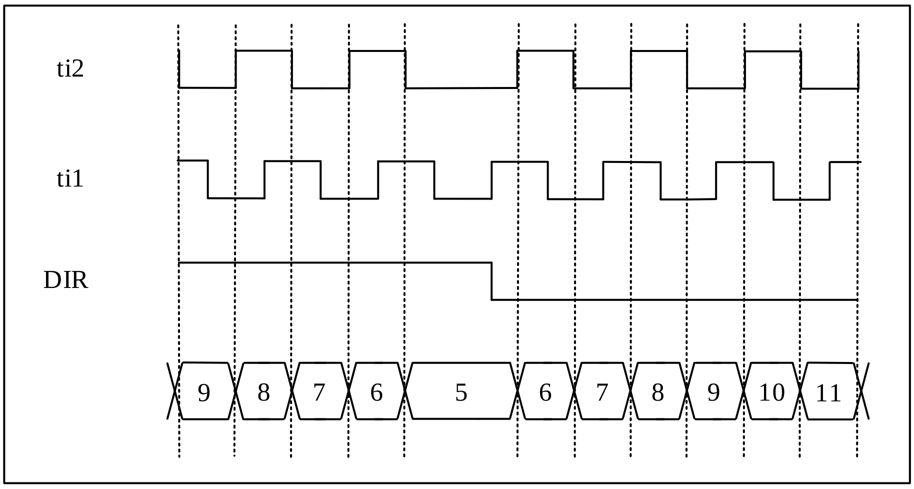

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Figure 14-26 The encoder counts on TI1 and TI2

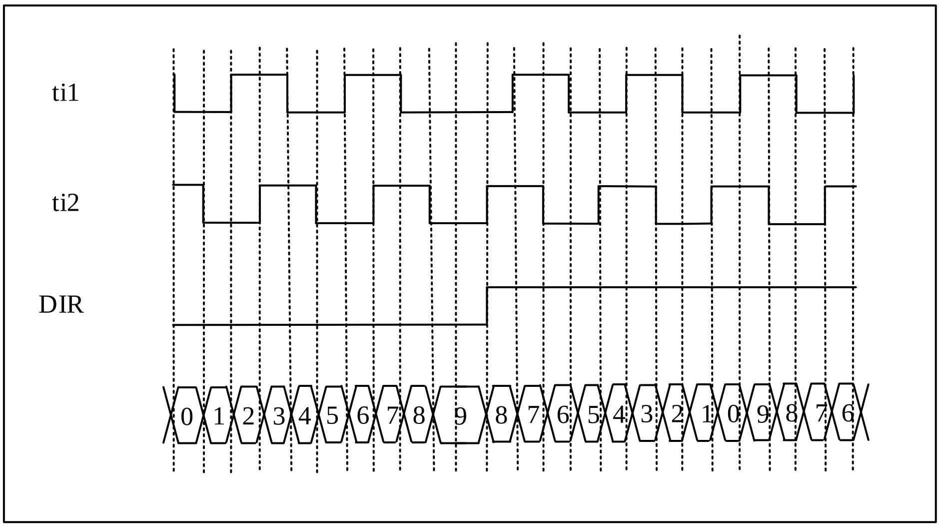


Figure 14-27 When T2 is high, the counter only increments during TI1

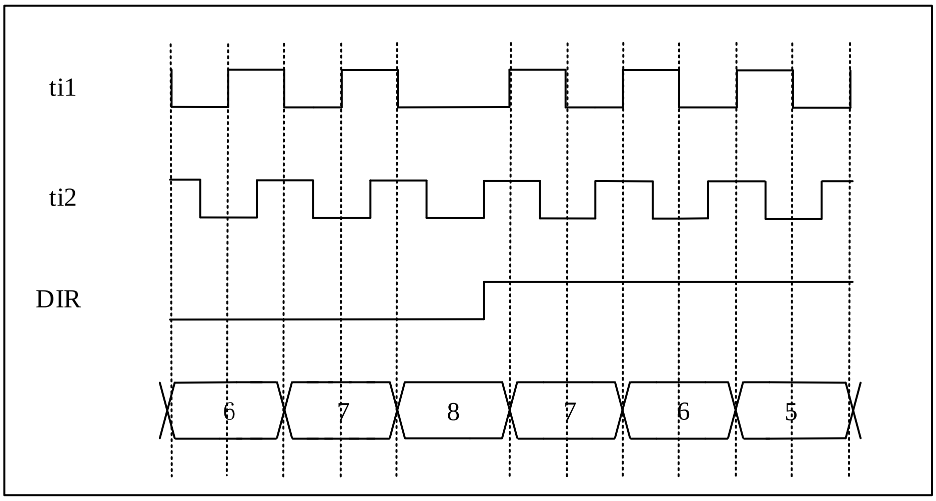
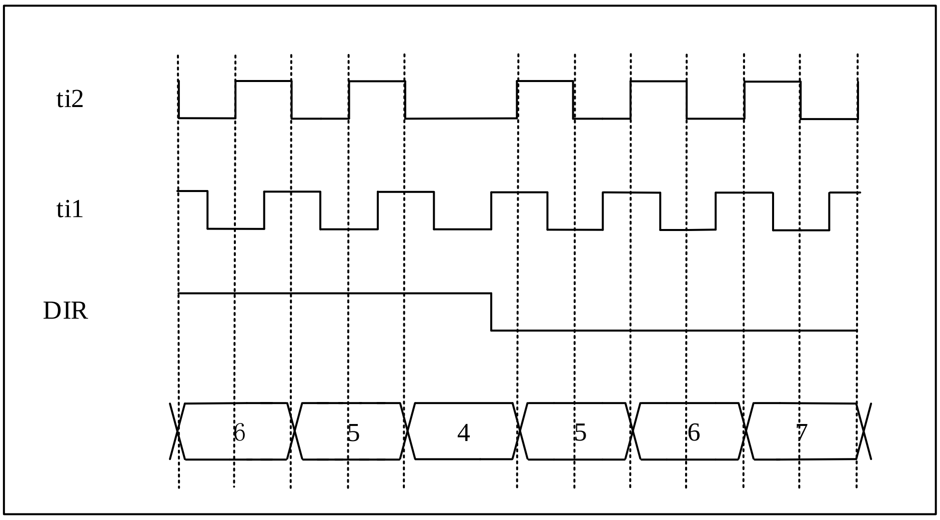


Figure 14-28 When T1 is high, the counter only increments during TI2



The following is an example of an encoder that employs a dual-edge trigger to suppress input jitter:

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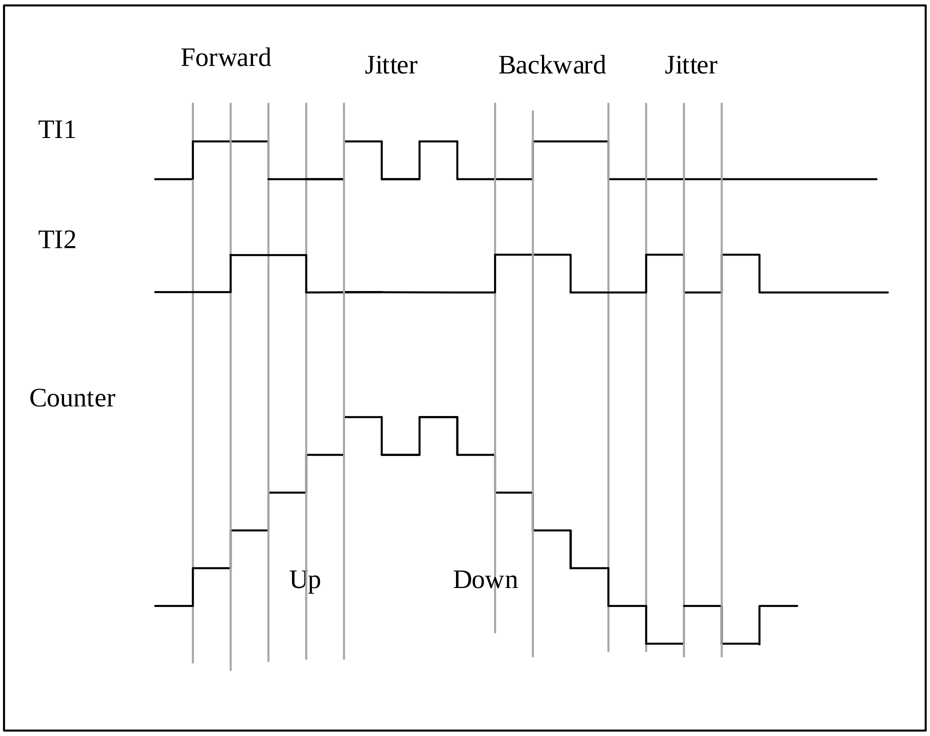
5. IC1FP1 is mapped to TI1 (TIMx_CCMOD1.CC1SEL = “01”), IC1FP1 is not inverted (TIMx_CCEN.CC1P = “0”);
6. IC1FP2 is mapped to TI2 (TIMx_CCMOD2.CC2SEL = “01”), IC2FP2 is not inverted (TIMx_CCEN.CC2P = “0”);
7. Input is valid on both rising and falling edges (TIMx_SMCTRL.SMSEL = “0011”);
8. Enable the counter TIMx_CTRL1.CNTEN = “1”;

Figure 14-29 Examples of counter operations in encoder mode



The figure below illustrates the counter behaviour when the polarity of IC1FP1 is reversed (CC1P = “1”, with all other configurations unchanged).

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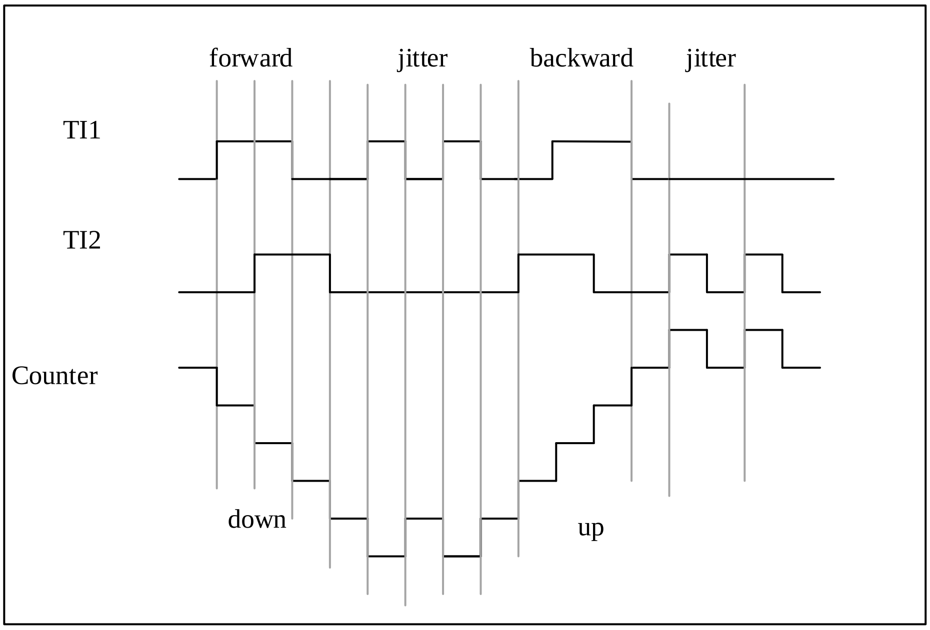
Figure 14-30 Example of IC1FP1 Inverted Encoder Interface Mode



14.3.16.2 Pulse Level Encoding Mode

In pulse level encoding mode, the clock is provided on a single line via TI2, whilst the counting direction is supplied by the TI1 input.

This mode is enabled via SMSEL[3:0] in the TIMx_SMCTRL register, as detailed below.

1011: Pulse level encoding mode 2, where the counter is updated on both the rising and falling edges of the clock. This mode may also be enabled by setting TIMx_ENCMCTRL.ENCMD = “0111”.

1100: Pulse Level Encoding Mode 1. Based on the CC2P value, the counter updates on a single clock edge. CC2P = 0 corresponds to rising edge counting, while CC2P = 1 corresponds to falling edge counting. This mode may also be enabled by setting TIMx_ENCMCTRL.ENCMD = “0110”.

The polarity of the direction signal for TI1 is configured via the CC1P bit. When CC2P = 0, TI1 counts upwards when high and counts downwards when low; when CC1P = 1, TI1 counts upwards when low and counts downwards when high.

The following diagram illustrates the case where CC1P = CC2P = 0:

Figure 14-31 Pulse Level Encoding Mode（CC1P=CC2P=0）

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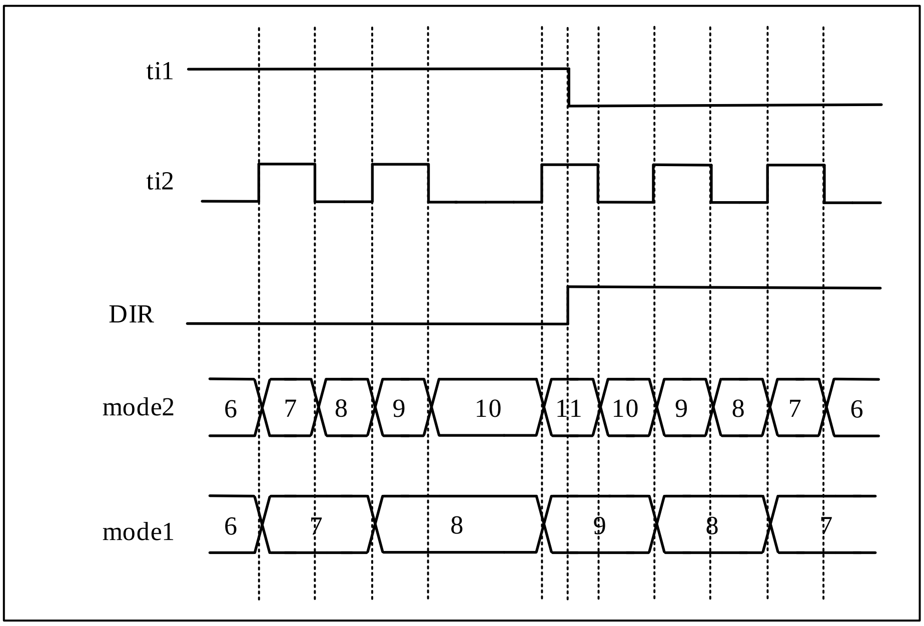

14.3.16.3 Dual-pulse coding mode

In the dual-pulse encoding mode, the clock is supplied on two lines, with only one line active at a time depending on the direction. This results in one clock line for upward counting and one for downward counting.

This mode is enabled via the SMSEL[3:0] bit field within the TIMx_SMCTRL register, as detailed below.

- 1000：Dual-pulse encoding mode 2, wherein the counter is updated on both the rising and falling edges of either clock line. The CC1P and CC2P bits encode the clock idle state. CCxP=0 corresponds to a high-level idle state, while CCxP=1 corresponds to a low-level idle state. This mode may also be enabled by setting TIMx_ENCMCTRL.ENCMD to “1011”.
- 1111：Dual-pulse encoding mode 1 updates the counter on a single clock edge based on the CC1P and CC2P bit values. CCxP = 0 corresponds to a falling edge and high logic state, while CCxP = 1 corresponds to a rising edge and low logic state. This mode may also be enabled by setting TIMx_ENCMCTRL.ENCMD to “1010”.

The table below describes the relationship between the counting direction and the encoder signal and polarity settings.

Table 14-2 The relationship between counting direction and encoder signal and polarity settings

Dual-pulse coding mode	SMSEL[3:0]	Relative signal levels (TI1FP1 corresponds to TI2, TI2FP2 corresponds to TI1)	TI1FP1 Signal		TI2FP2 Signal	
			Rise	Fall	Rise	Fall
Mode2	1000	High	count down	count down	count up	count up

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CCxP=0		Low	Not counted	Not counted	Not counted	Not counted
Mode2 CCxP=1	1000	High	Not counted	Not counted	Not counted	Not counted
		Low	count down	count down	count up	count up
Mode1 CCxP=0	1111	High	Not counted	count down	Not counted	count up
		Low	Not counted	Not counted	Not counted	Not counted
Mode1 CCxP=1	1111	High	Not counted	Not counted	Not counted	Not counted
		Low	count down	Not counted	count up	Not counted

The diagram below illustrates the counting method of a dual-pulse-coded mode counter.

Figure 14-32 Dual-pulse coding mode (CC1P = CC2P = 0)

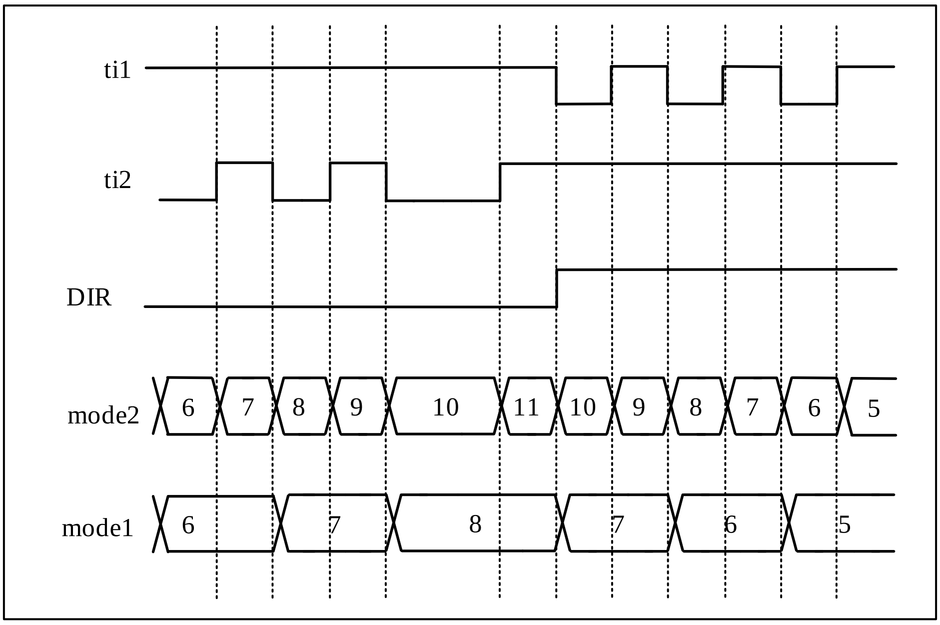

Figure 14-33 Dual-pulse coding mode (CC1P = CC2P = 1)

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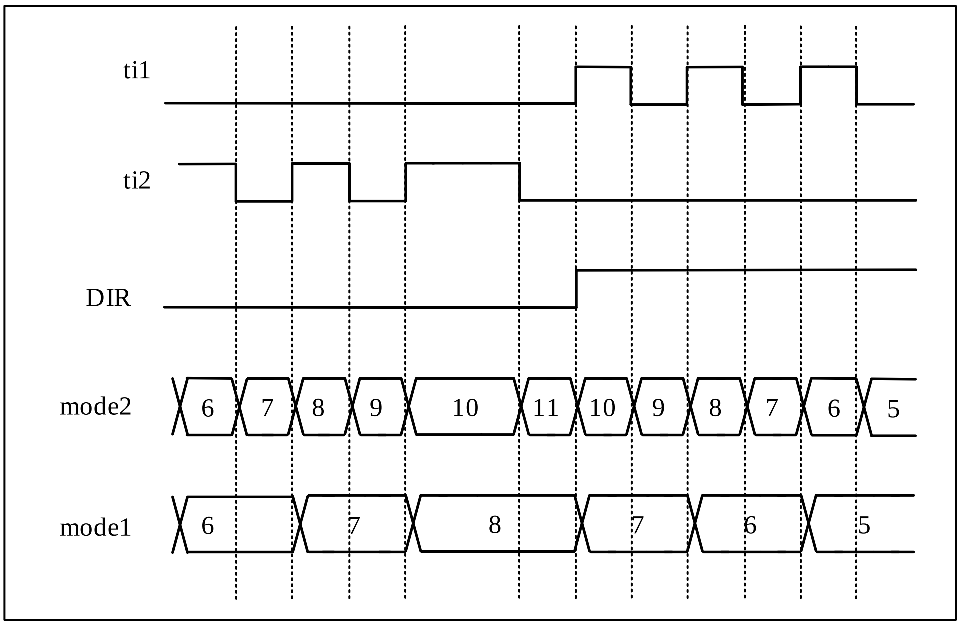

14.3.16.4 CCW/CW coding mode

CCW/CW Encoding mode: the counter increments upon a T1 edge transition and decrements upon a T2 edge transition. The counter may be configured to change state only on rising edges or on both rising and falling edges.

This mode is enabled via the ENCMD [3:0] bit field within the TIMx_ENCMCTRL register, as detailed below.

- 1001：CCW/CW encoding mode 2: The counter increments on both the rising and falling edges of TI1, and decrements on both the rising and falling edges of TI2.
- 1000：CCW/CW encoding mode 1: The counter increments on the rising edge of TI1 and decrements on the rising edge of TI2. The edge polarity of TI1 and TI2 can be selected via CCxP.

Table 14-3 The relationship between counting direction and encoder signal and polarity settings

Counting mode	ENCMD[3:0]	Transitional state			
		TI1 rising edge	TI1 falling edge	TI2 rising edge	TI2 falling edge
CCW/CW Encoding Mode1	1000	count up	Not counted	count down	Not counted
CCW/CW Encoding Mode2	1001	count up	count up	count down	count down

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Figure 14-34 CCW/CW Encoding Mode 2

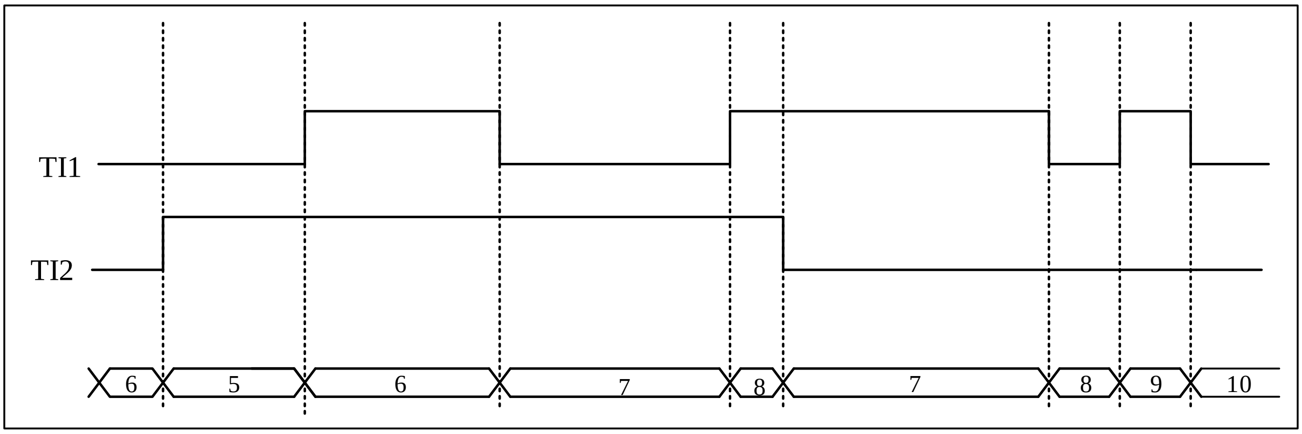
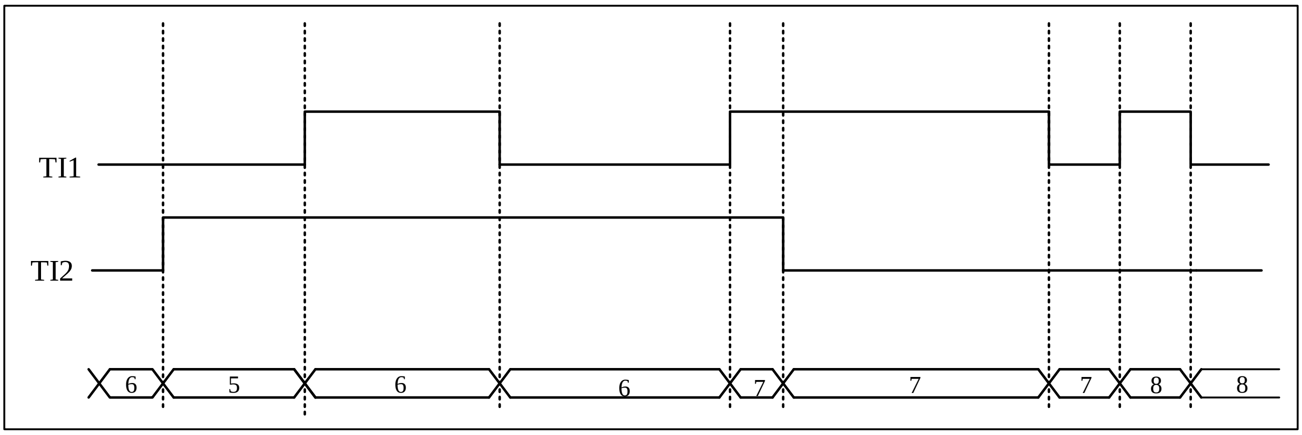


Figure 14-35 CCW/CW Encoding Mode 1（CC1P=CC2P=0）



14.3.16.5 Encoder Z-axis signal

The encoder generates one pulse per revolution, termed the zero pulse or reference pulse (i.e. the Z-phase signal). This zero pulse serves to determine the zero position or reference position. The encoder's Z-phase signal may be connected to the TI3 event to enable TI3 event-triggered loading functionality and TI3 event-triggered differential capture functionality. Refer to the TI3 event triggering functionality section for details.Please refer to Section TI3 Event Trigger Function.

14.3.17 Interface with Hall Effect Sensor

Please refer to Section 12.3.21.

14.4 TIMx Register Description (x=4)

For abbreviations used in the registers, please refer to Section 1.1.

These peripheral registers can be operated as half-word (16 bits) or word (32 bits).

14.4.1 Register Overview

Table 14-4 Register Overview

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Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
000h	TIM_CTRL1	Reserve															C1SEL	Reserve		CLRSEL	Reserve			ARPEN	ONEPM	Reserve		UPDIS	UPRS	CAMSEL[1:0]		DIR	CNTEN
004h	TIM_CTRL2	Reserve												T1SEL	Reserve	CCDSEL	Reserve		MMSEL[2:0]			Reserve											
008h	TIM_STS	Reserve													TITF	Reserve	UDITF	Reserve					CC3OCF	CC2OCF	CC1OCF	C3LDCNTITF	Reserve				CC3ITF	CC2ITF	CC1ITF
00Ch	TIM_EVTGEN	Reserve																					TGN	Reserve	UDGN	Reserve					CC3GN	CC2GN	CC1GN
010h	TIM_SMCTRL	Reserve															MSMD	EXTF[3:0]				EXTP	EXCEN	EXTPS[1:0]		SMSEL[3:0]				Reserve	TSEL[2:0]		
014h	TIM_DINTEN	Reserve										TDEN	Reserve	UDEN	Reserve	TIEN	UIEN	Reserve					CC3DEN	CC2DEN	CC1DEN	C3RSTCNTIEN	Reserve				CC3IEN	CC2IEN	CC1IEN
018h	TIM_CCMOD1_OUT	Reserve																OC2MD[2:0]			OC2CEN	OC2FEN	OC2PEN	CC2SEL[1:0]		OC1MD[2:0]			OC1CEN	OC2FEN	OC1PEN	CC1SEL[1:0]	
	TIM_CCMOD1_IN	Reserve																IC2F[3:0]				IC2PSC[1:0]		CC2SEL[1:0]		IC1F[3:0]				IC1PSC[1:0]		CC1SEL[1:0]	
01Ch	TIM_CCMOD2_OUT	Reserve																OC4MD[2:0]			OC4CEN	OC4FEN	OC4PEN	CC4SEL[1:0]		OC3MD[2:0]			OC3CEN	OC3FEN	OC3PEN	CC3SEL[1:0]	
	TIM_CCMOD2_IN	Reserve																								IC3F[3:0]				IC3PSC[1:0]		CC3SEL[1:0]	
024h	TIM_CCEN	Reserve																				CC3P	CC3EN	Reserve		CC2P	CC2EN	Reserve		CC1P	CC1EN	Reserve	
028h	TIM_CCDAT1	CCDAT1[31:0]																															
02Ch	TIM_CCDAT2	CCDAT2[31:0]																															
030h	TIM_CCDAT3	CCDAT3[31:0]																															
040h	TIM_PSC	Reserve																PSC[15:0]															
044h	TIM_AR	AR[31:0]																															
048h	TIM_CNT	CNT[31:0]																															
064h	TIM_C1FILT	Reserve		THRESH[5:0]						Reserve	WSIZE[5:0]						FILTEN	Reserve															
068h	TIM_C2FILT	Reserve		THRESH[5:0]						Reserve	WSIZE[5:0]						FILTEN	Reserve															
06Ch	TIM_C3FILT	Reserve		THRESH[5:0]						Reserve	WSIZE[5:0]						FILTEN	Reserve															
074h	TIM_FILTO	Reserve																													C3FILTO	C2FILTO	C1FILTO
088h	TIM_ENCDAT	ENCDAT[31:0]																															

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08Ch	TIM_ENCMCTRL	ENCDATS	Reserve	ENCMD[3:0]	C3LDCNTSEL[1:0]	C3LDCNTEN
090h	TIM_ENCLVR	LVR[31:0]				
094h	TIM_DCTRL	Reserve	DBADDR[5:0]	Reserve	DBLEN[5:0]	
098h	TIM_DADDR	BURST[31:0]				

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14.4.2 Control Register 1 (TIMx_CTRL1)

Offset address：0x00

Reset value：0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															C1SEL
															rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved		CLRSEL	Reserved			ARPEN	ONEPM	Reserved		UPDIS	UPRS	CAMSEL[1:0]		DIR	CNTEN
		rw				rw	rw			rw	rw	rw		rw	rw

Bit Field	Name	Description
31:17	Reserved	Reserved, the reset value must be maintained
16	C1SEL	Channel 1 Selection 0: Select the external CH1 (from IOM) signal. 1: Select internal CH1 (from COMP) signal.
15:14	Reserved	Reserved, the reset value must be maintained
13	CLRSEL	OcxRef Clear Selection 0: Select the external Ocxclr (ETR) signal 1: Select the internal Ocxclr (from COMP) signal
12:10	Reserved	Reserved, the reset value must be maintained
9	ARPEN	Auto-reload preload enable 0: Shadow register disable for TIMx_AR register 1: Shadow register enable for TIMx_AR register
8	ONEPM	One-pulse mode 0: Disable one-pulse mode, the counter counts are not affected when an update event occurs。 1: Enable one-pulse mode, the counter stops counting when the next update event occurs
7:6	Reserved	Reserved, the reset value must be maintained
5	UPDIS	Update disable This bit is used to enable/disable the Update event (UEV) events generation by software. 0: Enable UEV. And UEV will be generated if one of following condition been fulfilled: – Counter overflow/underflow – The TIMx_EVTGEN.UDGN bit is set – Update generation from the slave mode controller Shadow registers will update with preload value. 1: UEV disabled. No update event is generated, and the shadow registers (AR, PSC,

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Bit Field	Name	Description
		and CCDATx) keep their values. If the TIMx_EVTGEN.UDGN bit is set or a hardware reset is issued by the slave mode controller, the counter and prescaler are reinitialized.
4	UPRS	Update request source This bit is used to select the UEV event sources by software. 0: If update interrupt or DMA request is enabled, any of the following events will generate an update interrupt or DMA request – Counter overflow/underflow – TIMx_EVTGEN.UDGN bit is set – Update generation from the slave mode controller 1: If update interrupt or DMA request is enabled, only counter overflow/underflow will generate update interrupt or DMA request
3:2	CAMSEL[1:0]	Center-aligned mode selection 00: Edge-aligned mode. TIMx_CTRL1.DIR specifies up-counting or down-counting。 01: Center-aligned mode 1. The counter counts in center-aligned mode, and the output compare interrupt flag bit is set to 1 when down-counting。 10: Center-aligned mode 2. The counter counts in center-aligned mode, and the output compare interrupt flag bit is set to 1 when up-counting。 11: Center-aligned mode 3. The counter counts in center-aligned mode, and the output compare interrupt flag bit is set to 1 when up-counting or down-counting。 *Note: Switching from edge-aligned mode to center-aligned mode is not allowed when the counter is still enabled (TIMx_CTRL1.CNTEN = 1)*
1	DIR	Direction 0: Up-counting 1: Down-counting *Note: This bit is read-only when the counter is configured in center-aligned mode or encoder mode.*
0	CNTEN	Counter enable 0: Disable counter 1: Enable counter *Note: external clock, gating mode and encoder mode can only work after TIMx_CTRL1.CNTEN bit is set in the software. Trigger mode can automatically set TIMx_CTRL1.CNTEN bit by hardware.* *Note: After setting the CNTEN bit in the software, it is necessary to wait for at least two TIMx_CLK cycles for the CNTEN synchronisation from TIMx_PCLK to TIMx_CLK to take effect.*

14.4.3 Control Register 2 (TIMx_CTRL2)

Offset address: 0x04

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

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Reserved												TI1SEL	Reserved	CCDSEL	Reserved
												rw		rw	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MMSEL[3:0]				Reserved					OI4	Reserved	OI3	Reserved			
rw									rw		rw				

Bit Field	Name	Description
31:20	Reserved	Reserved, the reset value must be maintained
19	TI1SEL	TI1 selection 0: TIMx_CH1 pin connected to TI1 input; 1: TIMx_CH1, TIMx_CH2, and TIMx_CH3 pins are XOR connected to the TI1 input.
18	Reserved	Reserved, the reset value must be maintained
17	CCDSEL	Capture/compare DMA selection 0: When a CCx event occurs, a DMA request for CCx is sent； 1: When an update event occurs, a DMA request for CCx is sent.
16	Reserved	Reserved, the reset value must be maintained
15:12	MMSEL[3:0]	Master Mode Selection These 4 bits (TIMx_CTRL2. MMSEL [3:0]) are used to select the synchronization information (TRGO) sent to the slave timer in the master mode. Possible combinations are as follows： x000: Reset –When the TIMx_EVTGEN.UDGN is set or a reset is generated by the slave mode controller, a TRGO pulse occurs. And in the later case, the signal on TRGO is delayed compared to the actual reset. x001: Enable - The TIMx_CTRL1.CNTEN bit is used as the trigger output (TRGO). Sometimes you need to start multiple timers at the same time or enable slave timer for a period of time. The counter enable signal is set when TIMx_CTRL1.CNTEN bit is set or the trigger input in gated mode is high. When the counter enable signal is controlled by the trigger input, there is a delay on TRGO except if the master/slave mode is selected (see the description of the TIMx_SMCTRL.MSMD bit). x010: Update - The update event is selected as the trigger output (TRGO). For example, a master timer clock can be used as a slave timer prescaler. x011: Compare pulse - Triggers the output to send a positive pulse (TRGO) when the TIMx_STS.CC1ITF is to be set (even if it is already high), when a capture or a comparison succeeds. x100: Compare - OC1REF signal is used as the trigger output (TRGO). x101: Compare - OC2REF signal is used as the trigger output (TRGO). x110: Compare - OC3REF signal is used as the trigger output (TRGO). Other: Reserved.
11:0	Reserved	Reserved, the reset value must be maintained

14.4.4 Status Registers (TIMx_STS)

Offset address: 0x08

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Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved													TITF	Reserved	UDITF
													rc_w0		rc_w0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved					CC3OCF	CC2OCF	CC1OCF	C3LDCNTITF	Reserved				CC3ITF	CC2ITF	CC1ITF
					rc_w0	rc_w0	rc_w0	rc_w0					rc_w0	rc_w0	rc_w0

Bit Field	Name	Description
31:19	Reserved	Reserved, the reset value must be maintained
18	TITF	Trigger interrupt flag This bit is set by hardware when an active edge is detected on the TRGI input when the slave mode controller is in a mode other than gated. This bit is set by hardware when any edge in gated mode is detected. This bit is cleared by software. 0: No trigger event occurred； 1: Trigger interrupt occurred.
17	Reserved	Reserved, the reset value must be maintained
16	UDITF	Update interrupt flag This bit is set by hardware when an update event occurs under the following conditions： –When TIMx_CTRL1.UPDIS = 0, and repetition counter value overflow or underflow (when repetition counter equal to 0 an update event is generated). – When TIMx_CTRL1.UPRS = 0, TIMx_CTRL1.UPDIS = 0, and set the TIMx_EVTGEN.UDGN bit by software to reinitialize the CNT. –When TIMx_CTRL1.UPRS = 0, TIMx_CTRL1.UPDIS = 0, and the counter CNT is reinitialized by the trigger event. (See TIMx_SMCTRL Register description) This bit is cleared by software. 0: No update event occurred 1: Update interrupt occurred
15:11	Reserved	Reserved, the reset value must be maintained
10	CC3OCF	Capture/Compare 3 overcapture flag See TIMx_STS.CC1OCF description.
9	CC2OCF	Capture/Compare 2 overcapture flag See TIMx_STS.CC1OCF description.
8	CC1OCF	Capture/Compare 1 overcapture flag This bit is set by hardware only when the corresponding channel is configured in input capture mode. Cleared by software writing 0. 0: No overcapture occurred; 1: TIMx_STS.CC1ITF was already set when the value of the counter has been captured in the TIMx_CCDAT1 register.
7	C3LDCNTITF	TI3 valid event trigger counter loaded with LVR value interrupt flag 0: No occurrence of TI3 valid event trigger counter loaded with LVR value 1: Occurrence of TI3 valid event trigger counter loaded with LVR value

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Bit Field	Name	Description
6:3	Reserved	Reserved, the reset value must be maintained.
2	CC3ITF	Capture/Compare 3 interrupt flag See TIMx_STS.CC1ITF description.
1	CC2ITF	Capture/Compare 2 interrupt flag See TIMx_STS.CC1ITF description.
0	CC1ITF	Capture/Compare 1 interrupt flag **When the corresponding channel of CC1 is in output mode:** Except in center-aligned mode, this bit is set by hardware when the counter value is the same as the compare value (see TIMx_CTRL1.CAMSEL bit description). This bit is cleared by software. 0: No match occurred. 1: The value of TIMx_CNT is the same as the value of TIMx_CCDAT1. When the value of TIMx_CCDAT1 is greater than the value of TIMx_AR, the TIMx_STS.CC1ITF bit will go high if the counter overflows (in up-counting and up/down-counting modes) and underflows in down-counting mode. **When the corresponding channel of CC1 is in input mode:** This bit is set by hardware when the capture event occurs. This bit is cleared by software or by reading TIMx_CCDAT1. 0: No input capture occurred. 1: Input capture occurred. Counter value has captured in the TIMx_CCDAT1. An edge with the same polarity as selected has been detected on IC1.

14.4.5 Event Generation Registers (TIMx_EVTGEN)

Offset address: 0x0C

Reset values: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved					TGN	Reserved	UDGN	Reserved					CC3GN	CC2GN	CC1GN
					w		w					w	w	w	w

Bit Field	Name	Description
31:11	Reserved	Reserved, the reset value must be maintained
10	TGN	Trigger generation This bit can generate a trigger event when set by software. And at this time TIMx_STS.TITF = 1, if the corresponding interrupt and DMA are enabled, the corresponding interrupt and DMA will be generated. This bit is automatically cleared by hardware. 0: No action No action 1: Generated a trigger event

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Bit Field	Name	Description
9	Reserved	Reserved, the reset value must be maintained
8	UDGN	Update generation This bit can generate an update event when set by software. And at this time the counter will be reinitialized, the prescaler counter will be cleared, the counter will be cleared in center-aligned or up-counting mode, but take TIMx_AR in down-counting mode the value of the register. This bit is automatically cleared by hardware. 0: No action 1: Generated an update event
7:3	Reserved	Reserved, the reset value must be maintained
2	CC3GN	Capture/Compare 3 generation See TIMx_EVTGEN.CC1GN description.
1	CC2GN	Capture/Compare 2 generation See TIMx_EVTGEN.CC1GN description.
0	CC1GN	Capture/Compare 1 generation This bit can generate a capture/compare event when set by software. This bit is automatically cleared by hardware. **When the corresponding channel of CC1 is in output mode:** The TIMx_STS.CC1ITF flag will be pulled high, if the corresponding interrupt and DMA are enabled, the corresponding interrupt and DMA will be generated. **When the corresponding channel of CC1 is in input mode:** TIMx_CCDAT1 will capture the current counter value, and the TIMx_STS.CC1ITF flag will be pulled high, if the corresponding interrupt and DMA are enabled, the corresponding interrupt and DMA will be generated. If The IMx_STS.CC1ITF is already pulled high, pull TIMx_STS.CC1OCF high. 0: No action 1: Generated a CC1 capture/compare event

14.4.6 Slave Mode Control Register (TIMx_SMCTRL)

Offset address: 0x10

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															MSMD
															rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EXTF[3:0]				EXTP	EXCEN	EXTPS[1:0]		Reserved	SMSEL[2:0]			Reserved	TSEL[2:0]		
rw				rw	rw	rw			rw				rw		

Bit Field	Name	Description
31:17	Reserved	Reserved, the reset value must be maintained
16	MSMD	Master/slave mode

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Bit Field	Name	Description
		0: No effect; 1: The event on the trigger input (TRGI) is delayed to allow perfect synchronization between the current timer (via TRGO) and its slave timers. This is very useful for cases where multiple timers need to be synchronized to a single external event.
15:12	EXTF[3:0]	External trigger filter These bits define the length of the ETRP digital filter (the RCC_TIMFILTCFG.TIM4FILTCLK[4:0] register determines the sampling frequency of the corresponding digital filter). The digital filter consists of an event counter which generates an output transition after recording N events: 0000：No filter, sampled using TIM's internal operating clock 0001：N=1 0010：N=2 0011：N=3 0100：N=4 0101：N=5 0110：N=6 0111：N=7 1xxx：N=8
11	EXTP	External trigger polarity This bit is used to select whether the trigger operation is to use tim_etr_in or the inversion of tim_etr_in. 0: tim_etr_in active at high level or rising edge. 1: tim_etr_in active at low level or falling edge.
10	EXCEN	External clock enable This bit is used to enable external clock mode 2, and the counter is driven by any active edge on the ETRF signal in this mode. 0: External clock mode 2 disable. 1: External clock mode 2 enable. *Note1: When external clock mode 1 and external clock mode 2 are enabled at the same time, the input of the external clock is ETRF.* *Note2: The following slave modes can be used simultaneously with external clock mode 2: reset mode, gated mode and trigger mode; However, TRGI cannot connect to ETRF (TIMx_SMCTRL.TSEL ≠ '111').* *Note3: Setting the TIMx_SMCTRL.EXCEN bit has the same effect as selecting external clock mode 1 and connecting TRGI to ETRF (TIMx_SMCTRL.SMSEL = 0111 and TIMx_SMCTRL.TSEL = 111).*
9:8	EXTPS[1:0]	External trigger prescaler The frequency of the external trigger signal ETRP must be at most 1/4 of TIMxCLK frequency. When a faster external clock is input, a prescaler can be used to reduce the frequency of ETRP. 00: Prescaler disable 01: ETRP frequency divided by 2 10: ETRP frequency divided by 4 11: ETRP frequency divided by 8

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Bit Field	Name	Description
7:4	SMSEL[2:0]	Slave mode selection When an external signal is selected, the active edge of the trigger signal (TRGI) is linked to the selected external input polarity (see input control register and control register description) 0000: Disable slave mode. If TIMx_CTRL1.CNTEN = 1, the prescaler is driven directly by the internal clock. 0001: Encoder mode 1. According to the level of TI2FP2, the counter up-counting or down-counting on the edge of TI1FP1。 0010: Encoder mode 2. According to the level of TI1FP1, the counter up-counting or down-counting on the edge of TI2FP2. 0011: Encoder mode 3. According to the input level of another signal, the counter up-counting or down-counting on the edges of TI2FP1 and TI2FP2 0100: Reset mode. On the rising edge of the selected trigger input (TRGI), the counter is reinitialized and the shadow register is updated 0101: Gated mode. When the trigger input (TRGI) is high, the clock of the counter is enabled. Once the trigger input becomes low, the counter stops counting, but is not reset. In this mode, the start and stop of the counter are controlled 0110: Trigger mode. When a rising edge occurs on the trigger input (TRGI), the counter is started but not reset. In this mode, only the start of the counter is controlled. 0111: External clock mode 1. The counter is clocked by the rising edge of the selected trigger input (TRGI). 1000：Dual-pulse coding mode 2. 1001：Orthogonal Encoder Mode 4 – Based on the level of TI2FP2, the counter increments/decrements on the rising/falling edge of TI1FP1. The counting edge is selected via CC1P. 1010：Orthogonal Encoder Mode 5 – Based on the level of TI1FP1, the counter increments/decrements on the rising/falling edge of TI2FP2. The counting edge is selected via CC2P. 1011：Pulse Level Modulation Mode 2. 1100：Pulse level encoding mode 1. Set the counting edge of TI2FP2 via CC2P. 1101：Reserved. 1110：Reserved. 1111： Dual-pulse encoding mode 1. Configure the count-sensitive edges for TI1FP1 and TI2FP2 via CC1P and CC2P. *Note: Do not use gated mode if TI1F_ED is selected as the trigger input (TIMx_SMCTRL.TSEL=100). This is because TI1F_ED outputs a pulse for each TI1F transition, whereas gated mode checks the level of the triggered input.*
3	Reserved	Reserved, the reset value must be maintained
2:0	TSEL[2:0]	Trigger selection These 3 bits are used to select the trigger input of the synchronous counter. 000: Internal trigger 0 (ITR0) 100: Edge detector for TI1 (TI1F_ED) 001: Internal trigger 1 (ITR1) 101: Filtered timer input 1 (TI1FP1) 010: Internal trigger 2 (ITR2) 110: Filtered timer input 2 (TI2FP2) 011: Internal trigger 3 (ITR3) 111: External trigger input (ETRF)

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Bit Field	Name	Description
		For further details regarding ITRx, see Table 14-5. *Note: These bits must be changed only when not in use (e. g. TIMx_SMCTRL.SMSEL=0000) to avoid false edge detection at the transition.* *Note: When enabling the external event (TRGI) trigger to load counter values, if output comparison mode is simultaneously employed, either ETRF or ITRx must be selected as the trigger source.*

Table 14-5 TIMx Internal Trigger Connection

Slave timer	ITR0 (TSEL = 000)	ITR1 (TSEL = 001)	ITR2 (TSEL = 010)	ITR3 (TSEL = 011)
TIM1	TIM3	NA	NA	NA
TIM3	TIM1	NA	NA	NA
TIM4	NA	NA	NA	NA

14.4.7 DMA/Interrupt Enable Registers (TIMx_DINTEN)

Offset address: 0x14

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved										TDEN	Reserved	UDEN	Reserved	TIEN	UIEN
										rw		rw		rw	rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved					CC3DEN	CC2DEN	CC1DEN	C3LDCNTIEN	Reserved				CC3IEN	CC2IEN	CC1IEN
				rw	rw	rw	rw					rw	rw	rw	rw

Bit Field	Name	Description
31:22	Reserved	Reserved, the reset value must be maintained
21	TDEN	Trigger DMA request enable 0: Disable trigger DMA request. 1: Enable trigger DMA request
20	Reserved	Reserved, the reset value must be maintained
19	UDEN	Update DMA request enable 0: Disable update DMA request. 1: Enable update DMA request
18	Reserved	Reserved, the reset value must be maintained
17	TIEN	Trigger interrupt enable 0: Disable trigger interrupt 1: Enable trigger interrupt
16	UIEN	Update interrupt enable 0: Disable update interrupt

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Bit Field	Name	Description
		1: Enables update interrupt
15:12	Reserved	Reserved, the reset value must be maintained
10	CC3DEN	Capture/Compare 3 DMA request enable 0: Disable capture/compare 3 DMA request 1: Enable capture/compare 3 DMA request
9	CC2DEN	Capture/Compare 2 DMA request enable 0: Disable capture/compare 2 DMA request 1: Enable capture/compare 2 DMA request
8	CC1DEN	Capture/Compare 1 DMA request enable 0: Disable capture/compare 1 DMA request 1: Enable capture/compare 1 DMA request
7	C3LDCNTIEN	Enable TI3 active event to trigger counter loading as LVR value interrupt 0: Disable TI3 active event to trigger counter loading as LVR value interrupt 1: Enable TI3 active event to trigger counter loading as LVR value interrupt
6:3	Reserved	Reserved, the reset value must be maintained
2	CC3IEN	Capture/Compare 3 interrupt enable 0: Disable capture/compare 3 interrupt 1: Enable capture/compare 3 interrupts
1	CC2IEN	Capture/Compare 2 interrupt enable 0: Disable capture/compare 2 interrupt 1: Enables capture/compare 2 interrupts
0	CC1IEN	Capture/Compare 1 interrupt enable 0: Disable capture/compare 1 interrupt 1: Enables capture/comparing 1 interrupt

14.4.8 Capture/Compare Mode Register 1 (TIMx_CCMOD1)

Offset address: 0x18

Reset value: 0x0000 0000

Channels can be used for input (capture mode) or output (compare mode), and the direction of the channel is defined by the corresponding CCxSEL bit. The other bits of the register act differently in input and output modes. OCx describes the function of a channel in output mode, ICx describes the function of a channel in input mode. Hence, please note that the same bit can have different meanings for output mode and for input mode.

Output compare mode:

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OC2MD[2:0]			OC2CEN	OC2FEN	OC2PEN	CC2SEL[1:0]		OC1MD[2:0]			OC1CEN	OC1FEN	OC1PEN	CC1SEL[1:0]	
rw			rw	rw	rw	rw		rw			rw	rw	rw	rw	

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Bit Field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained
15:13	OC2MD[2:0]	Output Compare 2 mode
12	OC2CEN	Output Compare 2 clear enable
11	OC2FEN	Output Compare 2 fast enable
10	OC2PEN	Output Compare 2 preload enable
9:8	CC2SEL[1:0]	Capture/Compare 2 selection These bits are used to select the input/output and input mapping of the channel 00: CC2 channel is configured as output. 01: CC2 channel is configured as input, IC2 is mapped on TI2 10: CC2 channel is configured as input, IC2 is mapped on TI1 11: CC2 channel is configured as input, IC2 is mapped on TRC. This mode is only active when the internal trigger input is selected by TIMx_SMCTRL.TSEL. *Note: CC2SEL is writable only when the channel is off (TIMx_CCEN.CC2EN = 0).*
7:5	OC1MD[2:0]	Output Compare 1 mode These bits are used to manage the output reference signal OC1REF, which determines the values of OC1 and OC1N, and is valid at high levels, while the active levels of OC1 and OC1N depend on the TIMx_CCEN.CC1P and TIMx_CCEN.CC1NP bits. 000: Frozen. Comparison between TIMx_CCDAT1 register and counter TIMx_CNT has no effect on OC1REF signal. 001: Set channel 1 to the active level on match. When TIMx_CCDAT1 = TIMx_CNT, OC1REF signal will be forced high. 010: Set channel 1 as inactive level on match. When TIMx_CCDAT1 = TIMx_CNT, OC1REF signal will be forced low. 011: Toggle. When TIMx_CCDAT1 = TIMx_CNT, OC1REF signal will be toggled. 100: Force to inactive level. OC1REF signal is forced low. 101: Force to active level. OC1REF signal is forced high. 110: PWM mode 1 - In up-counting mode, if TIMx_CNT < TIMx_CCDAT1, OC1REF signal of channel 1 is high, otherwise it is low. In down-counting mode, if TIMx_CNT > TIMx_CCDAT1, OC1REF signal of channel 1 is low, otherwise it is high. 111: PWM mode 2 - In up-counting mode, if TIMx_CNT < TIMx_CCDAT1, OC1REF signal of channel 1 is low, otherwise it is high. In down-counting mode, if TIMx_CNT > TIMx_CCDAT1, OC1REF signal of channel 1 is high, otherwise it is low. *Note 1: In PWM mode 1 or PWM mode 2, the OC1REF level changes only when the comparison result changes or when the output compare mode is switched from frozen mode to PWM mode.*
4	OC1CEN	Output Compare 1 clear enable 0: OC1REF is not affected by tim_ocref_clr_in input level. 1: OC1REF is cleared immediately when the tim_ocref_clr_in input level is detected as high (the source of tim_ocref_clr_in is controlled by TIMx_CTRL1.CLRSEL).
3	OC1FEN	Output Compare 1 fast enable This bit is used to speed up the response of the CC output to the trigger input event. 0: CC1 behaves normally depending on the counter and CCDAT1 values, even if the trigger is

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Bit Field	Name	Description
		ON. The minimum delay for activating CC1 output when an edge occurs on the trigger input is 5 clock cycles 1: An active edge of the trigger input acts like a comparison match on CC1 output. Therefore, OC is set to the comparison level regardless of the comparison result. The delay time for sampling the trigger input and activating the CC1 output is reduced to 3 clock cycles. OCxFEN only works if the channel is configured in PWM1 or PWM2 mode.
2	OC1PEN	Output Compare 1 preload enable 0: Disable preload function of TIMx_CCDAT1 register. Supports write operations to TIMx_CCDAT1 register at any time, and the written value is effective immediately. 1: Enable preload function of TIMx_CCDAT1 register. Only read and write operations to preload registers. When an update event occurs, the value of TIMx_CCDAT1 is loaded into the active register. *Note 1: Only when TIMx_CTRL1.ONEPM = 1(In one-pulse mode), PWM mode can be used without verifying the preload register, otherwise no other behavior can be predicted.*
1:0	CC1SEL[1:0]	Capture/Compare 1 selection These bits are used to select the input/output and input mapping of the channel 00: CC1 channel is configured as output. 01: CC1 channel is configured as input, IC1 is mapped on TI1. 10: CC1 channel is configured as input, IC1 is mapped on TI2 11: CC1 channels are configured as inputs and IC1 is mapped to TRC. This mode is only active when the internal trigger input is selected by TIMx_SMCTRL.TSEL. *Note: CC1SEL is writable only when the channel is off (TIMx_CCEN.CC1EN = 0).*

Iutput capture mode:

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IC2F[3:0]				IC2PSC[1:0]		CC2SEL[1:0]		IC1F[3:0]				IC1PSC[1:0]		CC1SEL[1:0]	
rw				rw		rw		rw				rw		rw	

Bit Field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained
15:12	IC2F[3:0]	Input capture 2 filter
11:10	IC2PSC[1:0]	Input capture 2 prescaler
9:8	CC2SEL[1:0]	Capture/Compare 2 selection These bits are used to select the input/output and input mapping of the channel: 00: CC2 channel is configured as output 01: CC2 channel is configured as input, IC2 is mapped on TI2 10: CC2 channel is configured as input, IC2 is mapped on TI1 11: CC2 channel is configured as input, IC2 is mapped on TRC. This mode is only active

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Bit Field	Name	Description
		when the internal trigger input is selected by TIMx_SMCTRL.TSEL. *Note: CC2SEL is writable only when the channel is off (TIMx_CCEN.CC2EN = 0).*
7:4	IC1F[3:0]	Input capture 1 filter These bits define the length of the ETRP digital filter (the RCC_TIMFILTCFG.TIM4FILTCLK[4:0] register determines the sampling frequency of the corresponding digital filter). The digital filter consists of an event counter which generates an output transition after recording N events: 0000：No filter, sampled using TIM's internal operating clock 0001：N=1 0010：N=2 0011：N=3 0100：N=4 0101：N=5 0110：N=6 0111：N=7 1xxx：N=8
3:2	IC1PSC[1:0]	Input capture 1 prescaler These bits are used to select the ratio of the prescaler for IC1 (CC1 input). When TIMx_CCEN.CC1EN = 0, the prescaler will be reset. 00: No prescaler, capture is done each time an edge is detected on the capture input 01: Capture is done once every 2 events 10: Capture is done once every 4 events 11: Capture is done once every 8 events
1:0	CC1SEL[1:0]	Capture/Compare 1 Selection These bits are used to select the input/output and input mapping of the channel 00: CC1 channel is configured as output 01: CC1 channel is configured as input, IC1 is mapped on TI1 10: CC1 channel is configured as input, IC1 is mapped on TI2 11: CC1 channel is configured as input, IC1 is mapped to TRC. This mode is only active when the internal trigger input is selected by TIMx_SMCTRL.TSEL. *Note: CC1SEL is writable only when the channel is off (TIMx_CCEN.CC1EN = 0).*

14.4.9 Capture/Compare Mode Register 2 (TIMx_CCMOD2)

Offset address: 0x1C

Reset value: 0x0000 0000

See the description of the CCMOD1 register above

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								OC3MD[2:0]			OC3CEN	OC3FEN	OC3PEN	CC3SEL[1:0]	

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rw	rw	rw	rw	rw

Output comparison mode:

Bit Field	Name	Description
31:8	Reserved	Reserved, the reset value must be maintained
7:5	OC3MD[2:0]	Output compare 3 mode
4	OC3CEN	Output compare 3 clear enable
3	OC3FEN	Output compare 3 fast enable
2	OC3PEN	Output compare 3 preload enable
1:0	CC3SEL[1:0]	Capture/Compare 3 selection These bits are used to select the input/output and input mapping of the channel 00: CC3 channel is configured as output 01: CC3 channel is configured as input, IC3 is mapped to TI3 10: Reserved 11: CC3 channel is configured as input, IC3 is mapped to TRC. This mode is only active when the internal trigger input is selected by TIMx_SMCTRL.TSEL. *Note: CC3SEL is writable only when the channel is off (TIMx_CCEN.CC3EN = 0).*

Input capture mode:

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								IC3F[3:0]				IC3PSC[1:0]		CC3SEL[1:0]	
								rw				rw		rw	

Bit Field	Name	Description
31:8	Reserved	Reserved, the reset value must be maintained
7:4	IC3F[3:0]	Input capture 3 filter
3:2	IC3PSC[1:0]	Input capture 3 prescaler
1:0	CC3SEL[1:0]	Capture/compare 3 selection These bits are used to select the input/output and input mapping of the channel 00: CC3 channel is configured as output 01: CC3 channel is configured as input, IC3 is mapped to TI3 10: CC3 channel is configured as input, IC3 is mapped on TI4 11: CC3 channel is configured as input, IC3 is mapped to TRC. This mode is only active when the internal trigger input is selected by TIMx_SMCTRL.TSEL. *Note: CC3SEL is writable only when the channel is off (TIMx_CCEN.CC3EN = 0).*

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14.4.10 Capture/Compare Enable Registers (TIMx_CCEN)

Offset address: 0x24

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved				CC3P	CC3EN	Reserved		CC2P	CC2EN	Reserved		CC1P	CC1EN	Reserved	
rw	rw			rw	rw			rw	rw			rw	rw		

Bit Field	Name	Description
31:12	Reserved	Reserved, the reset value must be maintained.
11	CC3P	Capture/Compare 3 output polarity See TIMx_CCEN.CC1P description.
10	CC3EN	Capture/Compare 3 output enabl） See TIMx_CCEN.CC1EN description.
9:8	Reserved	Reserved, the reset value must be maintained.
7	CC2P	Capture/Compare 2 output polarity See TIMx_CCEN.CC1P description.
6	CC2EN	Capture/Compare 2 output enable See TIMx_CCEN.CC1EN description.
5:4	Reserved	Reserved, the reset value must be maintained.
3	CC1P	Capture/Compare 1 output polarity **When the corresponding channel of CC1 is in output mode:** 0: OC1 active high 1: OC1 active low **When the corresponding channel of CC1 is in input mode:** At this time, this bit is used to select whether IC1 or the inverse signal of IC1 is used as the trigger or capture signal. 0: non-inverted: Capture action occurs when IC1 generates a rising edge. When used as external trigger, IC1 is non-inverted. 1: inverted: Capture action occurs when IC1 generates a falling edge. When used as external trigger, IC1 is inverted.
2	CC1EN	Capture/Compare 1 output enable **When the corresponding channel of CC1 is in output mode:** 0: Disable - Disable output OC1 signal. Therefore, the output level of OC1 depends on the values of MOEN, OSSI, OSSR, OI1, OI1N, and CC1NEN bits. 1: Enable - Enable output OC1 signal. The OC1 signal is output to the corresponding output pin, and its output level depends on the values of the MOEN, OSSI, OSSR, OI1, OI1N, and CC1NEN bits. **When the corresponding channel of CC1 is in input mode:**

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Bit Field	Name	Description
		At this time, this bit is used to disable/enable the capture function. 0: Disable capture 1: Enable capture
1:0	Reserved	Reserved, the reset value must be maintained.

Table 14-6 Output Control Bits of Standard OCx Channel

CCxEN	OCx Output Status
0	Disable output (OCx=0)
1	OCx = OCxREF + polarity

Note: The state of external I/O pins connected to standard OCx channels depends on the OCx channel state and GPIO and AFIO registers.

14.4.11 Capture/Compare Register 1 (TIMx_CCDAT1)

Offset address: 0x28

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CCDAT1[31:0]															
rw															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CCDAT1[31:0]															
rw															

Bit Field	Name	Description
31:0	CCDAT1[31:0]	Capture/Compare 1 value CC1 channel is configured as output: CCDAT1 contains the value to be compared to the counter TIMx_CNT, signaling on the OC1 output. If the preload feature is not selected in TIMx_CCMOD1.OC1PEN bit, the written value is immediately transferred to the active register. Otherwise, this preloaded value is transferred to the active register only when an update event occurs. CC1 channel is configured as input: CCDAT1 contains the counter value transferred by the last input capture 1 event (IC1). When configured as input mode, register CCDAT1 is only readable. When configured as output mode, register CCDAT1 is readable and writable.

14.4.12 Capture/Compare Register 2 (TIMx_CCDAT2)

Offset address: 0x2C

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

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CCDAT2[31:0]
rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CCDAT2[31:0]															
rw															

Bit Field	Name	Description
31:0	CCDAT2[31:0]	Capture/Compare 2 value CC2 channel is configured as output: CCDAT2 contains the value to be compared to the counter TIMx_CNT, signaling on the OC2 output. If the preload feature is not selected in TIMx_CCMOD1.OC2PEN bit, the written value is immediately transferred to the active register. Otherwise, this preloaded value is transferred to the active register only when an update event occurs. CC2 channel is configured as input: CCDAT2 contains the counter value transferred by the last input capture 2 event (IC2). When configured as input mode, register CCDAT2 is only readable. When configured as output mode, register CCDAT2 is readable and writable.

14.4.13 Capture/Compare Register 3 (TIMx_CCDAT3)

Offset address: 0x30

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CCDAT3[31:0]															
rw															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CCDAT3[31:0]															
rw															

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Bit Field	Name	Description
31:0	CCDAT3[31:0]	Capture/Compare 3 value CC3 channel is configured as output: CCDAT3 contains the value to be compared to the counter TIMx_CNT, signaling on the OC3 output. If the preload feature is not selected in TIMx_CCMOD2.OC3PEN bit, the written value is immediately transferred to the active register. Otherwise, this preloaded value is transferred to the active register only when an update event occurs. CC3 channel is configured as input: CCDAT3 contains the counter value transferred by the last input capture 3 event (IC3). When configured as input mode, register CCDAT3 is only readable. When configured as output mode, register CCDAT3 is readable and writable.

14.4.14 Prescaler (TIMx_PSC)

Offset address: 0x40

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PSC[15:0]															
rw															

Bit Field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained.
15:0	PSC[15:0]	Prescaler value Counter clock $f_{CK\_CNT} = f_{CK\_PSC}/$ (PSC [15:0] +1). Each time an update event occurs, the PSC value is loaded into the active prescaler register.

14.4.15 Auto-reload Register (TIMx_AR)

Offset address: 0x44

Reset value: FFFF FFFF

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
AR[31:0]															
rw															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
AR[31:0]															
rw															

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Bit Field	Name	Description
31:0	AR[31:0]	Auto-reload value AR contains the value to be loaded into the actual auto-reload register. For details, refer to Section 12.3.1 Updates and Actions Concerning AR. When the auto-reload value is empty, the counter does not operate.

14.4.16 Counters (TIMx_CNT)

Offset address: 0x48

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CNT[31:0]															
rw															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CNT[31:0]															
rw															

Bit Field	Name	Description
31:0	CNT[31:0]	Counter value

14.4.17 Channel 1 Filter Register（TIMx_C1FILT）

Offset address: 0x64

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved		THRESH						Reserved	WSIZE						FILTEN
		rw							rw						rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved															

Bit field	Name	Description
31:30	Reserved	Reserved, the reset value must be maintained.
29:24	THRESH[5:0]	Threshold number of valid logic level samples, maximum 63: the threshold for valid logic levels. Within the sampling window, if the quantity of logic highs is greater than or equal to the threshold, the next logic level will be a logic high. The same rule applies to logic lows. If the quantity of high and low logic levels within the window is less than the threshold, the filter output remains unchanged. The threshold should be set to a value greater than or equal to half of the Window value Recommended threshold range: **Minimum value:** one additional pre-scaler clock period beyond the maximum glitch size limit (pre-scaler clock period), and must be greater than half of the window size.

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		For example, if the glitch size is 3.2 * (the pre-scaler clock period), then the threshold should be ┌3.2┐ = 4 + 1 =5 **Maximum value:** the lower limit of the minimum size of the valid signal (in pre-scaler clock periods), and must be less than the window size. For example, if the minimum signal size is 3.2 * (the pre-scaler clock period), then the threshold should be the lower limit (3.2) = 3.
23	Reserved	Reserved, the reset value must be maintained.
22:17	WSIZE[5:0]	Window size value for logic level checking, maximum 63: The window size determines how many sample values will be considered when obtaining the next logic level. The built-in FIFO is 64 bits, with a maximum index of 63, so the window size can only be set to 63.
16	FILTEN	Filter enable: 0: Filter disable 1: Filter enable
15:0	Reserved	Reserved, the reset value must be maintained.

14.4.18 Channel 2 Filter Register（TIMx_C2FILT）

Offset address: 0x68

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved		THRESH						Reserved	WSIZE						FILTEN
		rw							rw						rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved															

Bit field	Name	Description
31:30	Reserved	Reserved, the reset value must be maintained.
29:24	THRESH[5:0]	Threshold number of valid logic level samples, maximum 63: the threshold for valid logic levels. Within the sampling window, if the quantity of logic highs is greater than or equal to the threshold, the next logic level will be a logic high. The same rule applies to logic lows. If the quantity of high and low logic levels within the window is less than the threshold, the filter output remains unchanged. The threshold should be set to a value greater than or equal to half of the Window value Recommended threshold range: **Minimum value:** one additional pre-scaler clock period beyond the maximum glitch size limit (pre-scaler clock period), and must be greater than half of the window size. For example, if the glitch size is 3.2 * (the pre-scaler clock period), then the threshold should be ┌3.2┐ = 4 + 1 =5 **Maximum value:** the lower limit of the minimum size of the valid signal (in pre-scaler clock periods), and must be less than the window size. For example, if the minimum signal size is 3.2 * (the pre-scaler clock period), then the threshold

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		should be the lower limit (3.2) = 3.
23	Reserved	Reserved, the reset value must be maintained.
22:17	WSIZE[5:0]	Window size value for logic level checking, maximum 63: The window size determines how many sample values will be considered when obtaining the next logic level. The built-in FIFO is 64 bits, with a maximum index of 63, so the window size can only be set to 63.
16	FILTEN	Filter enable: 0: Filter disable 1: Filter enable
15:0	Reserved	Reserved, the reset value must be maintained.

14.4.19 Channel 3 Filter Register（TIMx_C3FILT）

Offset address: 0x6C

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved		THRESH						Reserved	WSIZE						FILTEN
		rw							rw						rw
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reserved															

Bit field	Name	Description
31:30	Reserved	Reserved, the reset value must be maintained.
29:24	THRESH[5:0]	Threshold number of valid logic level samples, maximum 63: the threshold for valid logic levels. Within the sampling window, if the quantity of logic highs is greater than or equal to the threshold, the next logic level will be a logic high. The same rule applies to logic lows. If the quantity of high and low logic levels within the window is less than the threshold, the filter output remains unchanged. The threshold should be set to a value greater than or equal to half of the Window value Recommended threshold range: **Minimum value:** one additional pre-scaler clock period beyond the maximum glitch size limit (pre-scaler clock period), and must be greater than half of the window size. For example, if the glitch size is 3.2 * (the pre-scaler clock period), then the threshold should be ┌3.2┐ = 4 + 1 =5 **Maximum value:** the lower limit of the minimum size of the valid signal (in pre-scaler clock periods), and must be less than the window size. For example, if the minimum signal size is 3.2 * (the pre-scaler clock period), then the threshold should be the lower limit (3.2) = 3.
23	Reserved	Reserved, the reset value must be maintained.
22:17	WSIZE[5:0]	Window size value for logic level checking, maximum 63: The window size determines how many sample values will be considered when obtaining the next logic level. The built-in FIFO is 64 bits, with a maximum index of 63, so the window size

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		can only be set to 63.
16	FILTEN	Filter enable: 0: Filter disable 1: Filter enable
15:0	Reserved	Reserved, the reset value must be maintained.

14.4.20 Input Channel Filter Output Register（TIMx_FILTO）

Offset address: 0x74

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved													C3FILTO	C2FILTO	C1FILTO
												r	r	r	r

Bit field	Name	Description
31:3	Reserved	Reserved, the reset value must be maintained.
2	C3FILTO	Channel 3 filter output level status 0: Output low level; 1: Output high level;
1	C2FILTO	Channel 2 filter output level status 0: Output low level; 1: Output high level;
0	C1FILTO	Channel 1 filter output level status 0: Output low level; 1: Output high level;

14.4.21 Encoder Capture Data Register（TIMx_ENCDAT）

Offset address: 0x88

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ENCDAT [31:0]															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ENCDAT [31:0]															
r															

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Bit field	Name	Description
31:0	ENCDAT[31:0]	Encoder capture data register. Upon detecting a valid edge of the TI3 event (when TIMx_ENCMCTRL.C3LDCNTSEL[1:0]=2’bx0, rising edge valid; or when TIMx_ENCMCTRL.C3LDCNTSEL[1:0]=2’bx1, the falling edge is active), this register records the absolute value of the difference between the current counter value and the LVR value, i.e. TIMx_ENCDAT.ENCDAT = | TIMx_CNT.CNT - TIMx_ENCLVR.LVR |.

14.4.22 Encoder Mode Control Register（TIMx_ENCMCTRL）

Offset address: 0x8C

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ENCDATS	Reserved														
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved									ENCMD[3:0]				C3LDCNTSEL[1:0]		C3LDCNTEN
									rw				rw		rw

Bit field	Name	Description
31	ENCDATS	Encoder capture data register sign. Upon detection of the TI3 event's active edge (when TIMx_ENCMCTRL.C3LDCNTSEL[1:0]=2’bx0, rising edge active; or when TIMx_ENCMCTRL.C3LDCNTSEL[1:0]=2’bx1, the falling edge is active), this register records the sign of the difference between the current counter value and the LVR value, namely: 0: TIMx_ENCDAT.ENCDAT is positive, i.e. TIMx_CNT.CNT - TIMx_ENCLVR.LVR is greater than or equal to 0. 1: TIMx_ENCDAT.ENCDAT is negative, i.e. TIMx_CNT.CNT - TIMx_ENCLVR.LVR is less than 0.
30:7	Reserved	Reserved, the reset value must be maintained.
6:3	ENCMD[3:0]	Encoder mode selection. 0000: None 0001: Quadrature encoder mode 1 – Counter increments/decrements on the rising/falling edge of TI1FP1 based on the level of TI2FP2. 0010: Quadrature encoder mode 2 – Counter increments/decrements on the rising/falling edge of TI2FP2 based on the level of TI1FP1. 0011: Quadrature Encoder Mode 3 – Counter increments/decrements on the edge of TI1FP1 and TI2FP2 based on the input level of another signal. 0100: Quadrature Encoder Mode 4 – Counter increments/decrements on the edge of TI1FP1

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Bit field	Name	Description
		based on the level of TI2FP2. Counting edge selected via CC1P. 0101: Quadrature encoder mode 5 – The counter increments/decrements on the edge of TI2FP2 based on the level of TI1FP1. The counting edge is selected via CC2P. 0110: Pulse-level encoding mode 1. The counting edge for TI2FP2 is set via CC2P. 0111: Pulse-level encoding mode 2. 1000: CCW/CW encoding mode 1, counter increments/decrements on TI1FP1 edge. 1001: CCW/CW encoding mode 2 1010: Dual-pulse encoding mode 1. Counting sensitive edges for TI1FP1 and TI2FP2 are set via CC1P and CC2P. 1011: Dual-pulse encoding mode 2. 1100–1111: Reserved *Note: These bits are only active when TIMx_SMCTRL.SMSEL[3:0]=4'b0000.* *Note: These encoder modes have the same effect as the encoder modes in TIMx_SMCTRL.SMSEL[3:0]. For example, ENCMD[3:0]=4'b0001 and TIMx_SMCTRL.SMSEL[3:0]=4'b0001 both correspond to Quadrature Encoder Mode 1.*
2:1	C3LDCNTSEL[1:0]	TI3 Event Selection. 00: TI3 event active high 01: TI3 event active low 10: TI3 event active on rising edge 11: TI3 event active on falling edge
0	C3LDCNTEN	TI3 valid event trigger counter load enabled as LVR value. 0: TI3 valid event cannot trigger counter load as LVR value 1: TI3 valid event can trigger counter load as LVR value

14.4.23 External Event Counter Load Value Register（TIMx_ENCLVR）

Offset address: 0x90

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
LVR[31:16]															
rw															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LVR[15:0]															
rw															

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Bit field	Name	Description
31:0	LVR[31:0]	An external event (TI3) triggers the counter load value. Upon detection of a valid TI3 event (selectable as active-high, active-low, rising edge, or falling edge, depending on the TIMx_ENCMCTRL.C3LDCNTSEL[1:0] register), the counter shall be loaded with the LVR value.

14.4.24 DMA Control Register (TIMx_DCTRL)

Offset address: 0x94

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved		DBADDR[5:0]						Reserved		DBLEN[5:0]					
		rw								rw					

Bit Field	Name	Description
31:14	Reserved	Reserved, the reset value must be maintained
13:8	DBADDR[5:0]	DMA base address This bit field defines the first address where the DMA accesses the TIMx_DADDR register. When access is done through the TIMx_DADDR first time, this bit-field specifies the address you just access. And then the second access to the TIMx_DADDR, you will access the address of "DMA Base Address + 4" 000000：TIMx_CTRL1, 000001：TIMx_CTRL2, 000010：TIMx_SMCTRL, ... 100101：TIMx_DCTRL
7:6	Reserved	Reserved, the reset value must be maintained
5:0	DBLEN[5:0]	DMA burst length This bit field defines the number DMA will accesses (write/read) TIMx_DADDR register. 000000: 1 time transfer 000001: 2 time transfer 000010: 3 time transfer … 010001: 18 time transfer 100010: 35 time transfer

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14.4.25 DMA Transfer For Full Transfer Register (TIMx_DADDR)

Offset address: 0x98

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
BURST[31:16]															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BURST[15:0]															
rw															

Bit Field	Name	Description
31:0	BURST[31:0]	DMA Access Buffer When a read or write operation is assigned to this register, the register located at the address range (DMA base address + DMA burst length ×4) will be accessed. DMA base address = The address of TIM_CTRL1 + TIMx_DCTRL. DBADDR * 4； DMA burst len = TIMx_DCTRL.DBLEN + 1. Example: If TIMx_DCTRL.DBLEN = 0x3(4 transfers), TIMx_DCTRL.DBADDR = 0xD (TIMx_CCDAT1), DMA data length = half word, DMA memory address = buffer address in SRAM, DMA peripheral address = TIMx_DADDR address. When an event occurs, TIMx will send requests to the DMA, and transfer data 4 times. For the first time, DMA access to the TIMx_ DADDR register will be mapped to access TIMx_CCDAT1 register; For the second time, DMA access to the TIMx_ DADDR register will be mapped to access TIMx_CCDAT2 register; … … For the fourth time, DMA access to the TIMx_ DADDR register will be mapped to access TIMx_CCDAT4 register;

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15 Basic Timer (TIM6)

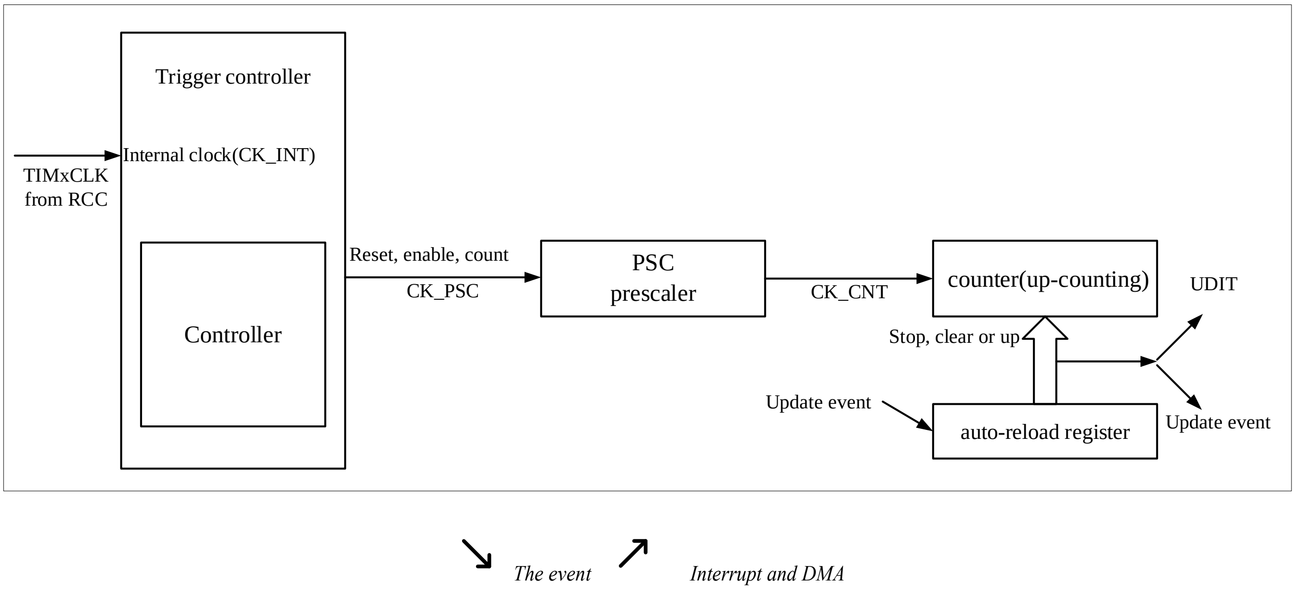
15.1 Basic Timer Introduction

Basic timers TIM6 contain a 32-bit auto-reload counter.

15.2 Basic Timer Main Features

- 32-bit auto-reload up-counting counter.
- 16-bit programmable prescaler (The prescaler factor can be configured with any value between 1 and 65536).
- The events that generate the interrupt/DMA are as follows:
  - Update event
- Supports STOP mode wake-up: When the clock source is configured as LSI, STOP mode can be woken via an update interrupt (connected to EXTI 9).

Figure 15-1 Block Diagram Of TIM6



15.3 Basic Timer Description

15.3.1 Time-base Unit

The time-base unit mainly includes: prescaler, counter and auto-reload register. When the time base unit is working, the software can read and write the corresponding registers (TIMx_PSC, TIMx_CNT and TIMx_AR) at any time.

Note: When the clock source is configured as LSI, TIMx_CNT does not support writing.

Depending on the setting of the auto-reload preload enable bit (TIMx_CTRL1.ARPEN), the value of the preload register is transferred to the shadow register immediately or at each update event UEV. When

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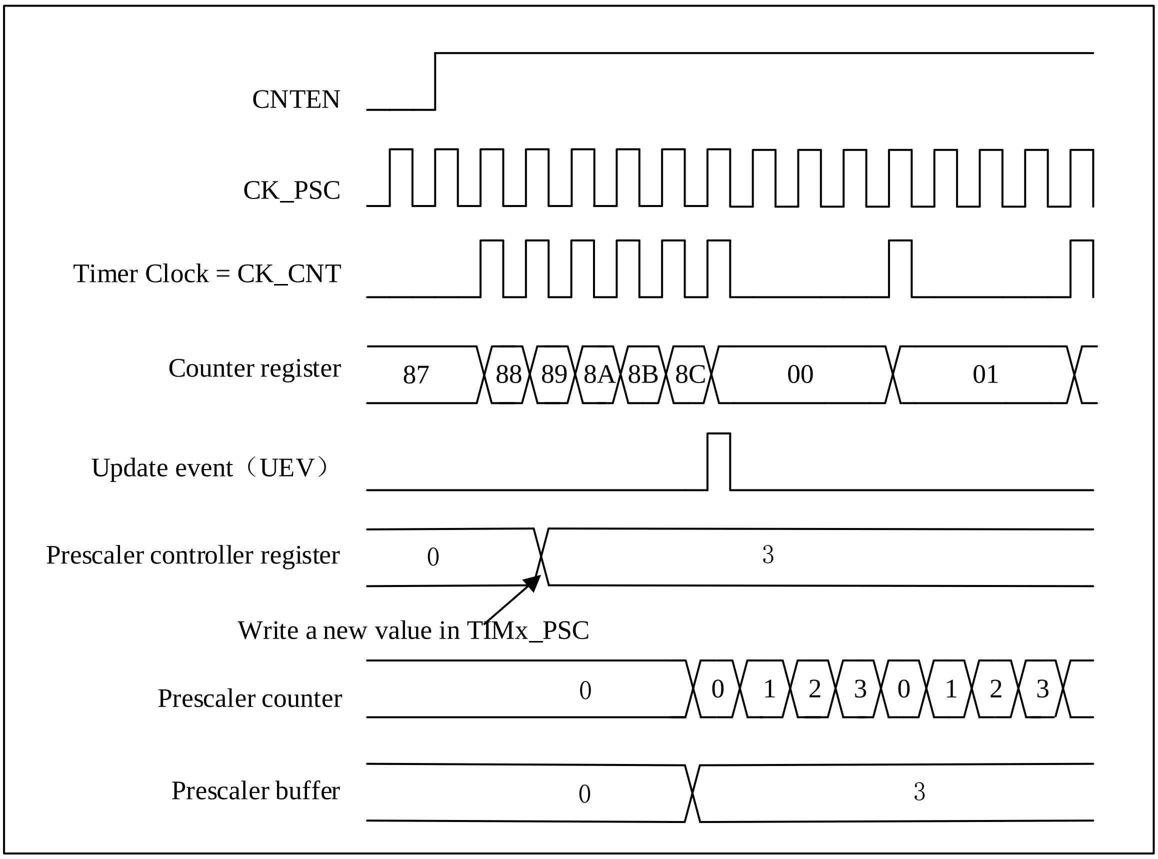
TIMx_CTRL1.UPDIS=0, an update event is generated when the counter reaches the overflow condition, or when the TIMx_EVTGEN.UDGN bit is set by software. The counter CK_CNT is valid only when the TIMx_CTRL1.CNTEN bit is set. The counter starts counting one clock cycle after the TIMx_CTRL1.CNTEN bit is set.

15.3.1.1 Prescaler Description

The TIMx_PSC register consists of a 16-bit counter that can be used to divide the counter clock frequency by any factor between 1 and 65536. It can be changed on the fly as it is buffered. The prescaler value is only taken into account at the next update event.

Figure 15-2 Counter Timing Diagram With Prescaler Division Change From 1 To 4



15.3.2 Counting Mode

15.3.2.1 Up-counting mode

In up-counting mode, the counter will count from 0 to the value of the register TIMx_AR, then it resets to 0. And a counter overflow event is generated.

If the TIMx_CTRL1.UPRS bit (select update request) and the TIMx_EVTGEN.UDGN bit are set, an update event (UEV) will generate, but TIMx_STS.UDITF will not be set by hardware. Therefore, no update interrupts or DMA update requests are generated. This setting is used in scenarios where you want to clear the counter but do not want to generate an update interrupt.

Depending on the update request source is configured in TIMx_CTRL1.UPRS, when an update event occurs, TIMx_STS.UDITF is set and all registers are updated：

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- Update auto-reload shadow registers with preload value(TIMx_AR), when TIMx_CTRL1.ARPEN = 1.
- The prescaler shadow register is reloaded with the preload value(TIMx_PSC).

To avoid updating the shadow registers when new values are written to the preload registers, you can disable the update by setting TIMx_CTRL1.UPDIS=1.

In this way,when an update event occurs, the counter and the prescaler counter will also be reset to 0 (but the prescaler rate will remain unchanged).

The figure below shows some examples of the counter behavior and the update flags for different clock frequencies in the up-counting mode.

Figure 15-3 Timing Diagram Of Up-Counting. The Internal Clock Divider Factor = 2/N

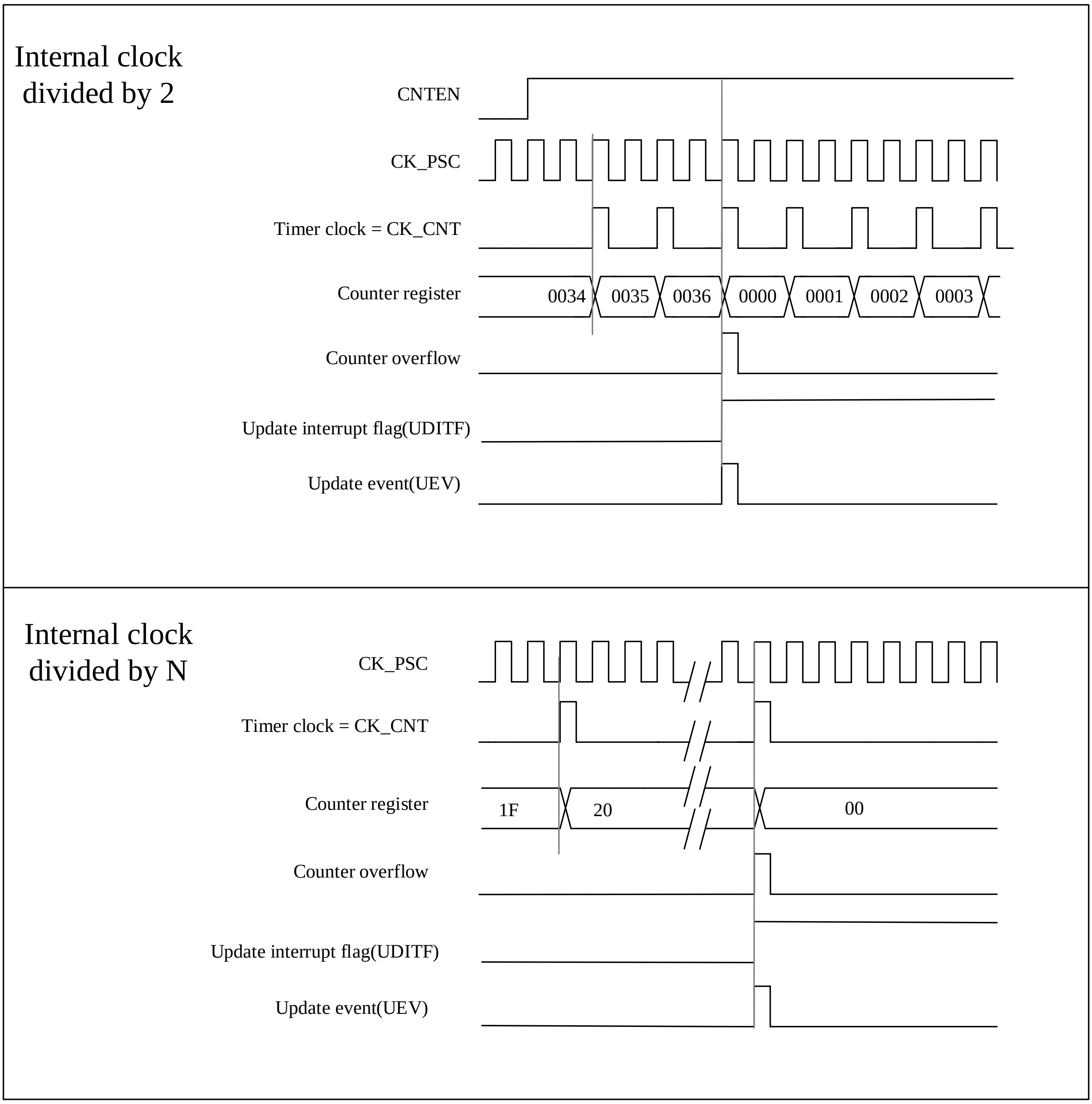

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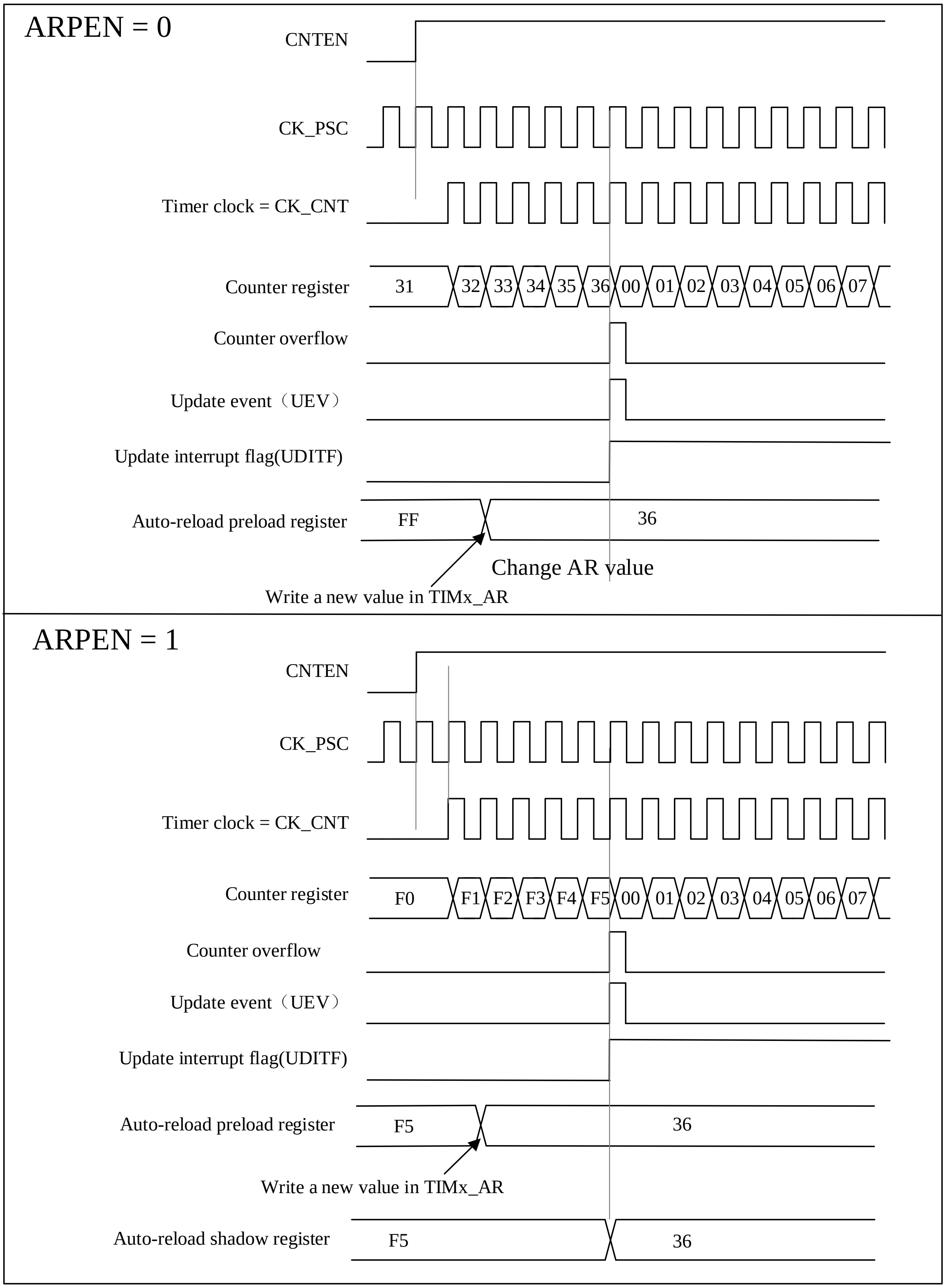
Figure 15-4 Timing diagram of up-counting and update event when ARPEN=0/1



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15.3.3 Clock Selection

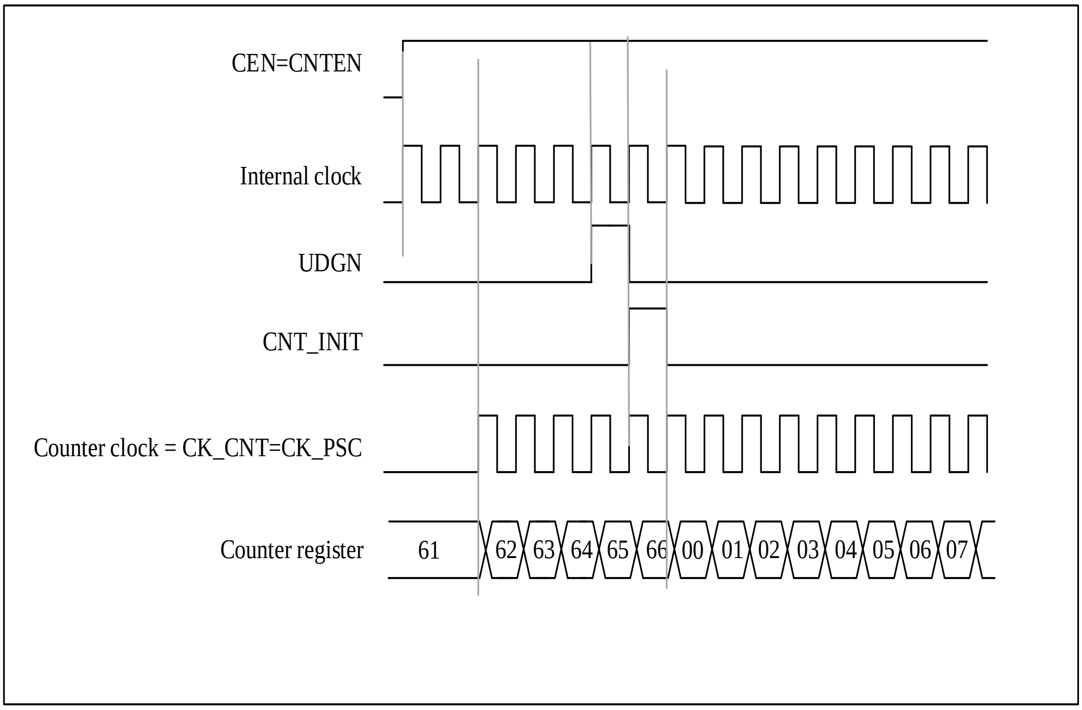
- The internal clock of timers : CK_INT

Note: The maximum operating clock for BTIM1-2 is 180MHz. Therefore, if the AHB is greater than 180MHz and BTIM1-2 is needed, the APB1 cannot be divided by 1 or 2. For example, with an AHB frequency of 240MHz and the need to use BTIM1, the APB1 can only be divided by 4 to achieve 60MHz, resulting in the BTIM1 operating at 120MHz.

15.3.3.1 Internal clock source (CK_INT)

It is provided that the TIMx_CTRL1.CNTEN bit is written as '1' by software, the clock source of the prescaler is provided by the internal clock CK_INT.

Figure 15-5 Control Circuit In Normal Mode, Internal Clock Divided By 1



15.3.4 Debug Mode

When the microcontroller is in debug mode (with the Cortex-M0 core halted), the TIM6 counter may continue to operate normally or cease functioning, depending on the configuration of the DBG_CTRL.TIM6STP bit. For further details, see Section 3.3.1

15.4 TIM6 Register Description

For abbreviations used in registers, see Section 1.1

These peripheral registers can be operated as half word (16-bits) or one word (32-bits).

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15.4.1 Register Overview

Table 15-1 Register Overview

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
000h	TIM_CTRL1	Reserve																						ARPEN	ONEPM	Reserve		UPDIS	UPRS	Reserve			CNTEN
008h	TIM_STS	Reserve															UDITF	Reserve															
00Ch	TIM_EVTGEN	Reserve																							UDGN	Reserve							
014h	TIM_DINTEN	Reserve												UDEN	Reserve		UIEN	Reserve															
040h	TIM_PSC	Reserve																PSC[15:0]															
044h	TIM_AR	AR[31:0]																															
048h	TIM_CNT	CNT[31:0]																															

15.4.2 Control Register 1 (TIMx_CTRL1)

Offset address: 0x00

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved						ARPEN	ONEPM	Reserved		UPDIS	UPRS	Reserved			CNTEN
						rw	rw			rw	rw				rw

Bit Field	Name	Description
31:10	Reserved	Reserved, the reset value must be maintained
9	ARPEN	Auto-reload preload enable 0: Shadow register disable for TIMx_AR register 1: Shadow register enable for TIMx_AR register

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8	ONEPM	One pulse mode 0: Disable one-pulse mode, the counter counts are not affected when an update event occurs. 1: Enable one-pulse mode, the counter stops counting when the next update event occurs (clearing TIMx_CTRL1.CNTEN bit).
7:6	Reserved	Reserved, the reset value must be maintained
5	UPDIS	Update disable This bit is used to enable/disable the Update event (UEV) events generation by software. 0: Enable UEV. UEV will be generated if one of following condition been fulfilled： – Counter overflow – The TIMx_EVTGEN.UDGN bit is set Shadow registers will update with preload value。 1: Disabled UEV. No update event is generated, and the shadow registers (AR, PSC) keep their values. If the TIMx_EVTGEN.UDGN bit is set, the counter and prescaler are reinitialized.
4	UPRS	Update request source This bit is used to select the UEV event sources by software. 0: If update interrupt or DMA request is enabled, any of the following events will generate an update interrupt or DMA request： – Counter overflow – The TIMx_EVTGEN.UDGN bit is set 1: If update interrupt or DMA request is enabled, only counter overflow will generate update interrupt or DMA request
3:1	Reserved	Reserved, the reset value must be maintained
0	CNTEN	Counter enable 0: Disable counter 1: Enable counter

15.4.3 Status Registers (TIMx_STS)

Offset address: 0x08

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															UDITF
															rc_w0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved															

Bit Field	**Name**	**Description**
31:17	Reserved	Reserved, the reset value must be maintained
16	UDITF	Update interrupt flag This bit is set by hardware when an update event occurs under the following conditions： –When TIMx_CTRL1.UPDIS = 0, and counter value overflow。

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		–When TIMx_CTRL1.UPRS = 0, TIMx_CTRL1.UPDIS = 0, and set the TIMx_EVTGEN.UDGN bit by software to reinitialize the CNT。 This bit is cleared by software. 0: No update event occurred 1: Update interrupt occurred
15:0	Reserved	Reserved, the reset value must be maintained

15.4.4 Event Generation Register (TIMx_EVTGEN)

Offset address: 0x0C

Reset value: 0 x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved							UDGN	Reserved							
							w								

Bit Field	Name	Description
31:9	Reserved	Reserved, the reset value must be maintained.
8	UDGN	Update generation Software can set this bit to update configuration register value and hardware will clear it automatically. 0: No effect. 1: Timer will restart and all shadow register will be updated. It will restart prescaler counter also.
7:0	Reserved	Reserved, the reset value must be maintained.

15.4.5 DMA/Interrupt Enable Register (TIMx_DINTEN)

Offset address: 0x14

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved												UDEN	Reserved		UIEN
												rw			rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved															

Bit Field	Name	Description
31:20	Reserved	Reserved, the reset value must be maintained

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Bit Field	Name	Description
19	UDEN	Update DMA request enable 0: Disable update DMA request 1: Enable update DMA request
18:17	Reserved	Reserved, the reset value must be maintained
16	UIEN	Update interrupt enable 0: Disable update interrupt 1: Enable update interrupt
15:0	Reserved	Reserved, the reset value must be maintained

15.4.6 Prescaler (TIMx_PSC)

Offset address: 0x40

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PSC[15:0]															
rw															

Bit field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained
15:0	PSC[15:0]	Prescaler value PSC register value will be updated to prescaler register at update event. Counter clock frequency is input clock frequency divide PSC + 1。

15.4.7 Automatic Reload Register (TIMx_AR)

Offset address: 0x44

Reset value: 0x0000 FFFF

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
AR[31:0]															
rw															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
AR[31:0]															
rw															

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Bit field	Name	Description
31:0	AR[31:0]	Auto-reload value These bits define the value that will be loaded into the actual auto-reload register. See 15.3.1 for more details。 When the TIMx_AR.AR [15:0] value is null, the counter does not work.

15.4.8 Counter (TIMx_CNT)

Offset address: 0x48

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CNT[31:0]															
rw															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CNT[31:0]															
rw															

Bit Field	Name	Description
31:0	CNT[31:0]	Counter value

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16 Analog to Digital Conversion (ADC)

16.1 Introduction

The 12-bit ADC is a high-speed analog-to-digital converter using successive approximation. It can measure 16 channel signal sources. It has 11 external and 5 internal channels. Each channel of the A/D conversion performed in single, continuous or segment mode. ADC measurements are stored (left-aligned/ right-aligned) in 16-bit data registers. The application detects the input voltage within user-defined high/low thresholds by analog watchdog and the maximum frequency of the input clock to the ADC is 32MHz.

16.2 Main Features

- Supports 12-bit resolution
- Supports single-ended inputs
- Interrupts at the end of conversion, and simulated watchdog events
- Support single and continuous conversion modes
- 10 result registers with configurable channel numbers
- 16 (11 external + 5 internal) channel settings with individually configurable sampling times
- Single-segment, 2-segment, 3-segment, and 4-segment custom sampling sequences. The number of sequences and channel numbers can be flexibly configured
- Conversion completion interrupt: After each trigger source completes conversion, a conversion completion flag is automatically generated, which is set by hardware and cleared by software. Enabling the interrupt will generate interrupts, including segment interrupt, any channel completion interrupt, all conversion completion interrupt, and watchdog interrupt
- Data alignment with built-in data consistency
- Regular conversion has internnal and external triggering options
- Supports maximum sampling rate of 1MSPS
- Support for ADC linkage: Supports 16 optional trigger sources (including 14 TIM Trigger sources, EXTI and software triggers). After triggering, conversions with configurable length and specified channels can be generated
- ADC power supply requirements: 2.4V to 5.5V
- ADC input range: $0 \leq V_{IN} \leq V_{DDA}$

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16.3 Function Description

Below is a block diagram of an ADC module. Table 16-1 shows the description of ADC pins.

Figure 16-1 Block Diagram of ADC

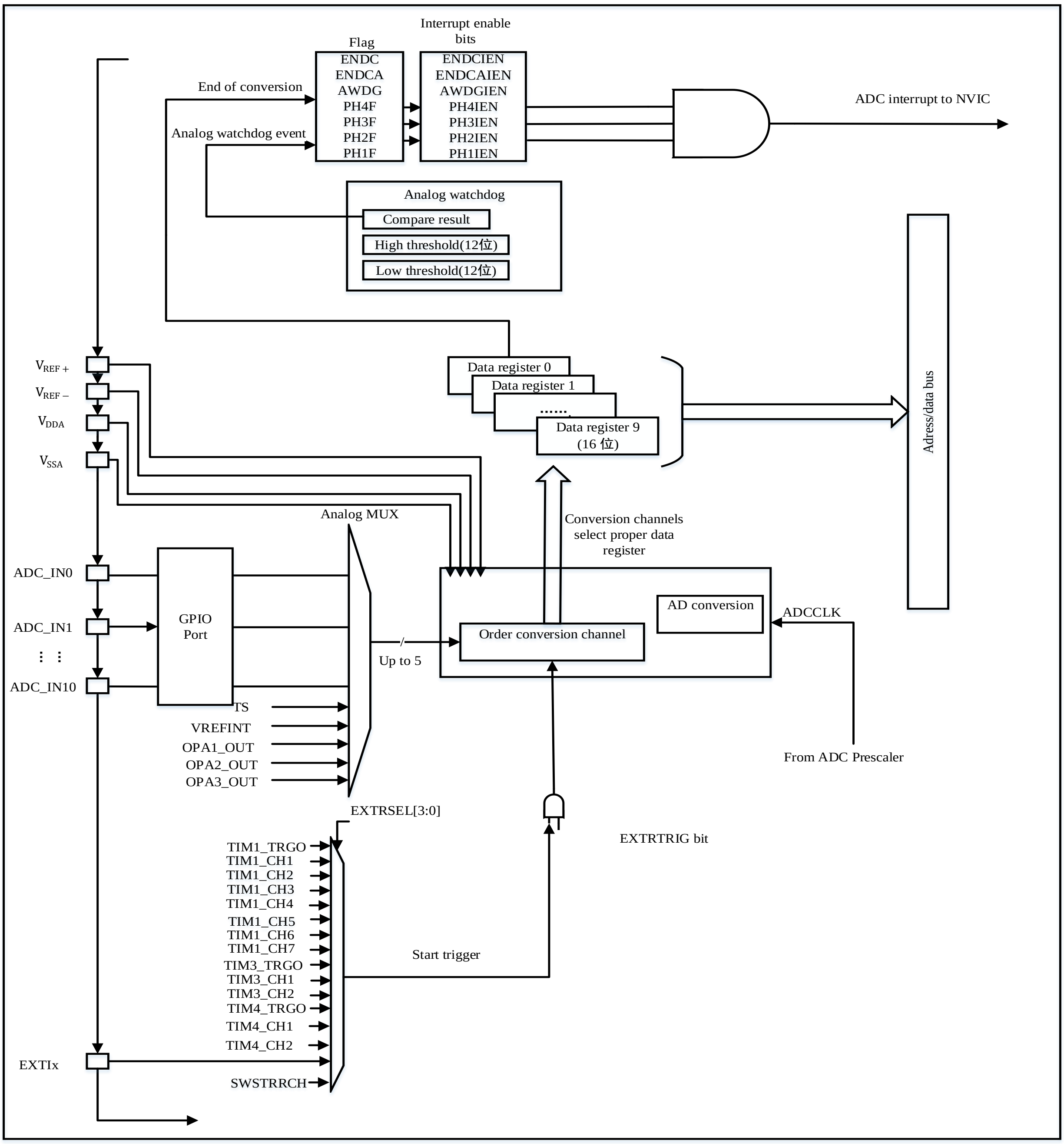

Table 16-1 ADC Pins

Name	Signal Types	Annotations
V_{REF+}	Input, Positive reference voltage	Positive reference voltage used by the ADC, 2.4V ≤ V_{REF+} ≤ V_{DDA} (5.5V)

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V_{DDA} [1]	Input, analog power supply	Equivalent to V_{DD} analog power supply and: $2V \leq V_{DD} \leq 5.5$ V
V_{REF-}	Input, Negative reference voltage	Negative reference voltage used by the ADC, $V_{REF-} = V_{SSA}$
V_{SSA} [1]	Input, analog power supply ground	Equivalent to V_{SS} analog power supply ground
ADCx_IN[10:0]	Analog input signal	11 analog external input channels

1. V_{DDA} and V_{SSA} should be connected to V_{DD} and V_{SS} respectively.

16.3.1 ADC Switch Control

User can proceed to the next step only after the power-up process is complete by polling the ADC_STS.RDY bit.

User can set the ADC_CTRL2.ON bit to turn on the ADC. When the ADC_CTRL2.ON bit is set for the first time, it wakes up the ADC from the power-off state. After a power-on delay of ADC (t_{STAB}), the conversion begins when the ADC_CTRL2.ON bit is set again.

The conversion can be stopped by clearing the ADC_CTRL2.ON bit and placing the ADC in power-off mode. In this mode, the ADC consumes almost no power consumption (just a few µA). Power-down state of ADC can be checked by polling the ADC_STS.PDRDY bit.

When the ADC is disabled, the default mode is power-down.

16.3.2 ADC Clock

An ADC requires three clocks, ADC_CLK, HCLK, and ADC_1MCLK.

- HCLK is used for the register access.
- ADC_CLK is the working clock of ADC, with a maximum support of 32M.
- ADC_1MCLK is used for internal timing function, configured in RCC, and its frequency must be configured to 1M

Note:

1. The ADC_CLK frequency division factor can be configured with maximum frequency of 32MHz. The ADC_CLK frequency division factor can be 2,4,8,16,32.

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16.3.3 Channel Selection

The ADC supports 16 channels of input, including 11 external channels and 5 internal channels. The connection relationships are as shown in the following table.

Table 16-2 Channel Correspondence Table

Channel	**Source**
CH0	PA0
CH1	PA1
CH2	PA2
CH3	PA3
CH4	PA4
CH5	PA5
CH6	PA6
CH7	PA7
CH8	PB0
CH9	PB1
CH10	PB2
CH11	Temp Seneor
CH12	VREFINT
CH13	OPA1.OUT
CH14	OPA2.OUT
CH15	OPA3.OUT

Note:

1. To test TS, the register ADC_CTRL3.TEMPEN must be set to 1'b1.

2. To test the internal reference voltage VREFINT, the register ADC_CTRL3.REFSEL must be set to 1'b1. Wait until ADC_STS.VREFRDY = 1 before performing ADC conversion.

3. To test the output of OPAMP1, the corresponding OPAMP1_CS.MOD[1:0] must be set to 2'b01.

4. To test the output of OPAMP2, the corresponding OPAMP2_CS.MOD must be set to 1'b0.

5. To test the output of OPAMP3, the corresponding OPAMP3_CS.MOD must be set to 1'b0.

16.3.4 Single Conversion Mode

The ADC can enter the single conversion mode by configuring ADC_CTRL2.CTU to 0.

After the conversion starts, when a regular channel conversion is completed, the any channel conversion end flag (ADC_STS.ENDCA) will be set to 1. If the arbitrary regular channel conversion end interrupt enable (ADC_CTRL1.ENDCAIEN) bit is set to 1, an interrupt will be generated, and the converted data will be stored in the ADC_DATx register.

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16.3.5 Continuous Conversion Mode

The ADC can enter the continuous conversion mode by configuring ADC_CTRL2.CTU to 1.

After the conversion starts, when a regular channel conversion is completed, the regular channel end of conversion flag (ADC_STS.ENDC) will be set to 1. If the regular channel end of conversion interrupt enable bit (ADC_INTEN.ENDCIEN) is set to 1, an interrupt will be generated. The converted data will be stored in the ADC_DATx register.

Note: Continuous conversion is only applicable to the first segment conversion.

16.3.6 Segment Sampling Mode

The ADC supports 1-segment, 2-segment, 3-segment, and 4-segment sampling modes. Each segment of sampling requires a specific external event to trigger. Each segment supports configurations of different sampling counts and sampling signal channels. Segment conversion is completed as a one-time conversion and does not support cyclic conversion.

- segment sampling means that the ADC completes a segment of sampling action upon receiving one trigger. A 1-segment sampling may include multiple samplings of analog signals. The number of samplings is configured by the segment sampling count register ADC_PHCFG. When the register value is 0~9 (maximum 9), the corresponding number of samplings is 1~10 (cannot exceed 10).
- 2-segment triggering requires two triggers to complete a full round of sampling. The first segment of sampling is performed when the first trigger arrives, and the second segment of sampling is performed when the second trigger arrives.
- 3-segment triggering requires three triggers to complete a full round of sampling. The first segment of sampling is performed when the first trigger arrives, the second segment when the second trigger arrives, and the third segment when the third trigger arrives.
- 4-segment triggering requires four triggers to complete a full round of sampling. The first segment of sampling is performed when the first trigger arrives, the second segment when the second trigger arrives, the third segment when the third trigger arrives, and the fourth segment when the fourth trigger arrives.

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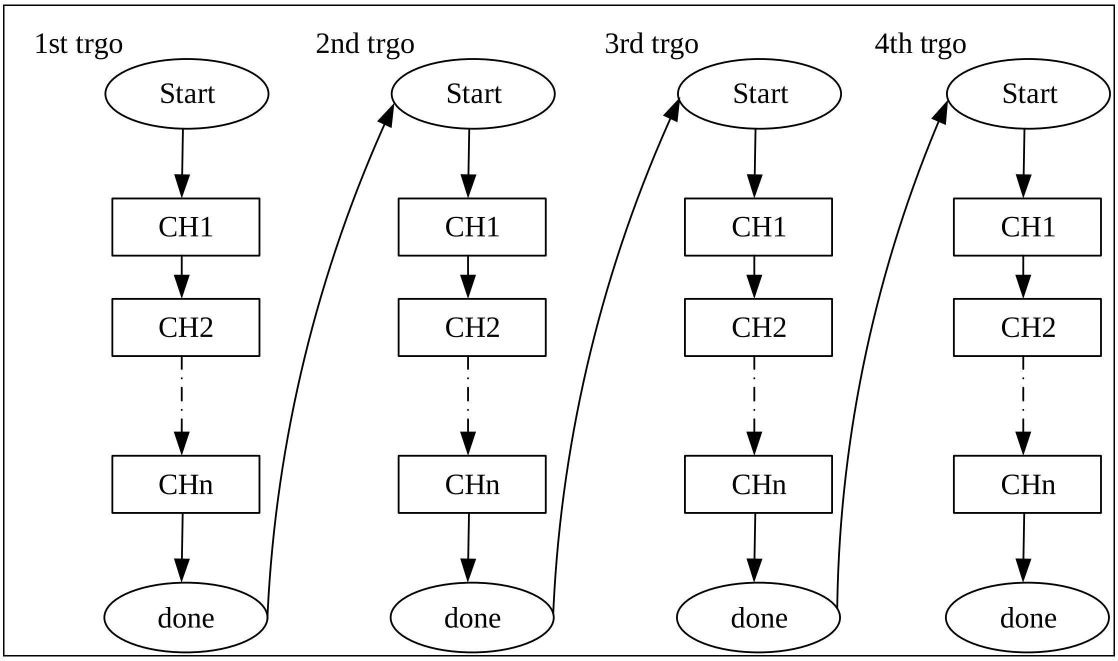
Figure 16-2 ADC segment conversion



Note:

1. *Currently, trgo is divided into 4 segments, each triggered independently. Each segment only requires one trgo to trigger sampling of multiple channels (configured via registers). A maximum of 4 segment sampling trgos can be received each time, and they will be automatically cleared after the segment conversion is completed.*

2. *The sum of the four ADC sampling segments must not exceed the number of registers (10 data registers). There are 10 registers corresponding to 10 channels. For example, the first segment includes channels 1, 2, and 4, and the second segment includes channels 1, 3, and 4. The storage order in the registers is 1, 2, 3, 4, 5, 6.*

3. *The total number of channels across the four segments should not exceed 10. If the configuration includes more than 10 channels, only 10 channels will be converted; the excess part will be directly ignored, and a segment completion flag for the converted channels will be generated.*

4. *The first segment has a trigger source preemption function. For example, with the configuration: segments 1, 2, and 3 are triggered. If triggers for segments 1 and 2 have been completed successively but the trigger for segment 3 has not occurred, and then a trigger for segment 1 arrives at this point, it indicates that the sampling of the previous round (segments 1, 2, 3) is incomplete. It is necessary to re-trigger the sampling of segments 1, 2, and 3.*

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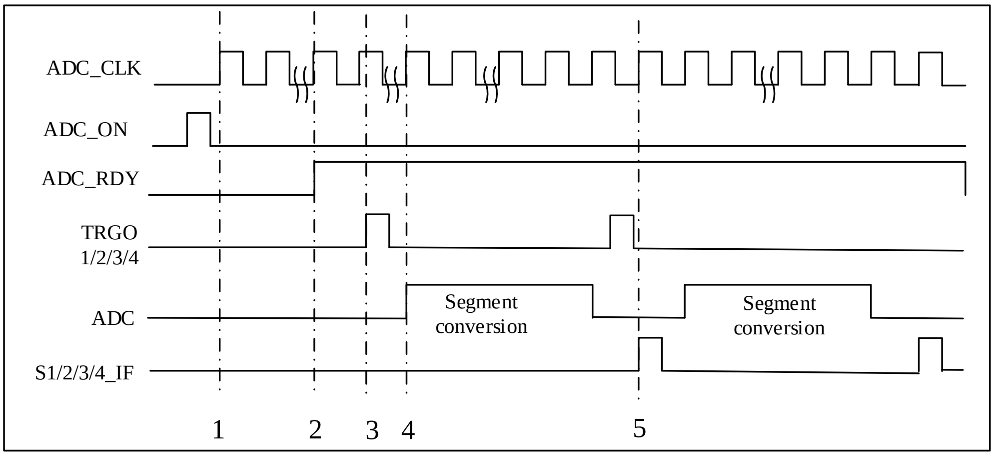
16.3.7 Timing Diagram

As shown in the figure below, set ADC_CTRL2.ON to 1, wait for ADC_STS.RDY to be set, then start the ADC conversion. Once the flag is set, the conversion result is stored in the ADC data register.

Figure 16-3 Timing Diagram



Note:

1. *Enable ADC, start ADC power-up*
2. *ADC power-up completed*
3. *ADC trigger starts*
4. *ADC segment conversion starts*
5. *ADC segment conversion completed*

16.3.8 Analog Watchdog

It supports independent watchdog interrupt enabling for 10 channels. The threshold of the analog watchdog is irrelevant to the data alignment method, because the comparison between the ADC conversion value and the threshold is completed before alignment. When the ADC conversion value is higher than the high threshold of the analog watchdog or lower than the low threshold of the analog watchdog, the analog watchdog flag (ADC_STS.AWDG) will be set to 1. If the analog watchdog of the corresponding channel is enabled, an interrupt will be generated at this time.

Note:

1. *The watchdog interrupt or flag is only set during ADC conversion, that is, the value in the data register after the conversion is completed will not generate an interrupt or flag.*

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16.3.9 Data Aligned

The ADC_CTRL2.ALIG bit selects the alignment mode for storing the converted data. The data can be left-aligned or right-aligned.

Right-align Data

0	0	0	0	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

Left-aligne Data

D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	0	0	0	0

16.3.10 Programmable Channel Sampling Time

ADC samples the input voltage using a number of ADC_CLK cycles. The number of sampling cycles can be modified via the SAMPx[3:0] bits in the ADC_SAMPTx register. Each channel can be sampled with a different duration. The total conversion time is calculated as follows:

$$T_{CONV} = \text{Sampling time} + 12 \text{ cycles}$$

Example:

With ADCCLK=16MHz, the sampling time is 4 cycle

$$T_{CONV} = 4 + 12 = 16 \text{ cycles}$$

16.3.11 Triggered Conversion

This sub-module mainly implements handshake synchronization for external TRGO signals and selects a TRGO that meets the current configuration requirements.

The signal source for each sampling is selected via register configuration. The selection of the signal source must be completed before triggering, and should not be changed until a single sampling process is finished.

Table 16-3 ADC Trigger and Channel Selection

TRIGSEL [3:0]	Trigger Source	Type
0000	TIM1.CC1 event	Internal signal from the on-chip timer
0001	TIM1.CC2 event	
0010	TIM1.CC3 event	
0011	TIM1.CC4 event	
0100	TIM1.CC5 event	
0101	TIM1.CC6 event	
0110	TIM1.CC7 event	
0111	TIM1.TRGO event	
1000	TIM3.CC1 event	
1001	TIM3.CC2 event	
1010	TIM3.TRGO event	

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TRIGSEL [3:0]	Trigger Source	Type
1011	TIM4.CC1 event	
1100	TIM4.CC2 event	
1101	TIM4.TRGO event	
1110	EXTI line 0~6 event	External pin/internal signal from on-chip timer
1111	SWSTRRCH	Software control bit

Note: When the same trigger source is used for two triggers, the interval between the two triggers must be at least 5 ADC_CLK cycles.

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16.3.12 ADC Interrupts

It supports 7 interrupts, including: Watchdog Interrupt (AWDG), All Channels (Segments) Conversion Completion Interrupt (ENDC), Any Channel Conversion Completion Interrupt (ENDCA), 1st Segment Sampling Conversion Completion Interrupt (PH1F), 2nd Segment Sampling Conversion Completion Interrupt (PH2F), 3rd Segment Sampling Conversion Completion Interrupt (PH3F), and 4th Segment Sampling Conversion Completion Interrupt (PH4F).

1-segment trigger sampling completion interrupt: ADC_STS.PH1F is set when sampling is completed.

2-segment trigger sampling completion interrupt: ADC_STS.PH1F is set when the 1st segment sampling is completed, and ADC_STS.PH2F is set when the 2nd segment sampling is completed.

3-segment trigger sampling completion interrupt: ADC_STS.PH1F is set when the 1st segment sampling is completed, ADC_STS.PH2F is set when the 2nd segment sampling is completed, and ADC_STS.PH3F is set when the 3rd segment sampling is completed.

4-segment trigger sampling completion interrupt: ADC_STS.PH1F is set when the 1st segment sampling is completed, ADC_STS.PH2F is set when the 2nd segment sampling is completed, ADC_STS.PH3F is set when the 3rd segment sampling is completed, and ADC_STS.PH4F is set when the 4th segment sampling is completed.

If the relevant interrupt bit is enabled, the corresponding interrupt will be generated.

Table 16-4 ADC Trigger and Channel Selection

Interrupt Event	Event Flag	Enable Control Bit
All Channels Conversion Completion Enable	ADC_STS.ENDC	ADC_CTRL1.ENDCIEN
Analog Watchdog Status Bit Set Enable	ADC_STS.AWDG	ADC_CTRL1.AWDGIEN
Any Regular Channel Interrupt Enable	ADC_STS.ENDCA	ADC_CTRL1.ENDCAIEN
1st Segment Sampling Conversion Completion Enable	ADC_STS.PH1F	ADC_CTRL1.PH1IEN
2nd Segment Sampling Conversion Completion Enable	ADC_STS.PH2F	ADC_CTRL1.PH2IEN
3rd Segment Sampling Conversion Completion Enable	ADC_STS.PH3F	ADC_CTRL1.PH3IEN
4th Segment Sampling Conversion Completion Enable	ADC_STS.PH4F	ADC_CTRL1.PH4IEN

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16.4 ADC Registers

16.4.1 ADC Register Overview

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x00	ADC_STS	Reserved																				PDRDY	RDY	VREFRDY	STR	Reserved	AWDG	ENDCA	ENDC	PH4F	PH3F	PH2F	PH1F
0x04	ADC_CTRL1	Reserved																									AWDGIEN	ENDCAIEN	ENDCIEN	PH4IEN	PH3IEN	PH2IEN	S1_IE
0x08	ADC_CTRL2	Reserved																											RSTA	Reserved	ALIG	CTU	ON
0xC	ADC_CTRL3	Reserved																										TEMPEN	Reserved	REFSEL	VREFEN	Reserved	
0x10	ADC_SAMPT1	SAMP7[3:0]				SAMP6[3:0]				SAMP5[3:0]				SAMP4[3:0]				SAMP3[3:0]				SAMP2[3:0]				SAMP1[3:0]				SAMP0[3:0]			
0x14	ADC_SAMPT2	SAMP15[3:0]				SAMP14[3:0]				SAMP13[3:0]				SAMP12[3:0]				SAMP11[3:0]				SAMP10[3:0]				SAMP9[3:0]				SAMP8[3:0]			
0x18	ADC_AWDHIGH	Reserved																				HTH[11:0]											
0x1C	ADC_AWDLOW	Reserved																				LTH[11:0]											
0x20	ADC_AWDEN	Reserved																					AWDENx[9:0]										
0x24	ADC_PHCFG	Reserved														TRIGMD		PH4CHNUM				PH3CHNUM				PH2CHNUM				PH1CHNUM			
0x28	ADC_TRIGSEL	PH4EXTSEL				PH3EXTSEL				PH2EXTSEL				PH1EXTSEL				SWSTRRCH	EXTRTRIG	TIM4_TRGOEN	TIM4_CC2EN	TIM4_CC1EN	TIM3_TRGOEN	TIM3_CC2EN	TIM3_CC1EN	TIM1_TRGOEN	TIM1_CC7EN	TIM1_CC6EN	TIM1_CC5EN	TIM1_CC4EN	TIM1_CC3EN	TIM1_CC2EN	TIM1_CC1EN

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0x2C	ADC_PHSWTRIG	Reserved				PHSWSTART			
0x30	ADC_SEQ1	SEQ8[3:0]	SEQ7[3:0]	SEQ6[3:0]	SEQ5[3:0]	SEQ4[3:0]	SEQ3[3:0]	SEQ2[3:0]	SEQ1[3:0]
0x34	ADC_SEQ2	Reserved						SEQ10[3:0]	SEQ9[3:0]
0x38	ADC_DAT0	Reserved				DAT0[11:0]			
0x3C	ADC_DAT1	Reserved				DAT1[11:0]			
0x40	ADC_DAT2	Reserved				DAT2[11:0]			
0x44	ADC_DAT3	Reserved				DAT3[11:0]			
0x48	ADC_DAT4	Reserved				DAT4[11:0]			
0x4C	ADC_DAT5	Reserved				DAT5[11:0]			
0x50	ADC_DAT6	Reserved				DAT6[11:0]			
0x54	ADC_DAT7	Reserved				DAT7[11:0]			
0x58	ADC_DAT8	Reserved				DAT8[11:0]			
0x5C	ADC_DAT9	Reserved				DAT9[11:0]			

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16.4.2 ADC Status Register (ADC_STS)

Address offset: 0x00

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved				PDRDY	RDY	VREFRDY	STR	Reserved	AWDG	ENDCA	ENDC	PH4F	PH3F	PH2F	PH1F
				r	r	r	rc-w1		rc-w1	rc-w1	rc-w1	rc-w1	rc-w1	rc-w1	rc-w1

Bit Field	Name	Description
31:12	Reserved	Reserved, the reset value must be maintained
11	PDRDY	ADC Power Down Ready 0: Not ready; 1: Ready.
10	RDY	ADC Ready 0: Not ready; 1: Ready.
9	VREFRDY	VREFINT Ready (VREFINT_READY) This bit indicates the ready status of the ADC Internal Input Buffer. Before measuring VREFINT, the software must check this status bit. 0: VREFINT is not ready; 1: VREFINT is ready.
8	STR	Regular channel start flag This bit is set by hardware at the start of regular channel conversion and cleared by software. 0: Regular channel conversion has not started. 1: Regular channel conversion has started.
7	Reserved	Reserved, the reset value must be maintained
6	AWDG	Analog Watchdog Flag (Analog watchdog flag) This bit is set to 1 by hardware when the converted voltage value exceeds the range defined by the ADC_AWDHIGH.HTH and ADC_AWDLOW.LTH registers, and is cleared by software. 0: No analog watchdog event has occurred; 1: An analog watchdog event has occurred.
5	ENDCA	Any End of Conversion Flag (Any End of conversion flag) This bit is set to 1 by hardware when the conversion of any regular channel is completed. 0: Conversion has not been completed; 1: Conversion has been completed.
4	ENDC	End of Conversion Flag (End of conversion) This bit is set to 1 by hardware when the conversion of all channel sequences is completed. 0: Conversion has not been completed; 1: Conversion has been completed.

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3	PH4F	4th Segment Sampling Completion Flag 0: Conversion has not been completed; 1: Conversion has been completed.
2	PH3F	3rd Segment Sampling Completion Flag 0: Conversion has not been completed; 1: Conversion has been completed.
1	PH2F	2nd Segment Sampling Completion Flag 0: Conversion has not been completed; 1: Conversion has been completed.
0	PH1F	1st Segment Sampling Completion Flag 0: Conversion has not been completed; 1: Conversion has been completed.

16.4.3 ADC Control Register 1 (ADC_CTRL1)

Address offset: 0x04

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved									AWDG IEN	ENDCA IEN	ENDCIEN	PH4IEN	PH3IEN	PH2IEN	PH1IEN
									rw	rw	rw	rw	rw	rw	rw

Bit Field	Name	Description
31:7	Reserved	Reserved, the reset value must be maintained
6	AWDGIEN	Analog Watchdog Interrupt Enable (Analog watchdog interrupt enable) This bit is set and cleared by software to disable or enable the analog watchdog from generating an interrupt. 0: Disable analog watchdog interrupt; 1: Enable analog watchdog interrupt.
5	ENDCAIEN	Interrupt Enable for ENDCA (Any End of conversion flag) This bit is set and cleared by software to disable or enable the generation of an interrupt after the completion of a regular conversion sequence. 0: Disable ENDCA interrupt; 1: Enable ENDCA interrupt.
4	ENDCIEN	Interrupt Enable for ENDC (Interrupt enable for ENDC) This bit is set and cleared by software to disable or enable the generation of an interrupt after the completion of a regular conversion sequence. 0: Disable ENDC interrupt;

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Bit Field	Name	Description
		1: Enable ENDC interrupt.
3	PH4IEN	4th Segment Sampling Completion Interrupt Enable
2	PH3IEN	3rd Segment Sampling Completion Interrupt Enable
1	PH2IEN	2nd Segment Sampling Completion Interrupt Enable
0	PH1IEN	1st Segment Sampling Completion Interrupt Enable

16.4.4 ADC Control Register 2 (ADC_CTRL2)

Address offset: 0x08

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved													ALIG	CTU	ON
													rw	rw	rw

Bit Field	Name	Description
31:3	Reserved	Reserved, the reset value must be maintained
2	ALIG	Data alignment This bit is set and cleared by software. 0: Right-aligned; 1: Left-aligned.
1	CTU	Continuous conversion This bit is set and cleared by software. If this bit is set, the conversion will continue until the bit is cleared. 0: Single conversion mode; 1: Continuous conversion mode.
0	ON	A/D converter ON/OFF This bit is set and cleared by software. When this bit is "0", writing "1" will wake the ADC from power-down mode.It should be noted that there is a delay t_{STAB} between the converter power-on and the start of conversion. 0: Disable ADC conversion/calibration and enter power-down mode; 1: Start the ADC and initiate conversion.

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16.4.5 ADC Control Register 3 (ADC_CTRL3)

Address offset: 0x0C

Reset value: 0x0000 0400

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved										TEMPEN	Reserved	REFSEL	VREFEN	Reserved	
										rw		rw	rw		

Bit Field	Name	Description
31:6	Reserved	Reserved, the reset value must be maintained
5	TEMPEN	Temperature Sensor Enable This bit is set and cleared by software to enable or disable the temperature sensor channel. 0: Disable temperature sensor measurement; 1: Enable temperature sensor measurement.
4	Reserved	Reserved, the reset value must be maintained
3	REFSEL	Switch Selection Signal for ADC VREFP 0: Select VDDA; 1: Select internal 3.6V.
2	VREFEN	VREFINT Enable (VREFINT_EN) This bit enables the ADC internal input buffer. Before measuring VREFINT, the software must enable this bit. 0: Disable VREFINT measurement; 1: Enable VREFINT measurement.
1:0	Reserved	Reserved, the reset value must be maintained

16.4.6 ADC Sampling Time Register1 (ADC_SAMPT1)

Address offset: 0x10

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SAMP7[3:0]				SAMP6[3:0]				SAMP5[3:0]				SAMP4[3:0]			
rw				rw				rw				rw			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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SAMP3[3:0]	SAMP2[3:0]	SAMP1[3:0]	SAMP0[3:0]
rw	rw	rw	rw

Bit Field	Name	Description
31:0	SAMPx[3:0]	Channel x Sample Time Selection These bits are used to independently select the sampling time for each channel. The channel selection bits must remain unchanged during sampling. 0000: 4 Cycles 0001: 6 Cycles 0010: 14 Cycles 0011: 20 Cycles 0100: 29 Cycles 0101: 42 Cycles 0110: 56 Cycles 0111: 72 Cycles 1000: 88 Cycles 1001: 120 Cycles 1010: 182 Cycles 1011: 240 Cycles 1100: 300 Cycles 1101: 400 Cycles 1110: 480 Cycles 1111: 600 Cycles

16.4.7 ADC Sampling Time Register2(ADC_SAMPT2)

Address offset: 0x14

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SAMP15[3:0]				SAMP14[3:0]				SAMP13[3:0]				SAMP12[3:0]			
rw				rw				rw				rw			

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SAMP11[3:0]				SAMP10[3:0]				SAMP9[3:0]				SAMP8[3:0]			
rw				rw				rw				rw			

Bit Field	Name	Description
31:0	SAMPx[3:0]	Channel x Sample Time Selection These bits are used to independently select the sampling time for each channel. The channel selection bits must remain unchanged during sampling.

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Bit Field	Name	Description
		0000: 4 Cycles 0001: 6 Cycles 0010: 14 Cycles 0011: 20 Cycles 0100: 29 Cycles 0101: 42 Cycles 0110: 56 Cycles 0111: 72 Cycles 1000: 88 Cycles 1001: 120 Cycles 1010: 182 Cycles 1011: 240 Cycles 1100: 300 Cycles 1101: 400 Cycles 1110: 480 Cycles 1111: 600 Cycles

16.4.8 ADC Watchdog High Threshold Register (ADC_WDGHIGH)

Address offset: 0x18

Reset value: 0x0000 0FFF

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved				HTH[11:0]											
				rw											

Bit Field	Name	Description
31:12	Reserved	Reserved, the reset value must be maintained.
11:0	HTH[11:0]	Analog watchdog high threshold These bits define the high threshold for analog watchdog.

16.4.9 ADC Watchdog Low Threshold Register (ADC_WDGLOW)

Address offset: 0x1C

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

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Reserved	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved				LTH[11:0]											
				rw											

Bit Field	Name	Description
31:12	Reserved	Reserved, the reset value must be maintained.
11:0	LTH[11:0]	Analog watchdog low threshold These bits define the low threshold low threshold for analog watchdog.

16.4.10 ADC Watchdog Enable Register (ADC_AWDEN)

Address offset: 0x20

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved						AWDENx[9:0]									
						rw									

Bit Field	Name	Description
31:10	Reserved	Reserved, the reset value must be maintained.
9:0	AWDENx[9:0]	ADC Analog Watchdog Monitoring Data Enable Bits BIT0: DAT0 Watchdog Monitoring Enable BIT1: DAT1 Watchdog Monitoring Enable … BIT8: DAT8 Watchdog Monitoring Enable BIT9: DAT9 Watchdog Monitoring Enable

16.4.11 ADC Segment Configuration Register (ADC_PHCFG)

Address offset:0x24

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

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Reserved														TRIGMD[1:0]	
														rw	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PH4NUM[3:0]				PH3NUM[3:0]				PH2NUM[3:0]				PH1NUM[3:0]			
rw				rw				rw				rw			

Bit Field	Name	Description
31:18	Reserved	Reserved, the reset value must be maintained.
17:16	TRIGMD[1:0]	Trigger Mode Selection 0: Single-segment trigger; 1: Two-segment trigger; 2: Three-segment sampling; 3: Four-segment trigger
15:12	PH4NUM[3:0]	Number of Samplings for the 4th Segment in Four-segment Sampling Mode
11:8	PH3NUM[3:0]	Number of Samplings for the 3rd Segment in Four-segment Sampling Mode
7:4	PH2NUM[3:0]	Number of Samplings for the 2nd Segment in Four-segment Sampling Mode
3:0	PH1NUM[3:0]	Number of Samplings for the 1st Segment in Four-segment Sampling Mode

16.4.12 ADC Trigger Selection Register (ADC_TRIGSEL)

Address offset:0x28

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PH4EXTSEL[3:0]				PH3EXTSEL[3:0]				PH2EXTSEL[3:0]				PH1EXTSEL[3:0]			
rw				rw				rw				rw			

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SWEN	EXTEN	TIM4_TRGOEN	TIM4_CC2EN	TIM4_CC1EN	TIM3_TRGOEN	TIM3_CC2EN	TIM3_CC1EN	TIM1_TRGOEN	TIM1_CC7EN	TIM1_CC6EN	TIM1_CC5EN	TIM1_CC4EN	TIM1_CC3EN	TIM1_CC2EN	TIM1_CC1EN
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Bit Field	Name	Description
31:16	PHxEXT SEL[3:0]	External Event Select for Regular Group These bits select the external event to start the regular sequence conversion. 0000: TIM1 CC1 event 0001: TIM1 CC2 event 0010: TIM1 CC3 event 0011: TIM1 CC4 event 0100: TIM1 CC5 event 0101: TIM1 CC6 event 0110: TIM1 CC7 event

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Bit Field	Name	Description
		0111: TIM1 TRGO event 1000: TIM3 CC1 event 1001: TIM3 CC2 event 1010: TIM3 TRGO event 1011: TIM4 CC1 event 1100: TIM4 CC2 even 1101: TIM4 TRGO event 1110: EXTI line 1111: SWSTART
15	SWEN	Software Trigger Event 0: Software trigger disabled; 1: Software trigger enabled.
14	EXTIEN	External EXTI Line Event 0: External EXTI line disabled; 1: External EXTI line enabled.
13	TIM4_TRGOEN	Timer 4 TRGO Event 0: Conversion event disabled; 1: Conversion event enabled.
12	TIM4_CC2EN	Timer 4 CC2 Event 0: Conversion event disabled; 1: Conversion event enabled.
11	TIM4_CC1EN	Timer 4 CC1 Event 0: Conversion event disabled; 1: Conversion event enabled.
10	TIM3_TRGOEN	Timer 3 TRGO Event 0: Conversion event disabled 1: Conversion event enabled
9	TIM3_CC2EN	Timer 3 CC2 Event 0: Conversion event disabled 1: Conversion event enabled
8	TIM3_CC1EN	Timer 3 CC1 Event 0: Conversion event disabled 1: Conversion event enabled
7	TIM1_TRGOEN	Timer 1 TRGO Event 0: Conversion event disabled 1: Conversion event enabled
6	TIM1_CC7EN	Timer 1 CC7 Event 0: Conversion event disabled 1: Conversion event enabled
5	TIM1_CC6EN	Timer 1 CC6 Event 0: Conversion event disabled 1: Conversion event enabled
4	TIM1_CC5EN	Timer 1 CC5 Event

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Bit Field	Name	Description
		0: Conversion event disabled 1: Conversion event enabled
3	TIM1_CC4EN	Timer 1 CC4 Event 0: Conversion event disabled 1: Conversion event enabled
2	TIM1_CC3EN	Timer 1 CC3 Event 0: Conversion event disabled 1: Conversion event enabled
1	TIM1_CC2EN	Timer 1 CC2 Event 0: Conversion event disabled 1: Conversion event enabled
0	TIM1_CC1EN	Timer 1 CC1 Event 0: Conversion event disabled 1: Conversion event enabled

16.4.13 ADC Software Configuration Register (ADC_PHSWTRIG)

Address offset:0x2C

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHSWSTART[15:0]															
rw															

Bit Field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained.
15:0	PHSWSTART	Start Conversion in Software Trigger Mode For the 1st segment: Software writes 0xA5A1 For the 2nd segment: Software writes 0xF0F2 For the 3rd segment: Software writes 0x5A53 For the 4th segment: Software writes 0x0FA4

16.4.14 ADC Sequence Register 1 (ADC_SEQ1)

Address offset:0x30

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Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEQ8[3:0]				SEQ7[3:0]				SEQ6[3:0]				SEQ5[3:0]			
rw				rw				rw				rw			

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEQ4[3:0]				SEQ3[3:0]				SEQ2[3:0]				SEQ1[3:0]			
rw				rw				rw				rw			

Bit Field	Name	Description
31:28	SEQ8[3:0]	8th conversion channel number in sequence
27:24	SEQ7[3:0]	7th conversion channel number in sequence
23:20	SEQ6[3:0]	6th conversion channel number in sequence
19:16	SEQ5[3:0]	5th conversion channel number in sequence
15:12	SEQ4[3:0]	4th conversion channel number in sequence
11:8	SEQ3[3:0]	3rd conversion channel number in sequence
7:4	SEQ2[3:0]	2nd conversion channel number in sequence
3:0	SEQ1[3:0]	1st conversion channel number in sequence 0000: channel 0 … 1111：channel 15

16.4.15 ADC Sequence Register 2(ADC_SEQ2)

Address offset:0x34

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								SEQ10[3:0]				SEQ9[3:0]			
								rw				rw			

Bit Field	Name	Description
31:8	Reserved	Reserved, the reset value must be maintained.
7:4	SEQ10[3:0]	10th conversion channel number in sequence
3:0	SEQ9[3:0]	9th conversion channel number in sequence 0000: channel 0

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Bit Field	Name	Description
		… 1111：channel 15

16.4.16 ADC Regular Data Register x (ADC_DATx) (x = 0..9)

Address offset:0x38 – 0x5C

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATx[15:0]															
r															

Bit Field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained.
15:0	DATx[15:0]	Regular Conversion Data These bits are read-only and contain the conversion results of the regular channels. The data is either left-aligned or right-aligned.

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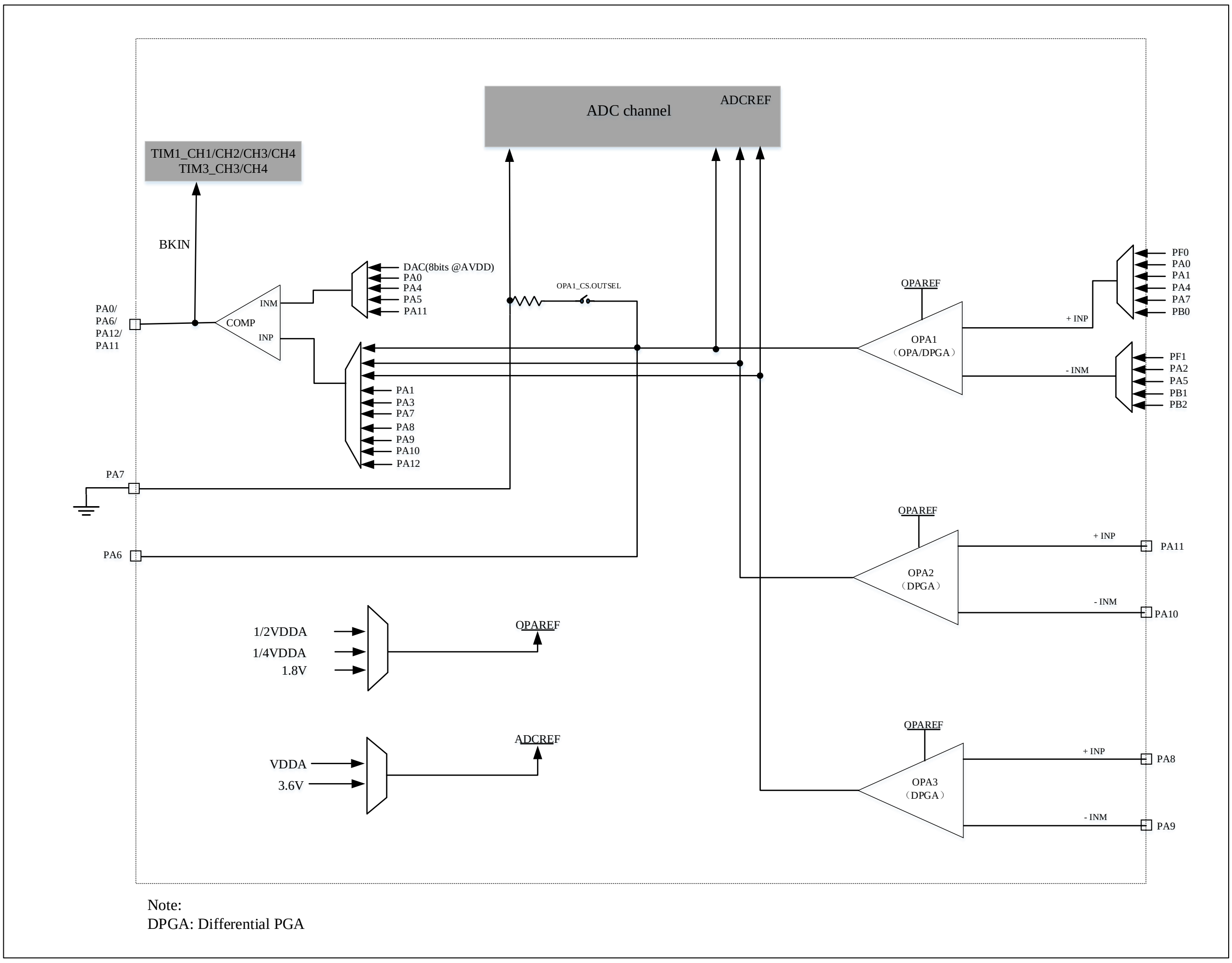
17 Comparator (COMP)

The COMP module is used to compare the analog voltages of two inputs and output high/low levels based on the comparison results.When the input voltage of "INP" is higher than the input voltage of "INM", the comparator output is high; when the input voltage of "INP" is lower than the input voltage of "INM", the comparator output is low.

17.1 COMP System Connection Block Diagram

The COMP module supports an independent comparator, which is connected to the APB bus.

Figure 17-1 Comparator System Connection Diagram



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17.2 COMP Features

- One independent comparator
- Internal reference input for the independent 8-bit DAC
- Supports filter clock
- Output polarity can be configured as high and low
- The hysteresis can be configured with none, low, medium, or high
- The comparison result can be output to the I/O port or trigger timer, which is used to capture events, OCREF_CLR events, brake events, and generate interrupts
- Input channels can select I/O ports or the dedicated 8-bit DAC (multiple selections allowed)
- The COMP_CTRL register can be configured as read-only or read-write; when locked, it can only be unlocked via system reset or module resetSupports blanking, configurable blanking source
- Supports blanking, with configurable blanking sources for generating blanking signals
- Filter window size can be configured
- Filter threshold size can be configured
- Filter sampling frequency can be configured

17.3 COMP Configuration Precedure

The complete configuration items are as follows. If the default configuration is used, skip the corresponding configuration items.

- Configure hysteresis level COMP_CTRL.HYST[1:0].
- Configure the output polarity COMP_CTRL.POL.
- Configure input selection, comparator positive COMP_CTRL.INPSEL[3:0], negative COMP_CTRL.INMSEL[2:0].
- Configure the blanking source COMP_CTRL.BLKING[2:0].
- Configure the filter sampling window COMP_FILC.SAMPW[4:0].
- Configure the threshold COMP_FILC.THRESH[4:0](Threshold should be greater than COMP_FILC.SAMPW[4:0]/2).
- Configure the filter sampling frequency
- Enable COMP_FILC.FILEN filter.
- Enable COMP_CTRL.EN on the comparator.

Note:

1. *For the above steps, the filter should be enabled first and then the comparator should be enabled. The comparator should be enabled after the filtering (if enabled) is configured and enabled. In addition, when the comparator control register is locked, it can only be unlocked by reset.*

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2. *For potential glitches in the comparator input signal, configure the filter length and hysteresis level according to the actual glitch size to filter them out.*

17.4 COMP Operating Mode

17.4.1 Independent Comparator

One comparator can be configured independently to complete the comparator functions. The output of the comparator can be output to I/O ports. The comparator supports different remapping ports. And the output of the comparator can be selected and connected to the corresponding port by configuration.

The comparator output supports triggering events, for example, it can be configured as timer 1 brake function.

Note: Refer to the comparator interconnection for specific configuration

17.5 Comparator Interconnection

For the interconnection of comparator output ports, you can refer to the chapter on GPIO multiplexing functions, which defines the remapping values of the comparator OUT.

The comparator OUT pins are as follows:

Table 17-1 OUT pin

COMP_OUT
PA0
PA6
PA11
PA12

The comparator INP pins have the following configurations:

Table 17-2 INP pins congfiguration

INPSEL	COMP
0000	OPA1.out
0001	OPA2.out
0010	OPA3.out
0011	PA1
0100	PA3
0101	PA7
0110	PA8
0111	PA9
1000	PA10
1001	PA12
Other:Reserved	

The comparator INM pins have the following configuration:

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Table 17-3 INM pins congfiguration

INMSEL	COMP1
000	VREF1
001	PA0
010	PA4
011	PA5
100	PA11

17.6 Interrupt

COMP supports interrupt response. There are two types of interrupts.

- The polarity of COMP_CTRL.POL is not reversed and the interrupt is enabled. When INPSEL > INMSEL, the comparator interrupt will be generated when COMP_CTRL.OUT is set to 1 by hardware.
- The polarity of COMP_CTRL.POL is reversed and the interrupt is enabled. When INPSEL < INMSEL, the comparator interrupt will be generated when COMP_CTRL.OUT is set to 1 by hardware.

Note: To use the COMP interrupt, you must first configure the EXTI line. Please refer to the NVIC chapter.

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17.7 COMP Registers

17.7.1 COMP Register Overview

Table 17-4 COMP Register Overview

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
00h	COMP_INTEN	Reserved																															CMPIEN
04h	COMP_INTSTS	Reserved																															CMPIS
08h	Reserved																																
0Ch	COMP_LOCK	Reserved																															CMPLK
10h	COMP_CTRL	Reserved										CLKSEL	PWRMD	Reserved	OUT	Reserved		BLKING	HYST		POL	Reserved				INPSEL[2:0]			INMSEL[3:0]				EN
14h	COMP_FILC	Reserved																					SAMPW [4:0]					THRESH [4:0]					FILEN
18h	COMP_FILP	Reserved																CLKPSC[15:0]															
1Ch ~ 3Ch	Reserved																																
40h	COMP_INVREF	Reserved																					VREFSEL[7:0]										VREFEN

17.7.2 COMP Interrupt Enable Register (COMP_INTEN)

Address offset : 0x00

Reset value : 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved															CMPIEN

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rw

Bit Field	Name	Description
31:1	Reserved	Reserved, the reset value must be maintained
0	CMPIEN	Comparator Interrupt Enable 0: Disable comparator interrupt 1: Enable comparator interrupt

17.7.3 COMP Interrupt Status Register (COMP_INTSTS)

Address offset : 0x04

Reset value : 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved															CMPIS
															rc_w1

Bit Field	Name	Description
31:1	Reserved	Reserved, the reset value must be maintained
0	CMPIS	Comparator Interrupt Status Bit Writing 1 clears the bit

17.7.4 COMP Lock Register (COMP_LOCK)

Address offset : 0x0C

Reset value : 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved															CMPLK
															rw

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Bit Field	Name	Description
31:1	Reserved	Reserved, the reset value must be maintained
0	CMPLK	It can only be written once and is controlled by software; it can only be cleared via system reset/module reset. Setting this bit configures COMP_CTRL register as read-only. 0: COMP_CTRL is read-write 1: COMP_CTRL is read-only

17.7.5 COMP Control Register (COMP_CTRL)

Address offset : 0x10

Reset value : 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved											CLKSEL	PWRMD	Reserved	OUT	Reserved
											rw	rw		rw	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved	BLKING	HYST[1:0]		POL	Reserved			INPSEL[3:0]				INMSEL[2:0]			EN
	rw	rw		rw				rw				rw			rw

Bit Field	Name	Description
31:21	Reserved	Reserved, the reset value must be maintained
20	CLKSEL	Clock Selection 0: COMP clock is selected from HSI (64M); 1: COMP clock is selected from LSI (32K), which is often used in low-power mode;
19	PWRMD	Indication of Comparator Control Mode Selection 0: Normal mode 1: Low-power mode
18	Reserved	Reserved, the reset value must be maintained
17	OUT	Indication of Comparator Output Status 0: Output low 1: Output high
16:15	Reserved	Reserved, the reset value must be maintained
14	BLKING	Comparator Output Blanking 0: No blanking 1: Select TIM1_CC5 as the blanking source
13:12	HYST[1:0]	These bits select the hysteresis level of the comparator. 00: No hysteresis 01: Low hysteresis 10: Medium hysteresis

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Bit Field	Name	Description
		11: High hysteresis
11	POL	This bit is used to invert the comparator output. 0: Output not inverted 1: Output inverted
10:8	Reserved	Reserved, the reset value must be maintained
7:4	INPSEL[3:0]	4'b0000: Output of OPAMP1; 4'b0001: Output of OPAMP2; 4'b0010: Output of OPAMP3; 4'b0011: PA1; 4'b0100: PA3; 4'b0101: PA7; 4'b0110: PA8; 4'b0111: PA9; 4'b1000: PA10; 4'b1001: PA12; other: Reserved
3:1	INMSEL[2:0]	Comparator Negative Input Selection Bits 3'b000: VREF1(8-bit DAC); 3'b001: PA0; 3'b010: PA4; 3'b011: PA5; 3'b100: PA11
0	EN	Bit for Turning COMP On/Off 0: Comparator disable; 1: Comparator enable.

17.7.6 COMP Filter Control Register (COMP_FILC)

Address offset : 0x14

Reset value : 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved					SAMPW[4:0]					THRESH[4:0]					FILEN
							rw					rw			rw

Bit Field	Name	Description
31:11	Reserved	Reserved, the reset value must be maintained

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Bit Field	**Name**	**Description**
10:6	SAMPW[4:0]	Low-Pass Filter Sampling Window Size The sampling window size is calculated as Sampling Window = SAMPW + 1
5:1	THRESH[4:0]	Low-Pass Filter Threshold Setting This threshold specifies the minimum number of samples with an opposite state that must appear within the sampling window to change the output state. This value is required to be greater than SAMPW / 2.
0	FILEN	Filter Enable Bit 0: Disable; 1: Enable;

17.7.7 COMP Filter Clock Register (COMP_FILP)

Address offset : 0x18

Reset value : 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CLKPSC[15:0]															
rw															

Bit Field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained
15:0	CLKPSC[15:0]	Prescaler for Low-Pass Filter Sampling Clock The system clock division factor is calculated as System Clock Division Factor = CLKPSC + 1. 0: Every 1 clock cycle; 1: Every 2 clock cycles; 2: Every 3 clock cycles; … 65535: Every 65536 clock cycles;

17.7.8 COMP Reference Input Comparison Voltage Register (COMP_ INVREF)

Address offset : 0x40

Reset value : 0x0000 0000

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved							VREFSEL[7:0]								VREFEN
							rw								rw

Bit Field	Name	Description
31:9	Reserved	Reserved, the reset value must be maintained
8:1	VREFSEL[7:0]	Voltage Control Reference Input Comparison Voltage VREF1 Level Selection The value range 0 ~ 0b'11111111 corresponds to an output voltage range of 0 ~ VREF1+, with a total of 255 level. For example, a value of 51 represents an output voltage of: (51) × VREF1+ / 255 = (1/5)VREF1+.
0	VREFEN	Internal DAC Enable 0: Disable; 1: Enable;

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18 Operational Amplifier (OPAMP)

The OPAMP module supports flexible configuration and is suitable for applications in modes such as independent operational amplifier (op-amp), programmable gain amplifier (PGA), and voltage follower.OPAMP has an input range of 0V to VDDA and an output range of 0.4V to VDDA-0.4V.

18.1 OPAMP Features

- OPA1 supports independent op-amp mode, follower mode, differential PGA mode, and single-ended PGA mode; OPA2 and OPA3 support differential PGA mode and follower mode.
- Supports rail-to-rail input. The input range is 0 to VDDA, and the output range is 0.4 to VDDA - 0.4. Programmable gain is available.
- The OPAMP can be configured as an instrumentation amplifier via external resistor connection.
- The internal resistor feedback network is configurable , 2% accuracy
- Programmable gain setting.
- OPA1 single-ended PGA gain: 2X, 4X, 8X, 16X, 32X.
- OPA1 differential PGA gain: 1X, 2X, 4X, 8X, 16X, 32X.
- OPA2 and OPA3 differential PGA gain: 1X, 2X, 4X, 8X, 16X.
- Gain bandwidth: 5MHz
- Independent write protection is supported

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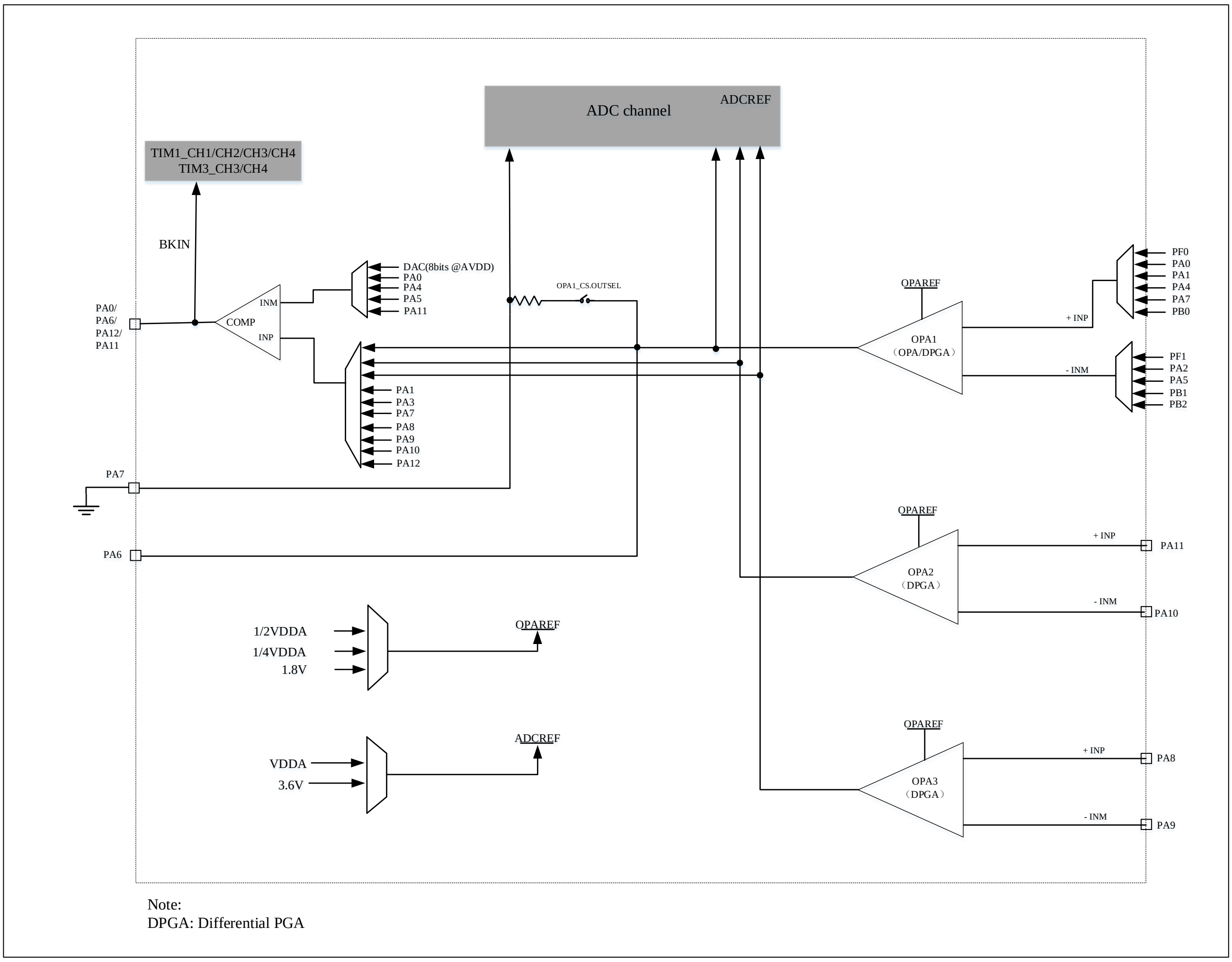
18.2 OPAMP Function Description

The OPAMP has two inputs (VP, VM) and one output. Different GPIOs can be selected for connection to the VP/VM input terminals, and the output of the OPAMP can be used as the input for the COMP (Comparator) or ADC (Analog-to-Digital Converter).

The specific connections are shown in the figure below

Figure 18-1 OPAMP System Connection Diagram



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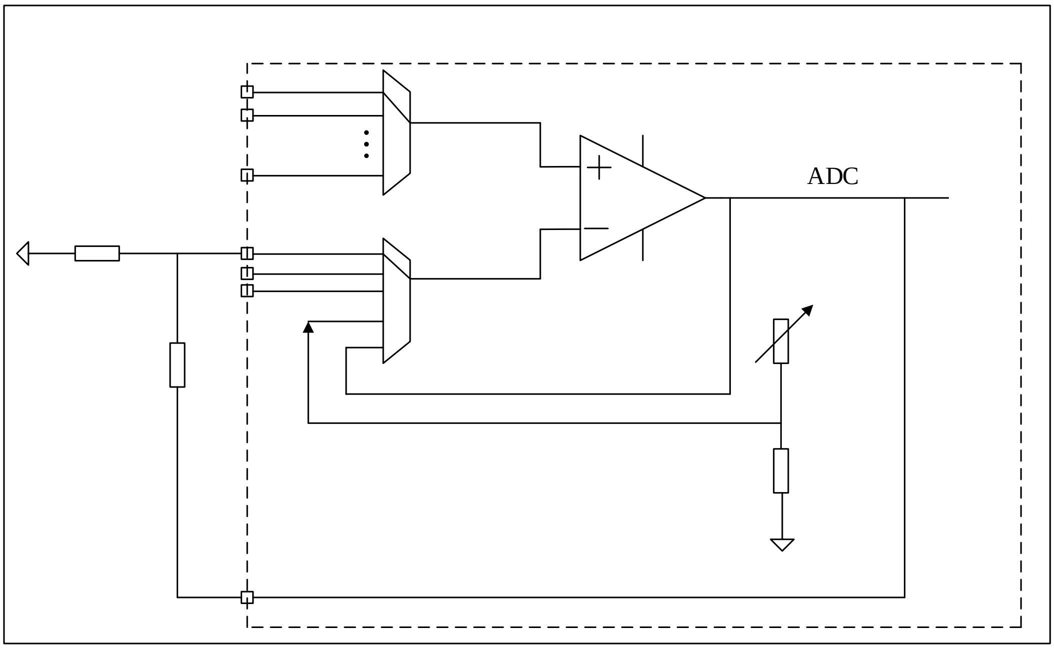
18.3 OPAMP Working Mode

18.3.1 OPAMP1 External Amplification Mode (Supported Only by OPA1)

In the external amplification mode, the amplification factor is determined by the connected resistors and capacitors. For OPAMP1_CS.MOD = 00 (general mode), OPAMP1_CS.VPSEL is used to select the non-inverting input (VP), and OPAMP1_CS.VMSEL is used to select the inverting input (VM). External resistors are used to form a closed-loop amplification system.

Figure 18-2 OPAMP1 External Amplification Mode



18.3.2 OPAMP1 Follow Mode

In follow mode, the voltage is directly follow. The VMSEL terminal must be directly connected to the OPAMP output port.

OPAMP1_CS.MOD = "11" enables the internal follower function. For this configuration, OPAMP1_CS.VPSEL is used to select the non-inverting input (VP), and OPAMP1_CS.VMSEL is internally connected to the output port by the chip. For OPAMP2, OPAMP2_CS.MOD = '1' enables the internal follower function; similarly, OPAMP3_CS.MOD = '1' enables the internal follower function for OPAMP3.

A VM pin that is not occupied can be used as another GPIO.

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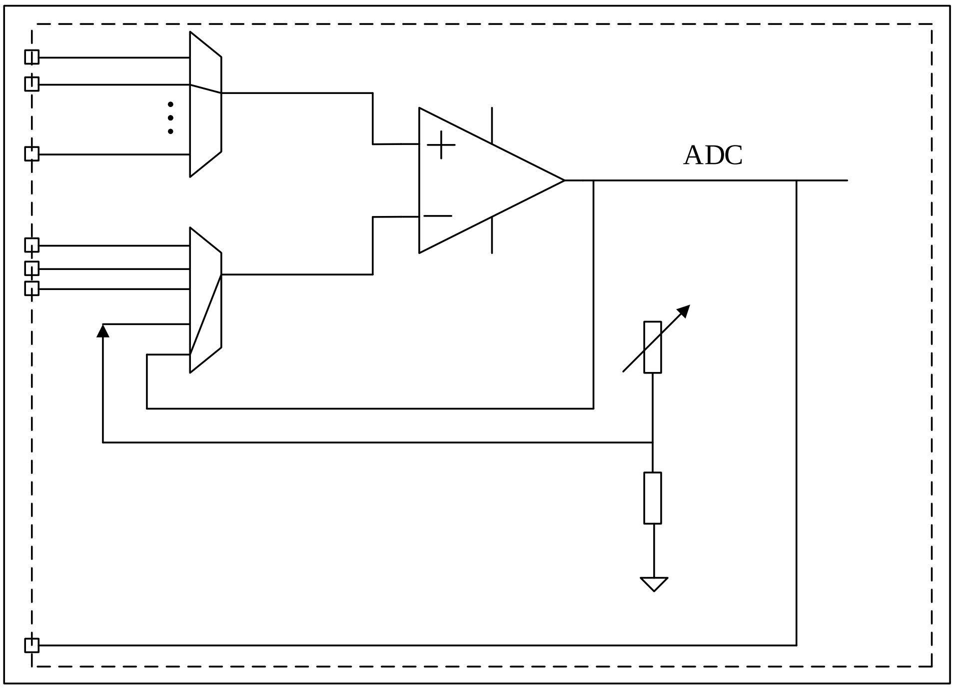
Figure 18-3 OPAMP1 Follow mode



18.3.3 OPAMP Internal Gain (PGA) mode

The single-ended gain amplification mode, the PGA (Programmable Gain Amplifier) mode, amplifies the input voltage through a built-in resistor feedback network.

When OPAMP1_CS.MOD is set to "10", the PGA function is enabled, supporting amplification factors of 2/ 4/ 8/ 16/ 32. The OPAMP1_CS.VMSEL pin must be configured as floating. OPAMP1_CS.VPSEL is used to select the non-inverting input (VP).

The unused input pins of OPAMP1's VM (inverting input) and VP (non-inverting input) can be used as ordinary GPIOs (General-Purpose Input/Output).

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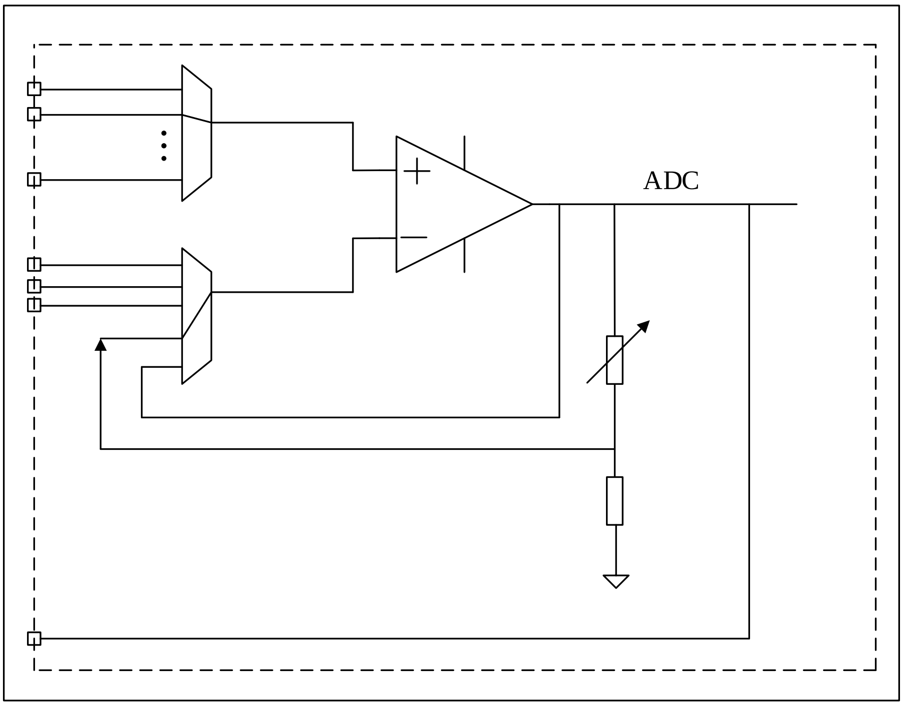
Figure 18-4 Internal gain mode



18.3.4 Differential Gain Mode

In the differential amplification mode, the amplification voltage is adjustable. OPAMP1 supports amplification factors of 1/ 2/ 4/ 8/ 16/ 32, while OPAMP2 and OPAMP3 support amplification factors of 1/ 2/ 4/ 8/ 16. Select appropriate VP (non-inverting input) and VM (inverting input) based on requirements: the output pin of OPAMP1 can be used as an amplified output, whereas OPAMP2 and OPAMP3 have no output pins.

Unused VP/VM input pins can be used as ordinary GPIO

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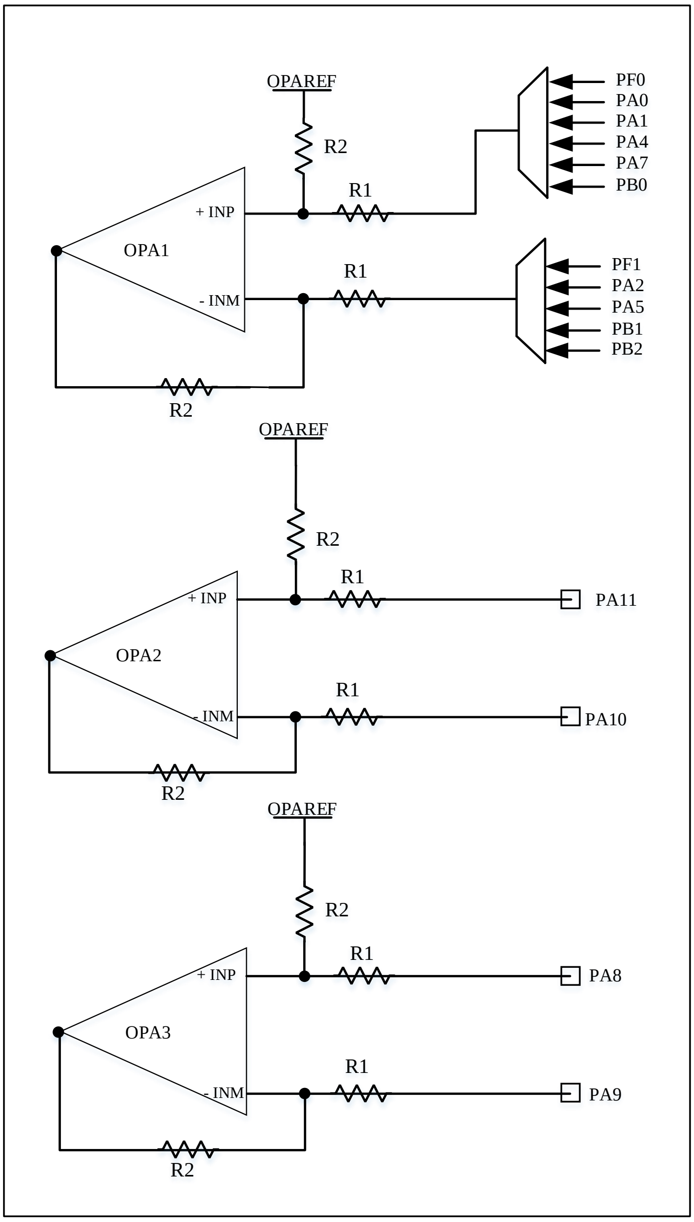
Figure 18-5 Differential Gain mode



18.3.5 OPAMP Write Protection

The write protection for OPAMP1, OPAMP2, and OPAMP3 can be configured by setting the OPAMP_LOCK register. Once write protection is enabled, the software will be unable to perform write operations on the corresponding control registers of OPAMP1, OPAMP2, and OPAMP3. The write protection function can be cancelled after chip reset or OPAMP module reset.

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18.4 OPAMP register

18.4.1 OPAMP register overview

Table 18-1 OPAMP register overview

<table>
<tr><th>Offset</th><th>Register</th><th>31</th><th>30</th><th>29</th><th>28</th><th>27</th><th>26</th><th>25</th><th>24</th><th>23</th><th>22</th><th>21</th><th>20</th><th>19</th><th>18</th><th>17</th><th>16</th><th>15</th><th>14</th><th>13</th><th>12</th><th>11</th><th>10</th><th>9</th><th>8</th><th>7</th><th>6</th><th>5</th><th>4</th><th>3</th><th>2</th><th>1</th><th>0</th></tr>
<tr><td>0x00</td><td>OPAMP1_CS</td><td colspan="16">Reserved</td><td>OUTSEL</td><td colspan="3">VMSEL[2:0]</td><td>Reserved</td><td colspan="3">VPSEL[2:0]</td><td colspan="2">Reserved</td><td colspan="3">GAIN[2:0]</td><td colspan="2">MOD[1:0]</td><td>EN</td></tr>
<tr><td>0x04</td><td>OPAMP2_CS</td><td colspan="26">Reserved</td><td colspan="3">GAIN[2:0]</td><td>Reserved</td><td>MOD</td><td>EN</td></tr>
<tr><td>0x08</td><td>OPAMP3_CS</td><td colspan="26">Reserved</td><td colspan="3">GAIN[2:0]</td><td>Reserved</td><td>MOD</td><td>EN</td></tr>
<tr><td>0xC</td><td>OPAMP_LOCK</td><td colspan="31">Reserved</td><td>OPAMP0LK</td></tr>
<tr><td>0x10</td><td>OPAMP_VREFSEL</td><td colspan="26">Reserved</td><td colspan="2">OPA3SEL[1:0]</td><td colspan="2">OPA2SEL[1:0]</td><td colspan="2">OPA1SEL[1:0]</td></tr>
</table>

18.4.2 OPAMP Control Register 1(OPAMP1_CS)

Offset address: 0x00

Reset value: 0x0000 0000

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="16">Reserved</td></tr>
</table>

<table>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>OUTSEL</td><td colspan="3">VMSEL[2:0]</td><td>Reserved</td><td colspan="3">VPSEL[2:0]</td><td colspan="2">Reserved</td><td colspan="3">GAIN[2:0]</td><td colspan="2">MOD[1:0]</td><td>EN</td></tr>
<tr><td>rw</td><td colspan="3">rw</td><td></td><td colspan="3">rw</td><td colspan="2"></td><td colspan="3">rw</td><td colspan="2">rw</td><td>rw</td></tr>
</table>

Bit Field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained
15	OUTSEL	1: A 40k resistor is added externally to the OPAMP1 output. 0: No 40k resistor is added to the OPAMP1 output.
14:12	VMSEL [2:0]	Inverted input selection for OPAMP1: 000: PF1

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Bit Field	Name	Description
		001: PA2 010: PA5 011: PB1 100: PB2 Default value = 3'b000
11	Reserved	Reserved, the reset value must be maintained
10:8	VPSEL[2:0]	Non inverted input selection for OPAMP1 000: PF0 001: PA0 010: PA1 011: PA4 100: PA7 101: PB0 default value =0000
7:6	Reserved	Reserved, the reset value must be maintained
5:3	GAIN[2:0]	OPAMP1 Gain Control When OPAMP1_CS.MOD[1:0] = 2b'01: 000: Differential PGA Gain = 1; 001: Differential PGA Gain = 2; 010: Differential PGA Gain = 4; 011: Differential PGA Gain = 8; 100: Differential PGA Gain = 16; 101: Differential PGA Gain = 32; When OPAMP1_CS.MOD[1:0] = 2b'10: 000: Internal PGA Gain = 2; 001: Internal PGA Gain = 4; 010: Internal PGA Gain = 8; 011: Internal PGA Gain = 16; 100: Internal PGA Gain = 32;
2:1	MOD[1:0]	OPAMP1 Operating Mode Selection 00: General OPA Mode; 01: Differential PGA Mode; 10: Internal PGA Mode; 11: Internal BUFFER Mode;
0	EN	OPAMP1 Enable 0: Disable 1: Enable

18.4.3 OPAMP Control Register 2 (OPAMP2_CS)

Offset address: 0x4

Reset value: 0x0000 0000

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved										GAIN[2:0]			Reserved	MOD	EN
											rw			rw	rw

Bit Field	Name	Description
31:6	Reserved	Reserved, the reset value must be maintained
5:3	GAIN[2:0]	OPAMP2 Gain Control 000: Differential PGA2 Gain = 1; 001: Differential PGA2 Gain = 2; 010: Differential PGA2 Gain = 4; 011: Differential PGA2 Gain = 8; 100: Differential PGA2 Gain = 16;
2	Reserved	Reserved, the reset value must be maintained
1	MOD	OPAMP2 Operating Mode Control Signal 0: Differential PGA Mode 1: Internal BUFFER Mode
0	EN	1：OPAMP2 Enable 0：OPAMP2 Disable

18.4.4 OPAMP Control Register 3（OPAMP3_CS）

Address offset:0x08

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved										GAIN[2:0]			Reserved	MOD	EN
											rw			rw	rw

Bit Field	Name	Description
31:6	Reserved	Reserved, the reset value must be maintained
5:3	GAIN[2:0]	OPAMP3 Gain Control 000: Differential PGA Gain = 1;

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Bit Field	Name	Description
		001: Differential PGA Gain = 2; 010: Differential PGA Gain = 4; 011: Differential PGA Gain = 8; 100: Differential PGA Gain = 16;
2	Reserved	Reserved, the reset value must be maintained
1	MOD	OPAMP3 Operating Mode Control Signal 0: Differential PGA Mode 1: Internal BUFFER Mode
0	EN	1：OPAMP3 Enable 0：OPAMP3 Disable

18.4.5 OPAMP Lock Register (OPAMP_LOCK)

Offset address: 0x0C

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved															OPALK
															rw

Bit Field	**Name**	**Description**
31:1	Reserved	Reserved, the reset value must be maintained
0	OPALK	Write-Once (WO): Controlled by software, and can only be cleared via system reset/module reset.Setting this bit configures the OPAMP1_CS/OPAMP2_CS/OPAMP3_CS registers as read-only. 0: The OPAMP1_CS/OPAMP2_CS/OPAMP3_CS registers are read-write. 1: The OPAMP1_CS/OPAMP2_CS/OPAMP3_CS registers are read-only…

18.4.6 OPAMP Reference Voltage Selection Register（OPAMP_VREFSEL）

Offset address: 0x10

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

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15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved										OPA3SEL[2:0]		OPA2SEL[2:0]		OPA1SEL[2:0]	
										rw		rw		rw	

Bit Field	Name	Description
31:6	Reserved	Reserved, the reset value must be maintained
5:4	OPA3SEL[1:0]	OPAMP3 Reference Voltage Selection 00: Reference voltage selected as 0.9V, output is 1.8V; 01: Reference voltage selected as VDD/8, output is VDD/4; 10: Reference voltage selected as VDD/4, output is VDD/2; 11: Reserved;
3:2	OPA2SEL[1:0]	OPAMP2 Reference Voltage Selection 00: Reference voltage selected as 0.9V, output is 1.8V; 01: Reference voltage selected as VDD/8, output is VDD/4; 10: Reference voltage selected as VDD/4, output is VDD/2; 11: Reserved;
1:0	OPA1SEL[1:0]	OPAMP1 Reference Voltage Selection 00: Reference voltage selected as 0.9V, output is 1.8V; 01: Reference voltage selected as VDD/8, output is VDD/4; 10: Reference voltage selected as VDD/4, output is VDD/2; 11: Reserved;

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19 Independent Watchdog (IWDG)

19.1 Introduction

A built-in Independent Watchdog (IWDG) is provided to address issues caused by software errors. The watchdog timer offers high flexibility in use, enhancing system security and the accuracy of timing control.

The Independent Watchdog (IWDG) is driven by a low-speed internal clock (LSI clock) operating at 32KHz. It remains operational even in the event of a dead loop or MCU lock-up, thereby providing a higher level of security, timing precision, and watchdog flexibility. It can resolve system failures caused by software glitches through reset. The IWDG is most suitable for applications that require the watchdog to run as a fully independent process outside the main application, with relatively low constraints on timing accuracy.

When the PWR_CTRL.IWDGRSTEN bit in the power control register is set to '1', a system reset will be generated when the IWDG counter reaches 0 (if this bit is set to '0', the IWDG will count but not generate a reset). The IWDG reset can also be used for low-power wake-up.

Note: This chapter is described based on the system default value of PWR_CTRL.IWDGRSTEN = 1.

19.2 Main Features

- Independent 14-bit downcounter
- RC oscillator provides an independent clock source, which can work normally in STOP mode
- Can support both reset and low-power wake-up functions
- When the downcounter reaches 0x000, the system resets (if the watchdog is activated)

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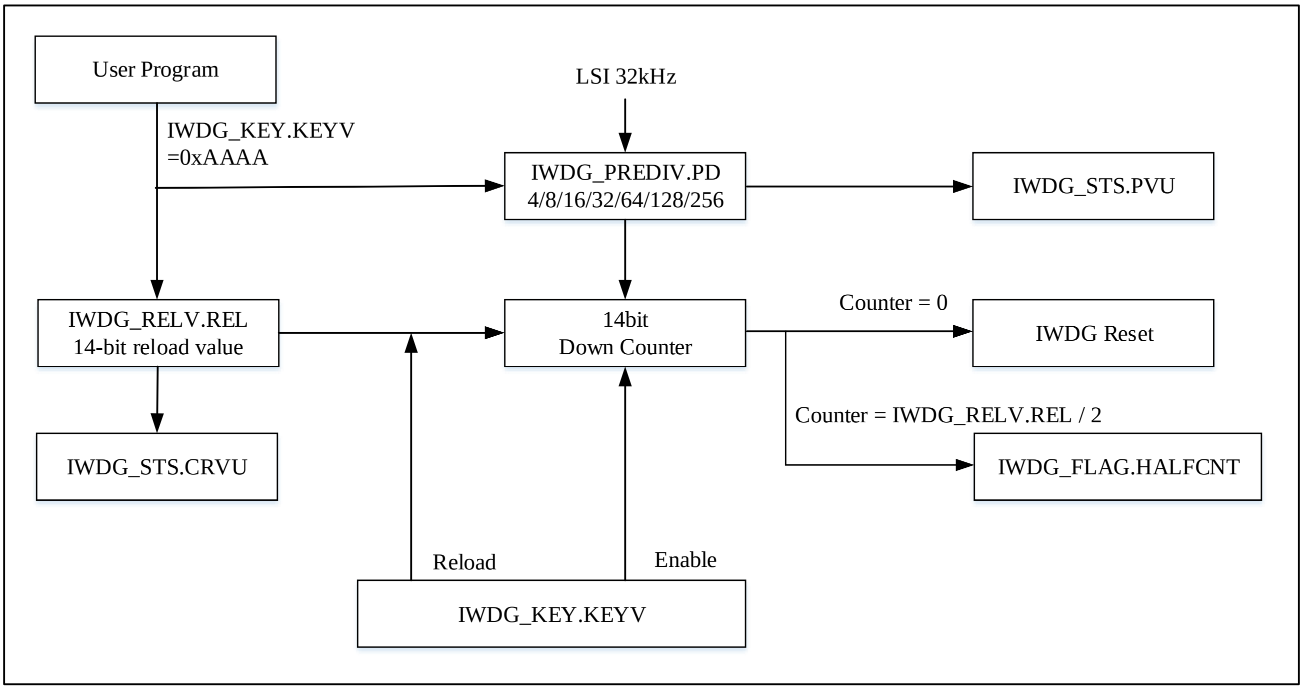
19.3 Functional Description

Figure 19-1 Independent Watchdog Functional Block Diagram



To enable the IWDG, we need to write 0xCCCC to the IWDG_KEY.KEYV[15:0] bits; the counter will then start decrementing. When the counter counts down to 0x000, it generates a reset signal (IWDG_RESET) to the MCU. In addition, as long as 0xAAAA (reload request) is written to the IWDG_KEY.KEYV[15:0] bits before the reset occurs, the counter value will be set to the reload value in the IWDG_RELV.REL[13:0] bits, thereby preventing the watchdog from resetting the entire device.

If the "Hardware Watchdog Timer" function is enabled via the option bytes, the watchdog will automatically start running after the system is powered on and generate a system reset—unless the software reloads the counter before the counter reaches '0'.

If the "Interrupt Function" is enabled, the watchdog will generate an interrupt after the counter reaches "IWDG_RELV.REL / 2".

19.3.1 Register Access Protection

The IWDG_PREDIV and IWDG_RELV registers have a write protection function. Before modifying the data in these two registers, the IWDG_KEY register must first be configured to 0x5555. Configuring it to any other value will re-enable the register write protection. IWDG_STS.PVU indicates whether the prescaler value update is in progress. IWDG_STS.CRVU indicates whether the IWDG is updating the reload value. When the prescaler value and/or reload value is being updated, the hardware sets the IWDG_STS.PVU bit and/or IWDG_STS.CRVU bit. After the prescaler value and/or reload value update is completed, the hardware clears the IWDG_STS.PVU bit and/or IWDG_STS.CRVU bit.

The reload operation (configuring IWDG_KEY to 0xAAAA) will also enable the write protection function.

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19.3.2 IWDG Interrupt

If IWDG_CTRL.ITE is configured to 1, when the DOWN COUNTER of the IWDG is less than or equal to IWDG_REVL.RVL[13:0]/2, the corresponding IWDG interrupt will be generated, and the interrupt must be exited by feeding the watchdog.

19.3.3 IWDG Freeze

Once IWDG is enabled (whether in hardware or software), it will not stop counting unless the system is reset or the IWDG is frozen.

Write 0x4567 to IWDG_KEY.KEYV [15:0] to enable freezing, and write 0x89AB to IWDG_KEY.KEYV [15:0] to exit thawing.

19.3.4 Debug Mode

In debug mode (when the Cortex-M0 core is halted), the IWDG counter will either continue to work normally or stop, depending on the DBG_CTRL.IWDG_STOP bit in the debug module. If this bit is set to "1", the counter stops. When this bit is "0", the counter works normally.

19.4 User Interface

The user interface of the IWDG module consists of 4 registers: the Key Register (IWDG_KEY), the Prescaler Register (IWDG_PREDIV), the Reload Register (IWDG_RELV), and the Status Register (IWDG_STS).

19.4.1 Operation Flow

The IWDG is enabled when reset either by software (writing 0xAAAA to the IWDG_KEY.KEYV[15:0] bits) or hardware (clearing the FLASH_OB.WDG_SW bit). Upon enabling, it starts counting down from 0xFFF. The interval of the down-counting is determined by the LSI clock after prescaling. After the counter is reloaded, the value for the new round of down-counting starts from the value in IWDG_RELV.REL[13:0] instead of 0xFFF.

During the normal operation of the program, the software needs to "feed the watchdog" before the counter reaches 0 to start a new round of down-counting. When the counter reaches 0, it indicates a program fault. In this case, the IWDG generates a reset signal.

If the user intends to configure the IWDG prescaler and reload value registers, they must first write 0x5555 to IWDG_KEY.KEYV[15:0], and then check the IWDG_STS.CRVU bit and IWDG_STS.PVU bit. The IWDG_STS.CRVU bit indicates that the reload value update is in progress, while the IWDG_STS.PVU bit indicates that the prescaler value update is in progress. The user can only update the corresponding values when both bits are 0. When an update is in progress, the hardware sets the corresponding bit to 1. At this time, reading IWDG_PREDIV.PD[2:0] or IWDG_RELV.REL[13:0] is invalid, as the data needs to be synchronized to the LSI clock domain. The values read from IWDG_PREDIV.PD[2:0] or IWDG_RELV.REL[13:0] will only become valid after the hardware clears the IWDG_STS.PVU bit or IWDG_STS.CRVU bit.

If the application uses multiple reload values or prescaler values, it must wait until the IWDG_STS.CRVU bit is reset before changing the reload value, and wait until the IWDG_STS.PVU bit is reset before changing the prescaler value.

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However, after updating both the prescaler value and the reload value, or only updating the prescaler value, or only updating the reload value, there is no need to wait for the IWDG_STS.CRVU bit or IWDG_STS.PVU bit to be reset before continuing to execute the code (even in the case of entering low-power mode, the write operation will be considered and completed).

The prescaler register and reload register control the time when a reset is generated, as shown in Table 19-1.

Table 19-1 IWDGMaximum and Minimum Reset Time of Counting

Prescaler Factor	PD [2:0]	Minimum Time（ms） REL[13:0]=0x000	Maximum Time（ms） REL[13:0]=0xFFF
/4	000	0.125	2048
/8	001	0.25	4096
/16	010	0.5	8192
/32	011	1.0	16384
/64	100	2	32768
/128	101	4	65536
/256	11x	8	131072

19.4.2 IWDG Configuration Flow

Software Configuration Flow:

1. Write 0x5555 to the IWDG_KEY.KEYV[15:0] bits to enable write access to the IWDG_PREDIV and IWDG_RELV registers;
2. Check the IWDG_STS.PVU bit or IWDG_STS.CRVU bit. If the bit is 0, proceed to the next step;
3. Configure the IWDG_PREDIV.PD[2:0] bits to select the prescaler value;
4. Configure the reload value for the IWDG_RELV.REL[13:0] bits;
5. Write 0xAAAA to the IWDG_KEY.KEYV[15:0] bits to update the counter with the reload value;
6. Enable the watchdog by writing 0xCCCC to the IWDG_KEY.KEYV[15:0] bits via software or hardware.

   If the user wants to change the prescaler value and reload value, repeat steps 1–5. If not, only perform the watchdog feeding operation as described in step 5.

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19.5 IWDG Registers

19.5.1 IWDG Registers Overview

Table 19-2 IWDG Registers Overview

<table>
<tr><th>Offset</th><th>Register</th><th>31</th><th>30</th><th>29</th><th>28</th><th>27</th><th>26</th><th>25</th><th>24</th><th>23</th><th>22</th><th>21</th><th>20</th><th>19</th><th>18</th><th>17</th><th>16</th><th>15</th><th>14</th><th>13</th><th>12</th><th>11</th><th>10</th><th>9</th><th>8</th><th>7</th><th>6</th><th>5</th><th>4</th><th>3</th><th>2</th><th>1</th><th>0</th></tr>
<tr><td>00h</td><td>IWDG_KEY</td><td colspan="16">Reserved</td><td colspan="16">KEYV[15:0]</td></tr>
<tr><td>04h</td><td>IWDG_STS</td><td colspan="29">Reserved</td><td>FREF</td><td>CRVU</td><td>PVU</td></tr>
<tr><td>08h</td><td>IWDG_PREDIV</td><td colspan="29">Reserved</td><td colspan="3">PD[2:0]</td></tr>
<tr><td>0Ch</td><td>IWDG_RELV</td><td colspan="18">Reserved</td><td colspan="14">REL[13:0]</td></tr>
<tr><td>10h</td><td>IWDG_CTRL</td><td colspan="31">Reserved</td><td>ITE</td></tr>
</table>

19.5.2 IWDG Key Register（IWDG_KEY）

Offset address: 0x00

Reset value: 0x0000 0000

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="16">Reserved</td></tr>
</table>

<table>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="16">KEYV[15:0]</td></tr>
<tr><td colspan="16">rc_w0</td></tr>
</table>

Bit Field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained
15:0	KEYV[15:0]	Key Register: Only specific values can perform specific functions 0xCCCC: Starts the watchdog counter; invalid if the hardware watchdog is enabled (Start) 0xAAAA: Reloads the counter with the REL value in the IWDG_RELV register to prevent reset (Watchdog Feeding) 0x5555: Disables the write protection of the IWDG_PREDIV and IWDG_RELV registers (Protection Release) 0x4567: IWDG freezes, counter stops running 0x89AB: Exit IWDG freeze state, counter resumes operation

19.5.3 IWDG Status Register (IWDG_STS)

Offset address: 0x04

Reset value: 0x0000 0000

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved													FREF	CRVU	PVU
													r	r	r

Bit Field	Name	Description
31:3	Reserved	Reserved, the reset value must be maintained
2	FREF	Watch dog frozen state Freeze status: This bit indicates the freeze function status. 0: Freeze function disabled 1: Freeze function enabled
1	CRVU	Watchdog Reload Value Update Reload Value Update: This bit indicates that the reload value is being updated. It is set and cleared by hardware. Software can only attempt to modify the value of IWDG_RELV.REL[13:0] when the value of IWDG_KEY.KEYV[15:0] is 0x5555 and this bit is 0.
0	PVU	Watchdog Prescaler Value Update Prescaler Value Update: This bit indicates that the prescaler value is being updated. It is set and cleared by hardware. Software can only attempt to modify the value of IWDG_PREDIV.PD[2:0] when the value of IWDG_KEY.KEYV[15:0] is 0x5555 and this bit is 0.

19.5.4 IWDG Prescaler Register (IWDG_PREDIV)

Offset address: 0x08

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved													PD[2:0]		
													rw		

Bit Field	Name	Description
31:3	Reserved	Reserved, the reset value must be maintained
2:0	PD[2:0]	It has write access protection when IWDG_KEY.KEYV[15:0] is not 0x5555. The IWDG_STS.PVU bit must be 0; otherwise, the PD[2:0] value cannot be modified. The prescaler factors are as follows: 000: Prescaler factor = 4 001: Prescaler factor = 8

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Bit Field	Name	Description
		010: Prescaler factor = 16 011: Prescaler factor = 32 100: Prescaler factor = 64 101: Prescaler factor = 128 Others: Prescaler factor = 256 Note: Reading this register will return the prescaler value from the VDD voltage domain. If a write operation is in progress, the read-back value may be invalid. Therefore, the read value is only valid when the IWDG_STS.PVU bit is 0.

19.5.5 IWDG Reload Register (IWDG_RELV)

Offset address:0x0C

Reset value: 0x00003FFF

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved		REL[13:0]													
		rw													

Bit Field	Name	Description
31:14	Reserved	Reserved, the reset value must be maintained
13:0	REL[13:0]	Watchdog Counter Reload Value It has write protection. It defines the reload value of the watchdog counter, which is loaded into the counter each time 0xAAAA is written to the IWDG_KEY.KEYV[15:0] bits. The counter then starts counting down from this value. The watchdog timeout period can be calculated based on this reload value and the clock prescaler value; refer to Table 19-1. This register can only be modified when the IWDG_STS.CRVU bit is 0. Note: Reading this register will return the reload value from the VDD voltage domain. If a write operation is in progress, the read-back value may be invalid. Therefore, the read value is only valid when the IWDG_STS.CRVU bit is 0.

19.5.6 IWDG Control Register (IWDG_CTRL)

Offset address:0x10

Reset value: 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

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15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved															ITE
															rw

Bit Field	Name	Description
31:1	Reserved	Reserved, the reset value must be maintained
0	ITE	IWDG Timer Interrupt Enable When the DOWN COUNTER in the IWDG is less than or equal to IWDG_REVL.RVL[13:0]/2, the IWDG outputs an interrupt. 0: Interrupt disabled 1: Interrupt enabled Note: The interrupt is exited by feeding the watchdog.

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20 Serial Peripheral Interface (SPI)

20.1 Introduction

SPI can operate in master mode or slave mode, supporting full-duplex and simplex high-speed communication modes, and has hardware CRC calculation capability and can be configured in multi-master mode.

20.2 Main Features

- Full-duplex and simplex synchronous mode.
- Support master mode, slave mode and multi-master mode.
- Supports 8-bit or 16-bit data frame format.
- Data bit sequence programmable.
- NSS management by hardware or software.
- Clock polarity and phase programmable.
- Transmitting and receiving support hardware CRC calculation and check.
- DMA capability for transmission and reception

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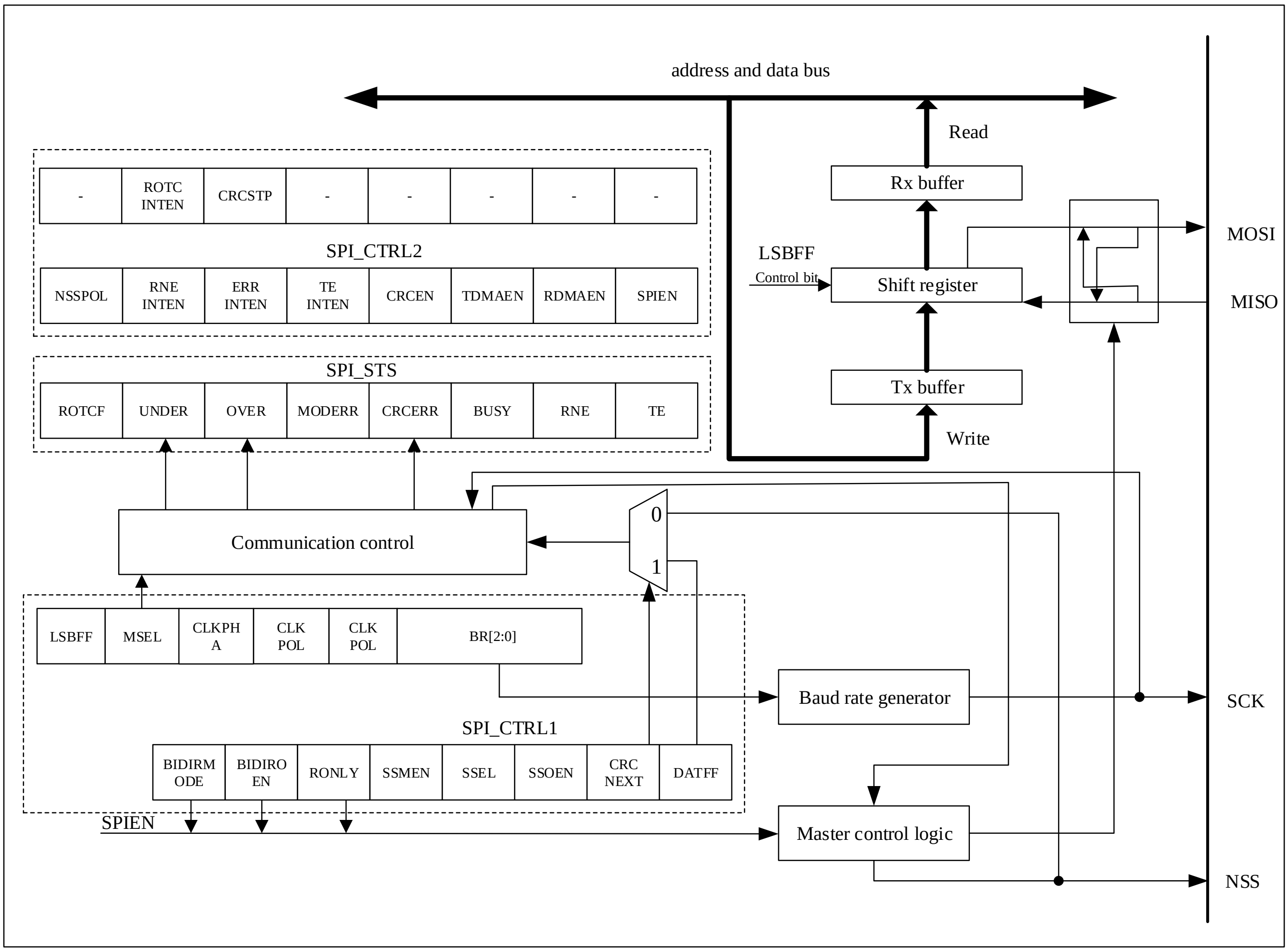
20.3 SPI Function Description

20.3.1 General Description

Figure 20-1 SPI Block Diagram



Usually, the SPI is connected to external devices through four pins:

- SCLK: serial clock pin. Serial clock signal is output from the SCLK pin of master device and input to SCLK pin of slave device.
- MISO: master input/slave output pin. Data is received from the MISO pin of master device and send by the MISO pin of slave device.
- MOSI: master output/slave input pin. Data is transmitted by the MOSI pin of master device and received from the MOSI pin of slave device.
- NSS: Slave select. There are two types of NSS pin, internal pin and external pin. If the internal pin detects a high level, SPI works in the master mode. Conversely, SPI works in the slave mode. Users can use a standard I/O pin of the master device to control the NSS pin of the slave device.

Software NSS mode

The software slave device management is enabled when SPI_CTRL1.SSMEN = 1.

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The NSS pin remains free in software NSS mode. In this mode the internal NSS signal level is driven by writing the SPI_CTRL1.SSEL bit (set SPI_CTRL1.SSEL=1 in master mode and set SPI_CTRL1.SSEL = 0 in slave mode).

Hardware NSS mode

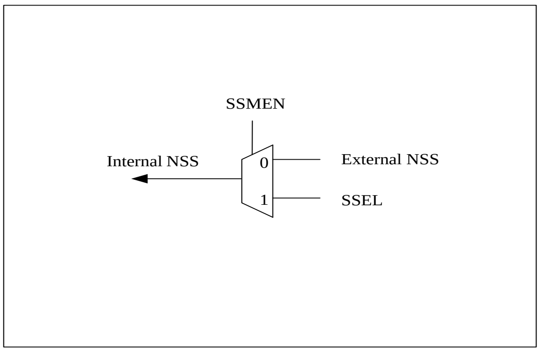
The software slave device management is disabled when SPI_CTRL1.SSMEN = 0.

NSS input mode: The NSS output of the master device is disabled (SPI_CTRL1.MSEL = 1, SPI_CTRL2.SSOEN = 0), allowing operation in multi-master mode. The master should connect NSS pin to the high level and the slave should connect NSS pin to the low level during the entire data frame transfer.

NSS output mode: NSS output of the master device is enable (SPI_CTRL1.MSEL = 1, SPI_CTRL2.SSOEN = 1). SPI as the master device must pull the NSS pin to low level, all device which connected to the master device and set to NSS hardware mode, will detect low level and enter the slave mode automatically. If the master device cannot pull the NSS pin to low level, device will enter the slave mode and generates the master mode fault error.

Note: The choice of software mode or hardware mode depends on whether NSS control is needed in the communication protocol. If not, you can choose the software mode, and release a GPIO pin for other purposes.

Figure 20-2 Selective Management of Hardware/Software



The following figure is an example of the interconnection of single master and single slave devices:

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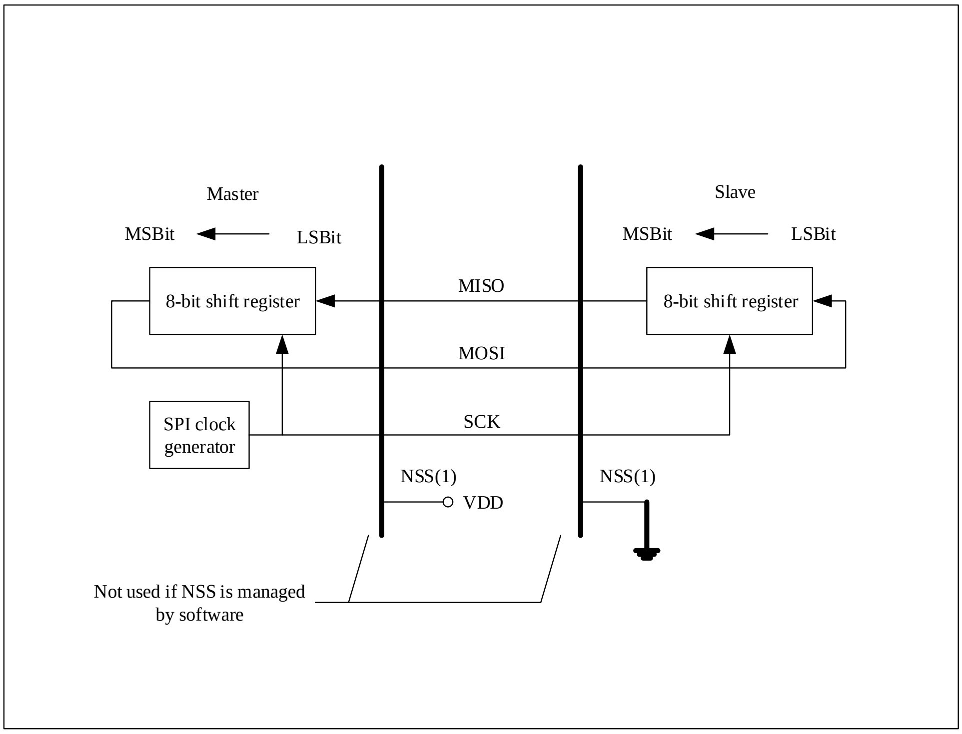
Figure 20-3 Master and Slave Applications



Note: (1)NSS pin is set as input

The master device outputs a synchronous clock signal through the SCLK pin, the MOSI pin of the master device is connected to the MOSI pin of the slave device, and the MISO pin of the master device is connected to the MISO pin of the slave device, so that data can be transferred between devices. Continuous data transfer between master and slave, sending data to slave through MOSI pin and slave sending data to master through MISO pin.

SPI timing mode

User can select the clock edge of data capture by setting SPI_CTRL1.CLKPOL bit and SPI_CTRL1.CLKPHA bit.

- When CLKPOL = 0, CLKPHA = 0, the SCLK pin will keep low in idle state, and the data will be sampled at the first edge, which is rising edge.
- When CLKPOL = 0, CLKPHA = 1, the SCLK pin will keep low in idle state, and the data will be sampled at the second edge, which is falling edge.
- When CLKPOL = 1, CLKPHA = 0, the SCLK pin will keep high in idle state, and the data will be sampled at the first edge, which is falling edge.
- When CLKPOL = 1, CLKPHA = 1, the SCLK pin will keep high in idle state, and the data will be sampled at the second edge, which is rising edge.

Regardless of the timing mode used, the master and slave configuration must be the same.

Figure 20-4 is the combination timing of four CLKPHA and CLKPOL bits transmitted by SPI when the SPI_CTRL1.LSBFF = 0.

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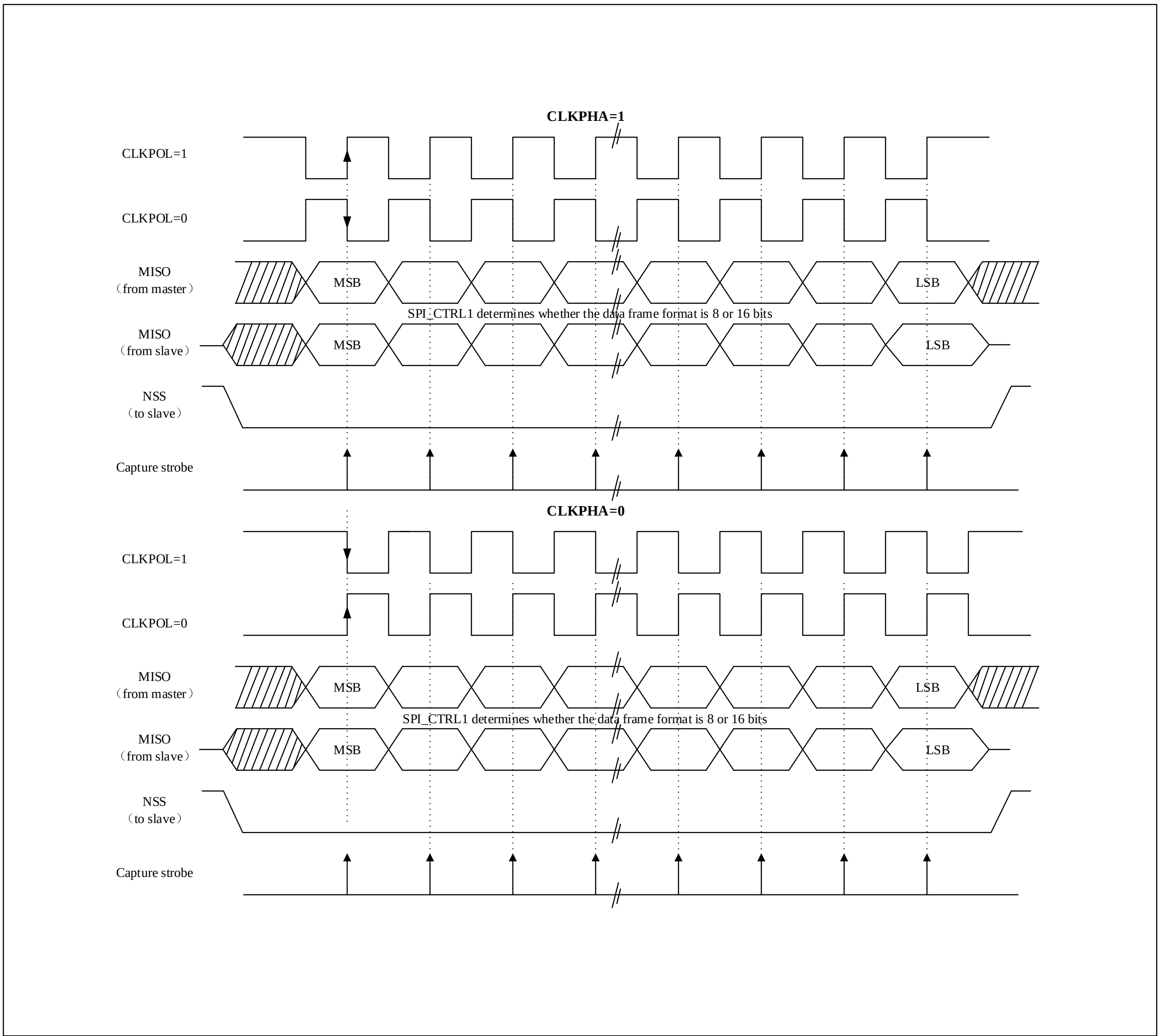
Figure 20-4 Data Clock Timing Diagram



Data format

User can selects the data order by setting the SPI_CTRL1.LSBFF bit. When SPI_CTRL1.LSBFF = 0, SPI will send the high-order data (MSB) first; When SPI_CTRL1.LSBFF = 1, SPI will send low-order data (LSB) first.

User can selects the data frame by setting the SPI_CTRL1.DATFF bit.

20.3.2 SPI Operating Mode

- **Master full duplex mode (SPI_CTRL1.MSEL = 1, SPI_CTRL1.BIDIRMODE = 0, SPI_CTRL1.RONLY = 0)**

After the first data is written to the SPI_DAT register, the transmission will start. When the first bit of the data is sent, the data bytes are loaded from the data register into the shift register in parallel, and then according to the configuration of the SPI_CTRL1.LSBFF bit, the data bits follow the MSB or LSB order are serially shifted to the MOSI pin. At the same time, the data receives on the MISO pin is serially shifted into the shift register in the same order and then loaded into the SPI_DAT register in parallel. The software operation process is as follows:

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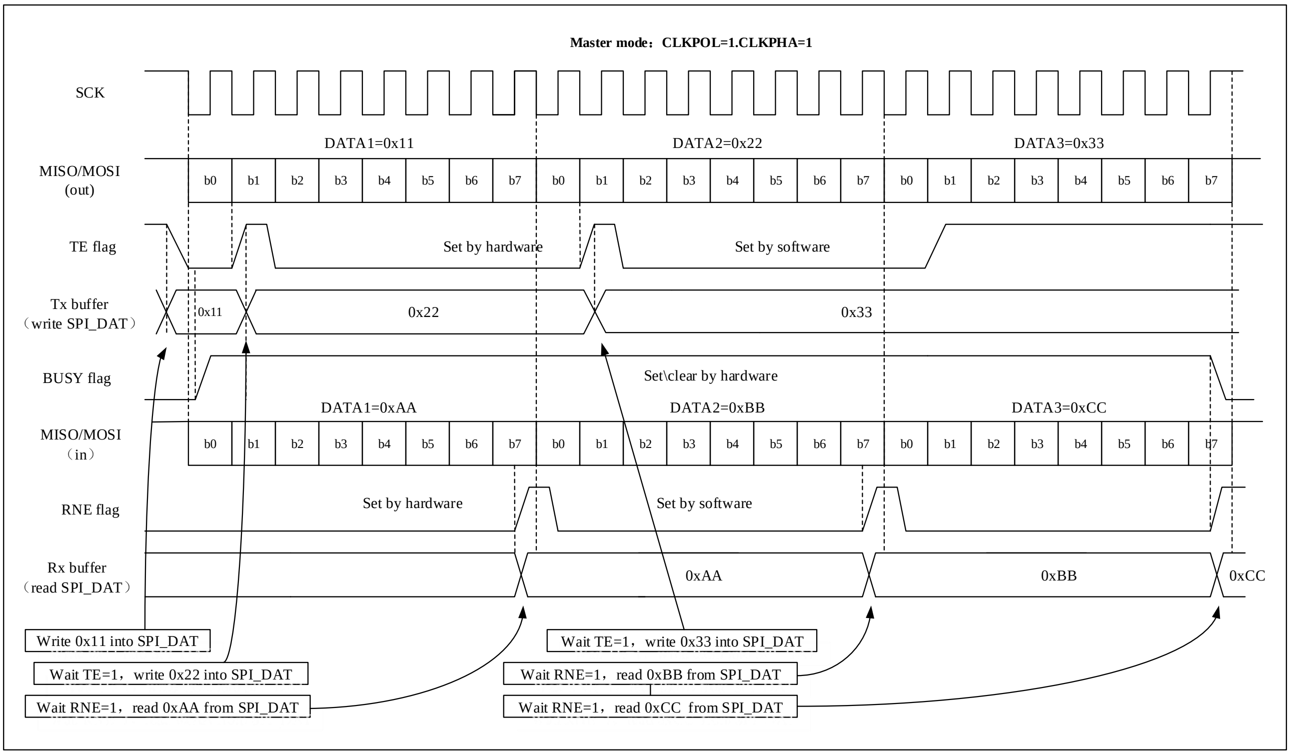
- Set SPI_CTRL2.SPIEN = 1, Enable SPI module.
- Write the first data to be sent into SPI_DAT register (this operation will clear SPI_STS.TE bit).
- Wait for SPI_STS.TE bit to be set to '1', and write the second data to be sent into SPI_DAT. Wait for SPI_STS.RNE bit to be set to '1', read SPI_DAT to get the first received data, and the SPI_STS.RNE bit will be cleared by hardware while reading SPI_DAT. Repeat the above operation, sending subsequent data and receiving n-1 data at the same time;
- Wait for SPI_STS.RNE bit to be set to '1' to receive the last data;
- Wait for SPI_STS.TE to be set to '1', then wait for SPI_STS.BUSY bit to be cleared and turn off SPI module.

The process of data transmitting and data receiving can also be implemented in the interrupt handler generated by the rising edge of the SPI_STS.RNE or SPI_STS.TE flag.

Figure 20-5 TE/RNE/BUSY Behavior in Master / Full-Duplex Mode (BIDIRMODE = 0, RONLY = 0) in Case of Continuous Transfers



- **Master two-wire unidirectional transmit-only mode (SPI_CTRL1.MSEL=1, SPI_CTRL1.BIDIRMODE = 0, SPI_CTRL1.RONLY = 0)**

Master two-wire unidirectional transmit-only mode is similar to master full-duplex mode. The difference is that this mode will not read the received data, so the SPI_STS.OVER bit will be set to '1', and the software will ignore it. The software operation process is as follows:

- Set SPI_CTRL2.SPIEN = 1 to enable SPI module.
- Write the first data to be sent into SPI_DAT register (this operation will clear SPI_STS.TE bit).
- Wait for SPI_STS.TE bit to be set to '1', and write the second data to be sent into SPI_DAT. Repeat this operation to send subsequent data;

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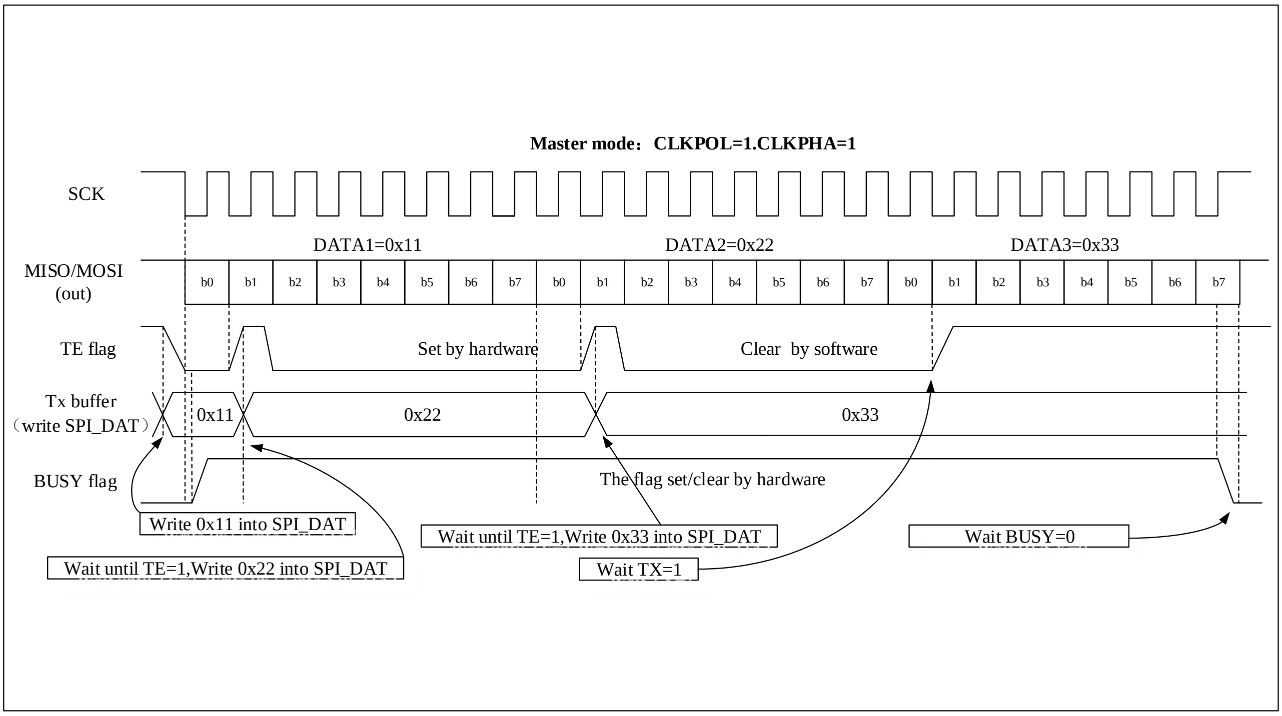
- After writing the last data to SPI_DAT, wait for SPI_STS.TE bit to set '1'; then wait for SPI_STS.BUSY bit to be cleared to complete the transmission of all data.

This process can also be implemented in the interrupt handler triggered by the rising edge of the SPI_STS.TE flag.

Figure 20-6 TXE/BSY Behavior in Master Transmit-Only Mode (BIDIRMODE = 0, RONLY = 0) in Case of Continuous Transfers



- **Master two-wire unidirectional receive-only mode (SPI_CTRL1.MSEL = 1, SPI_CTRL1.BIDIRMODE = 0, SPI_CTRL1.RONLY = 1)**

When SPI_CTRL2.SPIEN = 1, the receiving process starts. The data bits from the MISO pin are sequentially shifted into the shift register and then loaded into the SPI_DAT register(receive buffer) in parallel. The software operation process is as follows:

- Set SPI_CTRL1.RONLY = 1 to enable the receive-only mode.
- In master mode, setting the SPI_CTRL2.SPIEN bit to 1 enables the SPI module, and the SCLK signal is generated immediately. Data is continuously received until the SPI is disabled (SPI_CTRL2.SPIEN = 0). In slave mode, when the master device drives the NSS signal low and generates SCLK, data is continuously received.
- Wait for SPI_STS.RNE bit to be set to '1', read the SPI_DAT register to get the received data, and the SPI_STS.RNE bit will be cleared by hardware while reading SPI_DAT register. Repeat this operation to receive all data.

The process of data receiving can also be implemented in the interrupt handler generated by the rising edge of the RNE flag (SPI_STS.RNE).

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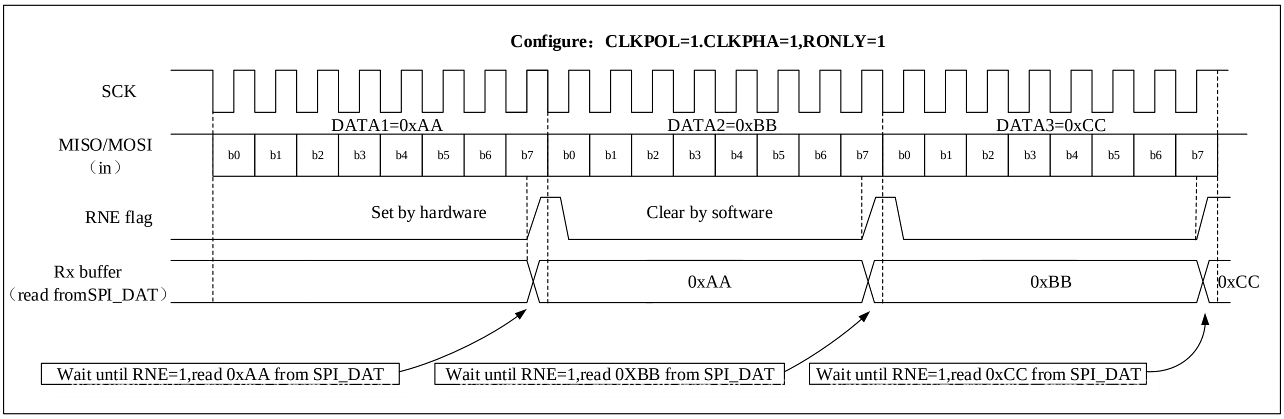
Figure 20-7 RNE Behavior in Receive-Only Mode in Case of Continuous Transfers (BIDIRMODE = 0, RONLY = 1)



- **Master one-wire bidirectional transmit mode (SPI_CTRL1.MSEL = 1, SPI_CTRL1.BIDIRMODE = 1, SPI_CTRL1.BIDIROEN = 1, SPI_CTRL1.RONLY = 0)**

After the data is written to the SPI_DAT register (send buffer), the transmission process starts. This mode does not receive data. At the same time as the first data bit is sent, the data to be sent is loaded into the shift register in parallel, and then according to the configuration of the SPI_CTRL1.LSBFF bit, the SPI serially shifts the data bits to the MOSI pin in MSB or LSB order.

The software operation flow of the master one-wire bidirectional transmit mode is the same as that of the transmit-only mode.

- **Master one-wire bidirectional receive mode (SPI_CTRL1.MSEL = 1, SPI_CTRL1.BIDIRMODE = 1, SPI_CTRL1.BIDIROEN = 0, SPI_CTRL1.RONLY = 0)**

When SPI_CTRL1.SPIEN = 1 , the receiving process starts. There is no data output in this mode, the received data bits are sequentially and serially shifted into the shift register, and then loaded into the SPI_DAT register (receive buffer) in parallel

The software operation flow of the master one-wire bidirectional receive mode is the same as that of the receive-only mode.

- **Slave full duplex mode (SPI_CTRL1.MSEL = 0, SPI_CTRL1.BIDIRMODE = 0, SPI_CTRL1.RONLY = 0)**

The data transfer process begins when the slave device receives the first clock edge. Before the master device initiates data transmission, the software must ensure that the data to be sent is written to the SPI_DAT register.

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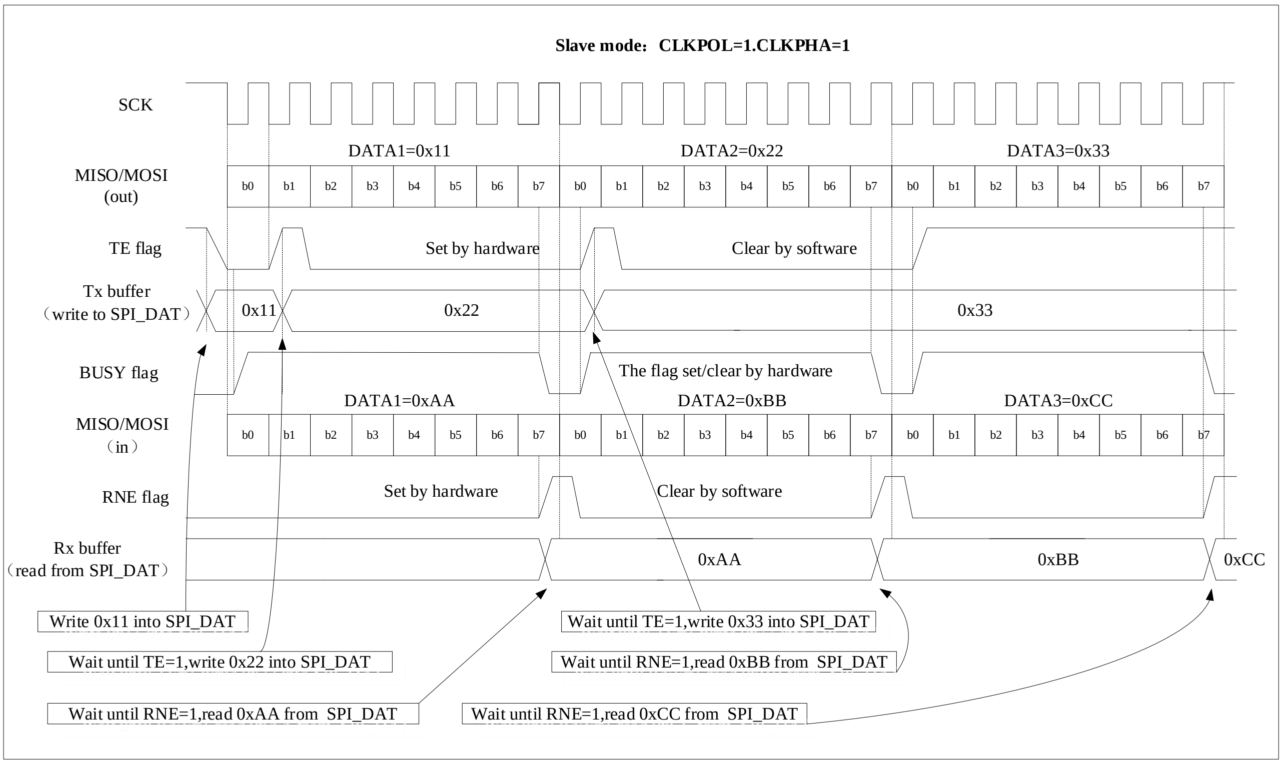
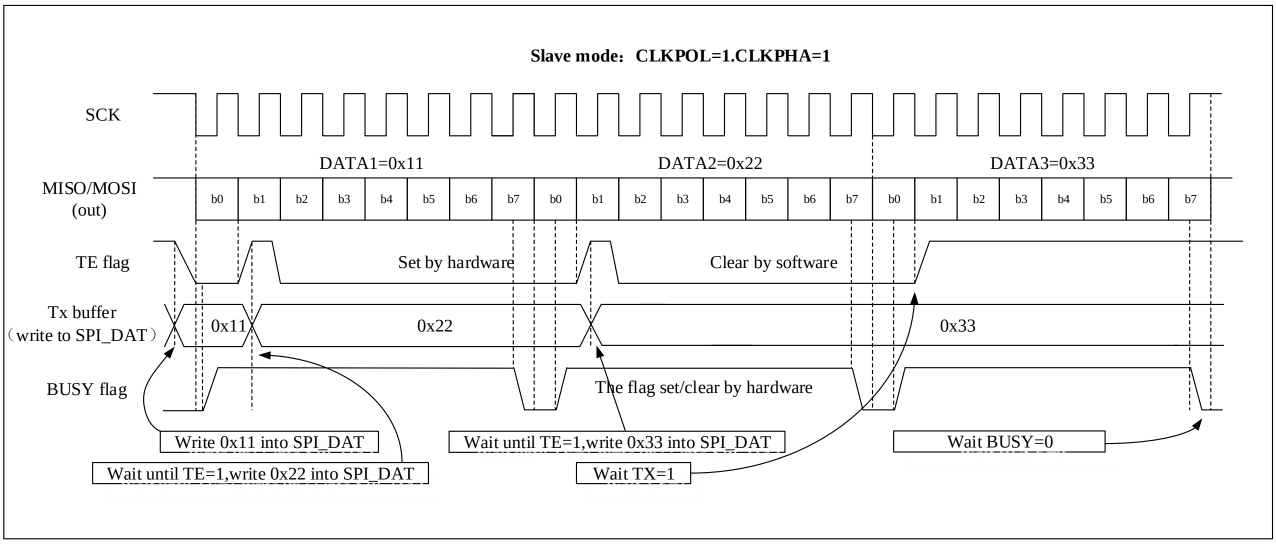
Figure 20-8 TE/RNE/BUSY Behavior in Slave / Full-Duplex Mode in Case of Continuous Transfers



- **Slave two-wire unidirectional transmit-only mode (SPI_CTRL1.MSEL = 0, SPI_CTRL1.BIDIRMODE = 0 and SPI_CTRL1.RONLY = 0)**

Figure 20-9 TE/BUSY Behavior in Slave Transmit-Only Mode in Case of Continuous Transfers



- **Slave two-wire unidirectional receive-only mode (SPI_CTRL1.MSEL = 0, SPI_CTRL1.BIDIRMODE = 0 and SPI_CTRL1.RONLY = 1)**

The data receiving process begins when the slave device receives the clock signal and the first data bit from the MOSI pin. The received data bits are sequentially and consecutively shifted serially into an shift register and then loaded into the SPI_DAT register (receive buffer) in parallel.

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- **Slave one-wire bidirectional transmit mode (SPI_CTRL1.MSEL = 0, SPI_CTRL1.BIDIRMODE = 1 and SPI_CTRL1.BIDIROEN = 1)**

When the slave device receives the first edge of the clock signal, the transmitting process starts. No data is received in this mode. Software must ensure that the data to be transmitted is written into the slave transmit register before the SPI master device starts data transfer.

- **Slave one-wire bidirectional receive mode (SPI_CTRL1.MSEL = 0, SPI_CTRL1.BIDIRMODE = 1 and SPI_CTRL1.BIDIROEN = 0)**

Data receiving begins when the slave device receives the first clock edge and a data bit from the MOSI pin. There is no data output in this mode, the received data bits are sequentially and consecutively shifted serially into an shift register, and then loaded into the SPI_DAT register (receive buffer) in parallel.

Note: The software operation process of the slave can refer to the master.

SPI initialization process

1) The baud rate of serial clock is defined by the SPI_CTRL1.BR[2:0] bits (this step is ignored if it is working in slave mode).
2) Select SPI_CTRL1.CLKPOL bit and SPI_CTRL1.CLKPHA bit to define the phase relationship between data transmission and serial clock.
3) Set SPI_CTRL1.DATFF bit to define 8-bit or 16-bit data frame format.
4) Configure the SPI_CTRL1.LSBFF bit to define the frame format.
5) Configure the NSS mode as described above for the NSS function.
6) Run mode is configured by SPI_CTRL1.MSEL bit, SPI_CTRL1.BIDIRMODE bit, SPI_CTRL1.BIDIROEN bit and SPI_CTRL1.RONLY bit.
7) Set the SPI_CTRL1.SPIEN = 1 to enable SPI.

Basic send and receive process

When SPI sends a data frame, it firstly loads the data frame from the data buffer into the shift register, and then starts to send the loaded data. When the data is transferred from the transmit buffer to the shift register, the transmit buffer empty flag is set (SPI_STS.TE = 1), and the next data can be loaded into the send buffer; if the TEINTEN bit is set (SPI_CTRL2.TEINTEN = 1), an interrupt will be generated; writing data to the SPI_DAT register will clear the SPI_STS.TE bit.

At the last edge of the sampling clock, when the data is transferred from the shift register to the receive buffer, the receive buffer non-empty flag is set (SPI_STS.RNE = 1), at this time the data is ready and can be read from the SPI_DAT register; if the receive buffer non-empty interrupt is enabled (SPI_CTRL2.RNEINTEN = 1), an interrupt will be generated; the SPI_STS.RNE bit can be cleared by reading the SPI_DAT register data.

In master mode, the transmitting process starts when data is written to the send buffer. If the next data has been written into the SPI_DAT register before the current data frame sending is completed, the continuous sending function

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can be achieved.

In slave mode, the NSS pin is low, and when the first clock edge arrives, the transmission process begins. In order to avoid accidental data transmission, software must write data to the transmit buffer before data transmission (it is recommended to enable the SPI module before the master sends the clock).

In some configurations, when the last data is sent, the BUSY flag (SPI_STS.BUSY) can be used to wait for the end of the data sending.

Continuous and discontinuous transmission.

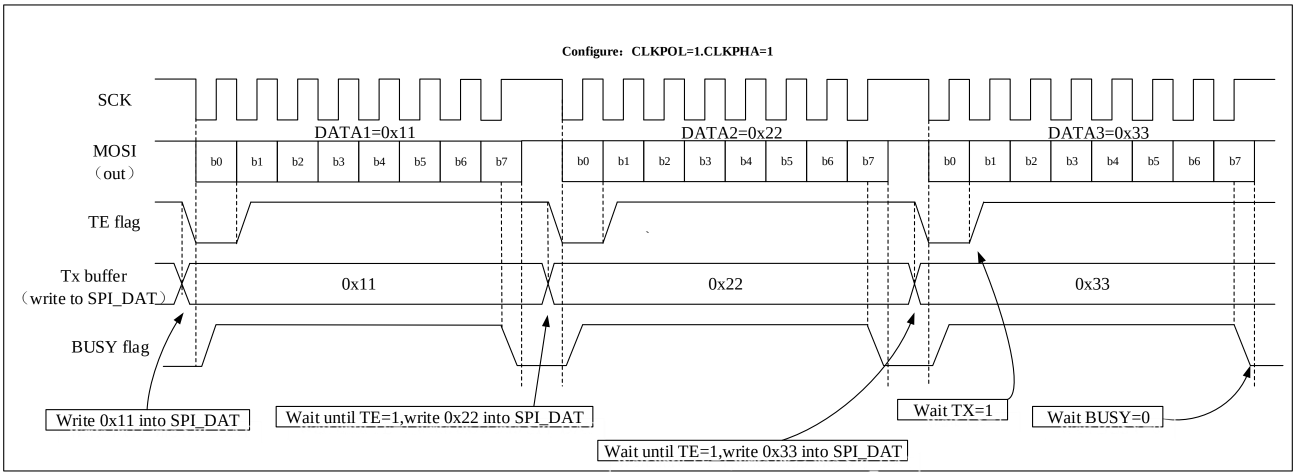
When sending data in master mode, if the software is fast enough to detect each TE (SPI_STS.TE) rising edge (or TE interrupt), and the data is written to the SPI_DAT register immediately before the end of the ongoing transmission. At this time, the SPI clock remains continuous between the transmission of data items, and the SPI_STS.BUSY bit will not be cleared, continuous communication can be achieved.

If the software is not fast enough, it will result in discontinuous communication; in this case, the SPI_STS.BUSY bit is cleared between the transmission of each data items (refer to Figure 20-10 below).

In master receive-only mode (SPI_CTRL1.RONLY = 1), communication is always continuous and the BUSY flag (SPI_STS.BUSY) is always high.

In slave mode, the continuity of communication is determined by the SPI master device. However, even if the communication is continuous, the BUSY flag (SPI_STS.BUSY) will be low for at least one SPI clock cycle between each data item (refer to Figure 20-9 below).

Figure 20-10 TE/BUSY Behavior in Non-Continuous Transmission (BIDIRMODE = 0 and RONLY = 0).



20.3.3 Status Flag

The SPI_STS register has 3 flag bits to monitor the status of the SPI:

Send buffer empty flag bit (TE)

When the send buffer is empty, the TE flag (SPI_STS.TE) is set to 1, which means that new data can be written into the SPI_DAT register. When the send buffer is not empty, the hardware will clear this flag to 0.

Receive buffer non-empty flag bit (RNE)

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When the receive buffer is not empty, the RNE flag (SPI_STS.RNE) is set to 1, so the user knows that there is data in the receive buffer. After reading the SPI_DAT register, the hardware will set this flag to 0.

BUSY flag bit (BUSY)

When the transmission starts, the hardware sets the BUSY flag (SPI_STS.BUSY) to 1, and after the transmission ends, the hardware sets the BUSY flag to 0.

Only when the device is in the master one-wire bidirectional receive mode, the BUSY flag (SPI_STS.BUSY) will be set to 0 when the communication is in progress.

The BUSY flag (SPI_STS.BUSY) will be cleared to 0 in the following cases:

- End of transmission (except for continuous communication in master mode);
- Disable the SPI module (SPI_CTRL2.SPIEN = 0);
- The master mode error occurs (SPI_STS.MODERR = 1)

When the communication is discontinuous: the BUSY flag (SPI_STS.BUSY) is cleared to '0' between the transmission of each data item.

When communication is continuous: in master mode, the BUSY flag (SPI_STS.BUSY) remains high during the entire transfer process; In slave mode, the BUSY flag (SPI_STS.BUSY) will be low for 1 SPI clock cycle between each data item transfer. So do not use the BUSY flag to handle the sending and receiving of each data item.

20.3.4 Disabling SPI

To disable the SPI module, different operation modes require different operation steps

Master or slave full duplex mode(SPI_CTRL1.BIDIMODE=0, SPI_CTRL1.RONLY=0)

1) Wait for the RNE flag (SPI_STS.RNE) to be set to 1 and the last byte to be received;
2) Wait for the TE flag (SPI_STS.TE) to be set to 1;
3) Wait for the BUSY flag (SPI_STS.BUSY) to be cleared to 0;
4) Turn off the SPI module (SPI_CTRL1.SPIEN = 0).

Two-wire unidirectional transmit-only mode(SPI_CTRL1.BIDIMODE=0, SPI_CTRL1.RONLY=0) or one-wire bidirectional transmit mode(SPI_CTRL1.BIDIMODE=1, SPI_CTRL1.BIDIROEN=1) for master or slave

1) After writing the last byte to the SPI_DAT register, wait for the TE flag (SPI_STS.TE) to be set to 1;
2) Wait for the BUSY flag (SPI_STS.BUSY) to be cleared to 0;
3) Disable the SPI module (SPI_CTRL1.SPIEN = 0).

Two-wire unidirectional receive-only mode (SPI_CTRL1.MSEL=1, SPI_CTRL1.BIDIMODE=0, SPI_CTRL1.RONLY=1) or one-wire bidirectional receive mode(SPI_CTRL1.MSEL=1, SPI_CTRL1.BIDIMODE=1, SPI_CTRL1.BIDIROEN=0) for master

1. Wait for the penultimate RNE (SPI_STS.RNE) to be set to 1;
2. Before closing the SPI module (SPI_CTRL1.SPIEN = 0), wait for 1 SPI clock cycle (using software delay);

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3. Wait for the last RNE (SPI_STS.RNE) to be set before entering shutdown mode (or disabling the SPI module clock).

Two-wire unidirectional receive-only mode(SPI_CTRL1.MSEL=0, SPI_CTRL1.BIDIMODE=0, SPI_CTRL1.RONLY=1) or one-wire bidirectional receive mode(SPI_CTRL1.MSEL=0, SPI_CTRL1.BIDIMODE=1, SPI_CTRL1.BIDIROEN=0) for slave

1. The SPI module can be disabled at any time (SPI_CTRL2.SPIEN = 0), and after the current transfer is over, the SPI module will be disabled;

2. If you want to enter the shutdown mode, you must wait for the BUSY flag (SPI_STS.BUSY) to be set to 0 before entering the shutdown mode (or disable the SPI module clock).

20.3.5 SPI Communication Using DMA

Users can choose DMA for SPI data transmission, application programs can be released, and system efficiency can be greatly improved.

When the send buffer DMA is enabled (SPI_CTRL2.TDMAEN = 1), each time the TE flag (SPI_STS.TE) bit is 1, a DMA request will be generated, and the DMA will automatically write the data to the SPI_DAT register, which will clear the TE flag (SPI_STS.TE) bit.

When the receive buffer DMA is enabled (SPI_CTRL2.RDMAEN = 1), each time the RNE flag (SPI_STS.RNE) bit is set to 1, a DMA request will be generated, and the DMA will automatically read the SPI_DAT register, which will clear the RNE flag (SPI_STS.RNE) bit.

When the SPI is only used for transmitting data, only the transmit DMA channel of the SPI needs to be enabled (SPI_CTRL2.TDMAEN = 1). At this time, since the received data has not been read, the OVER flag is set to '1' (software does not need to pay attention to this flag).

When the SPI is only used for receiving data, only the receive DMA channel of the SPI needs to be enabled (SPI_CTRL2.RDMAEN = 1).

In transmit mode, after DMA has sent all the data to be sent (DMA_INTSTS.TXCF = 1), BUSY flag (SPI_STS.BUSY) can monitor to confirm whether SPI communication is over, which can avoid destroying the transmission of the last data when the SPI is turned off or enters the shutdown mode. Therefore, the software needs to wait for the TE flag (SPI_STS.TE) bit to be set to 1, and wait for the BUSY flag (SPI_STS.BUSY) bit to be set to 0.

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Figure 20-11 Transmission Using DMA

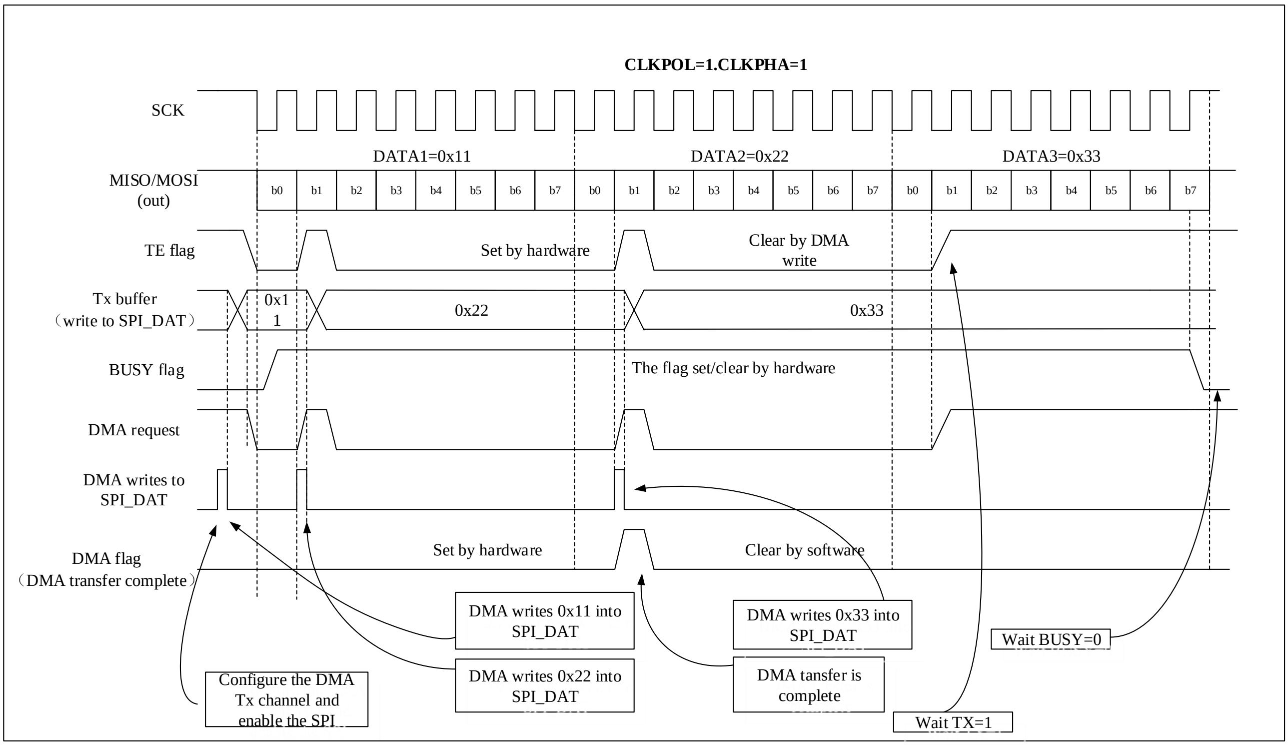
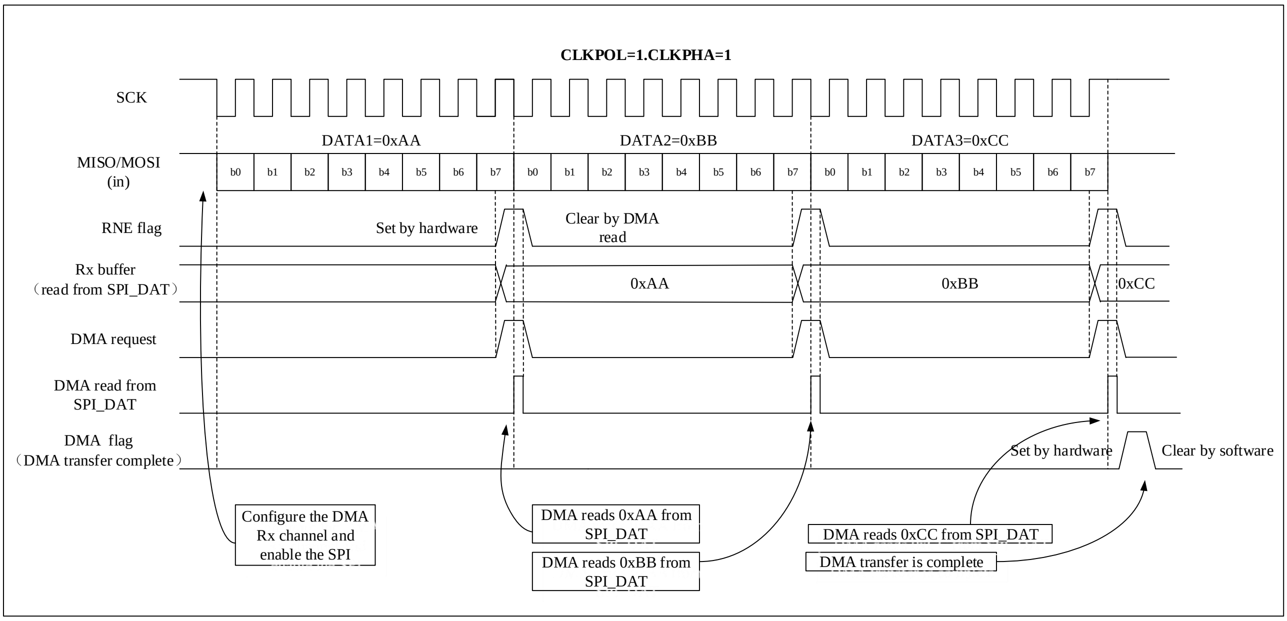


Figure 20-12 Reception Using DMA



20.3.6 CRC Calculation

SPI contains two independent CRC calculators for data transmission and reception to ensure the correctness of data transfer. Depending on the format of the transmitted and received data frames, different calculation methods are used for CRC, with CRC8 used for 8-bit data frames and CRC16 used for 16-bit data frames. The polynomial used for SPI CRC calculation is set by the SPI_CRCPOLY register, and users enable CRC calculation by setting the SPI_CTRL2.CRCEN bit.

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In transmit mode, after the final data is written to the transmit buffer, set the SPI_CTRL1.CRCNEXT bit to 1, which indicates that the hardware will start sending the CRC value (SPI_CRCTDAT value) after the data transmission is complete. During CRC transmission, the CRC calculation will stop.

In receive mode, after the second-to-last data frame is received, set the SPI_CTRL1.CRCNEXT bit to 1. Compare the received CRC with the SPI_CRCRDAT value, and if they are different, set the SPI_STS.CRCERR bit to 1. If SPI_CTRL2.ERRINTEN is set to 1, an interrupt will be generated.

To maintain synchronization of the next CRC calculation result between the master device and the slave device, the user should clear the CRC values of the master device and the slave device. Setting SPI_CTRL2.CRCEN to 1 will reset the SPI_CRCRDAT register and the SPI_CRCTDAT register. Follow the steps in the following sequence:

1. Set SPI_CTRL2.SPIEN = 0
2. Set SPI_CTRL2.CRCEN = 0
3. Set SPI_CTRL2.CRCEN = 1
4. Set SPI_CTRL2.SPIEN = 1.

Most importantly, when SPI is configured in slave mode with CRC enabled, the CRC calculation will still be performed as long as the SCLK pin has clock pulses, even if the NSS pin is high. This situation commonly occurs when the master device communicates alternately with multiple slave devices, so care must be taken to avoid CRC errors.

When hardware CRC checking is enabled (SPI_CTRL2.CRCEN = 1) and DMA is enabled, the hardware automatically completes the CRC byte transmission and reception at the end of communication.

20.3.7 Error Flag

Master mode fault (MODERR)

The following two conditions will cause the master mode fault:

- In NSS pin hardware management mode, the master device NSS pin is pulled low;
- In NSS pin software management mode, the SPI_CTRL1.SSEL bit is set to 0.
- When a master mode fault error occurs, the SPI_STS.MODERR bit is set to 1. An interrupt is generated if the user enables the corresponding interrupt (SPI_CTRL2.ERRINTEN = 1). The SPI_CTRL2.SPIEN bit and SPI_CTRL1.MSEL bit will be write protected and both are cleared by hardware. SPI is disabled and forced into slave mode.
- Performing a read or write operation on the SPI_STS register in software, followed by writing to the SPI_CTRL1 register, can clear the SPI_STS.MODERR bit (in multi-master configuration, the master's NSS pin must be pulled high first).
- Normally, the SPI_STS.MODERR bit of the slave cannot be set to 1. However, in a multi-master configuration, the slave's SPI_STS.MODERR bit may be set to 1. In this case, the SPI_STS.MODERR bit indicates that there is a multi-master collision. The interrupt routine can perform a reset or return to the default state to recover from an error state.

Overflow Error (OVER)

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When the SPI_STS.RNE bit is set to 1, but there is still data sent into the receive buffer, an overflow error will occur. At this point, the overflow flag SPI_STS.OVER is set to 1. If the user enables the corresponding interrupt, an interrupt will be generated. All received data is lost, and the SPI_DAT register retains only the data that was previously unread.

Reading the SPI_DAT register and then the SPI_STS register in sequence can clear the SPI_STS.OVER bit.

CRC Error (CRCERR)

The CRC error flag is used to check the validity of the received data. A CRC error occurs when the received CRC value does not match the SPI_CRCRDAT value. At this time, the SPI_STS.CRCERR flag bit is set to '1', and an interrupt will be generated if the user enables the corresponding interrupt (SPI_CTRL2.ERRINTEN = 1).

20.3.8 SPI Interrupt

Table 20-1 SPI Interrupt Request

Interrupt Event	Event Flag	Enable Control Bit
Transmit buffer empty flag	TE	TEINTEN
Receive buffer not empty flag	RNE	RNEINTEN
Master mode fault event	MODERR	ERRINTEN
Overflow error	OVER	
CRC error	CRCERR	

20.4 SPI Registers

20.4.1 SPI Register Overview

Table 20-2 SPI Register Overview

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
000h	SPI_CTRL1	Reserved																BIDIROEN	BIDIRMODE	RONLY	SSMEN	SSEL	SSOEN	CRCNEXT	DATFF	LSBFF	MSEL	CLKPHA	CLKPOL	Reserved	BR[2:0]		
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0		0	0	0
004h	SPI_CTRL2	Reserved																		CRCSTP	Reserved					NSSPOL	ERRINTEN	RNEINTEN	TEINTEN	CRCEN	TDMAEN	RDMAEN	SPIEN
	Reset Value																			0						0	0	0	0	0	0	0	0
008h	SPI_STS	Reserved																										OVER	MODERR	CRCERR	BUSY	RNE	TE
	Reset Value																											0	0	0	0	1	0
00Ch	SPI_DAT	Reserved																DAT[15:0]															
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
010h	SPI_CRCTDAT	Reserved																CRCTDAT[15:0]															
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
014h	SPI_CRCRDAT	Reserved																CRCRDAT[15:0]															
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
018h	SPI_CRCPOLY	Reserved																CRCPOLY[15:0]															
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1
038h	SPI_CTRL3	Reserved																												DELAYTIME[3:0]			

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	Reset Value		0	0	0	0

20.4.2 SPI Control Register 1 (SPI_CTRL1)

Address: 0x00

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BIDIR MODE	BIDIR OEN	RONLY	SSMEN	SSEL	SSOEN	CRC NEXT	DATFF	LSBFF	MSEL	CLKPHA	CLKPOL	Reserved	BR[2:0]		
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw		rw	rw	rw

Bit Field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained.
15	BIDIRMODE	Bidirectional data mode enable 0: Select the "two-wire one-way" mode. 1: Select the "one-wire bidirectional " mode.
14	BIDIROEN	Output enable in bidirectional mode Together with SPI_CTRL1.BIDIRMODE, this bit determines the transmission direction in single-line bidirectional mode. 0: Output disable (receive-only mode). 1: Output enabled (send-only mode). In master mode, the "one-wire" data line is the MOSI pin, and in slave mode, the "one-wire" data line is the MISO pin.
13	RONLY	Only receive mode This bit, together with the SPI_CTRL1.BIDIRMODE bit, determines the transfer direction in two-wire one-way mode. In the application scenario of multiple slave devices, this bit is only set to 1 by the unaccessed slave device, and only the accessed slave device can output, so as to avoid data line conflicts. 0: Full duplex (sending mode and receiving mode). 1: Disable output (receive-only mode).
12	SSMEN	Software slave device management When the SPI_CTRL1.SSMEN bit is set to 1, the NSS pin level is determined by the value of the SPI_CTRL1.SSEL bit. 0: Disable software slave device management. 1: Enable software slave device management.
11	SSEL	Internal slave device selection This bit only has meaning when the SPI_CTRL1.SSMEN bit is set. It determines the NSS level, and I/O operations on the NSS pin have no effect.
10	SSOEN	NSS output enable 0: Disable NSS output in master mode, the device can work in multi-master mode.

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Bit Field	Name	Description
		1: When the device is enabled, enable NSS output in the master mode, the device cannot work in the multi-master device mode.
9	CRCNEXT	Send CRC next 0: The next sent value comes from the send buffer. 1: The next send value comes from the CRC register. *Note: This bit should be set immediately after the last data is written in SPI_DAT register during transmission. This bit should be set immediately after receiving the second-to-last data during reception.*
8	DATFF	Data frame format 0: 8-bit data frame format is used for sending/receiving. 1: 16-bit data frame format is used for sending/receiving. *Note: This bit can only be written when SPI is disabled (SPI_CTRL1.SPIEN = 0), otherwise an error will occur.*
7	LSBFF	Frame format 0: Send MSB first. 1: Send LSB first. *Note: This bit cannot be changed during communication.*
6	MSEL	Master device selection 0: Configure as the slave device. 1: Configure as the master device. *Note: This bit cannot be changed during communication.*
5	CLKPHA	Clock phase 0: Data is sampled on the first clock edge. 1: Data is sampled on the second clock edge. *Note: This bit cannot be changed during communication.*
4	CLKPOL	Clock phase 0: Data is sampled on the first clock edge. 1: Data is sampled on the second clock edge. *Note:* *1.This bit cannot be changed during communication.* *2. When CLKPOL is set to 1, the corresponding I/O pin is configured as pull-up. When CLKPOL is set to 0, the corresponding I/O pin is configured as pull-down.*
3	Reserved	Reserved, the reset value must be maintained.
2:0	BR[2:0]	Baud rate control 000: $f_{PCLK}/2$ 001: $f_{PCLK}/4$ 010: $f_{PCLK}/8$ 011: $f_{PCLK}/16$ 100: $f_{PCLK}/32$ 101: $f_{PCLK}/64$ 110: $f_{PCLK}/128$ 111: $f_{PCLK}/256$ *Note: This bit cannot be changed during communication.*

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20.4.3 SPI Control Register 2 (SPI_CTRL2)

Address: 0x04

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved		CRCSTP	Reserved					NSSPOL	ERR INTEN	RNE INTEN	TE INTEN	CRCEN	TDMAEN	RDMAEN	SPIEN
	rw	rw						rw	rw	rw	rw	rw	rw	rw	rw

Bit Field	Name	Description
31:14	Reserved	Reserved, the reset value must be maintained.
13	CRCSTP	When NSS becomes invalid, whether the CRC stop calculating immediately. 0: CRC stop calculating immediately when NSS becomes invalid. 1: As long as there is a clock, the CRC calculation continues.
12:8	Reserved	Reserved, the reset value must be maintained.
7	NSSPOL	NSS polarity control 0: NSS valid level is low. 1: NSS valid level is high.
6	ERRINTEN	Error interrupt enable When an error (SPI_STS.CRCERR, SPI_STS.OVER, SPI_STS.UNDER, SPI_STS.MODERR) is generated, this bit controls whether an interrupt is generated 0: Disable error interrupt. 1: Enable error interrupt.
5	RNEINTEN	Receive buffer non-empty interrupt enable 0: Disable RNE interrupt. 1: Enable RNE interrupt, and generate interrupt request when RNE flag (SPI_STS.RNE) is set to ‘1’.
4	TEINTEN	Transmit buffer empty interrupt enable 0: Disable TE interrupt. 1: Enable TE interrupt, and interrupt request is generated when TE flag (SPI_STS.TE) is set to '1'.
3	CRCEN	Hardware CRC check enable 0: Disable CRC calculation. 1: Enable CRC calculation. *Note: This bit can only be written when SPI is disabled (SPI_CTRL1.SPIEN = 0), otherwise an error will occur.* This bit can only be used in full duplex mode.
2	TDMAEN	Transmit buffer DMA enable When this bit is set, a DMA request is issued as soon as the TE flag (SPI_STS.TE) is set

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Bit Field	Name	Description
		0: Disable transmit buffer DMA. 1: Enable transmit buffer DMA.
1	RDMAEN	Receive buffer DMA enable When this bit is set, a DMA request is issued as soon as the RNE flag (SPI_STS.RNE) is set 0: Disable receive buffer DMA. 1: Enable receive buffer DMA.
0	SPIEN	SPI enable 0: Disable SPI device. 1: Enable the SPI device. *Note: When turning off the SPI device, please follow paragraph 20.3.4 Section's procedure operation.*

20.4.4 SPI Status Register (SPI_STS)

Address: 0x08

Reset value: 0x0000 0001

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved										OVER	MODERR	CRCERR	BUSY	RNE	TE
r										r	r	rc_w0	r	r	r

Bit Field	Name	Description
31:6	Reserved	Reserved, the reset value must be maintained.
5	OVER	Overflow flag 0: No overflow error. 1: An overflow error occurred. This bit is set by hardware, and reading the data register first and then reading the status register will clear it. *Note:This bit is set by hardware and cleared according to the sequence of software operations. For detailed information on software sequences, refer to section 20.3.7.*
4	MODERR	Mode error 0: No mode error. 1: A mode error occurred. *Note:This bit is set by hardware and cleared according to the sequence of software operations. For detailed information on software sequences, refer to section 20.3.7.*
3	CRCERR	CRC error flag 0: The received CRC value matches the value the SPI_CRCRDAT register value. 1: The received CRC value does not match the SPI_CRCRDAT register value. *Note: this bit is set by hardware and cleared by software by writing 0.*

Bit Field	Name	Description
2	BUSY	Busy flag 0: SPI is not busy. 1: SPI is busy communicating or the send buffer is not empty. This bit is set or reset by hardware. *Note: Special care should be taken when using this flag, as described in sections 20.3.3 and 20.3.4.*
1	RNE	Receive buffer is not empty 0: The receive buffer is empty. 1: The receive buffer is not empty.
0	TE	The send buffer is empty 0: The send buffer is not empty. 1: The send buffer is empty.

20.4.5 SPI Data Register (SPI_DAT)

Address: 0x0C

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DAT[15:0]															
rw															

Bit Field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained.
15:0	DAT[15:0]	Data register Data to be sent or received. The data register corresponds to two buffers: one for write (transmit buffer); The other is for read (receive buffer).Write operation writes data to transmit buffer; The read operation will return the data in the receive buffer. Note on SPI mode: According to the selection of the data frame format by the SPI_CTRL1.DATFF bit, the data transmitting and receiving can be 8-bit or 16-bit. To ensure correct operation, the data frame format needs to be determined before enabling the SPI. For 8-bit data, the buffer is 8-bit, and only SPI_DAT[7:0] is used when transmitting and receiving. When receiving, SPI_DAT[15:8] is forced to 0. For 16-bit data, the buffer is 16-bit, and the entire data register is used when transmitting and receiving, that is, SPI_DAT[15:0].

20.4.6 SPI Transmit CRC Register（SPI_ CRCTDAT）

Address offset: 0x10

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Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CRCTDAT[15:0]															
r															

Bit Field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained.
15:0	CRCTDAT	Transmit CRC register When CRC calculation is enabled, CRCTDAT[15:0] contains the CRC value calculated by the bytes sent subsequently. This register is reset when '1' is written to the SPI_CTRL1.CRCEN bit. The CRC calculation uses the polynomial in SPI_CRCPOLY. When the data frame format is set to 8 bits, only the lower 8 bits participate in the calculation and follow the CRC8 standard; when the data frame format is 16 bits, all 16 bits in the register participate in the calculation and follow the CRC16 standard. *Note: reading this register when the BUSY flag (SPI_STS.BUSY) is '1' may read incorrect values.*

20.4.7 SPI Receive CRC Register (SPI_CRCRDAT)

Address offset: 0x14

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CRCRDAT[15:0]															
r															

Bit Field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained.
15:0	CRCRDAT	Receive CRC register When CRC calculation is enabled, CRCRDAT[15:0] will contain the calculated CRC value of subsequent received bytes. This register is reset when '1' is written to the SPI_CTRL1.CRCEN bit. The CRC calculation uses the polynomial in SPI_CRCPOLY. When the data frame format is set to 8 bits, only the lower 8 bits participate in the calculation and follow the CRC8 standard; when the data frame format is 16 bits, all 16 bits in the register

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		participate in the calculation and follow the CRC16 standard. *Note: reading this register when the BUSY flag (SPI_STS.BUSY) is '1' may read incorrect values.*

20.4.8 SPI CRC Polynomial Register (SPI_CRCPOLY)

Address: 0x18

Reset value: 0x0000 0007

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CRCPOLY[15:0]															
rw															

Bit Field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained.
15:0	CRCPOLY [15:0]	CRC polynomial register This register contains the polynomial used for the CRC calculation. The reset value is 0x0007, other values can be set according to the application.

20.4.9 SPI RX Sample Delay Register (SPI_CR3)

Address: 0x38

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved												DELAYTIME[3:0]			
												rw			

Bit Field	Name	Description
31:4	Reserved	Reserved, the reset value must be maintained.
3:0	DELAYTIME [15:0]	Configuration of SPI master sampling delay time, after setting the value of this register, the received data will be sampled using the delayed clock. 4'b0000: Bypass, no delay processing for the sampling clock. 4'b0001: Sample the data on the MISO port after a delay of 1/2 PCLK2 cycle. 4'b0010: Sample the data on the MISO port after a delay of 1 PCLK2 cycle. 4'b0011: Sample the data on the MISO port after a delay of 3/2 PCLK2 cycle.

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Bit Field	Name	Description
		4'b0100: Sample the data on the MISO port after a delay of 2 PCLK2 cycle. 4'b0101: Sample the data on the MISO port after a delay of 5/2 PCLK2 cycle. 4'b0110: Sample the data on the MISO port after a delay of 3 PCLK2 cycle. 4'b0111: Sample the data on the MISO port after a delay of 7/2 PCLK2 cycle. 4'b1000: Sample the data on the MISO port after a delay of 4 PCLK2 cycle. 4'b1001: Sample the data on the MISO port after a delay of 9/2 PCLK2 cycle. 4'b1010: Sample the data on the MISO port after a delay of 5 PCLK2 cycle. 4'b1011: Sample the data on the MISO port after a delay of 11/2 PCLK2 cycle. 4'b1100: Sample the data on the MISO port after a delay of 6 PCLK2 cycle. 4'b1101: Sample the data on the MISO port after a delay of 13/2 PCLK2 cycle. 4'b1110: Sample the data on the MISO port after a delay of 7 PCLK2 cycle. 4'b1111: Sample the data on the MISO port after a delay of 15/2 PCLK2 cycle. Note: This register can only be configured in SPI master full-duplex and SPI master receive modes. Configuring this bit in other SPI modes is invalid.

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21 Debug Support (DBG)

21.1 Overview

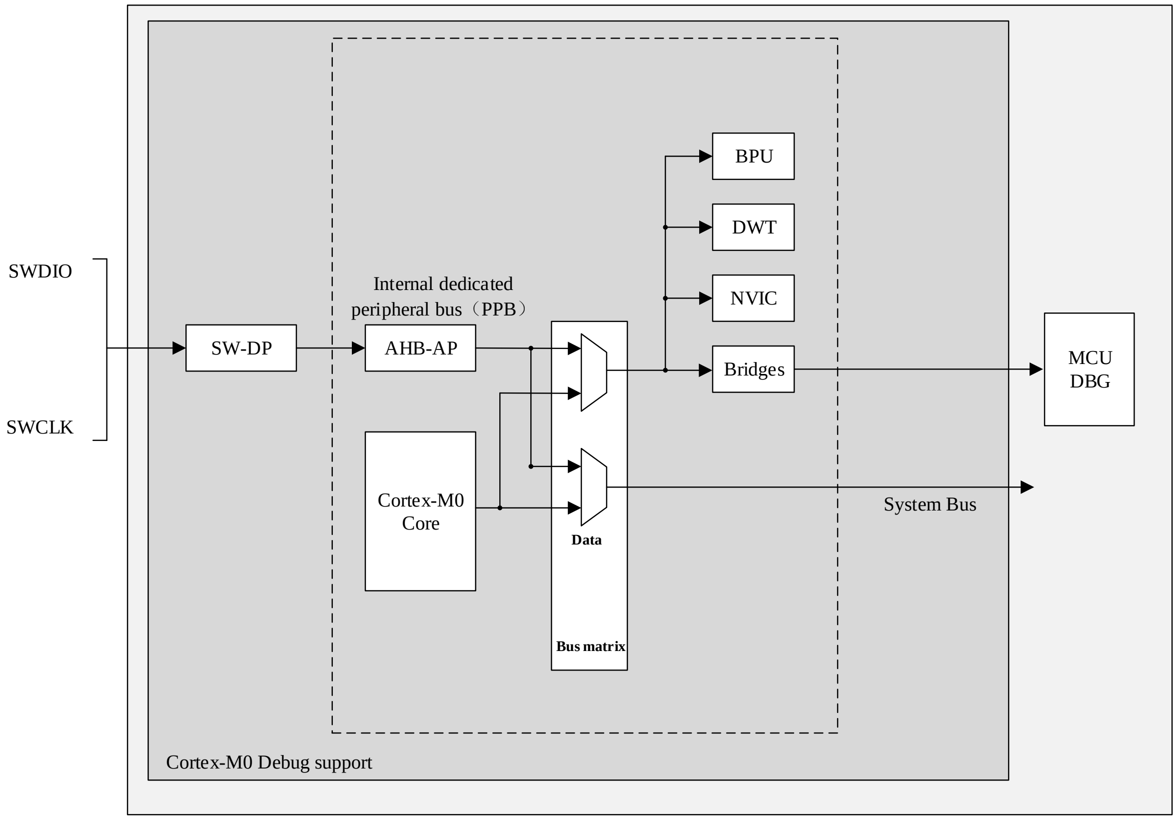
Using Cortex®-M0 core, which integrates hardware debugging module. It supports instruction breakpoint (stops when fetching instructions) and data breakpoint (stops when accessing data). When the core is stopped, the user can view the internal state of the core and the external state of the system. After the user's query operation is completed, the core and peripherals can be restored, and the corresponding program can continue to be executed.

The hardware debugging module of the core can be used when it is connected to the debugger (when it is not disabled).

Supports the following debugging interfaces:

- Serial interface

Figure 21-1 N32G033 Level And Cortex®-M0 Level Debugging Block Diagram



The ARM Cortex®-M0 core hardware debugging module can provide the following debugging functions:

- SW-DP: serial debugging port
- AHP-AP: AHB access port
- BPU: breakpoint generation
- DWT: data trigger

Reference:

- Cortex®-M0 Technical Reference Manual (TRM)

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- ARM debug interface V5 structure specification
- ARM CoreSight development tool set (r1p0 version) technical reference manual

21.2 SWD Function

The debugging tool can call the debugging function through the above-mentioned SWD debugging interface.

21.3 Pin Assignment

SWD (serial debug) interface consists of two pins: SWCLK (clock pin) and SWDIO (data input and output pin).

The pin assignment of SWD debug interface is shown in the following table:

Table 21-1 Debug Port Pin

Debug Port	Pin Assignment
SWDIO	PA13
SWCLK	PA14

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22 Unique Device Serial Number (UID)

22.1 Introduction

The MCU series products have two embedded unique device serial numbers with different lengths, namely 96-bit UID (Unique device ID) and 128-bit UCID (Unique Customer ID). These two device serial numbers are stored in the system configuration block of the Flash memory. The information they contain is written at the factory and ensures that each MCU is unique in any situation. They can be read by user applications or external devices through CPU or SWD interface and cannot be modified.

UID is 96 bits, which is usually used as serial number or password. When writing to Flash memory, this unique identifier is combined with software encryption and decryption algorithm to further improve the security of code in Flash memory, and it can also be used to activate Secure Bootloader with security function.

UCID is 128 bits and complies with the definition of the Nations Technologies chip serial number. It contains information about chip production and version.

In addition to the above two device serial numbers, there is also a 32-bit DBGMCU_ID, which contains the chip version number, chip model, and Flash/SRAM capacity information.

22.2 UID Register

Start address: 0x1FFF_F500, 96 bits in length.

22.3 UCID Register

Start address: 0x1FFF_F4D0, 128 bits in length.

22.4 DBGMCU_ID Register

Start address: 0x1FFF_F510, 32 bits in length. Different bytes are arranged with the low byte first and the high byte last; within the same byte, the high bit comes first and the low bit comes last.

Table 22-1 DBGMCU_ID Bit Description

Description	Size	Remark
Chip version number	4bit	The lower 4 bits of the chip version number.
	4bit	The upper 4 bits of the chip version number.
Chip model	4bit	The upper 4 bits of the device model number. The device model consists of 12 high, middle and low bits, representing the model of the chip.
	4bit	The middle 4 bits of the device model number.
	4bit	The lower 4 bits of the device model number.
Flash capacity	4bit	Flash capacity indicator. Fixed 64 KB
SRAM capacity	4bit	SRAM capacity indicator. Fixed 6 KB

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Reserved	4bit	1: G series.

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23 Version history

Date	Version	Modify
2025.10.11	V1.0.0	Initial version
2025.11.27	V1.1.0	1. Additional precautions for FLASH programming: After writing data, 3 NOPs need to be added 2. Section 5.2.4 adds a note that when using COMP interrupts and TIM6 interrupts, the associated EXTI can only be configured as a rising edge trigger. 3. Precautions for reusing registers: AF15 is GPIO and does not have multiplexing function 4. Precautions for adding GPIOD_DS.SDy registers: For other GPIO, VDD=5/3.3/2V corresponds to a driving capability of 12/6/3mA 5. Attention to the main features of DMA: It is not recommended to use DMA to program FLASH to avoid timing errors 6. Description of SQRT&HDIV initialization process added: SQRT_CTRLSTS.SQRTF uses default value of 0 for the first time 7. ADC-PHSWTRIG Description Update 8. 17.3 COMP Configuration Process Delete COMP_CTRL.OUTSEL Configuration 9. Add Table 17-1 COMP-OUT Pin 10. OPA write protection cancellation and addition of reset description through OPA module 11. Update of maximum and minimum reset time for IWDG count in Table 19-1 12. Precautions for adding HSI Trim and LSI Trim register descriptions 13. Precautions for adding RCC_EMCTRL.GVDET bits 14. Delete the description of the universal output leakage mode, which is not supported
2026.1.26	V1.1.1	1. Delete the description that executing code under SRAM cannot operate FLASH 2. Remove read-only access to Flash system storage area at L0 level during SRAM startup 3. Update DMA_CSELx register description 4. Precautions for adding TIMx_CTRL1.PBKPEN/LBKPEN positions 5. TIMx_ENCLVR.LVR update bit width is 16 bits 6. IWDG adds freeze mode related descriptions and register bits 7. SPI_STS register bit reset value update 8. COMP_CTRL.PWRMD bit description update
2026.3.30	V1.2.0	1. Update of NRST description in section 6.2.2 Status after Reset 2. Change the IO configuration of external devices TIM1_BKIN and TIM1_ETR to "input mode+multiplexing function" 3. Change the 11b value of OPAMP_VREFSEL.OPAxSEL[1:0] to be retained

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