N32H7xx Series Errata Sheet

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1 List of Errata

Table 1-1 Errata Overview

Errata Lit		Chip Revision			
		A	B	C	D
GPIO and AFIO **1.1 Digital Filter Cannot Be Enabled When Reading GPIO I/J/K Registers** **Description** The digital filter function cannot be enabled when reading GPIO I/J/K registers. Digital filters for other alternate functions work normally. **Workaround** None **2 PWR** **2.1 Debugger Connection Issue in Sleep Mode** **Description** After the chip enters sleep mode (SLEEP/STOP0/STOP2/STANDBY), the debugger cannot download or	Digital Filter Cannot Be Enabled When Reading GPIO I/J/K Registers	•			

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debug. The chip must exit sleep mode first before using the debugger to download and debug. **Workaround** None **3 AHB Cache** **3.1 Enabling AHB Cache Causes Legitimate Access to Be Blocked** **Description** When CM4 enables AHB Cache, access permissions for all regions are forcibly changed to match the debugger's access permissions, which causes some legitimate accesses to be blocked, such as certain user APIs that cannot be used. Workaround It is not recommended to enable AHB Cache when using CM4. It is recommended to execute CM4 programs in AHB SRAM, which is 0-wait access SRAM, therefore AHB Cache is not needed.					

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4 RTC **4.1 RTC Calibration Invalid** **Description** The RTC calibration mode does not work. **Workaround**					
PWR	Debugger Connection Issue in Sleep Mode	●			
AHB Cache	Enabling AHB Cache Causes Legitimate Access to Be Blocked	●			
RTC	RTC Calibration Invalid	●			
TIMER	Issue with Switching to 0% Duty Cycle PWM Mode in Force Active Mode	●			

●: Issue exists

-: Issue does not exist

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2 GPIO and AFIO

2.1 Digital Filter Cannot Be Enabled When Reading GPIO I/J/K Registers

Description

The digital filter function cannot be enabled when reading GPIO I/J/K registers. Digital filters for other alternate functions work normally.

Workaround

None

3 PWR

3.1 Debugger Connection Issue in Sleep Mode

Description

After the chip enters sleep mode (SLEEP/STOP0/STOP2/STANDBY), the debugger cannot download or debug. The chip must exit sleep mode first before using the debugger to download and debug.

Workaround

None

4 AHB Cache

4.1 Enabling AHB Cache Causes Legitimate Access to Be Blocked

Description

When CM4 enables AHB Cache, access permissions for all regions are forcibly changed to match the

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debugger's access permissions, which causes some legitimate accesses to be blocked, such as certain user APIs that cannot be used.

Workaround

It is not recommended to enable AHB Cache when using CM4. It is recommended to execute CM4 programs in AHB SRAM, which is 0-wait access SRAM, therefore AHB Cache is not needed.

5 RTC

5.1 RTC Calibration Invalid

Description

The RTC calibration mode does not work.

Workaround

It is recommended to use a precise clock source that does not require calibration, such as LSE.

6 TIMER

6.1 Issue with Switching to 0% Duty Cycle PWM Mode in Force Active Mode

Description

All ATIM/GTIM in force active mode (OC1MD[2:0]=101) cannot properly implement switching to PWM mode with 0% duty cycle.

Workaround

None

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7 I2C

Timeout Counter Reset in Debug Mode

Description

When in debug mode and the core is stopped, SMBus timeout can be set to stop or continue normal operation via DBG_M7/M4APB1FZ.I2CxSTOP. However, the timeout counter will be reset, causing incorrect timeout values during debugging.

Workaround

None

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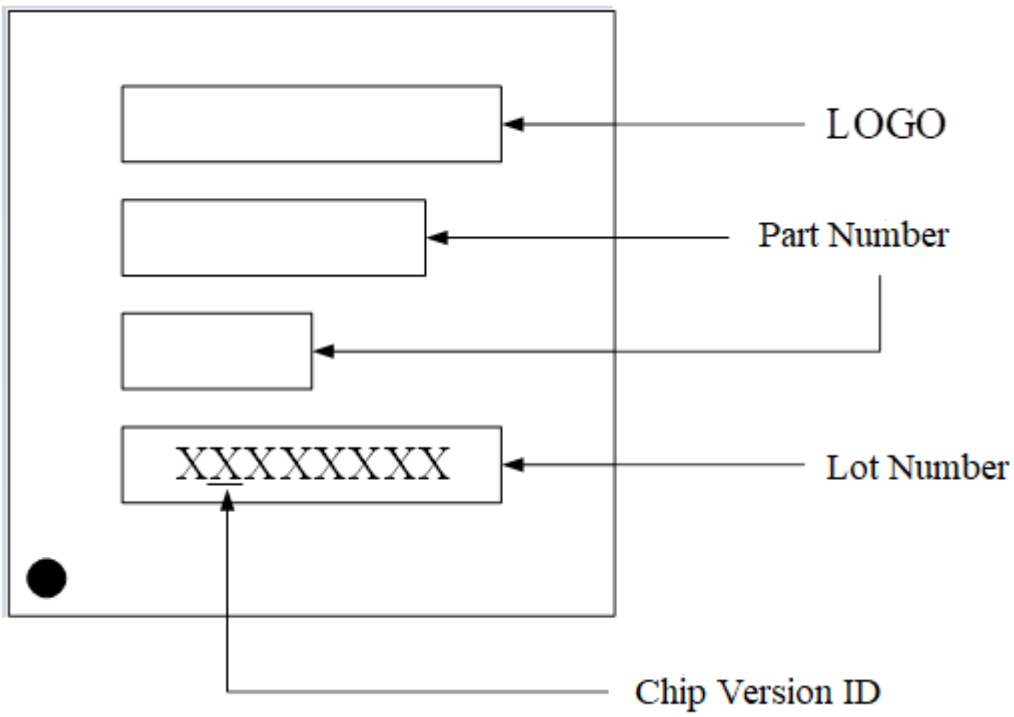
8 Chip Marking and Version Information



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9 Version History

Version	Date	Changes
V1.0.0	2025.4.24	First release

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