N32H785 Product Brief

The N32H785 series features a high-performance dual-core architecture. The ARM Cortex-M7 core serves as the main processor, running at frequencies up to 600MHz, supporting double-precision floating-point operations and DSP instructions. The Cortex-M4 core functions as an auxiliary processor, running at frequencies up to 300MHz. It integrates (2/4MB) of on-chip FLASH and up to 1504KB of SRAM (including 1024KB TCM SRAM and 480KB SRAM) + 4KB Backup SRAM. The series includes 3 12-bit 5Msps ADCs, 4 high-speed comparators, and 6 12-bit DACs. It integrates multiple high-speed communication interfaces including U(S)ART, I2C, xSPI, SPI, USBFS Dual Role, USBHS Dual Role, CAN-FD, SDRAM, FEMC, SDMMC, and 10/100/1000M Ethernet. It supports digital camera interfaces (DVP), TFT-LCD graphic interfaces, JPEG hardware codec, and GPU. It features a built-in high-performance encryption algorithm hardware acceleration engine that supports AES/TDES, SHA, and SM4 algorithms, as well as TRNG (True Random Number Generator) and CRC8/16/32. It supports up to 166 GPIOs and is available in LQFP176, UFBGA176+25, LQFP208, and TFBGA240+25 packages.

Key Features

Dual-Core CPU Architecture (Cortex-M7 and Cortex-M4F)

- **ARM Cortex-M7**
  - 32-bit ARM Cortex-M7 core with double-precision floating-point unit, supporting DSP instructions and MPU
  - Built-in 32KB instruction cache and 32KB data cache with ECC
  - Maximum frequency of 600MHz, 1284 DMIPS
- **ARM Cortex-M4F**
  - 32-bit ARM Cortex-M4F core + FPU, single-cycle hardware multiply/divide instructions, supporting DSP instructions and MPU
  - Built-in 16KB instruction cache and 16KB data cache with parity checking, supporting Flash acceleration unit for zero-wait program execution
  - Maximum frequency of 300MHz, 375 DMIPS
- **Encrypted Memory**
  - 2M/4M Byte on-chip Flash, supporting encrypted storage with automatic program decryption during execution
  - 1504KB built-in SRAM with ECC support
    - 1024KB TCM SRAM, configurable as D-TCM, I-TCM, or SRAM
    - 480KB on-chip SRAM
- **Operating Modes**
  - Run mode
  - SLEEP mode: AXI enabled, AHB enabled
  - Stop0 mode: SRAM, TCM, RTC, LSE, IWDG enabled
  - Stop2 mode: Flash in standby mode; SRAM, TCM, RTC, LSE, IWDG, Backup SRAM, backup registers enabled; I/O state maintained

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- Standby mode: Backup SRAM, RTC, IWDG, LSE, backup registers enabled; SRAM, TCM disabled
- VBAT mode: Backup SRAM, RTC, LSE, backup registers enabled

- **Clock**
  - 4MHz~48MHz external high-speed crystal
  - 4MHz~50MHz external clock input
  - 32.768KHz external low-speed crystal
  - Three built-in high-speed PLLs
  - Built-in MSI clock, configurable for 31.25K/62.5K/125K/250K/500K/1M/2M/4M/8M/16MHz
  - Internal high-speed RC 64MHz
  - Internal low-speed RC 32KHz
- **Reset**
  - Supports power-on/power-down/external pin reset
  - Supports watchdog reset and software system reset
  - Programmable voltage detection
- **High-Speed Communication Interfaces**
  - 8 USART interfaces/7 UART interfaces, supporting ISO7816, IrDA, LIN
  - 2 LPUART interfaces
  - 7 SPI interfaces, supporting master/slave modes, rates up to 50 MHz
  - 10 I2C interfaces, speeds up to 3.4 MHz, configurable master/slave modes, dual address response in slave mode
  - 1 USBHS Dual Role interface with built-in high-speed PHY
  - 1 USBFS Dual Role interface
  - 8 CAN-FD bus interfaces
  - 2 Ethernet MAC interfaces: ETH1 supporting 10M/100M/1000M communication rates, ETH2 supporting 10M/100M rates, both supporting IEEE 1588 time synchronization protocol
- **High-Performance Analog Interfaces**
  - 3 12-bit 5Msps ADCs, supporting 12-bit, 10-bit resolution, hardware oversampling up to 16-bit, supporting up to 55 external single-ended input channels, 5 internal single-ended input channels, supporting both single-ended and differential modes
  - 4 high-speed analog comparators
  - 6 12-bit DACs: 2 1Msps DACs supporting output with or without buffer independently, internal output only supports mode without buffer; simultaneous internal and external output requires buffer enabled; 4 additional DACs supporting only one internal output channel with 15Msps sampling rate and without buffer
  - 2 MCO outputs, configurable to output SYSCLK, HSE, MSI, LSE, LSI, HSI64, or PLL clock division
  - 1 reference voltage output VREFBUF (configurable to 1.5V/1.8V/2.048V/2.5V)
  - 1 temperature sensor
- **Audio Interfaces**

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- 4 I2S interfaces, supporting master/slave modes, audio sampling frequency support from 8KHz to 192KHz
- 8 PDM digital microphone interfaces built into the DSMU

- **Memory Expansion Interfaces**
  - 1 FEMC (Flexible External Memory Controller) interface, 100 MHz bus rate, configurable 16/32-bit data width for SRAM/PSRAM/Nor Flash, configurable 8/16-bit data width for NAND Flash
  - 1 xSPI interface, supporting 1/2/4/8-bit data width, master/slave configurable, rates up to 133 MHz, usable for external SRAM, PSRAM and Flash, supporting XIP
  - 1 SDRAM interface, rates up to 133 MHz
  - 2 SDMMC interfaces, supporting SD/SDIO 3.0, eMMC 4.51 format, rates up to 104MHz
- **Image Processing Interfaces**
  - 2 digital camera interfaces (DVP), supporting 8/10/12/16bit, rates up to 110MHz
  - 1 TFT-LCD display interface, supporting up to 24-bit parallel digital RGB LCD, providing all signal interfaces for direct connection to various LCD and TFT panels, resolution up to 1920x1080
  - Built-in 2.5D graphics processor, supporting image scaling, rotation, mixing, anti-aliasing, texture mapping, etc.
  - Hardware JPEG encoder/decoder
- **Up to 166 GPIOs, low-speed GPIOs supporting 5V tolerance (under VDD = 3.3V±10% conditions)**
- **Motor Control Cordic Accelerator, supporting trigonometric and hyperbolic function acceleration, floating-point input and output**
- **Delta Sigma Module Unit (DSMU)**
- **Built-in filter algorithm accelerator FMAC, supporting FIR, IIR filtering**
- **3 high-speed DMA controllers, each supporting 8 channels, 1 MDMA supporting 16 channels, configurable source and destination addresses for all channels**
- **RTC real-time clock, supporting leap year perpetual calendar, alarm events, periodic wake-up, internal and external clock calibration**
- **Timer Counters**
  - 2 16-bit super high-precision timer counters (SHRTIM1/SHRTIM2), highest control precision 100ps, each with 1 master timer and 6 16-bit slave timer units. Each timer unit has 2 independent channels, supporting 12 independent PWM outputs or 6 pairs of complementary PWM outputs
  - 4 16-bit advanced timer counters (ATIM1~4), supporting input capture, complementary output, quadrature encoding input, etc., highest control precision 3.3ns; each timer has 6 independent channels, 4 of which support 4 pairs of complementary PWM outputs
  - 10 16-bit general-purpose timers (GTIMA13), each with 4 independent channels, supporting input capture, output compare, PWM generation
  - 4 32-bit basic timer counters (BTIM1~4)
  - 5 16-bit low-power timers (LPTIM1~5), operable in Stop2 mode
  - 2x 24-bit SysTick, 2x 14-bit window watchdog (WWDG), 2x 12-bit independent watchdog (IWDG)

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- **Programming Methods**
  - Supporting SWD/JTAG for online debugging
  - Supporting USB, USART Bootloader
- **Security Features**
  - Flash has up to 4 encryption partitions, supporting storage encryption
  - Write protection (WRP), multiple read protection (RDP) levels (L0/L1/L2)
  - Built-in cryptographic algorithm hardware acceleration engine, supporting AES/TDES, SHA, SM4 algorithms
  - TRNG (True Random Number Generator), CRC8/16/32 operations
  - Secure boot, encrypted program download, secure update, detection of external high-speed and low-speed clock failures
  - Anti-tamper detection
- **128-bit UCID supported in OTP**
- **Operating Conditions**
  - Operating voltage range: 2.3V~3.6V
  - Chip junction temperature range: -40°C to 125°C
- **Certification**
  - USB IF
  - IEC61508 SIL2
- **Package**
  - LQFP176(24mm x 24mm)
  - UFBGA176+25(10mm x 10mm)
  - LQFP208(28mm x 28mm)
  - TFBGA240+25(14mm x 14mm)
- **Ordering Model**

Series	Model
N32H785xxx7	N32H785IKL7, N32H785IIL7, N32H785IKB7, N32H785IIB7, N32H785BKL7, N32H785BIL7, N32H785XKB7, N32H785XIB7

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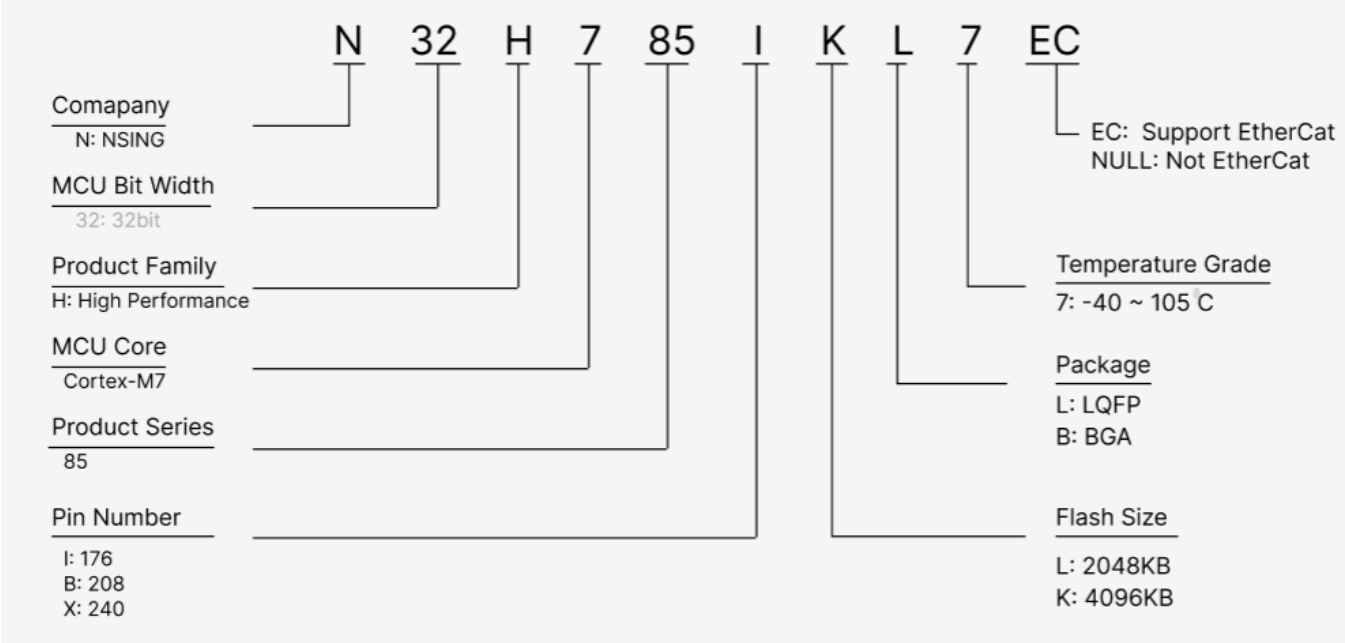
1 Naming Convention



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2 Product Model and Resource Configuration

Table 0-1 N32H785 Series Resource Configuration

Device Model		N32H785 IKL7	N32H785 IIL7	N32H785 IKB7	N32H785 IIB7	N32H785 BKL7	N32H785 BIL7	N32H785 XKB7	N32H785 XIB7
Flash（KB）		4096	2048	4096	2048	4096	2048	4096	2048
SRAM（KB）	TCM	1024							
	System RAM	480							
	Backup RAM	4							
Core	M7	600MHz							
	M4	300MHz							
Operating Voltage		2.3V~3.6V							
DCDC（step-down）		Yes							
Coprocessor	Cordic	Yes							
	DSMU	Yes							
	FMAC	Yes							
Timers	SHRTIM	2							
	ADTIM	4							
	GPTIM	10							
	BSTIM	4							
	LPTIM	5							
	SysTick timer	2							
	WWDG	2*14bit							
	IWDG	2*12bit							
	RTC	Yes							
Communication Interfaces	SPI/I2S	6/4				7/4			
	I2C	8				10			
	USART	7				8			
	UART	6				7			
	LPUART	2							
	USBHS Dual Role	1							
	USBFS Dual Role	1							
	CAN FD	8							
	10/100M ETH	1							
	10/100/1000 M ETH	1							
Expanded Storage	SDRAM	Yes							
	xSPI	1							
	FEMC	Yes							
	SDMMC	2							
Analog	12bit ADC	3							
	12bit DAC	2+4(1) 2 External channels							

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	Number of channels				
	Comparator	4			
	VREFBUF	Yes			
Imaging	LCDC	Yes			
	GPU	Yes			
	JPEG	Yes			
	DVP	2			
GPIO		117	126	148	166
DMA Number of channels		3 24Channel			
MDMA Number of channels		1 16Channel			
Algorithm Support		DES/3DES, AES, SHA1/SHA224/SHA256, CRC8/16/CRC32			
Security Protection		Read/write protection (RDP/WRP), storage encryption, secure boot			
Package		LQFP176	UFBGA176+25	LQFP208	TFBGA240+25

Note：4 DACs only support internal connection and cannot output to GPIO

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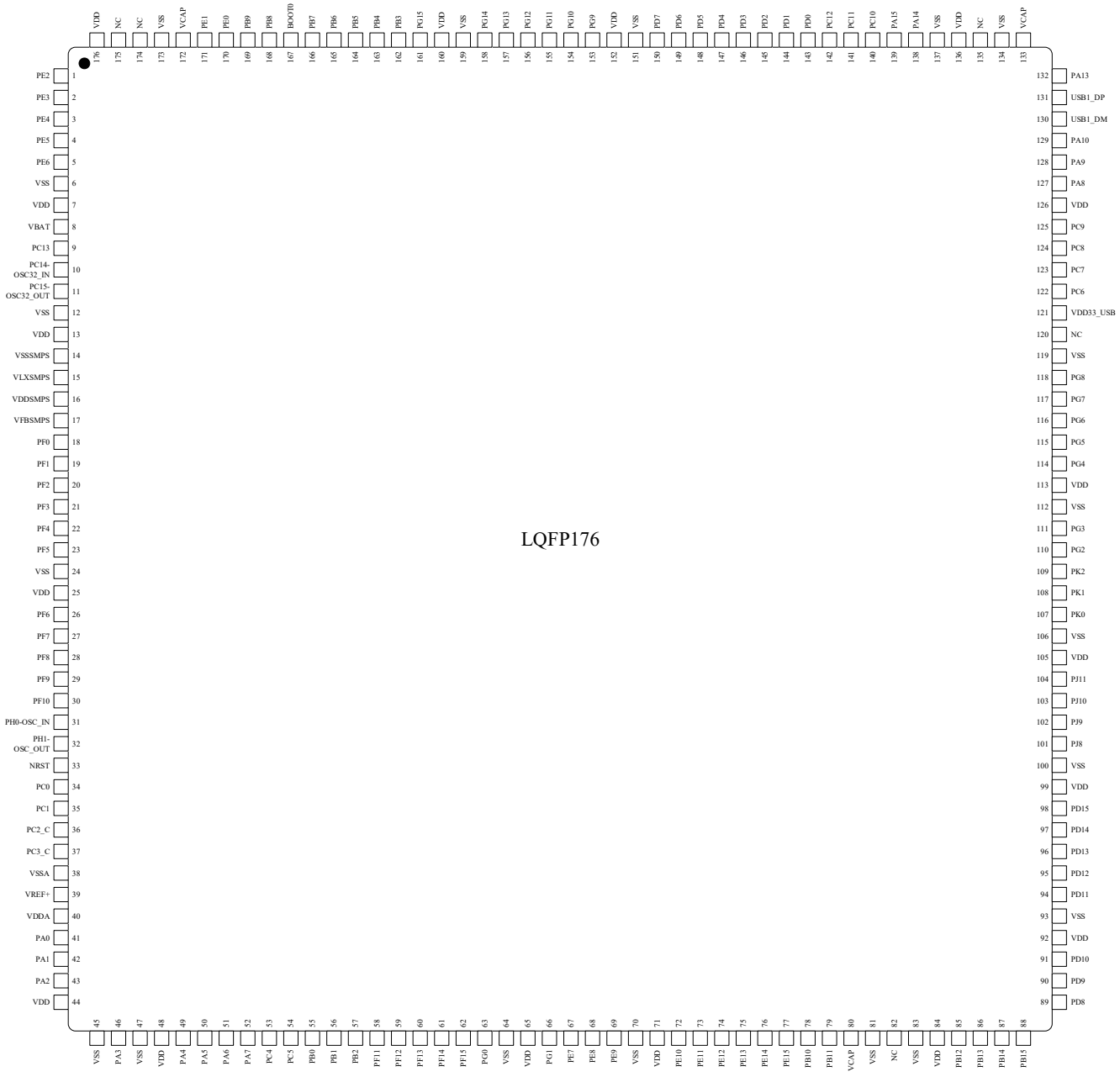
3 Package

LQFP176 Package

LQFP176 Pin Distribution



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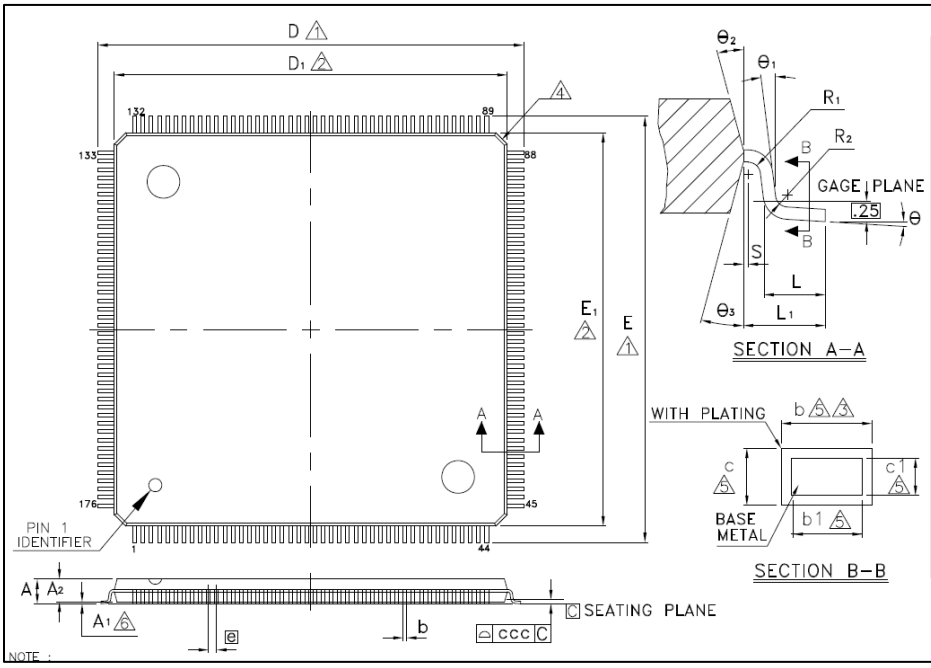
LQFP176 Package Size



Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	—	—	1.60	—	—	0.063
A1	0.025	—	0.127	0.001	—	0.005
A2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.17	0.22	0.27	0.007	0.009	0.011
b1	0.17	0.20	0.23	0.007	0.008	0.009
c	0.09	0.14	0.20	0.004	0.006	0.008
c1	0.09	0.12	0.16	0.004	0.005	0.006
D	25.85	26.00	26.15	1.018	1.024	1.030
D1	23.90	24.00	24.10	0.941	0.945	0.949
E	25.85	26.00	26.15	1.018	1.024	1.030
E1	23.90	24.00	24.10	0.941	0.945	0.949
e	0.50 BSC			0.020 BSC		
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF			0.039 REF		
R1	0.08	—	—	0.003	—	—
R2	0.08	—	0.20	0.003	—	0.008
S	0.20	—	—	0.008	—	—
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	0°	—	—	0°	—	—
θ2	11°	12°	13°	11°	12°	13°
θ3	11°	12°	13°	11°	12°	13°
ccc	0.08			0.003		

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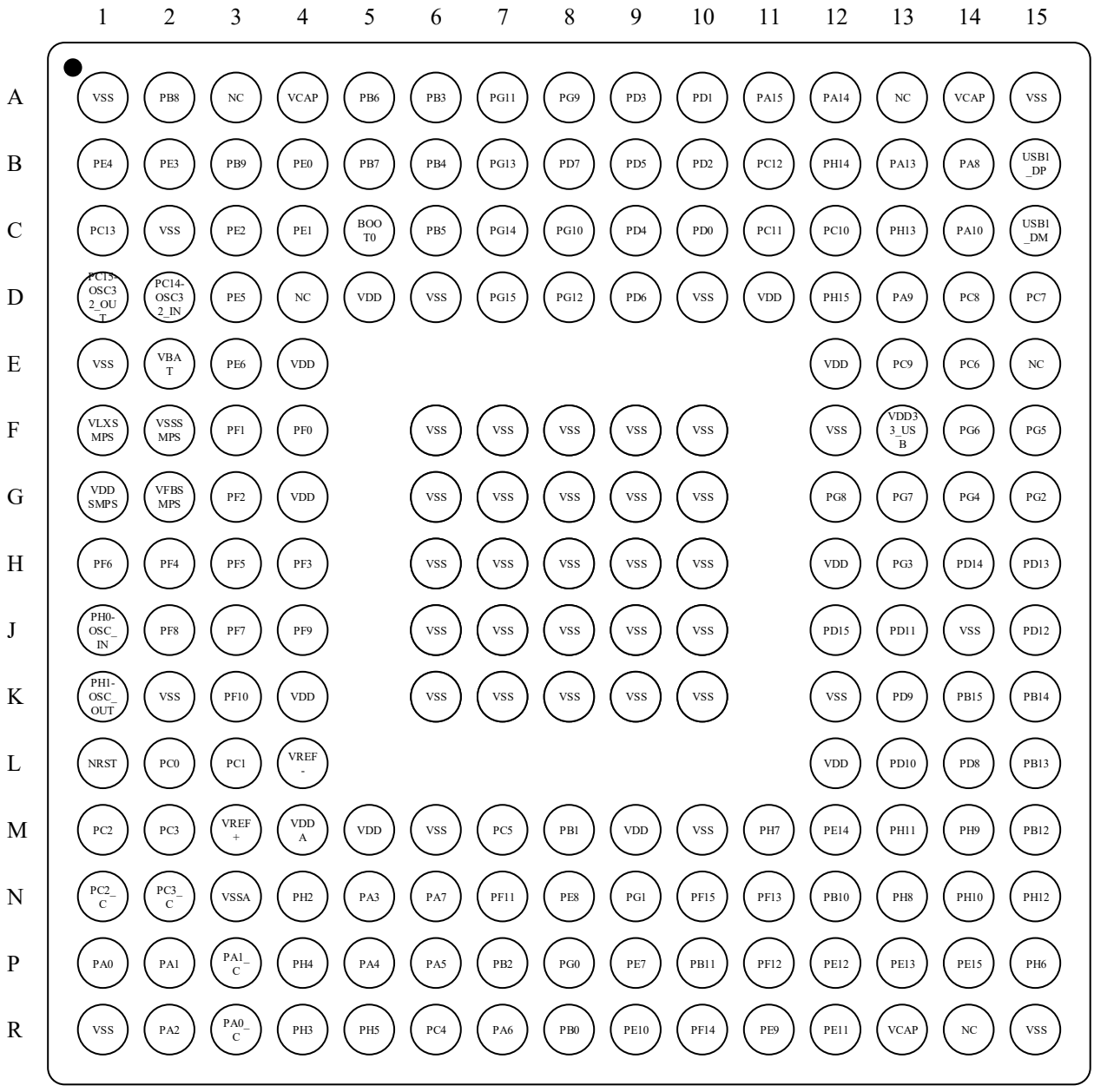
UFBGA176+25 Package

UFBGA176+25 Pin Distribution



	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
A	VSS	PB8	NC	VCAP	PB6	PB3	PG11	PG9	PD3	PD1	PA15	PA14	NC	VCAP	VSS
B	PE4	PE3	PB9	PE0	PB7	PB4	PG13	PD7	PD5	PD2	PC12	PH14	PA13	PA8	USB1_DP
C	PC13	VSS	PE2	PE1	BOOT0	PB5	PG14	PG10	PD4	PD0	PC11	PC10	PH13	PA10	USB1_DM
D	PC15-OSC32_OUT	PC14-OSC32_IN	PE5	NC	VDD	VSS	PG15	PG12	PD6	VSS	VDD	PH15	PA9	PC8	PC7
E	VSS	VBAT	PE6	VDD								VDD	PC9	PC6	NC
F	VLXSMPS	VSSSMPS	PF1	PF0		VSS	VSS	VSS	VSS	VSS		VSS	VDD33_USB	PG6	PG5
G	VDDSMPS	VFBSMPS	PF2	VDD		VSS	VSS	VSS	VSS	VSS		PG8	PG7	PG4	PG2
H	PF6	PF4	PF5	PF3		VSS	VSS	VSS	VSS	VSS		VDD	PG3	PD14	PD13
J	PH0-OSC_IN	PF8	PF7	PF9		VSS	VSS	VSS	VSS	VSS		PD15	PD11	VSS	PD12
K	PH1-OSC_OUT	VSS	PF10	VDD		VSS	VSS	VSS	VSS	VSS		VSS	PD9	PB15	PB14
L	NRST	PC0	PC1	VREF-								VDD	PD10	PD8	PB13
M	PC2	PC3	VREF+	VDDA	VDD	VSS	PC5	PB1	VDD	VSS	PH7	PE14	PH11	PH9	PB12
N	PC2_C	PC3_C	VSSA	PH2	PA3	PA7	PF11	PE8	PG1	PF15	PF13	PB10	PH8	PH10	PH12
P	PA0	PA1	PA1_C	PH4	PA4	PA5	PB2	PG0	PE7	PB11	PF12	PE12	PE13	PE15	PH6
R	VSS	PA2	PA0_C	PH3	PH5	PC4	PA6	PB0	PE10	PF14	PE9	PE11	VCAP	NC	VSS

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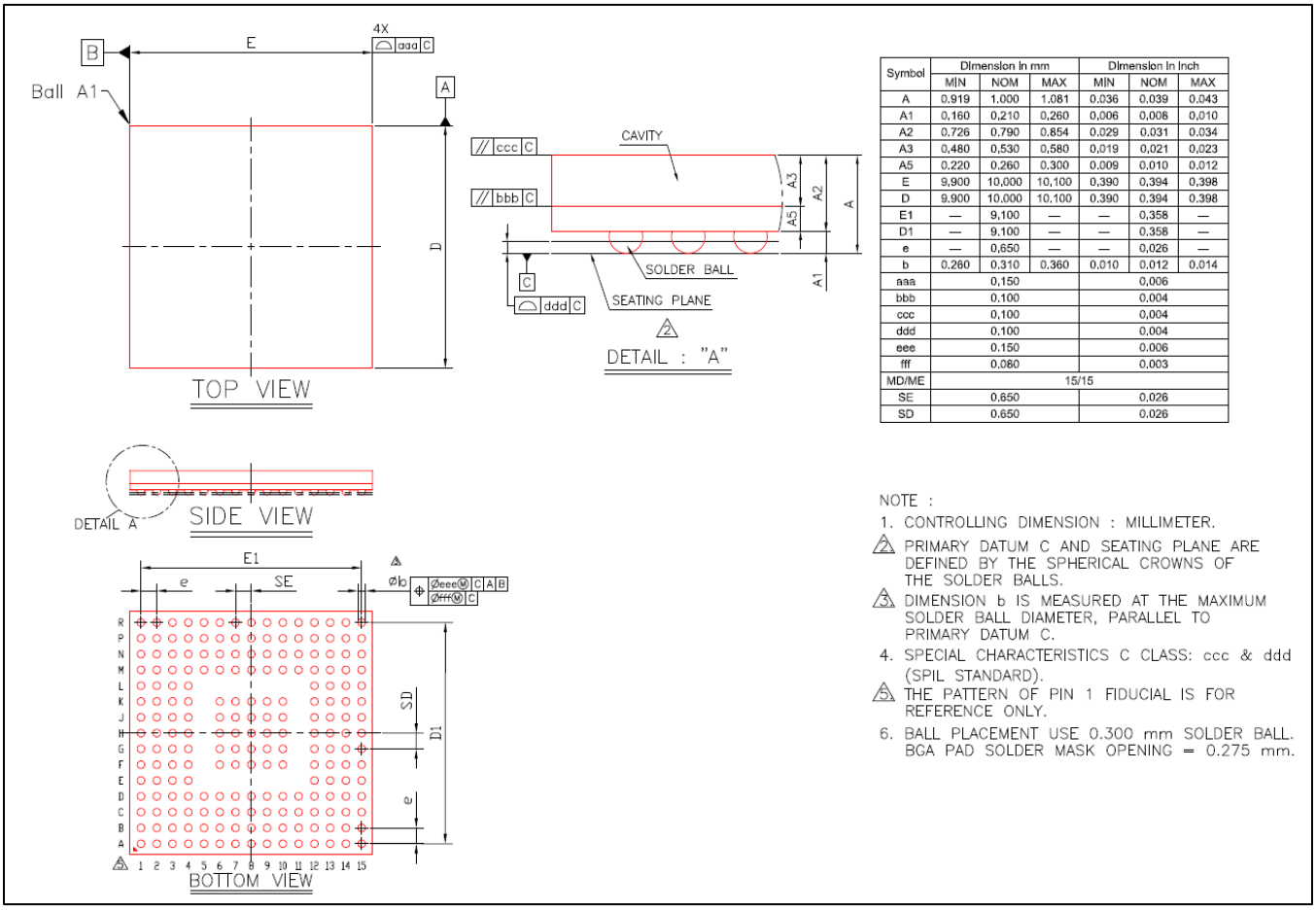
UFBGA176+25 Package Size



Symbol	Dimension in mm			Dimension in Inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.919	1.000	1.081	0.036	0.039	0.043
A1	0.160	0.210	0.260	0.006	0.008	0.010
A2	0.726	0.790	0.854	0.029	0.031	0.034
A3	0.480	0.530	0.580	0.019	0.021	0.023
A5	0.220	0.260	0.300	0.009	0.010	0.012
E	9.900	10.000	10.100	0.390	0.394	0.398
D	9.900	10.000	10.100	0.390	0.394	0.398
E1	—	9.100	—	—	0.358	—
D1	—	9.100	—	—	0.358	—
e	—	0.650	—	—	0.026	—
b	0.260	0.310	0.360	0.010	0.012	0.014
aaa		0.150			0.006	
bbb		0.100			0.004	
ccc		0.100			0.004	
ddd		0.100			0.004	
eee		0.150			0.006	
fff		0.080			0.003	
MD/ME		15/15				
SE		0.650			0.026	
SD		0.650			0.026	

NOTE :

1. CONTROLLING DIMENSION : MILLIMETER.
2. PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
3. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM C.
4. SPECIAL CHARACTERISTICS C CLASS: ccc & ddd (SPIL STANDARD).
5. THE PATTERN OF PIN 1 FIDUCIAL IS FOR REFERENCE ONLY.
6. BALL PLACEMENT USE 0.300 mm SOLDER BALL. BGA PAD SOLDER MASK OPENING = 0.275 mm.

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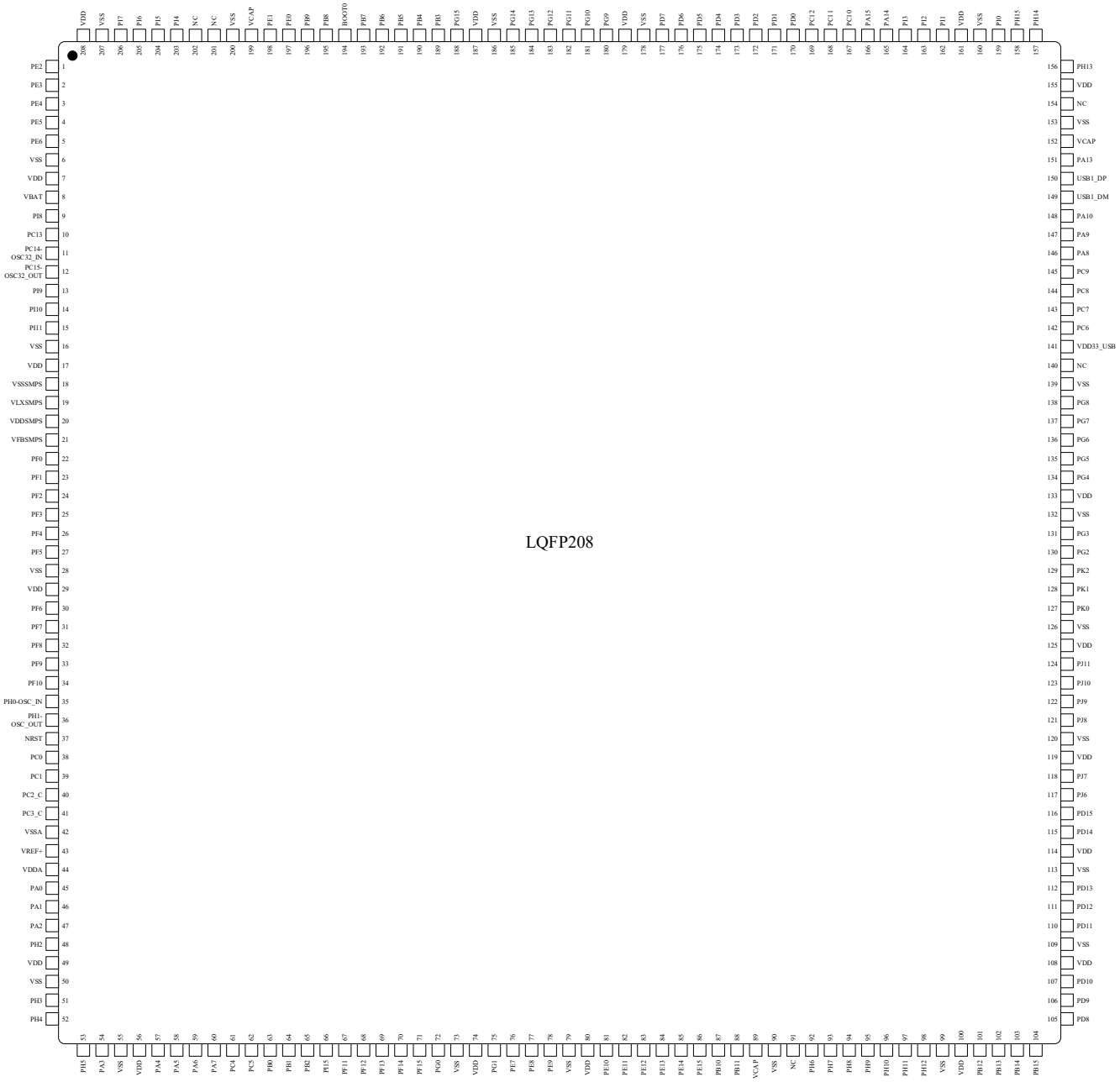
LQFP208 Package

LQFP208 Pin Distribution



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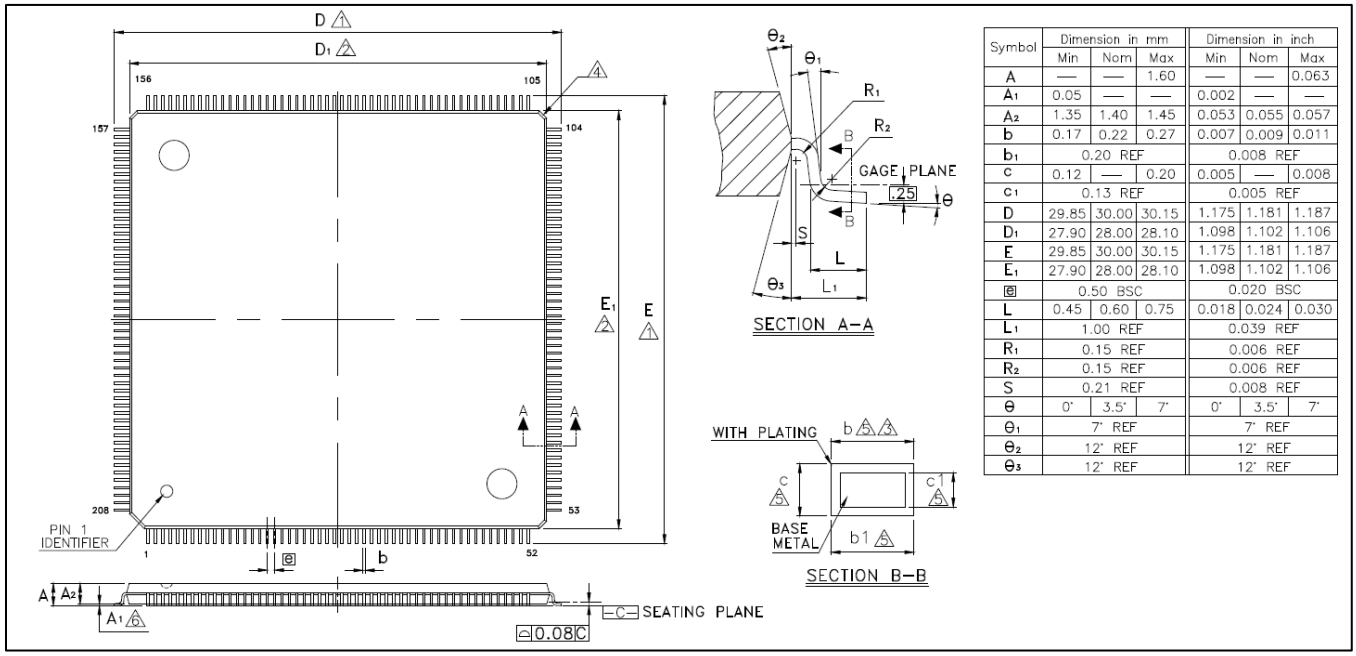
LQFP208 Package Size



Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	—	—	1.60	—	—	0.063
A_1	0.05	—	—	0.002	—	—
A_2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.17	0.22	0.27	0.007	0.009	0.011
b_1	0.20 REF			0.008 REF		
c	0.12	—	0.20	0.005	—	0.008
c_1	0.13 REF			0.005 REF		
D	29.85	30.00	30.15	1.175	1.181	1.187
D_1	27.90	28.00	28.10	1.098	1.102	1.106
E	29.85	30.00	30.15	1.175	1.181	1.187
E_1	27.90	28.00	28.10	1.098	1.102	1.106
e	0.50 BSC			0.020 BSC		
L	0.45	0.60	0.75	0.018	0.024	0.030
L_1	1.00 REF			0.039 REF		
R_1	0.15 REF			0.006 REF		
R_2	0.15 REF			0.006 REF		
S	0.21 REF			0.008 REF		
θ	0°	3.5°	7°	0°	3.5°	7°
$θ_1$	7° REF			7° REF		
$θ_2$	12° REF			12° REF		
$θ_3$	12° REF			12° REF		

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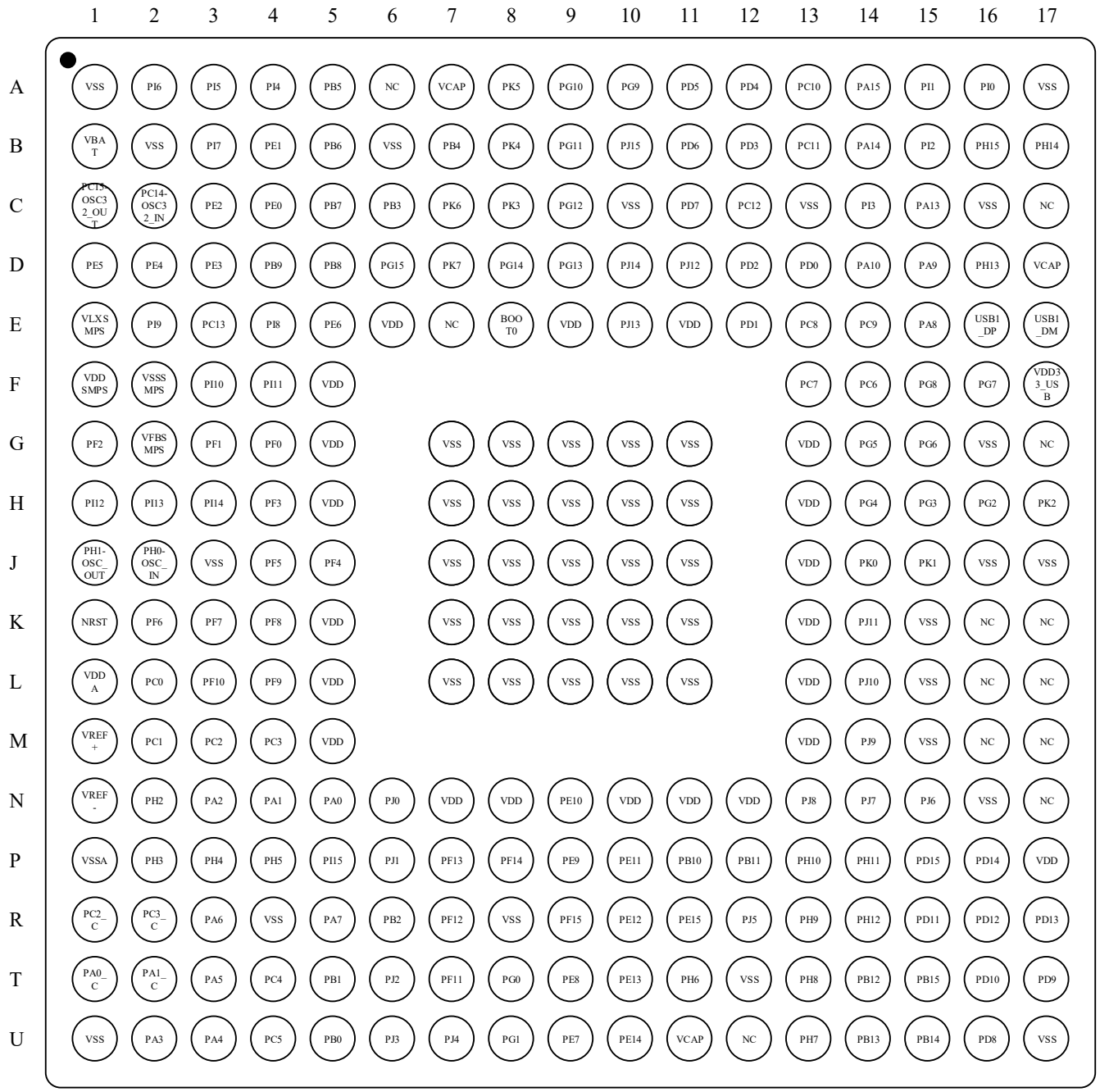
TFBGA240+25 Package

TFBGA240+25 Pin Distribution



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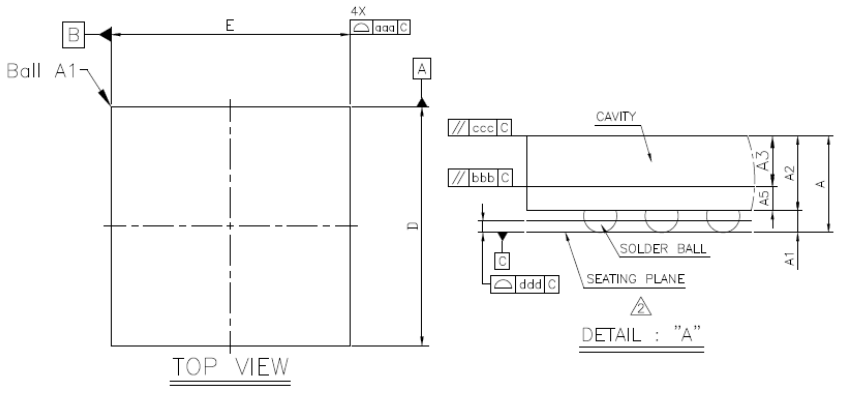
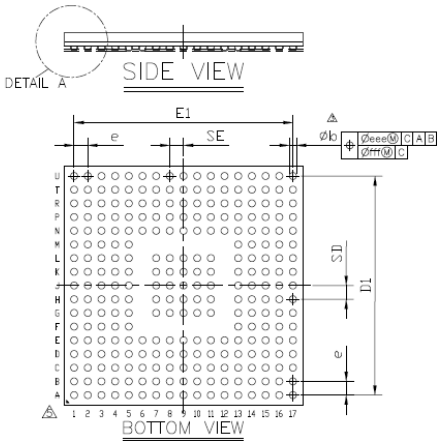
TFBGA240+25 Package Size



Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.009	1.090	1.171	0.040	0.043	0.046
A1	0.250	0.300	0.350	0.010	0.012	0.014
A2	0.726	0.790	0.854	0.029	0.031	0.034
A3	0.480	0.530	0.580	0.019	0.021	0.023
A5	0.220	0.260	0.300	0.009	0.010	0.012
E	13.900	14.000	14.100	0.547	0.551	0.555
D	13.900	14.000	14.100	0.547	0.551	0.555
E1	---	12.800	---	---	0.504	---
D1	---	12.800	---	---	0.504	---
e	---	0.800	---	---	0.031	---
b	0.360	0.410	0.460	0.014	0.016	0.018
aaa		0.150			0.006	
bbb		0.100			0.004	
ccc		0.100			0.004	
ddd		0.130			0.005	
eee		0.150			0.006	
fff		0.080			0.003	
MD/ME		17/17				
SE		0.800			0.031	
SD		0.800			0.031	



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4 Version History

Version	Date	Changes
V1.0.0	2025.4.22	First release

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