

N32H765EC

Product Brief

The N32H765EC series uses an ARM Cortex-M7 core, running at frequencies up to 600MHz, supporting double-precision floating-point operations and DSP instructions. It integrates (2/4MB) of on-chip FLASH and up to 1504KB of SRAM (including 1024KB TCM SRAM and 480KB SRAM) + 4KB Backup SRAM. The series includes 3 12-bit 5MSPS ADCs, 4 high-speed comparators, and 6 12-bit DACs. It integrates multiple high-speed communication interfaces including U(S)ART, I2C, xSPI, SPI, USBFS Dual Role, USBHS Dual Role, CAN-FD, SDRAM, FEMC, SDMMC, 10/100/1000M Ethernet, and EtherCAT. It supports a digital camera interface (DVP), TFT-LCD graphic interface, JPEG hardware codec, and GPU. It features a built-in high-performance encryption algorithm hardware acceleration engine that supports AES/TDES, SHA algorithms, as well as TRNG (True Random Number Generator) and CRC8/16/32. It supports up to 126 GPIOs and is available in UFBGA176+25 packaging.

Key Features

- **Core CPU**
 - 32-bit ARM Cortex-M7 core with double-precision floating-point unit, supporting DSP instructions and MPU
 - Built-in 32KB instruction cache and 32KB data cache with ECC
 - Maximum frequency of 600MHz, 1284 DMIPS
- **Encrypted Memory**
 - 2M/4M Byte on-chip Flash, supporting encrypted storage with automatic program decryption during execution
 - 1504KB built-in SRAM with ECC support
 - 1024KB TCM SRAM, configurable as D-TCM, I-TCM, or SRAM
 - 480KB on-chip SRAM
 - 4KB Backup SRAM with ECC support
- **Operating Modes**
 - Run mode
 - SLEEP mode: AXI enabled, AHB enabled
 - Stop0 mode: SRAM, TCM, RTC, LSE, IWDG enabled
 - Stop2 mode: Flash in standby mode; SRAM, TCM, RTC, LSE, IWDG, Backup SRAM, backup registers enabled; I/O state maintained
 - Standby mode: Backup SRAM, RTC, IWDG, LSE, backup registers enabled; SRAM, TCM disabled
 - VBAT mode: Backup SRAM, RTC, LSE, backup registers enabled
- **Clock**
 - 4MHz~48MHz external high-speed crystal
 - 4MHz~50MHz external clock input
 - 32.768KHz external low-speed crystal
 - Three built-in high-speed PLLs

NSING Technologies Pte. Ltd.

Address: 20 Science Park, #03-15/16

Teletech Park, East Wing, Singapore 117674

Email: sales@nsing.com.sg

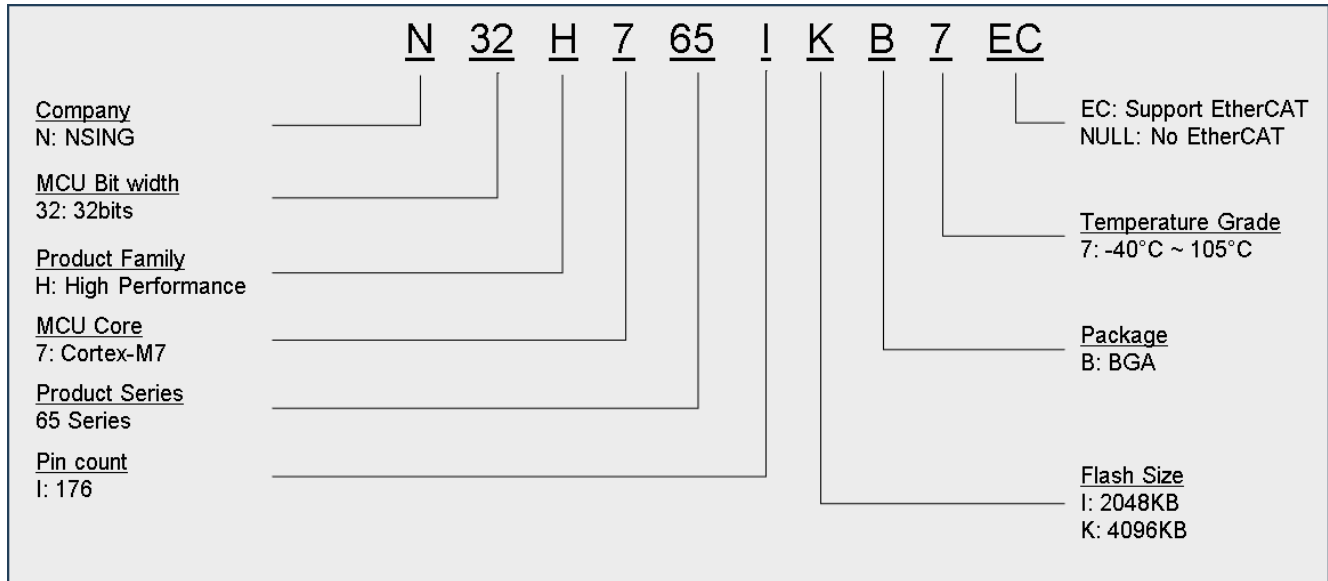
- Built-in MSI clock, configurable for 31.25K/62.5K/125K/250K/500K/1M/2M/4M/8M/16MHz
- Internal high-speed RC 64MHz
- Internal low-speed RC 32KHz
- **Reset**
 - Supports power-on/power-down/external pin reset
 - Supports watchdog reset and software system reset
 - Programmable voltage detection
- **High-Speed Communication Interfaces**
 - 7 USART interfaces/6 UART interfaces, supporting ISO7816, IrDA, LIN
 - 2 LPUART interfaces
 - 6 SPI interfaces, supporting master/slave modes, rates up to 50 MHz
 - 8 I2C interfaces, speeds up to 3.4 MHz, configurable master/slave modes, dual address response in slave mode
 - 1 USBHS Dual Role interface with built-in high-speed PHY
 - 1 USBFS Dual Role interface
 - 8 CAN-FD bus interfaces
 - 2 Ethernet MAC interfaces: ETH1 supporting 10M/100M/1000M communication rates, ETH2 supporting 10M/100M rates, both supporting IEEE 1588 time synchronization protocol
 - 1 EtherCAT slave interface (ESC) with transmission rates up to 100Mbit/s, supporting 2 MII ports, 8 field bus memory management units (FMMU), 8 synchronization managers (SM), 64-bit distributed clock (DC)
- **High-Performance Analog Interfaces**
 - 3 12-bit 5Msps ADCs, supporting 12-bit, 10-bit resolution, hardware oversampling up to 16-bit, supporting up to 55 external single-ended input channels, 5 internal single-ended input channels, supporting both single-ended and differential modes
 - 4 high-speed analog comparators
 - 6 12-bit DACs: 2 1Msps DACs supporting output with or without buffer independently, internal output only supports mode without buffer; simultaneous internal and external output requires buffer enabled; 4 additional DACs supporting only one internal output channel with 15Msps sampling rate and without buffer
 - 2 MCO outputs, configurable to output SYSCLK, HSE, MSI, LSE, LSI, HSI64, or PLL clock division
 - 1 reference voltage output VREFBUF (configurable to 1.5V/1.8V/2.048V/2.5V)
 - 1 temperature sensor
- **Audio Interfaces**
 - 4 I2S interfaces, supporting master/slave modes, audio sampling frequency support from 8KHz to 192KHz
 - 8 PDM digital microphone interfaces built into the DSMU
- **Memory Expansion Interfaces**
 - 1 FEMC (Flexible External Memory Controller) interface, 100 MHz bus rate, configurable 16/32-bit data width for SRAM/PSRAM/Nor Flash, configurable 8/16-bit data width for NAND Flash

- 1 xSPI interface, supporting 1/2/4/8-bit data width, master/slave configurable, rates up to 133 MHz, usable for external SRAM, PSRAM and Flash, supporting XIP
- 1 SDRAM interface, rates up to 133 MHz
- 2 SDMMC interfaces, supporting SD/SDIO 3.0, eMMC 4.51 format, rates up to 104MHz
- **Image Processing Interfaces**
 - 2 digital camera interfaces (DVP), supporting 8/10/12/16bit, rates up to 110MHz
 - 1 TFT-LCD display interface, supporting up to 24-bit parallel digital RGB LCD, providing all signal interfaces for direct connection to various LCD and TFT panels, resolution up to 1920x1080
 - Built-in 2.5D graphics processor, supporting image scaling, rotation, mixing, anti-aliasing, texture mapping, etc.
 - Hardware JPEG encoder/decoder
- **Up to 126 GPIOs, low-speed GPIOs supporting 5V tolerance (under VDD = 3.3V±10% conditions)**
- **Motor Control Cordic Accelerator, supporting trigonometric and hyperbolic function acceleration, floating-point input and output**
- **Delta Sigma Module Unit (DSMU)**
- **Built-in filter algorithm accelerator FMAC, supporting FIR, IIR filtering**
- **3 high-speed DMA controllers, each supporting 8 channels, 1 MDMA supporting 16 channels, configurable source and destination addresses for all channels**
- **RTC real-time clock, supporting leap year perpetual calendar, alarm events, periodic wake-up, internal and external clock calibration**
- **Timer Counters**
 - 2 16-bit super high-precision timer counters (SHRTIM1/SHRTIM2), highest control precision 100ps, each with 1 master timer and 6 16-bit slave timer units. Each timer unit has 2 independent channels, supporting 12 independent PWM outputs or 6 pairs of complementary PWM outputs
 - 4 16-bit advanced timer counters, supporting input capture, complementary output, quadrature encoding input, etc., highest control precision 3.3ns; each timer has 6 independent channels, 4 of which support 4 pairs of complementary PWM outputs
 - 10 16-bit general-purpose timers (GTIM1-13), each with 4 independent channels, supporting input capture, output compare, PWM generation
 - 4 32-bit basic timer counters (BTIM1~4)
 - 5 16-bit low-power timers (LPTIM1~5), operable in Stop2 mode
 - 1x 24-bit SysTick, 1x 14-bit window watchdog (WWDG), 1x 12-bit independent watchdog (IWDG)
- **Programming Methods**
 - **Supporting SWD/JTAG for online debugging**
 - **Supporting USB, UART Bootloader**
- **Security Features**
 - Flash has up to 4 encryption partitions, supporting storage encryption
 - Write protection (WRP), multiple read protection (RDP) levels (L0/L1/L2)

- Built-in cryptographic algorithm hardware acceleration engine, supporting AES/TDES, SHA, SM4 algorithms
- TRNG (True Random Number Generator), CRC8/16/32 operations
- Secure boot, encrypted program download, secure update, detection of external high-speed and low-speed clock failures
- Anti-tamper detection
- **128-bit UCID supported in OTP**
- **Operating Conditions**
 - Operating voltage range: 2.3V~3.6V
 - Chip junction temperature range: -40°C~125°C
- **Certification**
 - USB IF
 - IEC61508 SIL2
- **Package**
 - UFBGA176+25(10mm x 10mm)
- **Ordering Model**

Series	Model
N32H765Ix7EC	N32H765IKB7EC, N32H765IIB7EC

1 Naming Convention



2 Product Model Resources Configuration

Table 2-1 N32H765Ix7EC Series Resource Configuration

Device Model		N32H765IKB7EC	N32H765IIB7EC
Flash (KB)		4096	2048
SRAM (KB)	TCM	1024	
	System RAM	480	
	Backup RAM	4	
Core	M7	600MHz	
Operating Voltage		2.3V~3.6V	
DCDC(step-down)		Yes	
Coproductors	Cordic	Yes	
	DSMU	Yes	
	FMAC	Yes	
Timers	SHRTIM	2	
	ADTIM	4	
	GPTIM	10	
	BSTIM	4	
	LPTIM	5	
	SysTick timer	1	
	WWDG	1*14bit	
	IWDG	1*12bit	
	RTC	Yes	
Communication Interfaces	SPI/I2S	6/4	
	I2C	8	
	USART	7	
	UART	6	
	LPUART	2	
	USBHS Dual Role	1	
	USBFS Dual Role	1	
	CAN FD	8	
	ESC	Yes	
	10/100M ETH	1	
	10/100/1000M ETH	1	
Expanded storage	SDRAM	Yes	
	xSPI	1	
	FEMC	Yes	
	SDMMC	2	
Analog	12bit ADC	3	
	12bit DAC Number of channels	2+4 ⁽¹⁾ 2 External channels	
	Comparator	4	

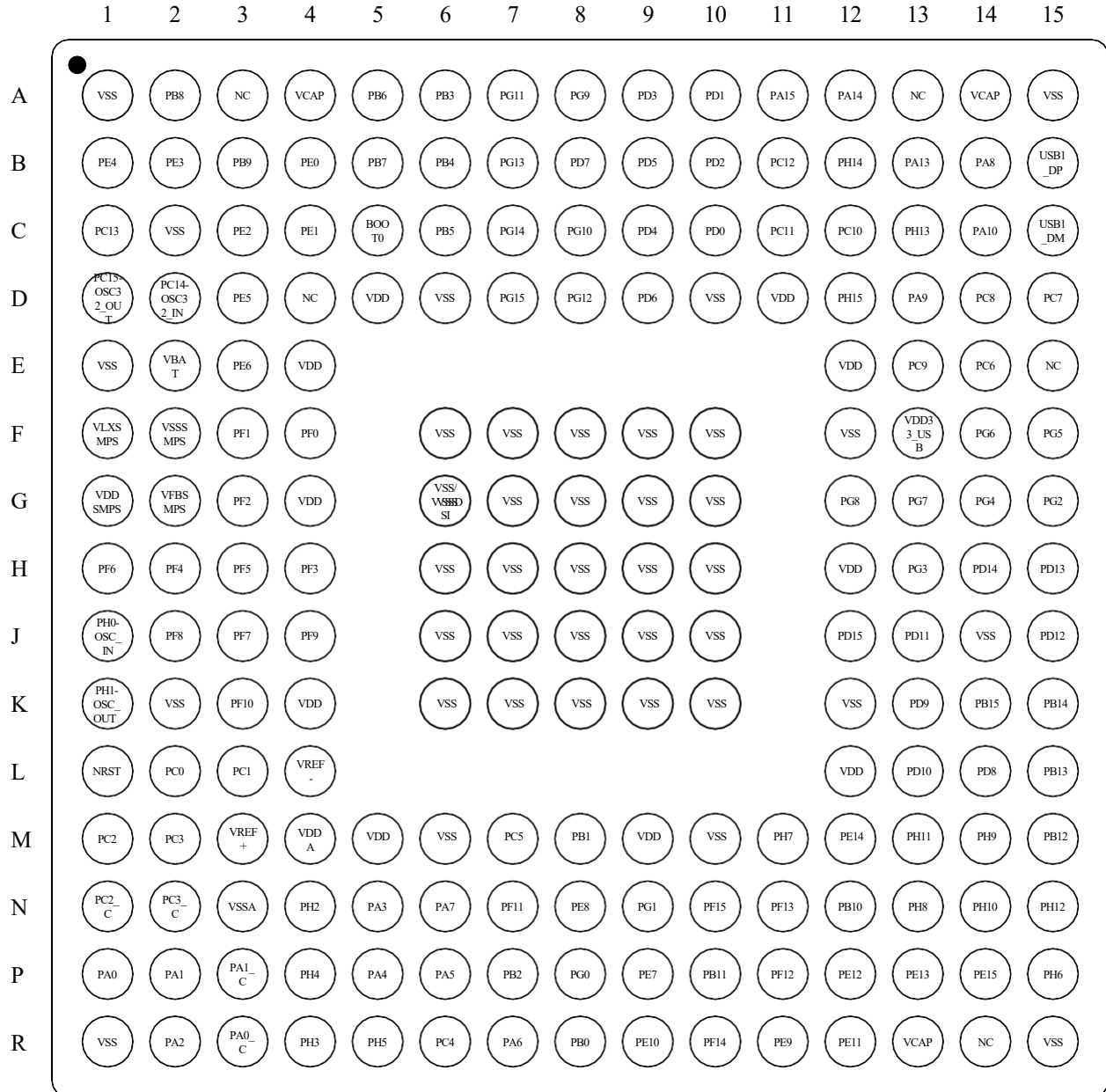
	VREFBUF	Yes
Imaging	LCDC	Yes
	GPU	Yes
	JPEG	Yes
	DVP	2
GPIO		126
DMA Number of channels		3 24Channel
MDMA Number of channels		1 16Channel
Algorithm Support		DES/3DES, AES, SHA1/SHA224/SHA256, CRC8/16/CRC32
Security Protection		Read WriteProtection (RDP/WRP) , storage encryption, secure boot
Package		UFBGA176+25

Note: 4 DACs only support internal connection and cannot output to GPIO

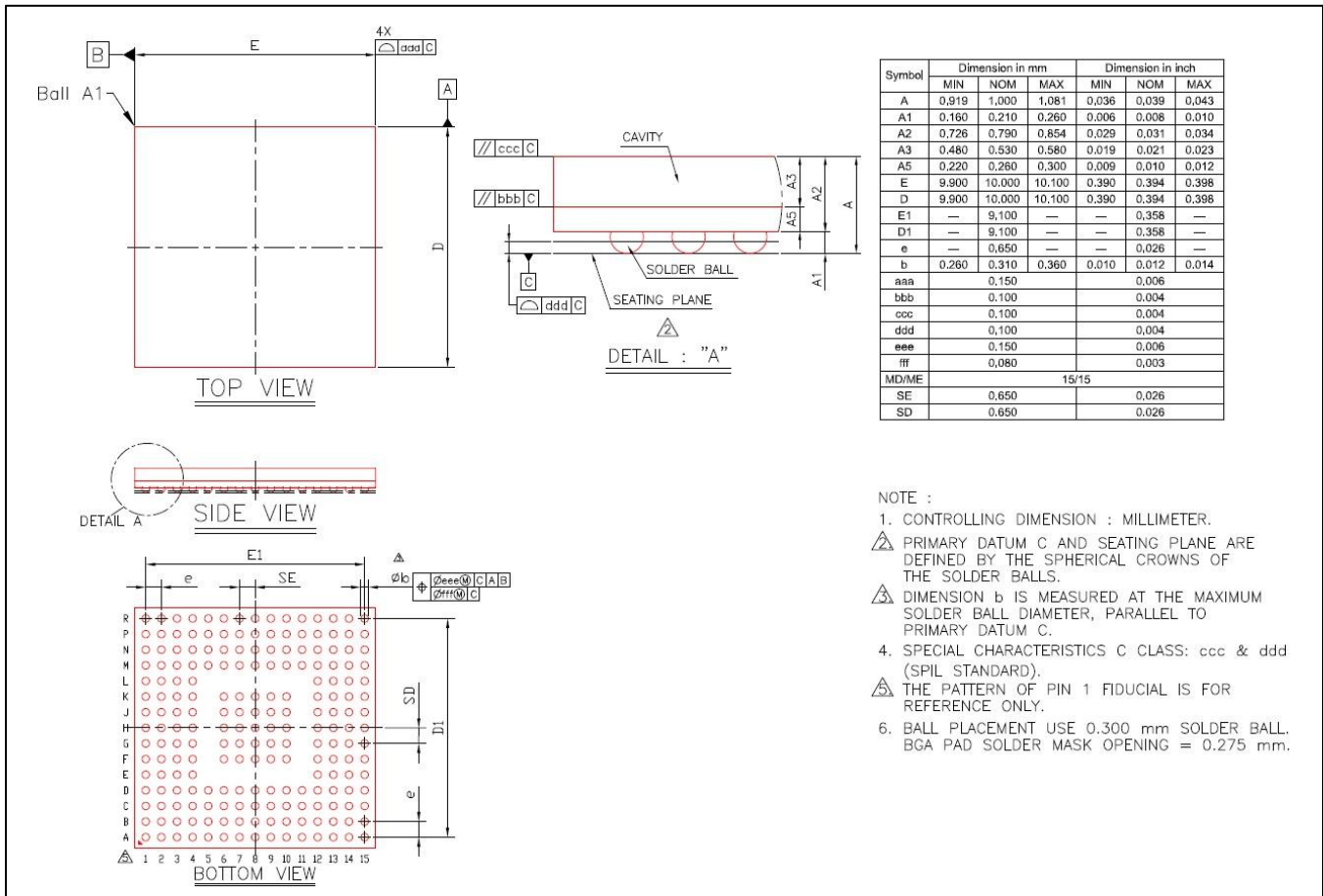
3 Package

3.1 UFBGA176+25 Package

3.1.1 UFBGA176+25 Pin Distribution



3.1.2 UFBGA176+25 Package Size



4 Version History

Version	Date	Changes
V0.0.1	2025.4.22	First release

5 Disclaimer

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