Design Guide

N32G05X Series Hardware Design Guide

Introduction

This document details the N32G05X series MCU hardware design checklist to provide users with hardware design guide.

NSING Technologies Pte. Ltd.
Add: NSING, Teletech Park #02-28, 20 Science Park Road,
Singapore 117674
Tel: +65 69268090
Email: sales@nsing.com.sg

CONTENS

NSING Technologies Pte. Ltd.
Add: NSING, Teletech Park #02-28, 20 Science Park Road,
Singapore 117674
Tel: +65 69268090
Email: sales@nsing.com.sg

1. N32G05X Series MCU Hardware Design Checklist

1.1 Introduction to Power Supply

The operating voltage (VDD) of the N32G05X series chips is 2.0V~5.5V. Mainly include: VDD/VDDA, VDD_LED pins. Please refer to the relevant data sheet for details.

1.2 VDD power supply scheme

VDD is the main power supply of the MCU and must be powered by a stable external power supply. The voltage range is 2.0V~5.5V. A 0.1uF decoupling capacitor and a 4.7uF decoupling capacitor need to be placed nearby the VDD pin. For the specific design of decoupling capacitors, please refer to the minimum system reference design schematic diagram of each package in Chapter 3.

VDD_LED is the power supply voltage of the LED module. It is recommended to place a 0.1uF decoupling capacitor and a 220uF decoupling capacitor nearby the VDD_LED pin. For the specific design of decoupling capacitors, please refer to the minimum system reference design schematic diagram of each package in Chapter 3.

When PB2 is multiplexed into the AVREFP[n1] function, it is recommended to connect an external 100nF+1uF capacitor. Please refer to the data sheet for detailed description.

1.3 RTC multiplexing pin

When the IO multiplexing is used as RTC TAMP function, this pin needs to be added with a pull-down resistor. The reference range of the pull-up/down resistor is 1K~10K.

1.4 External pin reset circuit

A system reset occurs when a low level appears on the NRST pin (external reset). The external NRST pin reset reference circuit is as follows.

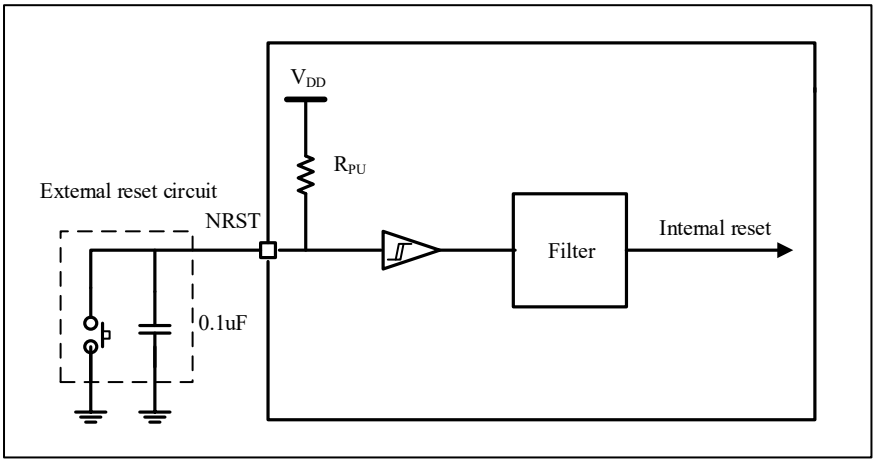

Figure 1-1 System reset diagram

Note: It is recommended that the reset pin NRST is not left floating during design. The external capacitor 0.1uF is

NSING Technologies Pte. Ltd.
Add: NSING, Teletech Park #02-28, 20 Science Park Road,
Singapore 117674
Tel: +65 69268090
Email: sales@nsing.com.sg

given as a typical reference value. If the reset time needs to be accelerated, the NRST pin can be externally pulled up. In addition, the user can decide whether to add a reset button according to the actual needs of the product.

1.5 External clock circuit

The N32G05X series MCU contains 1 external clock: external high-speed clock HSE (8MHz~16MHz).

HSE configures the corresponding load capacitance according to the characteristics of the crystal oscillator. For details, please refer to the description of the external clock characteristics in the relevant data sheet.

1.6 Boot Pin Connection

The figure below shows the external connections required when the N32G05X series chip selects boot memory. For information on startup mode, please refer to the relevant chapters of the user manual.

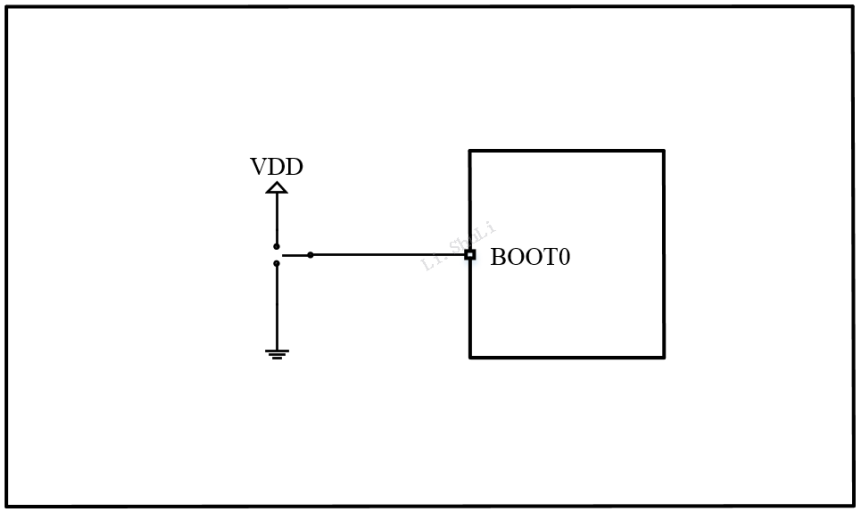

Figure 1-2 Implementation example of startup mode

In the default mode, the BOOT pin is pulled high, and the chip boots from the BOOT area after reset; the BOOT pin is pulled low, and the chip boots from the user area after reset.

1.7 Independent ADC Converter

Regarding ADC circuit design, please pay attention to the following points:

1） When using ADC sampling, it is recommended to shorten the external wiring distance of the ADC sampling channel;

2） It is recommended that the input signal surrounding the ADC be kept away from some high-frequency flip signals;

3） Note the maximum supported rate of the sampling channel:

When the ADC input clock of the N32G05X series is 24MHZ, the ADC sampling channel sampling rate does not exceed 1Msps;

Nations Technologies Inc.
Tel：+86-755-86309900
Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North.
Nanshan District, Shenzhen, 518057, P.R.China

4） During ADC conversion, the chip does not support modifying the ADC configuration. If you need to modify the configuration, you need to wait for the current conversion to end or turn off the ADC before configuring;

5） When using a certain ADC channel, you cannot apply a negative voltage (such as -0.2V) to other unused ADC sampling channels. If this negative voltage is applied, the voltage of the ADC channel for normal sampling will be pulled down, causing the read Data is inaccurate;

6） When using a certain ADC channel, do not apply high voltage (greater than the VDD voltage) to other unused ADC sampling channels. If this high voltage is applied, the voltage of the ADC channel for normal sampling will be pulled up, causing the read data to be incorrect. allow;

7） When using ADC, the maximum value of RAIN cannot be too large and needs to comply with the following formula:

$$R_{AIN} < \frac{T_S}{f_{ADC} \times C_{ADC} \times \ln(2^{N+2})} - R_{ADC}$$

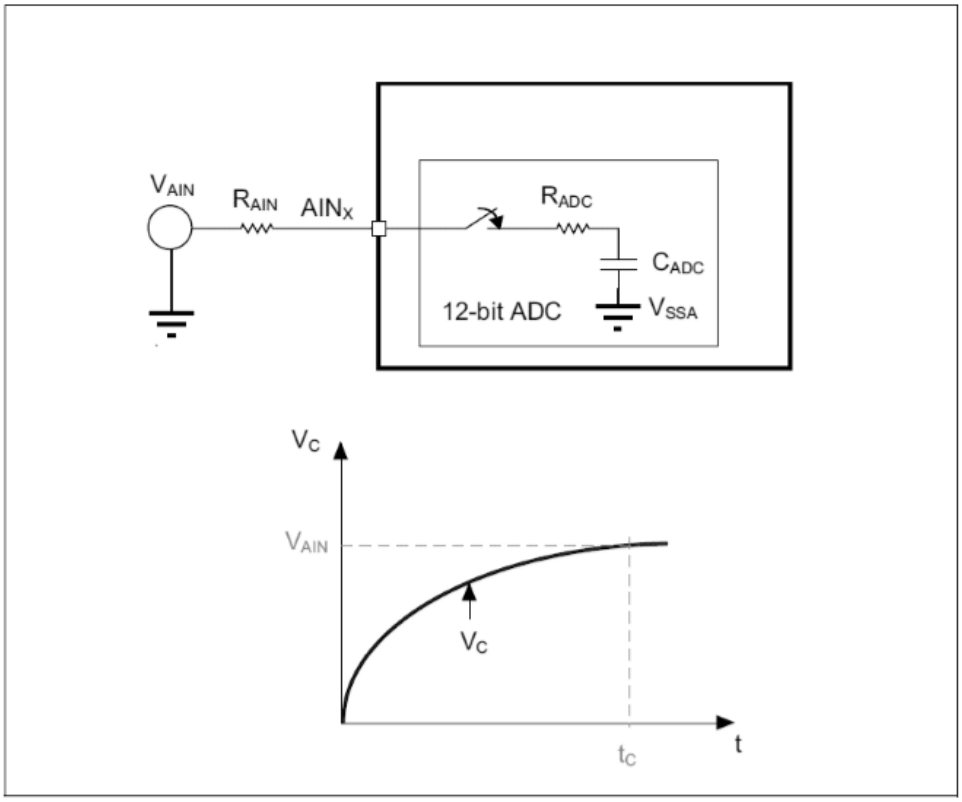

Figure 1-3 Influence of series resistance of ADC input port

Nations Technologies Inc.
Tel：+86-755-86309900
Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North.
Nanshan District, Shenzhen, 518057, P.R.China

ADC sampling schedule:

resolution	Rin（kΩ）	Minimum sampling time（ns）
12-bit	0.9	500
	1.2	583
	2.2	833
	3.8	1250
	8.1	2333
	10.8	3000
	18.7	5000
	28.9	7583
	38.5	10000
	61.6	15833

Figure 1-4 ADC sampling schedule

Note: The sampling time needs to be comprehensively configured based on the input clock and the optional sampling period of the ADC register. In principle, the ADC sampling period configuration should be greater than or equal to the minimum number of sampling periods in the table.

1.8 IO power-on pulse processing

During the power-on process, due to the high-impedance state of the IO and the coupling characteristics of the internal circuit, a high-level pulse will appear on the IO at the moment of power-on (please measure the actual high pulse voltage value by the user). If this pulse will affect its application, it is recommended to hang an appropriate capacitor (1nF~100nF) or add an appropriate pull-down resistor (10K~100K) on the corresponding IO.

The picture below shows the IO (PB12) waveform diagram during the power-on process of the development board N32G056RBQ7_STB_V1.0:

Nations Technologies Inc.
Tel：+86-755-86309900
Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North.
Nanshan District, Shenzhen, 518057, P.R.China

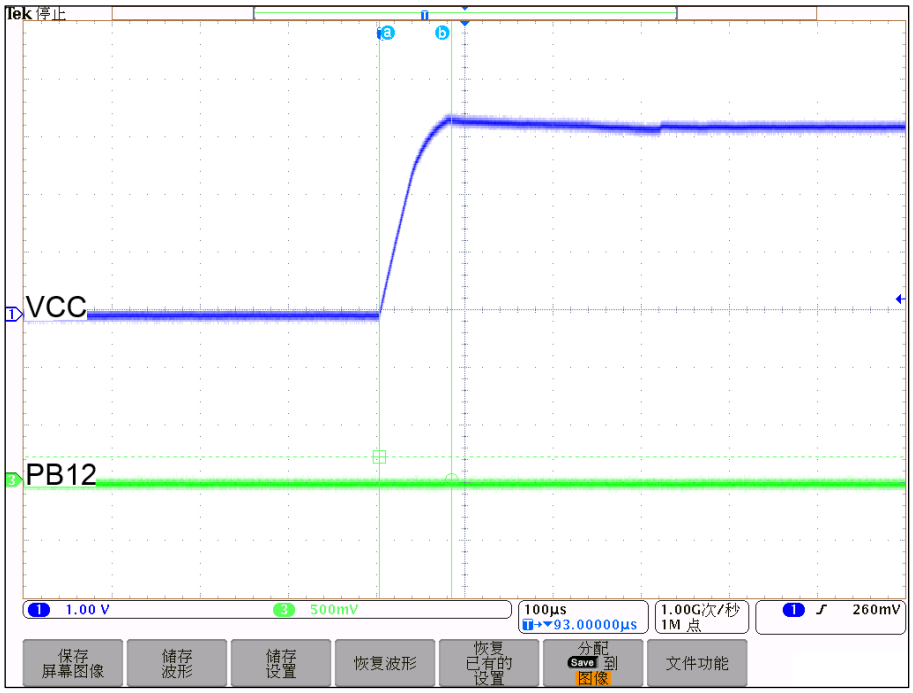

Figure 1-5 IO (PB12) waveform during power-on

The picture below shows the waveform of the development board N32G056RBQ7_STB_V1.0 after adding a 10K pull-down resistor to IO (PB12) during power-on:

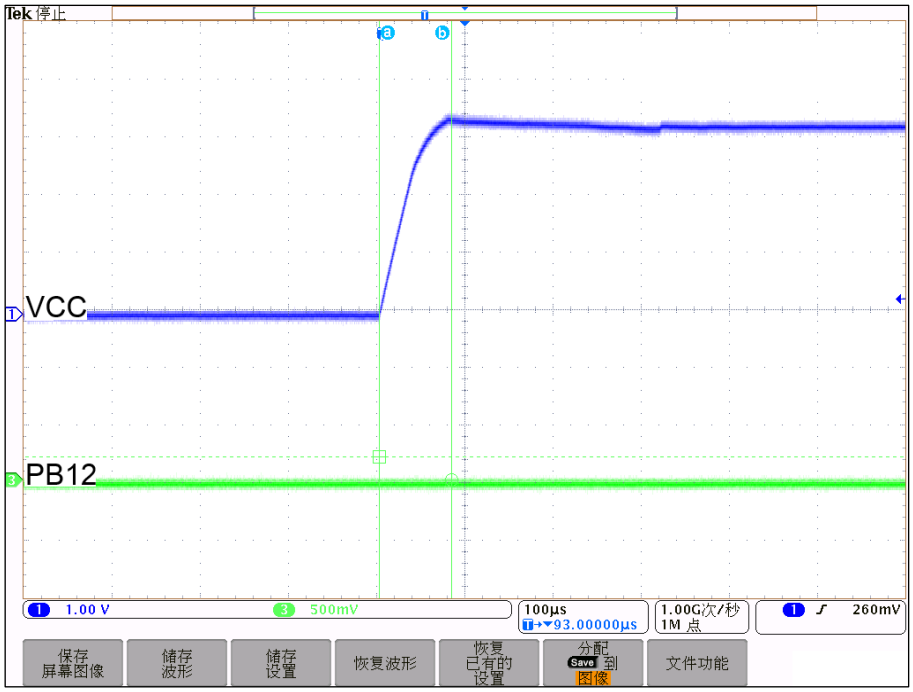

Figure 1-6 Waveform after IO (PB12) plus pull-down resistor during power-on process

1.9 IO withstand voltage

Please pay attention to the withstand voltage value of each IO when using the chip. In the I/O structure column defined by pin multiplexing in the data sheet, TC: 5V standard IO is marked. This type of IO communicates with

Nations Technologies Inc.
Tel：+86-755-86309900
Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North.
Nanshan District, Shenzhen, 518057, P.R.China

other external IOs in different voltage domains. , need to do level conversion.

Package		Pin name (function after reset)	Type(1)	IO(2)	Fail-safe(4)	Alternate functions(3)	
LQFP64	QFN64					Digital	Analog
1		PA7	I/O	TC	N	TIM1_CH1N TIM1_CH2N SPI3_NSS SPI3_MISO UART2_RX EVENTOUT	ADC_IN7 COMP2_OUT
2		PB0	I/O	TC	N	LCD_SEG0 TIM2_CH1 EVENTOUT	ADC_IN8 COMP1_INM
3		PB1	I/O	TC	N	LCD_SEG1	ADC_IN9 COMP1_INP

Figure 1-7 I/O structure defined by datasheet pin multiplexing

Note: TC: 5V standard IO; when using the chip, you need to pay attention to the withstand voltage value of the IO

1.10 Anti-static design

1.10.1 PCB Design

For the PCB design of ordinary two-layer boards, it is recommended to do wrapping around the signal lines, and try to cover the edges of the PCB as much as possible. If the cost allows, it can be designed with a four-layer board or a multi-layer board. In a multi-layer PCB, the ground plane acts as an important charge source, which can offset the charge on the electrostatic discharge source, which is conducive to reducing the electrostatic field band. The ground plane of the PCB can also be used as a shield for the signal line (of course, the larger the opening of the ground plane, the lower the shielding effectiveness). In addition, if a discharge occurs, since the ground plane of the PCB board is large, the charge is easily injected into the ground plane, rather than into the signal line. This will help protect the component, because the charge can be drained before causing component damage.

1.10.2 ESD Protection Devices

In the actual product design, the chip itself has a certain anti-static ability. The static level of N32G05X series MCU ESD (HBM) mode is +/-4KV, but if there is a higher ESD protection level requirement, and the pins of the chip need Direct external connection is used as the output or input port of the product. At this time, the pins of the chip are directly exposed to the outermost part of the product, and cannot be isolated by laying the ground or other means. Under this condition, it is generally necessary to consider an external ESD protection device. TVS diode is a typical ESD protection device. The following is an example of a typical connection method.

Nations Technologies Inc.
Tel：+86-755-86309900
Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North.
Nanshan District, Shenzhen, 518057, P.R.China

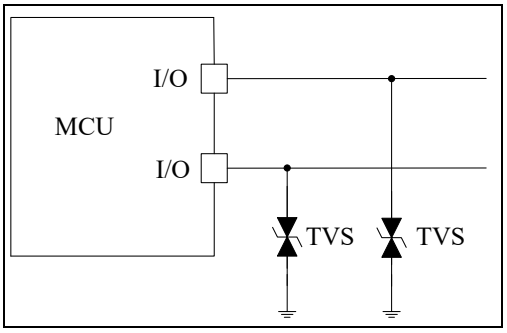

Figure 1-8 TVS connection on I/O pins

1.11 Debug Interface

N32G05X series chips support serial SWD debugging interface. Please refer to the relevant user manual for detailed applications..

Debug Signal	GPIO Pins
JTMS/SWDIO	PA13
JTCK/SWCLK	PA14

Table 1-1 Debug Interface

1.12 BOOT serial interface

N32G05X series chips support BOOT serial port communication. The serial port interface is as follows:

BOOT Serial Port	GPIO Pins
USART1_TX	PA9
USART1_RX	PA10

Table 1-2 Serial port interface

Note: The default serial port interface is PA9, PA10; it can be changed through the option byte, please see the user manual for details.

Nations Technologies Inc.
Tel：+86-755-86309900
Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North.
Nanshan District, Shenzhen, 518057, P.R.China

2. Overall Design Suggestions

1） Printed circuit board

It is recommended to use a multi-layer printed circuit board with a dedicated independent ground plane (VSS) and a dedicated independent power supply plane (VDD), which can provide good coupling performance and shielding effect. In practical applications, if a multi-layer printed circuit board cannot be used considering the economical reason, a good grounding and power supply structure must be ensured when designing the circuit.

2） Component layout

In PCB design, different circuits need to be laid out separately according to the different effects of each device on EMI. For example, high-current circuits, low-voltage circuits, and high-frequency devices. Thereby reducing cross-coupling on the PCB.

3） ground and Power (VSS, VDD)

Each module (analog circuit, digital circuit, low-sensitivity circuit) should be grounded separately, the digital ground and the analog ground should be separated, and all the grounds should be connected together at one point eventually. According to the size of the printed circuit board current, try to increase the width of the power line to reduce the loop resistance. At the same time, the direction of the power wire and the ground wire and the direction of the current should be as consistent as possible, and the power supply should be as close to the ground wire as possible to reduce the area of the loop. This helps to enhance noise immunity. The area on the PCB without devices needs to be filled with ground to provide good shielding effect.

4） Decoupling

All power pins need to be properly connected to power. These connections, including pads, wires, and vias, should have as low impedance as possible. The method of increasing the wiring width is usually adopted, and decoupling capacitors must be placed close to the chip for each pair of VDD and VSS pins. The figure below shows a typical layout of the power/ground pins.

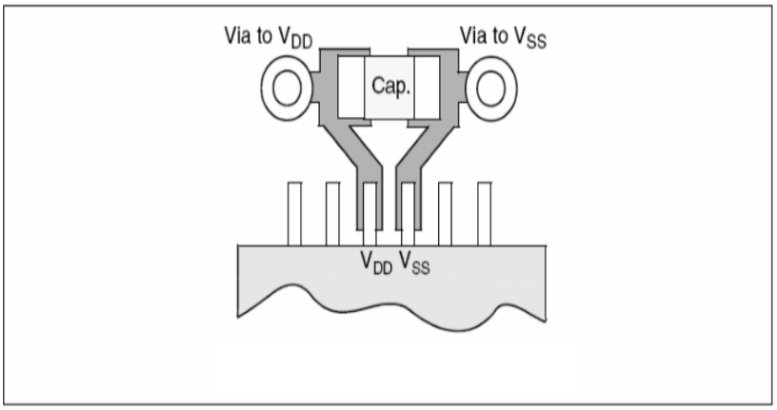

Figure 2-1 Typical layout of VDD/VSS pins

Nations Technologies Inc.
Tel：+86-755-86309900
Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North.
Nanshan District, Shenzhen, 518057, P.R.China

3. Minimum System Reference Design Schematic

3.1 QFN64 (with LED)

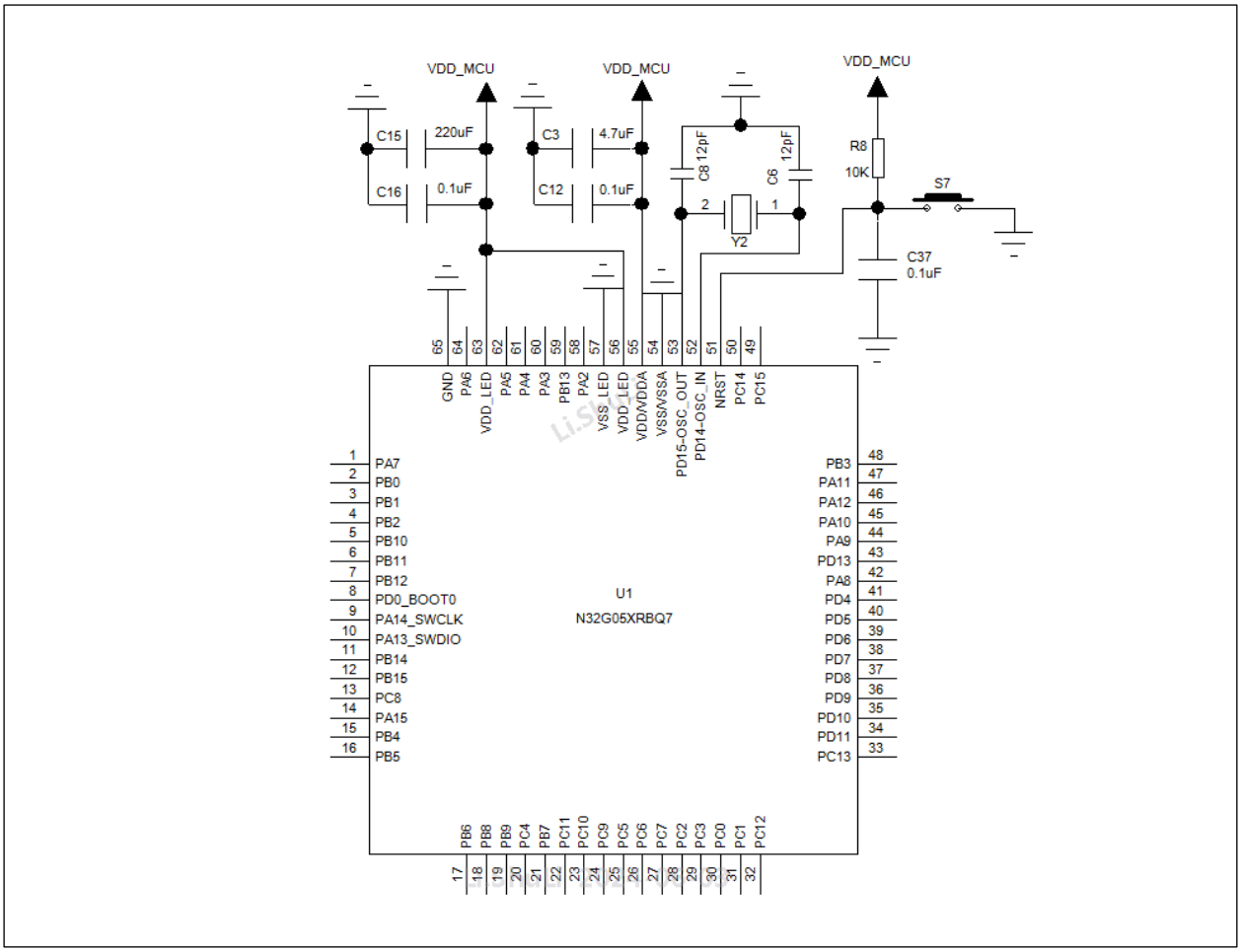

Figure 3-1 QFN64 package minimum system reference design schematic diagram

Nations Technologies Inc.
Tel：+86-755-86309900
Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North.
Nanshan District, Shenzhen, 518057, P.R.China

3.2 LQFP64 (with LED)

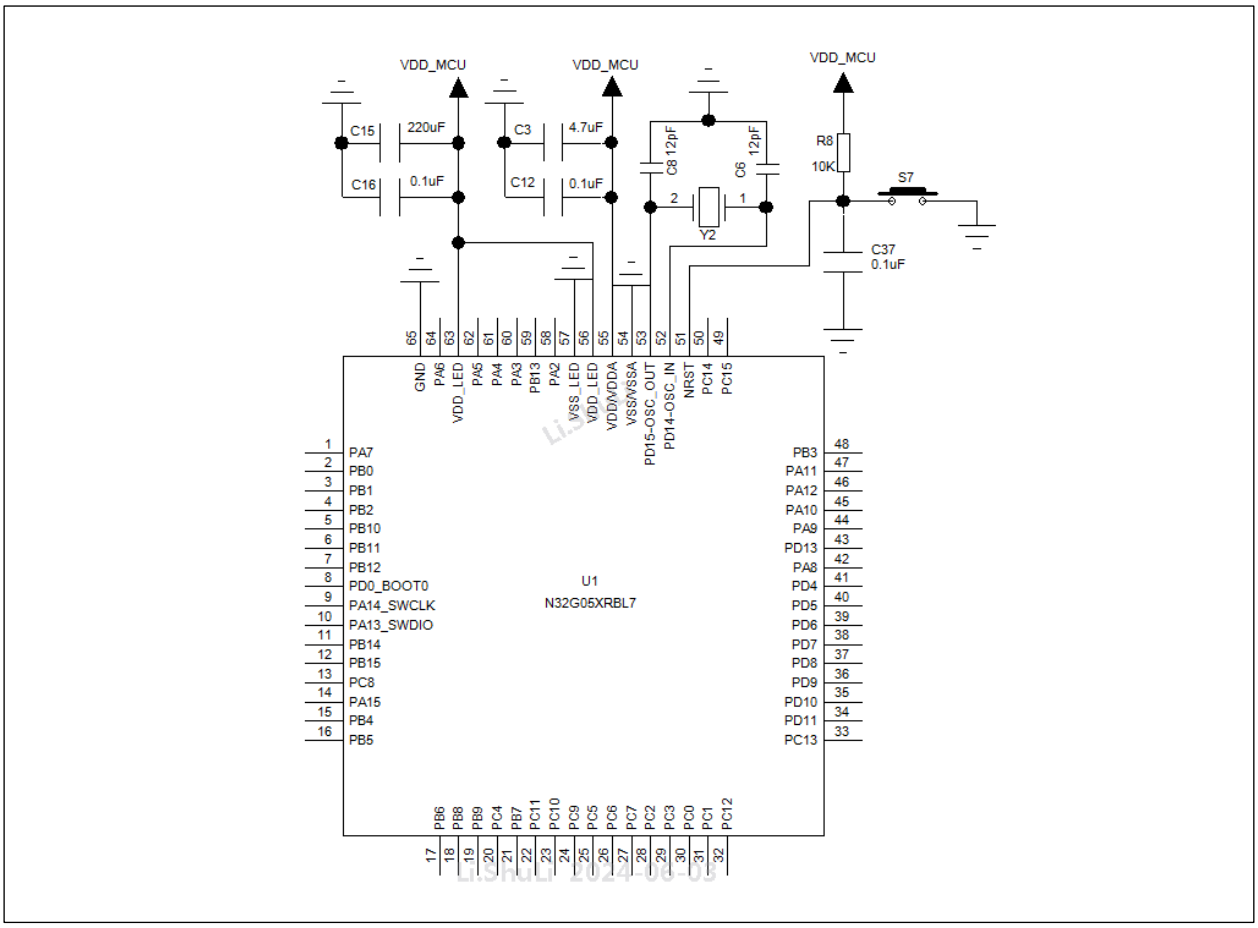

Figure 3-2 LQFP64 Package Minimum System Reference Design Schematic

Nations Technologies Inc.
Tel：+86-755-86309900
Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North.
Nanshan District, Shenzhen, 518057, P.R.China

3.3 LQFP64 (without LED)

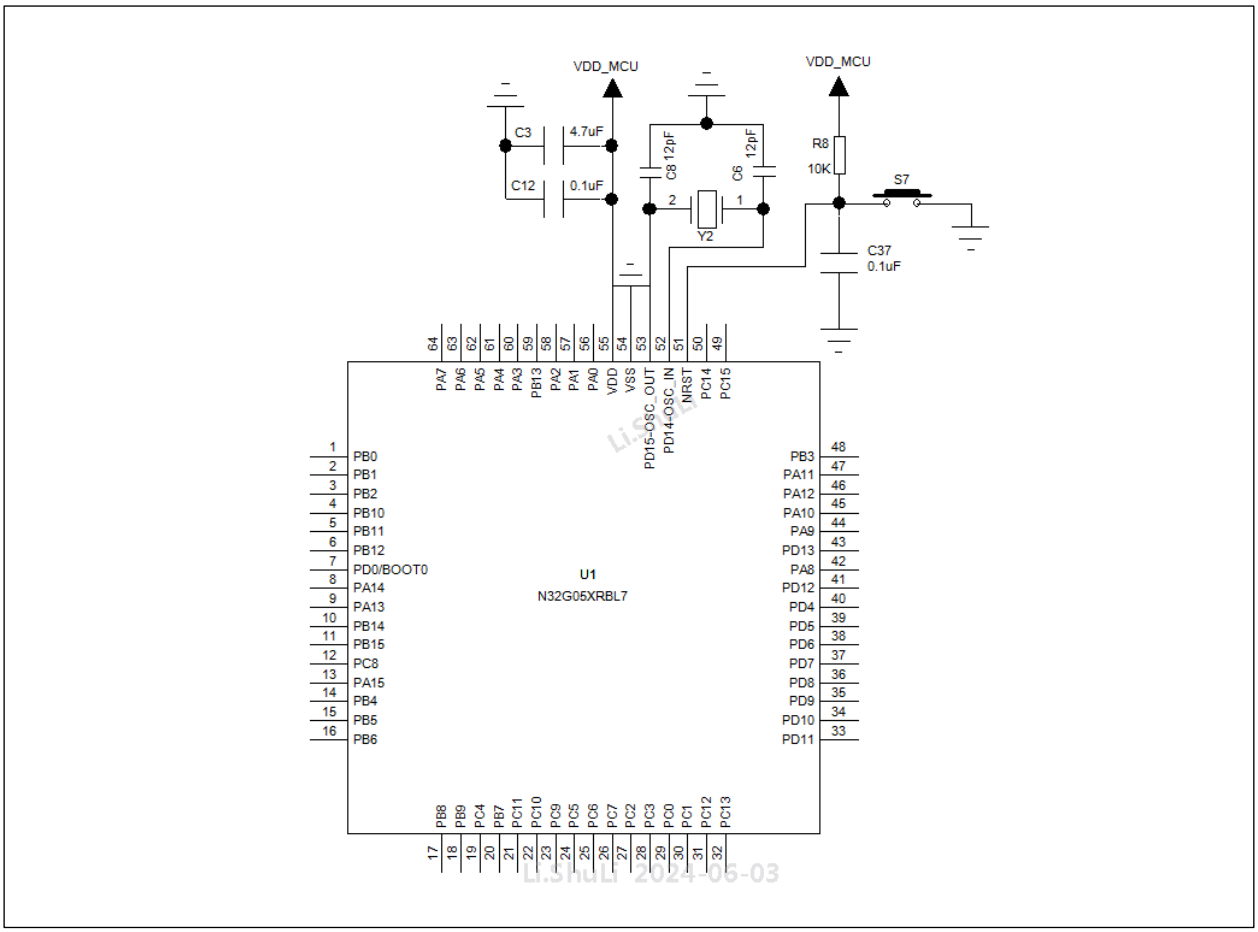

Figure 3-3 LQFP64 Package Minimum System Reference Design Schematic

Figure 3-1~Figure 3-3 is the minimum system reference design schematic diagram of each package of the N32G05X series, which mainly reflects the design of power supply decoupling capacitor, clock, reset circuit, etc.

Clock circuitry and battery backup depend on user design;

The chip supports internal high-speed and low-speed clocks for user selection.

Nations Technologies Inc.
Tel：+86-755-86309900
Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North.
Nanshan District, Shenzhen, 518057, P.R.China

4. PCB LAYOUT Reference

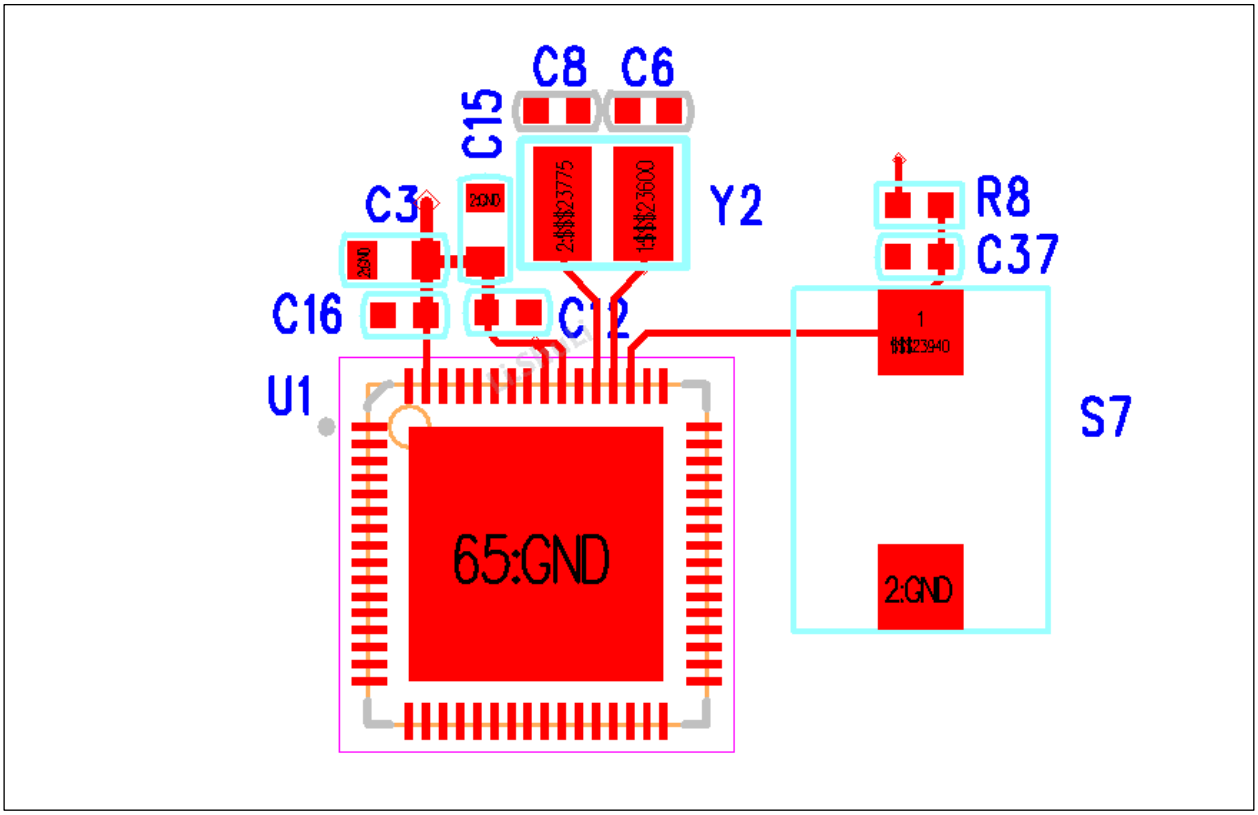

Figure 4-1 QFN64 Package PCB LAYOUT reference diagram

Note:

1、When designing PCB LAYOUT, each power pin needs to be placed with a decoupling capacitor nearby;

2、The external crystal and wiring of HSE should be covered with ground as much as possible. The area under the crystal near the crystal also needs to be paved. No signal lines can pass through to prevent the signal lines from interfering with the crystal signal;

3、When HSE is used as a crystal oscillator, the traces should not be too long to avoid antenna effects.

Nations Technologies Inc.
Tel：+86-755-86309900
Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North.
Nanshan District, Shenzhen, 518057, P.R.China

5. Version history

Version	Date	Changes
V1.0	2024-05-10	Create documentation

Nations Technologies Inc.
Tel：+86-755-86309900
Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North.
Nanshan District, Shenzhen, 518057, P.R.China

6. Disclaimer

This document is the exclusive property of NSING TECHNOLOGIES PTE. LTD. (Hereinafter referred to as NSING). This document, and the product of NSING described herein (Hereinafter referred to as the Product) are owned by NSING under the laws and treaties of Republic of Singapore and other applicable jurisdictions worldwide. The intellectual properties of the product belong to Nations Technologies Inc. and Nations Technologies Inc. does not grant any third party any license under its patents, copyrights, trademarks, or other intellectual property rights. Names and brands of third party may be mentioned or referred thereto (if any) for identification purposes only.

NSING reserves the right to make changes, corrections. enhancements, modifications, and improvements to this document at any time without notice. Please contact NSING and obtain the latest version of this document before placing orders. Although NATIONS has attempted to provide accurate and reliable information, NATIONS assumes no responsibility for the accuracy and reliability of this document. It is the responsibility of the user of this document to properly design, program, and test the functionality and safety of any application made of this information and any resulting product. In no event shall NATIONS be liable for any direct, indirect, incidental, special, exemplary, or consequential damages arising in any way out of the use of this document or the Product.

NATIONS Products are neither intended nor warranted for usage in systems or equipment, any malfunction or failure of which may cause loss of human life, bodily injury or severe property damage. Such applications are deemed, Insecure Usage'. Insecure usage includes, but is not limited to: equipment for surgical implementation, atomic energy control instruments, airplane or spaceship instruments, all types of safety devices, and other applications intended to supporter sustain life. All Insecure Usage shall be made at user's risk. User shall indemnify NATIONS and hold NATIONS harmless from and against all claims, costs, damages, and other liabilities, arising from or related to any customer's Insecure Usage Any express or implied warranty with regard to this document or the Product, including, but not limited to. The warranties of merchantability, fitness for a particular purpose and non-infringement are disclaimed to the fullest extent permitted by law. Unless otherwise explicitly permitted by NATIONS, anyone may not use, duplicate, modify, transcribe or otherwise distribute this document for any purposes, in whole or in part.

Nations Technologies Inc.
Tel：+86-755-86309900
Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North.
Nanshan District, Shenzhen, 518057, P.R.China