N32G030 x6/x8 Datasheet

The N32G030 series adopts a 32-bit Cortex®-M0 core, operating frequency up to 48MHz. The devices integrates up to 64KB embedded flash, 8KB SRAM, multiple communication bus interfaces like U(S)ART, I2C, SPI, and analog interfaces such as 1x12-bit 1Msps ADC, 1xOPAMP, 1xCOMP

Key Features

- **CPU Core**
  - A 32-bit general-purpose microcontroller based on the Arm® Cortex®-M0 core, Single-cycle hardware multiply instruction
  - Maximum frequency up to 48MHz
- **Memories**
  - Up to 64KByte on-chip Flash memory, supports encrypted storage function, supports hardware ECC check, 100,000 erase/write cycles, 10 years of data retention
  - Up to 8Kbyte on-chip SRAM , supports hardware parity
- **Low Power Management**
  - Stop mode: RTC Run, maximum 8KByte SRAM retention, CPU register retention, all IO retention
  - Power Down mode: supports wakeup from 3 IOs
- **Clock**
  - HSE: 4MHz~20MHz external high-speed crystal oscillator
  - LSE: 32.768KHz external low-speed crystal oscillator
  - HSI: Internal high-speed RC OSC 8MHz
  - LSI: Internal low-speed RC OSC 30KHz
  - Built-in high-speed PLL
  - MCO: Supports 2-channels clock output, configurable as system clock, HSI, HSE, LSI, LSE, and PLL clock output that can be divided.
- **Reset**
  - Supports power-on/power-down/external pin reset
  - Supports watchdog reset
- **Communication Interfaces**
  - 3x U(S)ART, with a maximum rate up to 3 Mbps
    - 2x USART interfaces (supports 1xISO7816, 1xIrDA, LIN)
    - 1x LPUART interface (supports low power mode, the maximum rate up to 9600bps in this mode, can wake up chip from STOP mode)
  - 2x SPI interfaces with speed up to 18 MHz, one supports multiplexing with I2S
  - 2x I2C interface with speed up to 1 MHz, which can be configured in master/slave mode and support dual address response in slave mode
- **Analog Interfaces**
  - 1x 12bit 1Msps ADC , up to 12 external single-ended input channels
  - 1x OPAMP, operational amplifier with built-in up to 32 times programmable gain amplifier(PGA)

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- 1x COMP, built-in 64-level adjustable comparison reference

- **GPIO**
  - Up to 40 GPIOs
  - Support multiplexed functions
- **DMA Controller**
  - 1x high-speed DMA controller
  - Each controller supports 5 channels
  - Channel source address and destination address can be configured arbitrarily
- **RTC Real-time Clock**
  - Supports leap year perpetual calendar, alarm event, periodic wake up
  - Supports internal and external clock calibration
- **Beeper**
  - 1x Beeper, support complementary output, 16mA output drive capacity
- **Timers and Counters**
  - 2x16-bit advanced timers
    - Supports input capture, complementary output, orthogonal encoding input
    - Each timer has 4 independent channels. 3 of which supports 6 pairs complementary PWM outputs
  - 1x16-bit general purpose timers,
    - Supports input capture/output compare/PWM output
    - Each timer has 4 independent channels
  - 1x 16-bit basic timer counters
  - 1x 16-bit low power timer counter
  - 1x 24-bit SysTick timer
  - 1x 7-bit Window Watchdog (WWDG)
  - 1x 12-bit Independent Watchdog (IWDG)
- **Programming Methods**
  - Supports SWD online debugging interface
  - Supports UART Bootloader
- **Hardware Divider (HDIV) aAnd Square Root(SQRT)**
- **Security Features**
  - Flash storage encryption
  - CRC16/32 computation
  - Supports write protection(WRP), multiple read protection(RDP) levels (L0/L1/L2)
  - Supports external clock failure detection, tamper detection
- **96-bit UID and 128-bit UCID**
- **Operating Conditions**
  - Operating voltage range: 1.8V~5.5V
  - Operating temperature range: -40℃~105℃

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- ESD: ±4KV (HBM model), ±1KV (CDM model)

- **Packages**
  - UFQFPN20(3mm x 3mm)
  - TSSOP20(6.5mm x 4.4mm)
  - QFN32(4mm x 4mm)
  - QFN32(5mm x 5mm)
  - LQFP32(7mm x 7mm)
  - LQFP48(7mm x 7mm)
  - TQFP48(7mm x 7mm)

- **Ordering Information**

Reference	Part Number
N32G030x6 N32G030x8	N32G030F6U7, N32G030F6S7 N32G030K6L7, N32G030K6Q7, N32G030K6Q7-1 N32G030K8L7, N32G030C8L7, N32G030C8T7, N32G030F8S7

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1 Introduction

The N32G030 series microcontrollers features a 32bit ARM Cortex®-M0 core. It supports maximum frequency of 48MHz, integrated up to 64KB of on-chip encrypted storage memory Flash, 8KB of embedded SRAM.

The device is equipped with internal high speed AHB bus, along with two low speed peripherals clock bus APB and bus matrix. It supports up to 40 reusable alternate I/Os and features a diverse range of high performance analog interfaces. These include a12-bit 1Msps ADC, with up to 12 external input channels, a independent operational amplifier, and a high-speed comparator.

At the same time, the N32G030 provides a variety of digital communication interfaces, including 3x U(S)ART, 2x I2C, 2xSPI, 1xI2S communication interfaces.

The N32G030 series operates reliably in the temperature range of -40°C to +105°C and supply voltage from 1.8V to 5.5V. It offers multiple power modes to cater to low-power applications. Available in different package ranging from 20 pins to 48 pins, the peripheral configuration varies based on the package type.

The N32G030 series microcontrollers are suitable for various application scenarios such as mobile devices, home appliance applications, motor control, balance vehicles, power management systems, etc

Figure 1-1 shows the bus block diagram of this series of products.

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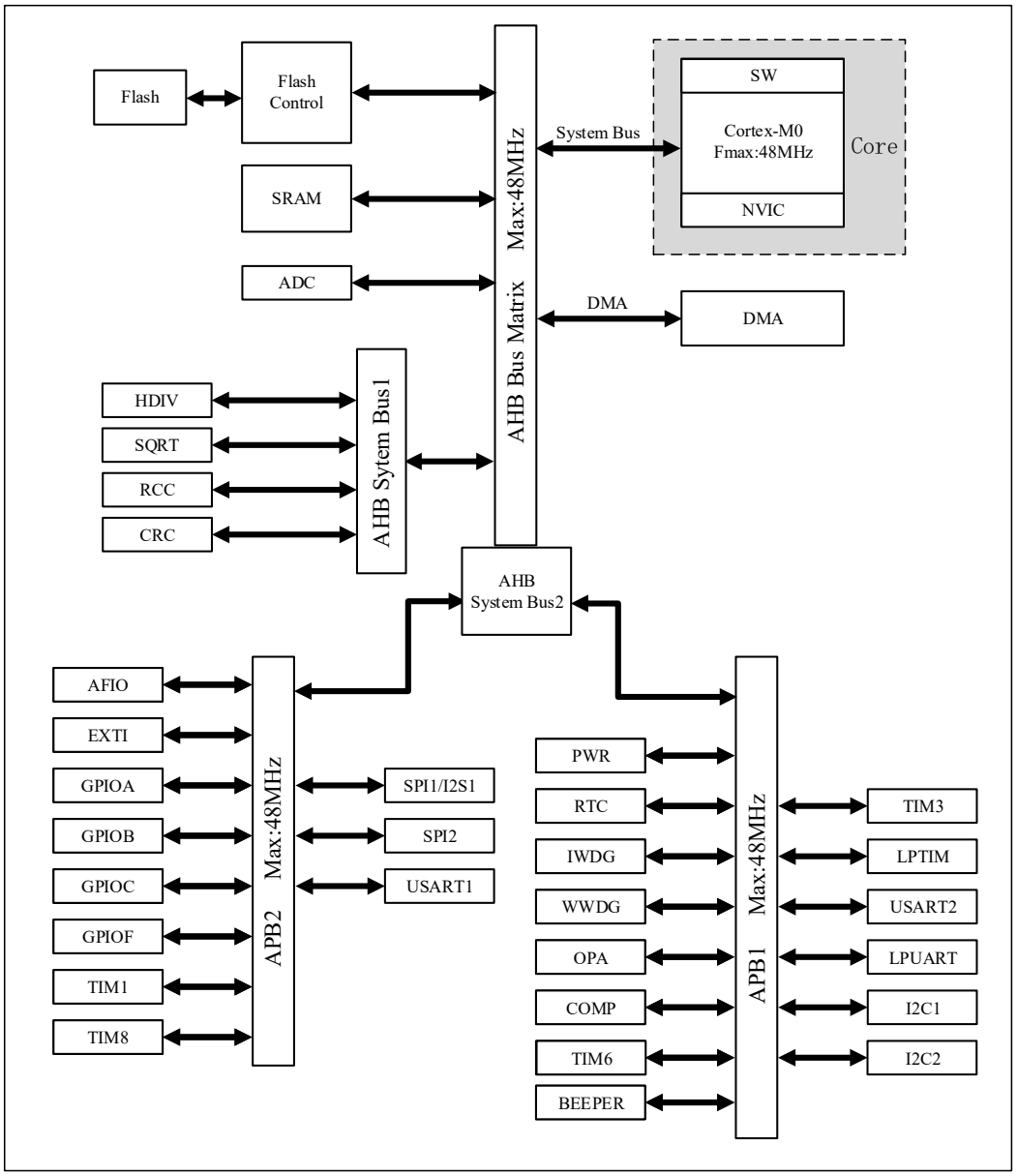
Figure 1-1 N32G030 Series Block Diagram



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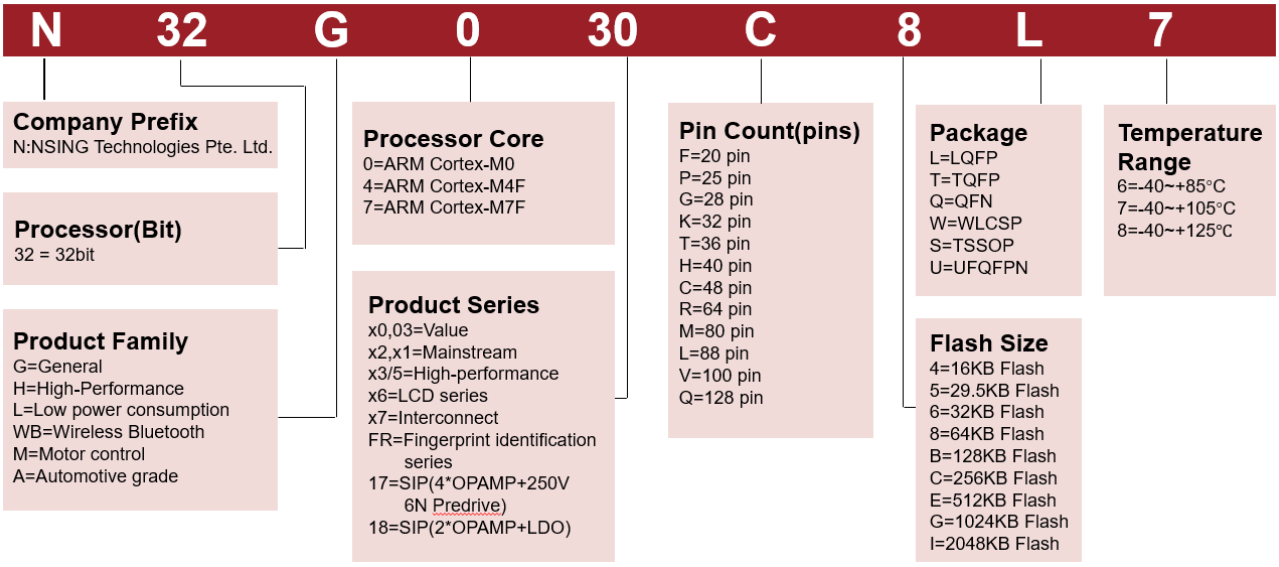
1.1 Naming Convention

Figure 1-2 N32G030 Series Part Number Information



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1.2 Product Configurations

Table 1-1 N32G030 Series Product Configuration

Device		N32G030F6U7	N32G030F6S7	N32G030K6Q7	N32G030K6Q71	N32G030K6L7	N32G030K8L7	N32G030C8L7	N32G030C8T7	N32G030F8S7
Flash Capacity (KB)		32	32	32	32	32	64	64	64	64
SRAM Capacity (KB)		8	8	8	8	8	8	8	8	8
CPU Frequency		ARM Cortex-M0 @48MHz								
Operating Environment		1.8~5.5V/-40~105℃								
Timer	General	1								
	Advanced	2								
	Basic	1								
	LPTIM	1								
	RTC	1								
Communication Interface	SPI	2								
	I2S	1								
	I2C	2								
	USART	2								
	LPUART	1								
GPIO		16		28		26		40		16
DMA Number of Channels		5								
12bit ADC Number of channels		1x12bit 7Channel	1x12bit 9Channel	1x12bit 10Channel				1x12bit 12Channel		1x12bit 9Channel
OPA/COMP		1/1								
Beeper		1								
Algorithm Support		CRC16/CRC32								
Security Protection		Read and Write Protection (RDP/WRP), Storage Encryption								

Note: (1) QFN32(5mm x 5mm)

(2) QFN32(4mm x 4mm)

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2 Functional Overview

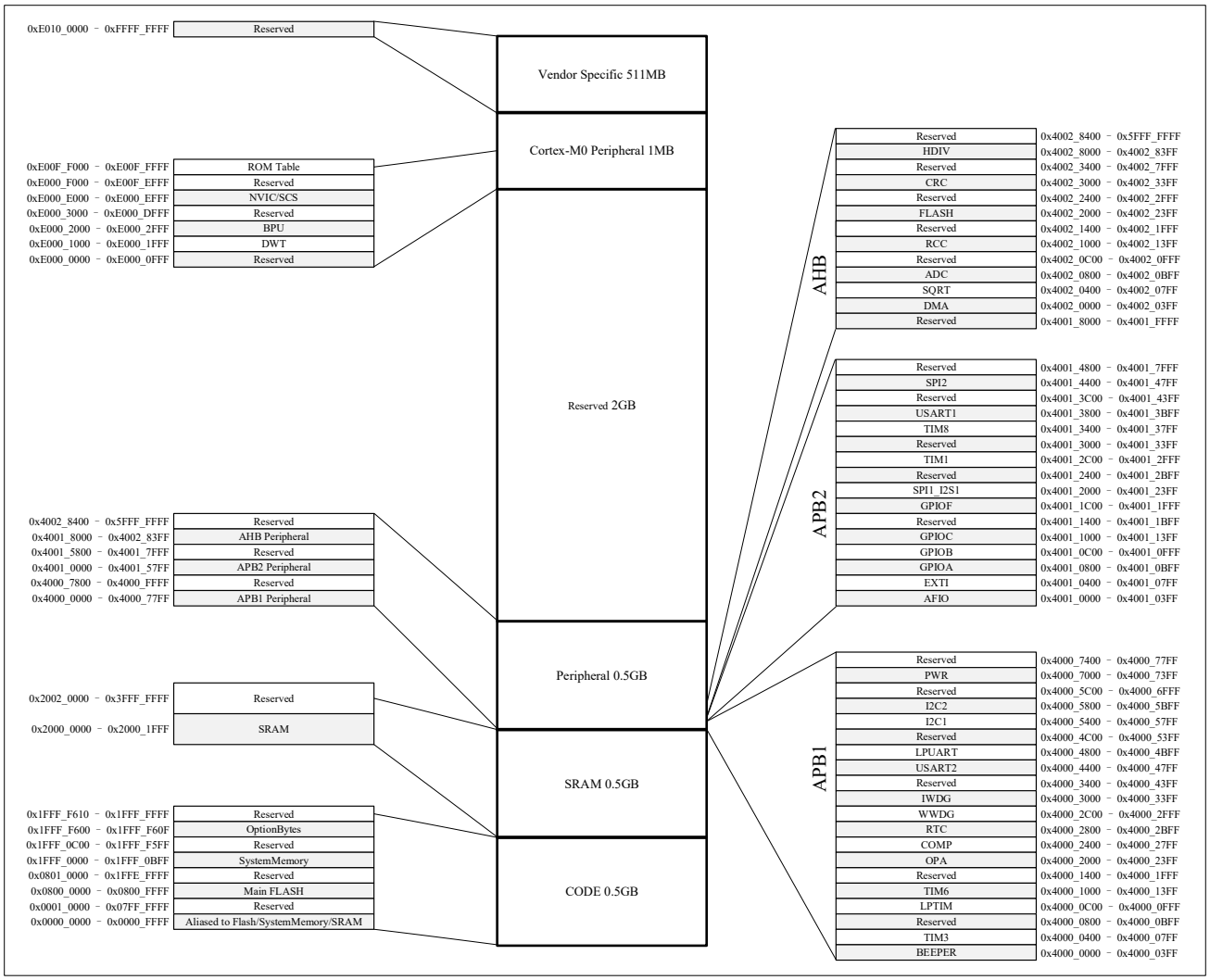
2.1 Processor Core

The N32G030 series integrates the latest generation of embedded ARM Cortex®-M0 processor

2.2 Memories

The N32G030 series include embedded encrypted Flash memory and embedded SRAM.

Figure 2-1 Memory Map



2.2.1 Embedded FLASH Memory

The integrated encrypted Flash memory ranges from 32K to 64K bytes, utilized for storing programs and data. The page size is 512 bytes, supporting page erasing, word writing, word reading, half word reading and byte reading operations.

It supports storage encryption protection, enabling automatic encryption during writing and decryption during reading (including program execution operation).

2.2.2 Embedded SRAM

The chip integrates a built-in SRAM of up to 8K bytes. SRAM can retain data in STOP mode.

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2.2.3 Nested Vectored Interrupt Controller (NVIC)

The built-in Nested Vectored Interrupt Controller (NVIC) is tightly connected to the interfaces of the core, which can realize low-latency interrupt handling and efficiently processing of late-arriving interrupts. The Nested Vectored Interrupt Controller manages interrupts including core exceptions.

- 32 maskable interrupt channels (excluding the16 interrupt lines of the Cortex®-M0)
- 4 programmable priority levels (using 2-bit interrupt priority levels)
- Low-latency exception and interrupt handling
- Power management control
- Realization of system control register

The module provides flexible interrupt management functions with minimal interrupt delay

2.3 Externed Interrupt/Event Controller (EXTI)

The externed interrupt/event controller contains 24 edge detectors used for generating interrupt/event requests. Each interrupt line can be independently configured with its trigger event (rising edge, falling edge or both) and can be individually masked. A pending register maintains the state of all interrupt requests. Interrupt requests can be cleared by writing '1' to the corresponding bit in the pending register.

2.4 Clock System

The device provides a variety of clocks for users to choose from, including high-speed internal RC HSI (8MHz), low-speed internal LSI (30KHz), high-speed external crystal oscillator HSE (4MHz~20MHz), low-speed external crystal oscillator LSE (32.768khz),PLL.

The system clock (SYSCLK) can choose the following clock sources:

- HSI
- HSE
- PLL
- LSI
- LSE

Secondary clock source:

- 30KHz low-speed internal RC oscillator, which can be used as the clock source of IWDG, RTC, LPTIM and LPUART. Used to automatically wake up the system from STOP mode.
- 32.768 KHz low-speed oscillator with external crystal can also be used as the clock source of RTC, LPTIM and LPUART.
- When not in use, any clock source can be independently shut down to reduce system power consumption.

Upon reset, the HSI clock is set as the default CPU clock, user can choose the HSE clock with failure monitoring function. When HSE clock failure is detected, it will be isolated, the system will automatically switch to HSI, and if interrupts are enabled, software can receive the corresponding interrupts. Similarly the system will automatically switch to MSI when the PLL clock was adopted and external oscillator fails.

Multiple prescaler are used to configure the frequency of AHB, APB (APB1 and APB2) regions. AHB has a maximum frequency of 48MHz, APB2 has a maximum frequency of 48MHz and APB1 has a maximum frequency of 48MHz.

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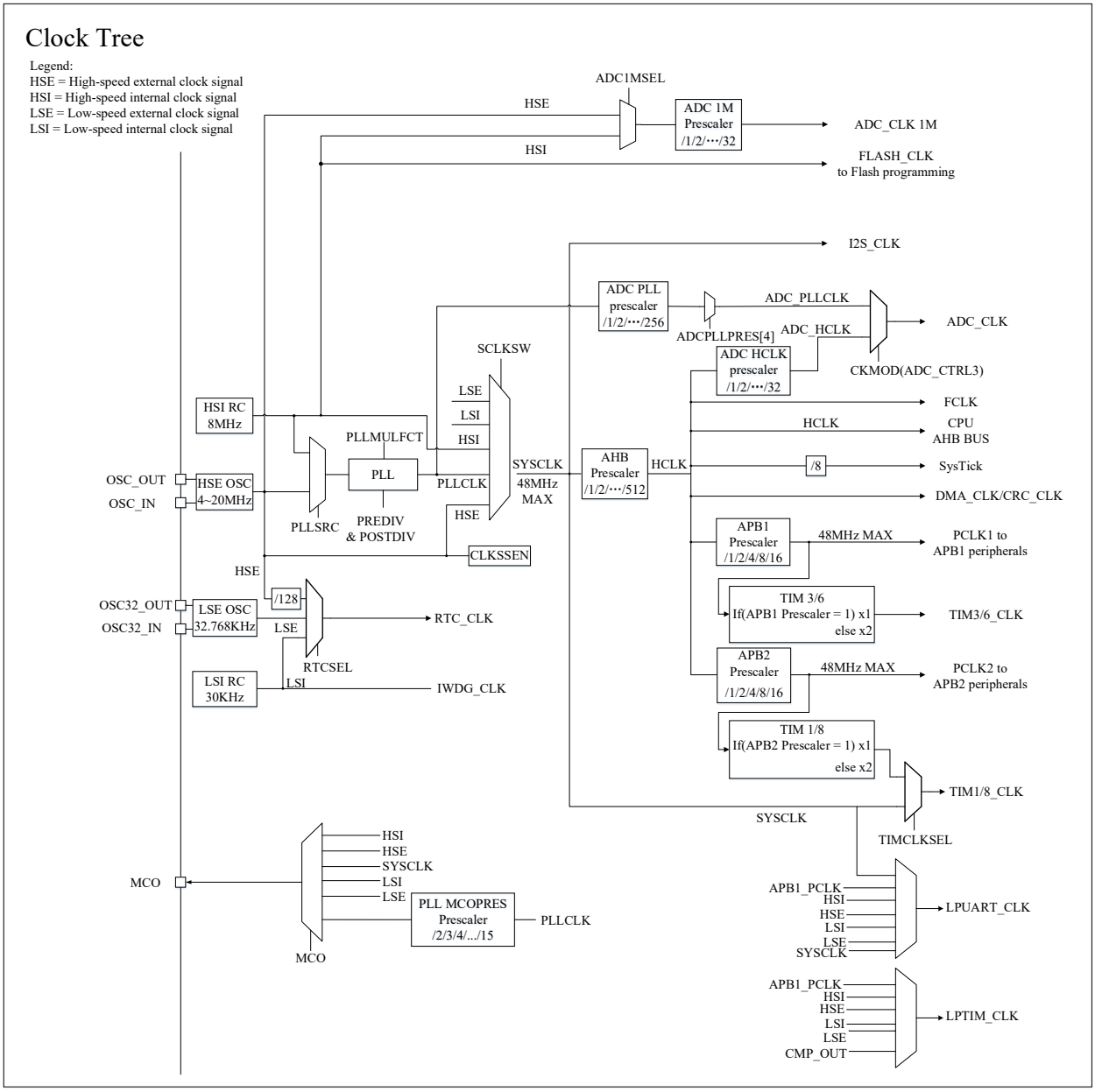
Figure 2-2 Clock Tree



2.5 Boot Mode

During startup, the BOOT mode after reset can be selected with the BOOT0 pin and option byte BOOT configuration (USER2).

- Boot from Flash memory
- Boot from system memory
- Boot from embedded SRAM

The Bootloader is stored in the system memory and can program the Flash memory through USART1 interface.

2.6 Power Supply Scheme

- V_{DD} = 1.8~5.5V: Mainly supplies power input for Main Regulator, IO and clock reset system.

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- V_{DDA} = 1.8~5.5V: Supplies power for most analog peripherals. For more information, please refer to the electrical characteristics section of the relevant data sheet.
- V_{DDD}: The voltage regulator supplies power for the CPU, AHB, APB, SRAM, Flash and most digital peripheral interfaces.
- PWR is the power control module for the entire device, its main function is to control N32G030 to enter different power modes and can be awakened by other events or interrupts. N32G030 supports RUN, LPRUN, SLEEP, STOP and PD modes.

2.7 Programmable Voltage Detector

The power-on reset (POR) and power-down reset (PDR) circuits are integrated internally. This part of the circuit is always in operating condition to ensure that the system operates normally when the power supply voltage exceeds 1.8V. When V_{DD} is lower than the set threshold ($V_{POR/PDR}$), the device remains in the reset state. The device has a built-in programmable voltage detector (PVD), which monitors the power supply of V_{DD}/V_{DDA} and compares it with the threshold V_{PVD}. When V_{DD} is lower or higher than the threshold V_{PVD}, it will generate an interrupt. The interrupt handler can send a warning message, and the PVD needs to be enabled through the program.

Table 4-6 is the value reference of $V_{POR/PDR}$ and V_{PVD}.

2.8 Low Power Mode

N32G030 is in operating mode after system reset or power-on reset. When the CPU does not need to run, you can choose to enter a low power mode to save power.

N32G030 has the following four low power modes:

- LPRUN mode (Low Power Operating mode, the system operates at 32.768KHz low-frequency mode)
- SLEEP mode (the core is stopped, all peripherals including Cortex®-M0 core peripherals (such as NVIC, SysTick) are still running)
- STOP mode (most of the clocks are turned off, the voltage regulator is still running in low power mode)
- PD mode (V_{DDD} power down mode, V_{DD} retention, 3 WAKEUP IO and NRST can wake up)
- In addition, the following methods can also reduce the power consumption in operating mode:
  - Reduce the system clock frequency
  - Disable the unused peripheral clocks on the APB and AHB buses
  - In Operating mode, by setting PWR_CTRL4.STBFLH, the Flash can enter deep STANDBY mode. When exiting, the system needs to wait about 10us before re-accessing Flash

2.9 Direct Memory Access (DMA)

The device integrates a flexible general-purpose DMA controller that supports 5 DMA channels. It can manage data transfers from memories to memories, peripherals to memories, and memories to peripherals.

Each channel has dedicated hardware DMA request logic, and each channel can be triggered by software. The transmission length, source address and destination address for each channel can be set separately by software.

DMA can be used with major peripherals: SPI, I2C, USART, TIMx (Advanced/General/Basic Timers), I2S and ADC.

2.10 Real Time Clock (RTC)

The Real Time Clock (RTC) has a set of independent continuous Binary Coded Decimal (BCD) timers/counters. With the corresponding software configuration, it can provide calendar functionality. The RTC also provides two programmable alarm clock interrupts.

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Two 32-bit registers contain Binary Coded Decimal (BCD) for subsecond, second, minute, hour (in 12 or 24 hour format), day of the week, day (date), month, and year.

Two 32-bit programmable alarms registers contain second, minute, hour, date, month, year and the day of the week.

Two 32-bit programmable alarms registers contain sub-seconds.

The RTC provides automatic wake up functionality in low power mode.

When a timestamp events or tamper detection event are enabled on GPIO, the current calendar is saved in a register.

2.11 Timer And Watchdog

Up to 2 advanced control timers, 1 general-purpose timers and 1 basic timers, 1 low power timer, 2 watchdog timers and 1 system tick timer.

The following table compares the functions of advanced control timer, general-purpose timer, basic timer and low power timer:

Table 2-1 Comparison of Timer Function

Timer	Counter Resolution	Counter Type	Prescaler Factor	Generate DMA Request	Capture/Compare Channel	Complementary Output
TIM1 TIM8	16-bit	Up,Down Up/Down	Any integer between 1~65536	Y	4	Y
TIM3	16-bit	Up,Down Up/Down	Any integer between 1~65536	Y	4	N
TIM6	16-bit	Up	Any integer between 1~65536	Y	0	N
LPTIM	16-bit	Up	1/2/4/8/16/32/64/128	N	0	N

2.11.1 Low Power Timer (LPTIM)

The LPTIM is a 16-bit timer with multiple clock sources, it can keep running in all power modes except for PD mode. LPTIM can run without internal clock source as a “Pulse Counter”. Also, the LPTIM can wake up the system from low-power modes, to realize “Timeout functions” with extremely low power consumption.

Main features:

- 16-bit up-counter
- 3-bit clock prescaler, 8 kinds of prescaler dividing factors (1,2,4,8,16,32,64,128)
- Multiple clock sources
  - Internal: HSI, HSE, LSI, LSE, COMP_OUT and APB1 clock
  - External: LPTIM input1 (operating without LP oscillator, for pulse counter application)
- 16-bit auto-reload register (LPTIM_ARR)
- 16-bit compare register (LPTIM_COMP)
- Continuous/One-shot counting mode
- Programmable software or hardware input trigger
- Programmable digital filter for glitch filtering
- Configurable output(square wave, PWM)

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- Configurable I/O polarity
- Encoder mode
- Pulse counting mode, support single pulse counting, double pulse counting (quadrature and non-quadrature)

2.11.2 Basic Timer (TIM6)

The basic timer contains a 16-bit counter.

Main features:

- 16-bit auto-reload up-counting counters.
- 16-bit programmable prescaler. (The prescaler factor can be configured with any value between 1 and 65536)
- Events that generate the interrupt/DMA is as follow:
  - Update event

2.11.3 General Purpose Timer (TIM3)

The general-purpose timers (TIM3) is mainly used in the following occasions: counting the input signal, measuring the pulse width of the input signal and generating the output waveform, etc.

Main features:

- 16-bit auto-reload counters. (It can realize up-counting, down-counting, up/down counting)
- 16-bit programmable prescaler. (The prescaler factor can be configured with any value between 1 and 65536)
- TIM3 up to 4 channels
- Channel's operating modes: PWM output, output compare, one-pulse mode output, input capture.
- Timer can be controlled by external signal
- Timers can be linked together internally for timer synchronization or chaining
- The events that generate the interrupt/DMA are as follows:
  - Update event
  - Trigger event
  - Input capture
  - Output compare
- Incremental (quadrature) encoder interface: used for tracking motion and resolving rotation direction and position;
- Hall sensor interface: used to do three-phase motor control;

2.11.4 Advanced Control Timers (TIM1 and TIM8)

The advanced control timers (TIM1 and TIM8) is mainly used in the following purpose: counting the input signal, measuring the pulse width of the input signal and generating the output waveform, etc.

Advanced timers have complementary output function with dead-time insertion and brake function. They are suitable for motor control.

Main features:

- 16-bit auto-reload counters. (It can realize up-counting, down-counting, up/down counting).
- 16-bit programmable prescaler. (The prescaler factor can be configured with any value between 1 and 65536)
- Programmable Repetition Counter
- TIM1 and TIM8 up to 6 channels

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- 4 capture/compare channels, the operating modes are PWM output, Ouput compare, One-pulse mode output, Input capture
- Timer can be controlled by external signal
- Timers can be linked together internally for timer synchronization or chaining
- TIM1_OC5 and TIM8_OC5 for COMP blanking.
- TIM1_OC6 for switch the master and slave channels of OPAMP.
- The events that generate the interrupt/DMA are as follows:
  - Update event
  - Trigger event
  - Input capture
  - Output compare
  - Break input
- Complementary outputs with programmable dead-time.
  - For TIM1 and TIM8, channel 1,2,3 support this feature
- Incremental (quadrature) encoder interface: used for tracking motion and resolving rotation direction and position;
- Hall sensor interface: used to do three-phase motor control;

2.11.5 SysTick Timer (SysTick)

This timer is dedicated to real-time operating systems and can also be used as a standard down-counter.

Main features:

- 24 bit down-counter
- Automatic reloading function
- A maskable system interrupt is generated when the counter is 0
- Programmable clock source

2.11.6 Watchdog (WDG)

Support for two watchdog independent watchdog (IWDG) and window watchdog (WWDG). Two watchdogs provide increased security, time accuracy, and flexibility in use.

Independent Watchdog (IWDG)

The independent watchdog is based on a 12-bit down-counter and a 3-bit prescaler. It is driven by a separate low-speed RC oscillator that remains active even if the master clock fails and operates in STOP modes. Once activated, if the watchdog is not fed (clears the watchdog counter) within the set time, the IWDG generates a reset when the counter counts to 0x000. It can be used to reset the entire system in the event of an application problem, or as a free timer to provide time-out management for applications. It is hardware or software configurable through the option byte. Reset and low power wake up are available.

Window Watchdog (WWDG)

A window watchdog is usually used to detect software failures caused by an application deviating from the normal running sequence due to external interference or unforeseen logical conditions. Unless the down-counter value is flushed before the T6 bit becomes zero, the watchdog circuit generates an MCU reset when the preset time period is reached. If the 7-bit decrement counter value (in the control register) is flushed before the decrement counter reaches the window register value, then an MCU reset will also occur. This indicates that the down-counter needs to be refreshed in a finite time window.

- Main features:

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- The clock of the window watchdog (WWDG) is obtained by the APB1 clock frequency by 4096.
- Programmable free-running down-counter;
- Reset condition:
  - When the down-counter is less than 0x40, a reset occurs (if the watchdog is started);
  - A reset occurs when the decrement counter is reloaded outside the window (if the watchdog is started);
- If the watchdog is enabled and interrupts are allowed, an early wake up interrupt (EWI) occurs when the down-counter equals 0x40, which can be used to reload the counter to avoid WWDG reset.

2.12 I2C Bus Interface (I2C)

The device integrates up to two independent I2C bus interfaces, which provide multi-master function and control all I2C bus-specific timing, protocol, arbitration and timeout. I2C bus interface supports multiple communication rate modes (up to 1MHz), supports DMA operations and is compatible with SMBus 2.0. The I2C module provides multiple functions, including CRC generation and verification, SMBus (System Management Bus), and PMBus (Power Management Bus).

Main features:

- Multi-master function: this module can be used as master device or slave device;
- I2C master device function:
  - Generate a clock;
  - Generate start and stop signals;
- I2C slave device function
  - Programmable address detection;
  - The I2C interface supports 7-bit or 10-bit addressing and dual-slave address response capability in 7-bit slave mode.
  - Stop bit detection;
- Generate and detect 7-bit / 10-bit addresses and general calls;
- Support different communication speeds;
  - Standard speed (up to 100 kHz);
  - Fast (up to 400 kHz);
  - Fast + (up to 1MHz);
- Status flags:
  - Transmitter/receiver mode flag;
  - Byte transfer complete flag;
  - I2C bus busy flag;
- Error flags:
  - Arbitration loss in master mode.
  - Acknowledge (ACK) fail after address/data transfer;
  - Error start or stop condition detected
  - Overrun or underrun when clock extending is disable;
- One interrupt vector:

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  - Event interrupts and error interrupts share one interrupt vector
- Optional extend clock function
- DMA of single-byte buffers;
- Generation or verification of configurable PEC(packet error checking)
  - In transmit mode, the PEC value can be transmitted as the last byte
  - PEC error check for the last received byte
- SMBus 2.0 compatible
  - Timeout delay for 25 ms clock low
  - 10 ms accumulates low clock extension time of master device
  - 25 ms accumulates low clock extension time of slave device
  - PEC generation/verification of hardware with ACK control
  - Support address resolution protocol (ARP)
- Compatible with the PMBus

2.13 Universal Synchronous/Asynchronous Transceiver (USART)

The N32G030 series products integrate up to 3 serial transceiver interfaces, including 2 universal synchronous/ asynchronous transceivers (USART1 and USART2) and 1 universal asynchronous transceivers (LPUART) supporting low power mode operation.

The USART1 and USART2 interfaces have hardware CTS and RTS signal management, ISO7816-compatible Smart card mode, and synchronous/asynchronous communication mode, supports for IrDA, SIR, ENDEC transmission codec, multi-processor communication mode, single-wire half-duplex communication mode, and LIN master/slave function, all of which can use DMA operations.

The LPUART interfaces have hardware CTS and RTS signal management, asynchronous communication mode, all of which can use DMA operations. LPUART can wakeup system from stop mode.

Main features:

- Full duplex, asynchronous communication
- NRZ standard format
- Fractional baud rate generator system, baud rate programmable, used for sending and receiving up to 3Mbits/s
- Programmable data word length (8 or 9 bits)
- Configurable stop bit, supporting 1 or 2 stop bits
- LIN master's ability to send synchronous interrupters and LIN slave's ability to detect interrupters. When USART hardware is configured as LIN, it generates 13 bit interrupters and detects 10/11 bit interrupters
- Output sending clock for synchronous transmission
- IrDA SIR encoder decoder, supports 3/16 bit duration in normal mode
- Smart card simulation function
  - The Smart-card interface supports the asynchronous Smart-card protocol defined in ISO7816-3.
  - 0.5 and 1.5 stop bits for smart cards
- Single-wire half duplex communication
- Configurable multi-buffer communication using DMA, receiving/sending bytes in SRAM using centralized DMA buffer

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- Independent transmitter and receiver enable bits
- Detect flag
  - Receive buffer is full
  - Send buffer empty
  - Transmission complete
- Parity control
  - Send parity bit
  - Check the received data
- Four error detection flags;
  - Overflow error
  - Noise error
  - Frame error
  - Parity error
- 10 USART interrupt sources with flags
  - CTS change
  - LIN break detection
  - Send data register is empty
  - Send complete
  - Received data register is full
  - Bus was detected to be idle
  - Overflow error
  - Frame error
  - Noise error
  - Parity error
- Multi-processor communication, if the address does not match, then enter the silent mode;
- Wake up from silent mode (via idle bus detection or address flag detection)
- Mode configuration:

USART modes	USART1	USART2	LPUART
Asynchronous mode	support	support	support
Hardware flow control	support	support	support
Multi-cache Communication (DMA)	support	support	support
Multiprocessor communication	support	support	nonsupport
Synchronous	support	support	nonsupport
Smart card	support	support	nonsupport
Half duplex (single wire mode)	support	support	nonsupport
IrDA	support	support	nonsupport
LIN	support	support	nonsupport

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2.14 Serial Peripheral Interface (SPI)

The device integrates two SPI interfaces, one of which multiplexed with I2S interface, shares resources with I2S.

SPI allow the chip to communicate with peripheral devices in a half/full duplex, synchronous, serial manner modes. This interface can be configured in master mode and provides a communication clock (SCLK) for external slave devices. Interfaces can also work in a multi-master configuration. It can be used for a variety of purposes, including two-line simplex synchronous transmission using a two-way data line, and reliable communication using CRC checks.

Main features:

- 3-wire full-duplex synchronous transmission;
- Two-wire simplex synchronous transmission with or without a third bidirectional data line
- 8 or 16 bit transmission frame format selection
- Master or slave operations
- Support multi-master mode
- Fast communication between master mode and slave mode
- NSS can be managed by software or hardware in both master and slave modes: dynamic change of master/slave modes
- Programmable clock polarity and phase
- Programmable data order, MSB before or LSB before
- Dedicated send and receive flags that trigger interrupts
- SPI bus busy flag
- Hardware CRC for reliable communication
  - In send mode, the CRC value can be sent as the last byte
  - In full-duplex mode, CRC is automatically performed on the last byte received
- Master mode failures, overloads, and CRC error flags that trigger interrupts
- Single-byte send and receive buffer with DMA capability: generates send and receive requests
- Maximum interface speed: 18Mbps

2.15 Serial Audio Interface (I2S)

I2S is a 3-pin synchronous serial interface communication protocol. The device integrates one I2S interfaces (multiplexed with SPI) and can operate in master or slave mode. I2S can be configured for 16-bit, 24-bit or 32-bit transmission, or as input or output channels, supporting audio sampling frequencies from 8KHz to 96KHz. It supports four audio standards, including Philips I2S, MSB and LSB alignment, and PCM.

It can operate in master and slave mode in half duplex communication. When it acts as a master device, it provides clock signals to external slave devices through an interface.

Main features:

- Simplex communication (send or receive only)
- Master or slave operations
- 8-bit linear programmable prescaler for accurate audio sampling frequencies (8 KHZ to 96KHz)
- The data format can be 16, 24, or 32 bits
- Audio channel fixed packet frame is 16 bit (16 bit data frame) or 32 bit (16, 24 or 32 bit data frame)
- Programmable clock polarity (steady state)

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- The overflows flag bit in slave sending mode and the overflows flag bit in master/slave receiving mode
- 16-bit data registers are used for sending and receiving, with one register at each end of the channel
- Supported I2S protocols
  - I2S Philips standard
  - MSB alignment standard (left aligned)
  - LSB alignment standard (right aligned)
  - PCM standard (16-bit channel frame with long or short frame synchronization or 16-bit data frame extension to 32-bit channel frame)
- The data direction is always MSB first
- Both send and receive have DMA capability
- The master clock can be output to external audio devices at a fixed rate of 256xFs(Fs is the audio sampling frequency)

2.16 General Purpose Input/Output (GPIO)

Up to 40 GPIOs, which can be divided into 4 groups (GPIOA/GPIOB/GPIOC/ GPIOF), Each group of GPIOA and GPIOB each has 16 pins, GPIOC has 3 pins and GPIOF has 5 pins. Each GPIO pin can be configured by software as an output (push-pull or open drain), input (with or without pull-up or pull-down) or alternate peripheral function ports (output/input). Most GPIO pins are shared with digital or analog alternate peripherals, and some I/O pins are multiplexed with clock pins. All GPIO pins have high current passing capability except ports with analog input capability.

Main features:

- Each bit of the GPIO port can be configured separately by the software into multiple modes
  - Input floating
  - Input pull-up
  - Input pull-down
  - Analog function
  - Open drain output and pull-up/pull-down can be configured
  - Push-pull output and pull-up/pull-down can be configured
  - Push-pull alternate function and pull-up/pull-down can be configured
  - Open-drain alternate function and pull-up/pull-down can be configured
- Separate bit setting or bit clearing functions
- All IO supports external interrupt function
- All IO supports low power mode wake-up, rising or falling edge configurable
  - 16 EXTIs can be used to wake up from SLEEP or STOP mode, and all I/Os can be reused as EXTIs
  - The three IO of PA0/PC13/PA2 three wake-up IO can be used for PD mode wake-up, the maximum I/O filter time is 1us
- Support software remapping I/O alternate function
- Support GPIO lock mechanism, when a lock is performed on a port bit, the configuration of the port bit cannot be changed until the next reset
- Each I/O port bit can be programmed arbitrarily, but I/O port registers must be accessed as 32-bit words

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(16-bit half-word or 8-bit byte access is not allowed). The following figure shows the basic structure of an I/O port.

2.17 Analog/Digital Converter (ADC)

The device supports a 12-bit Successive Approximation Register ADC with a sampling rate of 1Msps, measuring up to 12 external and 4 internal sources. The A/D conversion of each channel can be performed in single, continuous, scan, or burst mode. The results of the ADC can be stored in 16-bit data registers in either left-aligned or right-aligned format. Input clock of ADC can not exceed 18MHz.

Main features:

- Support 12-bit resolution, the maximum sampling rate is 1Msps
- ADC clock source is divided into working clock source, sampling clock source and timing clock source
  - AHB_CLK can be configured as the operating clock source, up to 48MHz
  - PLL can be configured as a sampling clock source, up to 18MHZ, support 1,2,3,4,6,8,10,12,16,32, 64,128,256 frequency division
  - The AHB_CLK can be configured as the sampling clock source, up to 18MHz, and supports frequency 1,2,3,4,6,8,10,12,16,32
  - The timing clock is used for internal timing functions and the frequency must be configured to 1MHz
- Supports timer trigger ADC sampling
- Interrupts when conversion ends, injection conversion ends, and analog watchdog events occur
- Single and continuous conversion modes
- Automatic scan mode from channel 0 to channel N
- Data alignment with embedded data consistency
- Sampling intervals can be programmed separately by channel.
- Both regular conversions and injection conversions have external triggering options
- Discontinuous mode
- ADC power supply requirements: 2.4V to 5.5V
- ADC input range: $0 \leq V_{IN} \leq V_{DDA}$
- ADC can use DMA operations, and DMA requests are generated during regular channel conversion.

2.18 Operational Amplifier (OPAMP)

The device intergrated an independent operational amplifier with multiple operating modes such as external amplifier, internal follower and programmable amplifier (PGA).

Main features:

- Support rail-to-rail input
- OPA linear output range 0.4V~VDDA-0.4V
- Can be configured as independent OPAMP and programmable gain OPAMP
- Non-inverted and inverted input multiple selection
- OPAMP working mode can be configured as:
  - Independent mode (external gain setting)

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  - PGA mode, programmable gain ranging of 2X, 4X, 8X, 16X, 32X
  - Follower mode
- The internally connected ADC channel is used to measure the output signal of the OPAMP

2.19 Analog Comparator (COMP)

The device integrates up to 1 comparators, support low power mode. It can be used as a separate device (all ports of the comparator are plugged into the I/O) or in combination with a timer. In the case of motor control, it can be combined with the PWM output from the timer to form periodic current control.

Main features:

- 1 independent COMP, support low power mode(can work at LPRUN, SLEEP, STOP mode)
- Internal 64-level programmable reference input compares voltage source VREF.
- Support filtered clock, filtered reset
- Output polarity can be configured to high or low
- Programmable hysteresis can be configured as no hysteresis, low hysteresis, medium hysteresis, and high hysteresis
- The comparator can output to either I/O or timer input for capturing events, OCREF_CLR events, breaking events, triggering event.
- Input channel can select I/O port, V_{REF}
- Can be configured with read-only or read-write, and needs to be reset to unlock when locked
- Support blanking, blanking source can be configured
- COMP can wake up the system from low power mode by generating an interrupt, and COMP has the ability to wake up the system from STOP. COMP output generate interrupt by connect to EXTI
- Configurable filter window size
- Configurable filter threshold size
- Configurable sampling frequency for filtering

2.20 Temperature Sensor (TS)

The temperature sensor generates a voltage that varies linearly with temperature in the range of 1.8V $<V_{DDA}<$5.5V. The temperature sensor is internally connected to the ADC_IN12 input channel for converting the output of the temperature sensor to a digital value.

2.21 Beeper

The beeper module supports complementary outputs and can generate periodic signals to drive external passive buzzers. Used to generate a beep or the alarm to sound.

2.22 HDIV/SQRT

The divider (HDIV) and square root (SQRT) are mainly used in some scenarios with high requirements for computing energy efficiency, and are used to partially supplement the deficiencies of the microcontroller in computing. The divider and square root calculator can perform division or square root calculation of unsigned 32-bit integers.

Main features:

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- Only support word operation
- 8 clock cycles to complete an unsigned integer division operation
- 32-bit dividend, 32-bit divisor, output 32-bit quotient and 32-bit remainder
- Divisor is zero warning flag, division operation end flag
- 32-bit unsigned radicand integer, 16-bit square root output
- 8 clock cycles to complete an unsigned integer square operation
- The completion of the calculation can be determined by enabling interrupts or querying relevant register bits

2.23 Cyclic Redundancy Check Calculation Unit (CRC)

The device integrates CRC32 and CRC16 functionalities. The cyclic redundancy check (CRC) calculation unit is based on a fixed generation polynomial to obtain arbitrary CRC calculation results. In many applications, CRC-based techniques are used to verify data transfer or storage consistency. Within the scope of the EN/IEC 60335-1 standard, it provides a means of detecting Flash memory errors, The CRC unit can be used to calculate signatures of software in real time and compare them with signatures generated during link-time and generating of the software.

Main features:

- CRC16: supports polynomials X16 + X15 + X2 + X0
- CRC32: supports polynomials X32 + X26 + X23 + X22 + X16 + X12 + X11 + X10 + X8 + X7 + X5 + X4 + X2 + X +1
- CRC16 calculation time: 1 AHB clock cycles (HCLK)
- CRC32 calculation time: 1 AHB clock cycles (HCLK)
- The initial value for cyclic redundancy computing is configurable
- Support DMA mode

2.24 Unique Device Serial Number (UID)

The N32G030 series products have two built-in unique device serial numbers of different lengths, which are 96-bit Unique Device ID (UID) and 128-bit Unique Customer ID (UCID). These two device serial numbers are stored in the system configuration block of Flash memory.The information they contain is written at the time of delivery and is guaranteed to be unique to any of the N32G030 series microcontrollers under any circumstances and can be read by user applications or external devices through the CPU or SWD interface and cannot be modified.

The 96-bit UID is usually used as a serial number or password. When writing Flash memory, this unique identifier is combined with software encryption and decryption algorithm to further improve the security of code in Flash memory.

The UCID is 128-bit, which complies with the definition of NSING chip serial number. It contains the information related to chip production and version.

2.25 Serial Wire SWD Debug port (SWD)

The device has an embedded Arm® SWD Interface.

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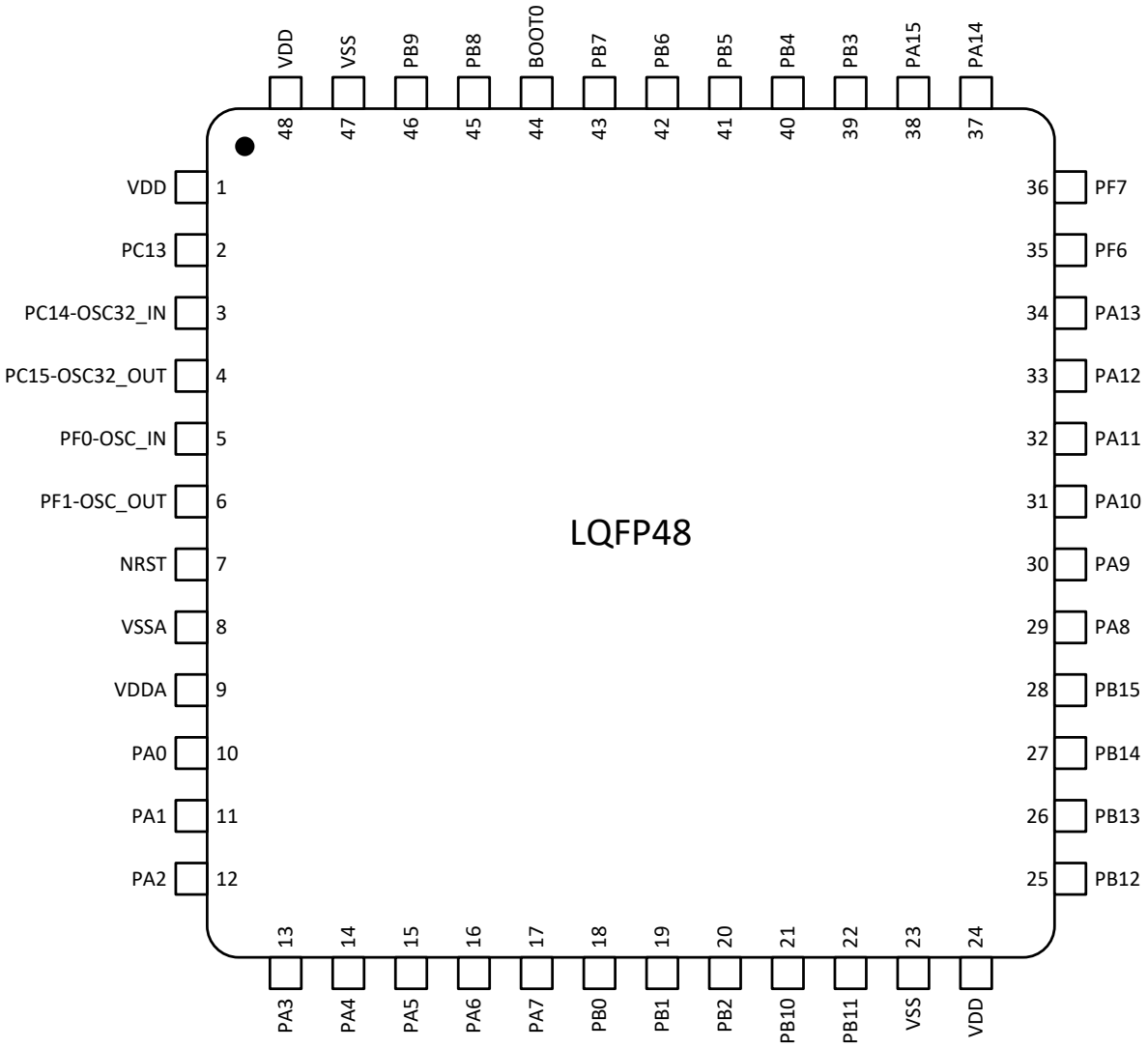
3 Pinouts And Pin Descriptions

3.1 Pinouts

3.1.1 LQFP48(7mm x 7mm)

Figure 3-1 N32G030 Series LQFP48 Pinouts



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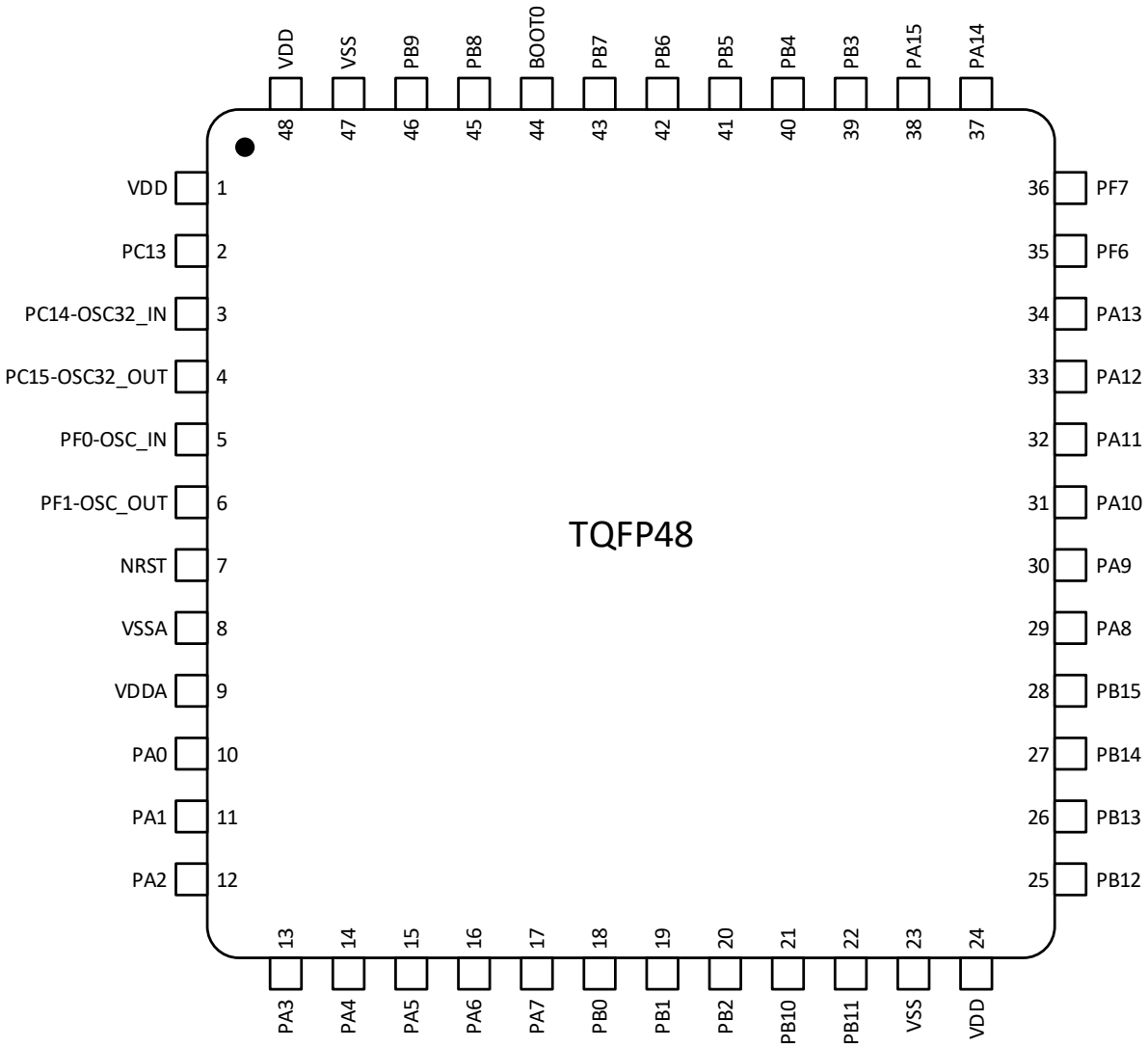
3.1.2 TQFP48(7mm x 7mm)

Figure 3-2 N32G030 Series TQFP48 Pinouts



3.1.3 LQFP32(7mm x 7mm)

Figure 3-3 N32G030 Series LQFP32 Pinouts

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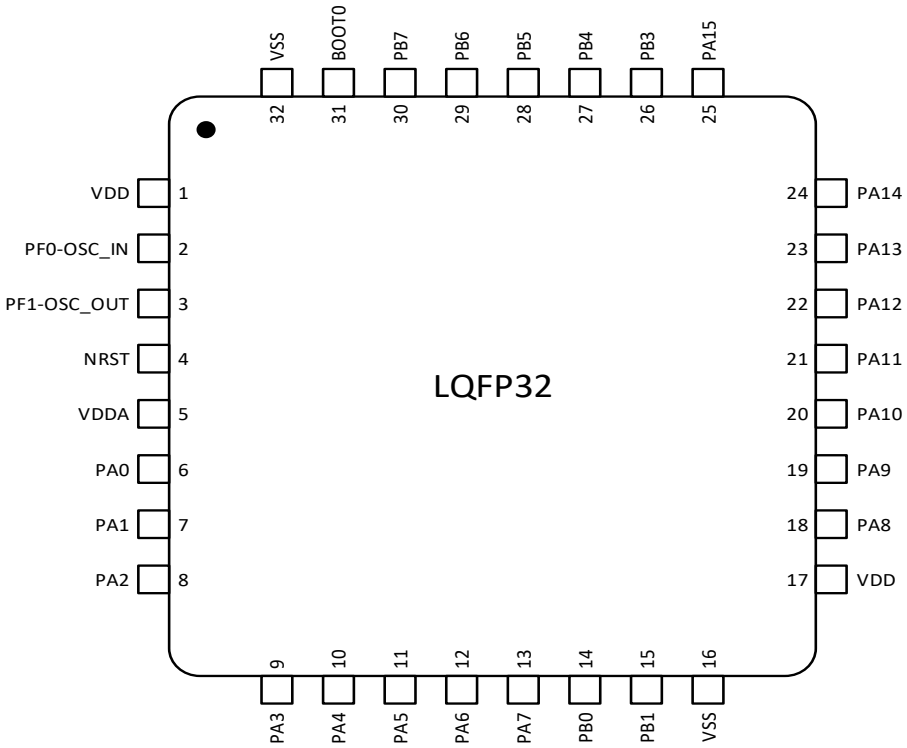

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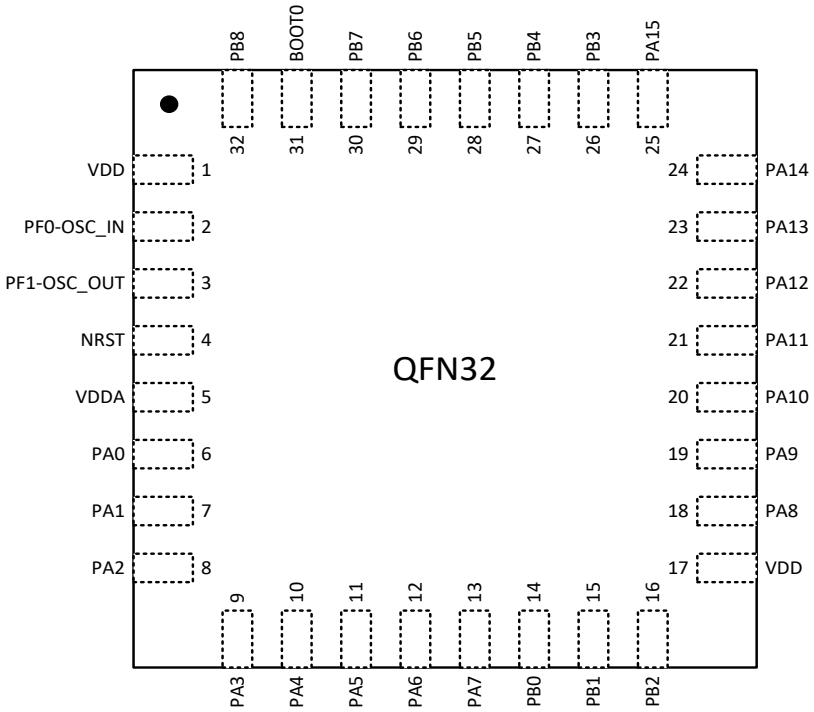
3.1.4 QFN32(5mm x 5mm)

Figure 3-4 N32G030 Series QFN32 (5mm x 5mm) Pinouts



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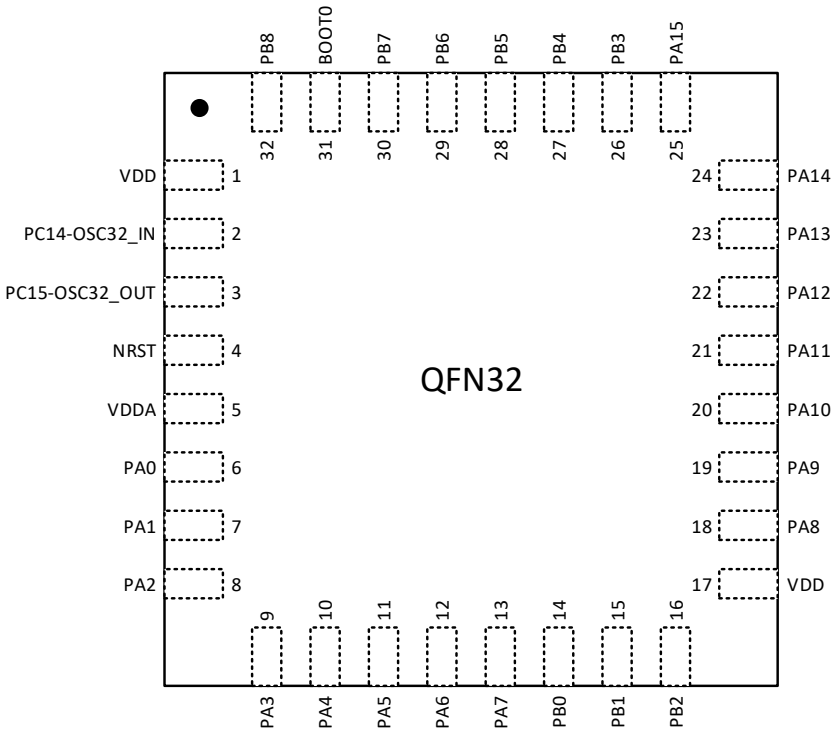
3.1.5 QFN32(4mm x 4mm)

Figure 3-5 N32G030 Series QFN32 (4mx4m) Pinouts



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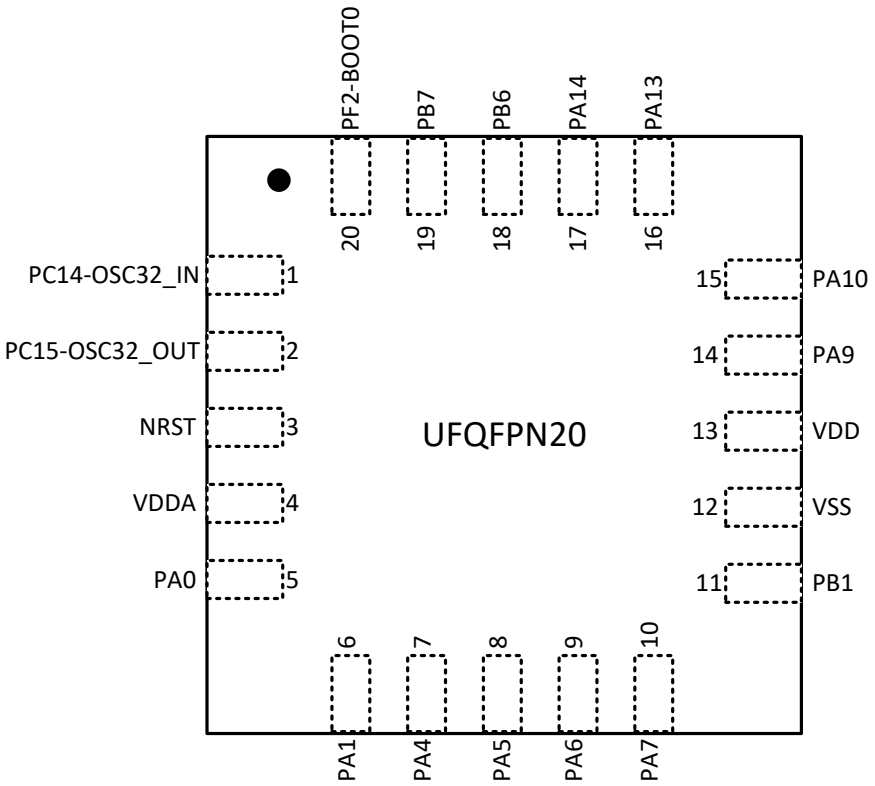
3.1.6 UFQFPN20(3mm x 3mm)

Figure 3-6 N32G030 Series UFQFPN20 Pinouts



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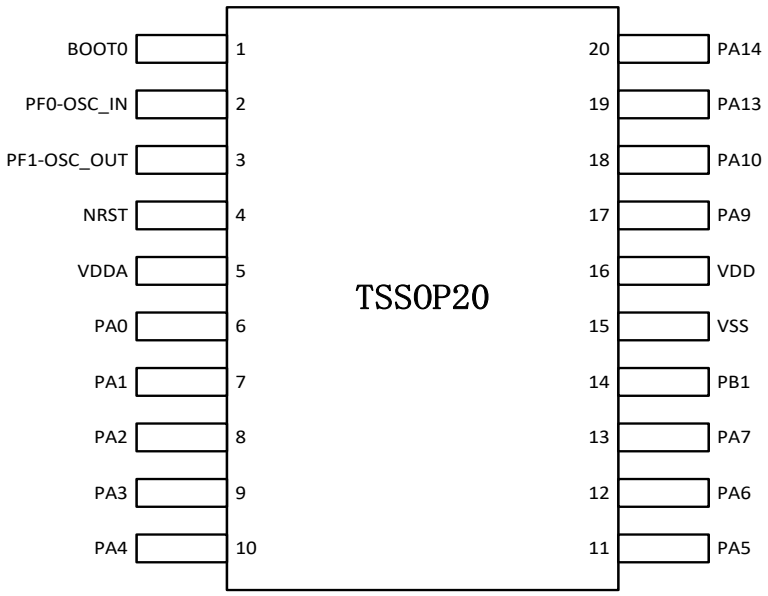
3.1.7 TSSOP20(6.5mm x 4.4mm)

Figure 3-7 N32G030 Series TSSOP20 Pinouts



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3.2 Pin Description

Table 3-1 Pin Description

Package						Pin Name (after reset)	Type(1)	I/O structure	Alternate Functions	Optional Functions
LQFP48	LQFP32	QFN32 (5mmx5mm)	QFN32 (4mmx4mm)	UFQFPN20	TSSOP20					
1	1	1	1	-	-	V_{DD}	S	-	Complementary power supply	
2	-	-	-	-	-	PC13	I/O	TC	RTC_TAMP1, RTC_TS, RTC_OUT,	WKUP1
3	-	-	2	1	-	PC14-OSC32_IN (PC14)	I/O	TC	-	OSC32_IN
4	-	-	3	2	-	PC15-OSC32_OUT (PC15)	I/O	TC	-	OSC32_OUT
5	2	2	-	-	2	PF0-OSC_IN (PF0)	I/O	TC	I2C1_SDA	OSC_IN, OPAMP_VINP
6	3	3	-	-	3	PF1-OSC_OUT (PF1)	I/O	TC	I2C1_SCL, USART1_CK, USART2_CK	OSC_OUT
7	4	4	4	3	4	NRST	I	RST	Device reset input / internal reset output (active low)	
8	-	-	-	-	-	VSSA	S	-	Analog ground	
9	5	5	5	4	5	V_{DDA}	S	-	Analog power supply	
10	6	6	6	5	6	PA0	I/O	TC	USART1_CTS USART2_CTS LPUART_TX, SPI1_SCK, I2S_CK USART2_RX, LPTIM_IN1, TIM8_CH1, TIM8_ETR, LPUART_RX,	ADC_IN0, RTC_TAMP2, WKUP0, COMP_INM, COMP_OUT, OPAMP_VINP
11	7	7	7	6	7	PA1	I/O	TC	USART1_RTS USART2_RTS, EVENTOUT, SPI1_NSS, I2S_WS, LPTIM_IN2, TIM8_CH2, I2C1_SMBA, TIM3_ETR, LPUART_TX	ADC_IN1, COMP_INP, OPAMP_VINP

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Package						Pin Name (after reset)	Type(1)	I/O structure	Alternate Functions	Optional Functions
LQFP48	LQFP32	QFN32 (5mmx5mm)	QFN32 (4mmx4mm)	UFQFPN20	TSSOP20					
12	8	8	8	-	8	PA2	I/O	TC	USART1_TX, USART2_TX, TIM8_CH3, SPI1_MOSI, I2S_SD, TIM1_BKIN	ADC_IN2, WKUP2, OPAMP_VINM
13	9	9	9	-	9	PA3	I/O	TC	USART1_RX, USART2_RX, TIM8_CH4, TIM1_CH2, SPI1_MISO, I2S_MCK, LPUART_RX	ADC_IN3, COMP_INP
14	10	10	10	7	10	PA4	I/O	TC	SPI1_MISO I2S_MCK, USART1_CK, USART2_CK, TIM3_CH1, TIM1_CH1, SPI1_NSS, I2S_WS, I2C1_SCL, TIM8_ETR, LPUART_TX	ADC_IN4, COMP_INM, OPAMP_VINP
15	11	11	11	8	11	PA5	I/O	TC	SPI1_SCK, I2S_CK, TIM8_ETR, TIM1_CH2N, TIM1_CH3 SPI1_MOSI, I2C_SD, TIM8_CH1	ADC_IN5, COMP_INM, OPAMP_VINM
16	12	12	12	9	12	PA6	I/O	TC	SPI1_MISO, TIM3_CH1, TIM1_BKIN, TIM8_CH1, EVENTOUT, LPUART_CTS, LPUART_TX, I2C2_SCL, LPTIM_ETR, BEEPER_OUT	ADC_IN6, COMP_OUT, OPAMP_VOUT
17	13	13	13	10	13	PA7	I/O	TC	SPI1_MOSI, SPI2_NSS, I2S_SD, TIM3_CH2, TIM1_CH1N, TIM8_CH2, EVENTOUT, LPUART_RX, I2C2_SDA, BEEPER_N_OUT, USART2_CTS,	ADC_IN7, OPAMP_VINP, COMP_INP

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Package						Pin Name (after reset)	Type(1)	I/O structure	Alternate Functions	Optional Functions
LQFP48	LQFP32	QFN32 (5mmx5mm)	QFN32 (4mmx4mm)	UFQFPN20	TSSOP20					
18	14	14	14	-	-	PB0	I/O	TC	TIM3_CH3, TIM1_CH2N, EVENTOUT, SPI2_SCK,	ADC_IN8, OPAMP_VINP
19	15	15	15	11	14	PB1	I/O	TC	TIM3_CH3, TIM3_CH4, TIM1_CH3N, LPUART_RTS, I2S_SD SPI2_MOSI, USART2_CK, SPI1_MOSI,	ADC_IN9, OPAMP_VINM
20	-	16	16	-	-	PB2	I/O	TC	I2C1_SMBA, I2C2_SMBA, TIM3_CH4, LPTIM_OUT	ADC_IN10, OPAMP_VINM
21	-	-	-	-	-	PB10	I/O	TC	SPI2_SCK, I2C1_SCL, I2C2_SCL, LPUART_TX, TIM3_ETR, SPI1_MOSI, I2S_SD	ADC_IN11
22	-	-	-	-	-	PB11	I/O	TC	I2C1_SDA, I2C2_SDA, EVENTOUT, LPUART_RX, TIM8_CH3	-
23	16	-	-	12	-	VSS	S	-	Ground	
24	17	17	17	13	-	V_{DD}	S	-	Digital power supply	
25	-	-	-	-	-	PB12	I/O	TC	SPI1_NSS, I2S_WS, SPI2_NSS, TIM1_BKIN, EVENTOUT, TIM8_CH1	-
26	-	-	-	-	-	PB13	I/O	TC	SPI1_SCK, I2S_CK, SPI2_SCK, I2C2_SCL, TIM1_CH1N, LPUART_CTS, TIM8_CH2	-

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Package						Pin Name (after reset)	Type(1)	I/O structure	Alternate Functions	Optional Functions
LQFP48	LQFP32	QFN32 (5mmx5mm)	QFN32 (4mmx4mm)	UFQFPN20	TSSOP20					
27	-	-	-	-	-	PB14	I/O	TC	SPI1_MISO, SPI2_MISO, I2C2_SDA, TIM1_CH2N, TIM8_CH3, LPUART_RTS	OPAMP_VINP
28	-	-	-	-	-	PB15	I/O	TC	SPI1_MOSI, I2S_SD, SPI2_MOSI, TIM1_CH3N, TIM8_CH3N, TIM8_CH4,	RTC_REFIN,
29	18	18	18	-	-	PA8	I/O	TC	USART1_CK, TIM1_CH1, EVENTOUT, MCO, SPI2_NSS, TIM8_CH2N,	-
30	19	19	19	14	17	PA9	I/O	TC	USART1_TX, TIM1_CH2, TIM8_BKIN, I2C1_SCL, I2C2_SCL, SPI2_SCK, TIM8_CH1N, LPTIM_OUT, USART2_TX, MCO	-
31	20	20	20	15	18	PA10	I/O	TC	USART1_RX, TIM1_CH3, TIM8_BKIN, I2C1_SDA, I2C2_SDA, SPI2_ MISO, USART2_RX, RTC_REFIN,	-
32	21	21	21	-	-	PA11	I/O	TC	USART1_CTS, TIM1_CH4, EVENTOUT, I2C2_SCL, SPI2_ MOSI	COMP_OUT
33	22	22	22	-	-	PA12	I/O	TC	USART1_RTS, TIM1_ETR, EVENTOUT, I2C2_SDA, SPI2_MISO,	COMP_OUT

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Package						Pin Name (after reset)	Type(1)	I/O structure	Alternate Functions	Optional Functions
LQFP48	LQFP32	QFN32 (5mmx5mm)	QFN32 (4mmx4mm)	UFQFPN20	TSSOP20					
34	23	23	23	16	19	PA13 (SWDIO)	I/O	TC	USART1_TX, SWDIO, USART1_RX, USART2_RX, I2C1_SDA, SPI1_SCK I2S_CK	-
35	-	-	-	-	-	PF6	I/O	TC	I2C1_SCL, I2C2_SCL, SPI2_SCK	-
36	-	-	-	-	-	PF7	I/O	TC	I2C1_SDA , I2C2_SDA , SPI2_NSS	-
37	24	24	24	17	20	PA14 (SWCLK)	I/O	TC	USART1_TX, USART2_TX, SWCLK, I2C1_SMBA, SPI1_MISO,	-
38	25	25	25	-	-	PA15	I/O	TC	SPI1_NSS, I2S_WS, USART1_RX, USART2_RX, LPUART_RTS, EVENTOUT	-
39	26	26	26	-	-	PB3	I/O	TC	SPI1_SCK, I2S_CK, EVENTOUT, LPUART_TX, TIM3_ETR	-
40	27	27	27	-	-	PB4	I/O	TC	SPI1_MISO, TIM3_CH1, EVENTOUT, TIM8_BKIN, LPUART_RX, LPTIM_OUT	-
41	28	28	28	-	-	PB5	I/O	TC	SPI1_MOSI, I2S_SD, I2C1_SMBA, TIM8_BKIN, TIM3_CH2, LPUART_TX, LPTIM_IN1, TIM8_CH3N	-
42	29	29	29	18	-	PB6	I/O	TC	I2C1_SCL, USART1_TX, TIM8_CH1N, TIM8_CH3, LPTIM_ETR	-

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Package						Pin Name (after reset)	Type(1)	I/O structure	Alternate Functions	Optional Functions
LQFP48	LQFP32	QFN32 (5mmx5mm)	QFN32 (4mmx4mm)	UFQFPN20	TSSOP20					
43	30	30	30	19	-	PB7	I/O	TC	I2C1_SDA, USART1_RX, TIM8_CH2N, LPUART_CTS, LPUART_RX, LPTIM_IN2, TIM8_CH4,	-
44	31	31	31	20	1	PF2-BOOT0	I	B	Boot memory selection	
45	-	32	32	-	-	PB8	I/O	TC	I2C1_SCL, TIM8_CH1	-
46	-	-	-	-	-	PB9	I/O	TC	I2C1_SDA, USART1_TX, SPI2_NSS, TIM8_CH2, EVENTOUT	-
47	32	-	-	-	15	VSS	S	-	Ground	
48	-	-	-	-	16	V_{DD}	S	-	Digital power supply	

(1) I = input, O = output, S = power, HiZ = High resistance, B = BOOT0 pin

(2) TC: Standard 5V I/O, RST: bidirectional reset pin with built-in weak pull-up resistor

(3) This alternate function can be configured by the software to other pins (if the corresponding package model has such pins). For detailed information, please refer to the alternate function I/O chapter and debug setting chapter of the N32G435xx user reference manual.

(4) During and immediately after the reset, the multiplexing function is not enabled, and the I/O port is configured as an analog input mode (PMODEx[1:0]=2'b11). But there are a few exception signals:

- *NRST has no GPIO function by default*
- *NRST pull-up input*
- *After reset, the default state of the pins related to the debugging system is the SWD function, and the SWD pin is configured to input pull-up or pull-down mode:*
  - *PA14: SWCLK is configured as input pull-down mode*
  - *PA13: SWDIO is configured as input pull-up mode*
- *PF0:*
  - *PF0 is configured as floating input mode by default*
  - *PF0 is multiplexed to OSC_IN*
- *BOOT0:*
  - *BOOT0 is configured as pull-down input mode by default*

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4 Electrical Characteristics

4.1 Parameter Conditions

All voltages are based on VSS unless otherwise specified.

4.1.1 Minimum And Maximum Values

Unless otherwise specified, all minimums and maximums will be guaranteed under the worst ambient temperature, supply voltage and clock frequency conditions by performing tests on 100% of the product on the production line at ambient temperatures T_A=25°C.

Note at the bottom of each form that data obtained through comprehensive evaluation, design simulation and/or process characteristics will not be tested on the production line. Base on the basis of comprehensive evaluation, the minimum and maximum values are obtained by samples tested.

4.1.2 Typical Values

Unless otherwise specified, typical data is based on TA=25°C and V_{DD}=3.3V (1.8V ≤ VDD ≤ 5.5V voltage range). These data are only used for design guidance and not tested.

Typical ADC accuracy values are obtained by sampling a standard batch, tested at all temperature ranges.

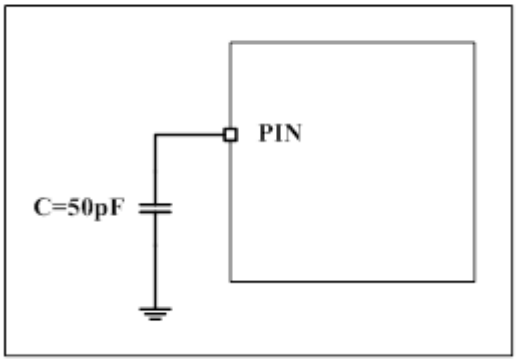
4.1.3 Typical Curves

Unless otherwise specified, typical curves are for design guidance only and have not been tested.

4.1.4 Loading Capacitor

The load conditions for measuring the pin parameters are shown in Figure 4-1.

Figure 4-1 Loading Conditions of Pins



4.1.5 Pin Input Voltage

The measurement of the input voltage on the pin is shown in Figure 4-2.

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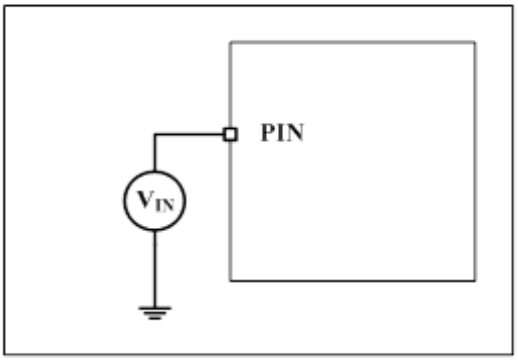
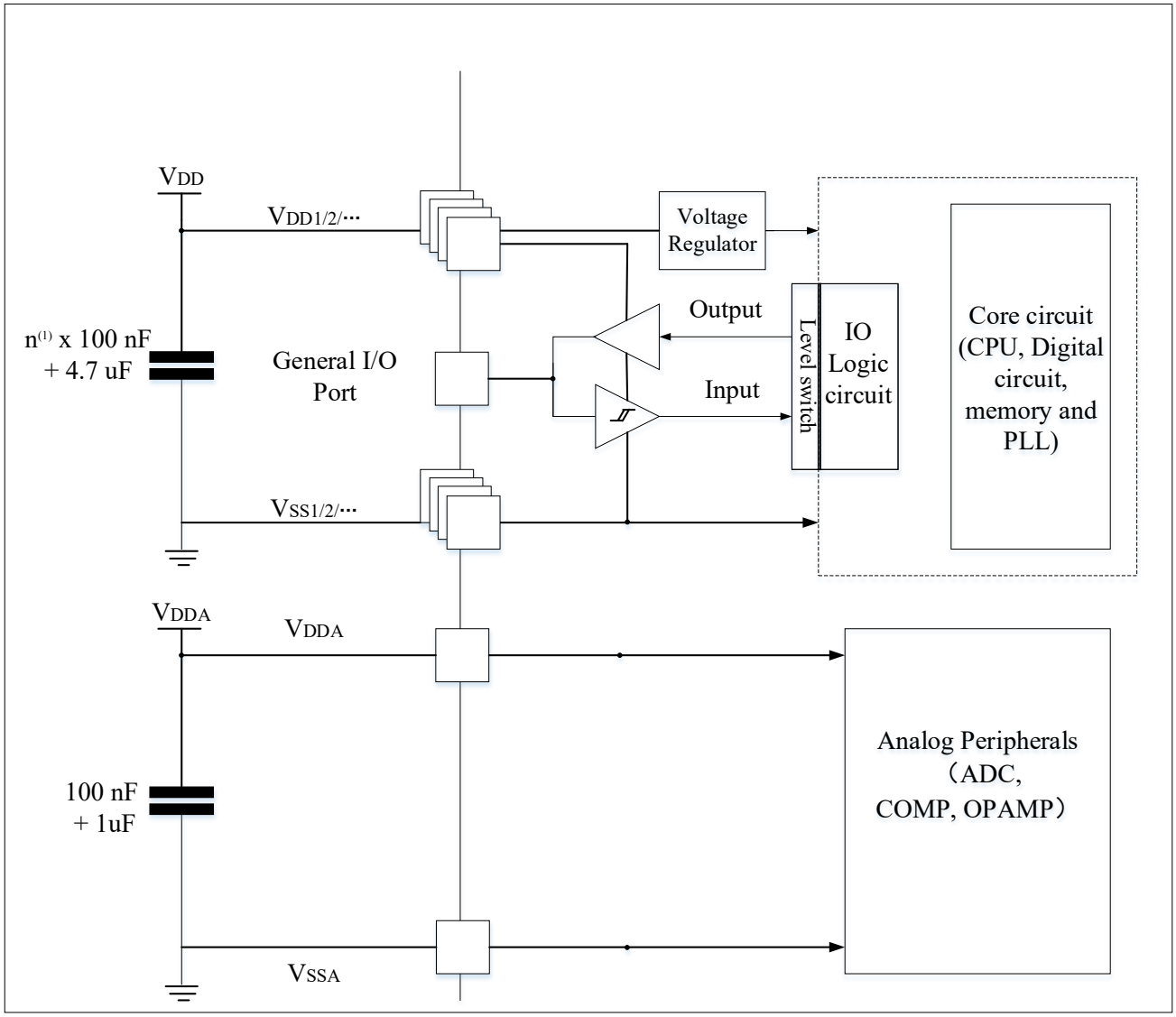
Figure 4-2 Pin Input Voltage



4.1.6 Power Supply Scheme

Figure 4-3 Power Supply Scheme



1. n is the count of VDD.

Note: Please refer to the hardware design guide for the capacitor connection method.

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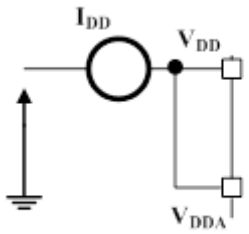
4.1.7 Current Consumption Measurement

Figure 4-4 Current Consumption Measurement Scheme



4.2 Absolute Maximum Rating

The load applied to the device may permanently damage the device if it exceeds the values given in the Absolute maximum rating list (**Error! Reference source not found.**, **Error! Reference source not found.**, **Error! Reference source not found.**). The maximum load that can be sustained is only given here, and it does not mean that the functional operation of the device under such conditions is correct. The reliability of the device will be affected when the device works for a long time under the maximum condition.

Table 4-1 Voltage Characteristics

Symbol	Describe	Min	Max	Unit
V_{DD}- V_{SS}	External supply voltage(including V_{DDA} and V_{DD})(1)	-0.3	5.5	V
V_{IN}	Input voltage on any I/O and control pins	V_{SS}-0.3	V_{DD} + 0.3	
$\lvert \Delta V_{DDx} \rvert$	Voltage difference between different power supply pins	-	50	mV
$\lvert V_{SSx}$- $V_{SS} \rvert$	Voltage difference between different ground pins	-	50	
$V_{ESD(HBM)}$	ESD electrostatic discharge voltage (human body model)	See section 4.3.11		

Note:

(1)All power (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to an external power supply within the allowable range.

Table 4-2 Current Caracteristics

Symbol	Describe	Max	Unit
I_{VDD}	Total current into V_{DD}/V_{DDA} power lines(1)	200	mA
I_{VSS}	Total current out of V_{SS} ground lines(1)	200	
I_{IO}	Output current sunk by any I/O and control pin	16	
	Output current source by any I/O and control pins	-16	
$I_{INJ(PIN)}$ (2)	Injected current of NRST pin	0/-5	
	Injected current of OSC_IN pin of HSE and OSC_IN pin of LSE	+/-5	
	Injected current of other pins	+/-5	

Note:

(1)All power (VDD, VDDA) and ground (VSS, VSSA) pins must always be connected to an external power supply within the allowable range.
(2)Negative injected current can interfere with the analog performance of the device. See section 4.3.17.

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Table 4-3 Temperature Characteristics

Symbol	Parameter	Value	Unit
T_{STG}	Storage temperature range	-40 ~ + 150	℃
T_J	Maximum junction temperature	125	℃

4.3 Operating Conditions

4.3.1 General Operating Conditions

Table 4-4 General Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
f_{HCLK}	AHB clock frequency	-	0	48	MHz
f_{PCLK1}	APB1 clock frequency	-	0	48	
f_{PCLK2}	APB2 clock frequency	-	0	48	
V_{DD}	Standard operating voltage	-	1.8	5.5	V
V_{DDA}	Analog operating voltage	Must be the same voltage as V_{DD}(1)	1.8	5.5	V
T_A	Temperature range	Maximum power consumption	-40	105	℃
T_J	Junction temperature range		-40	125	℃

Note:

(1)Use the same power supply to supply V_{DD} and V_{DDA}. During power-up and normal operation, a maximum difference of 300mV between V_{DD} and V_{DDA} is allowed.

4.3.2 Operating Conditions at Power-on and Power-down

The parameters given in the following table are based on testing under the ambient temperature listed in Table 4-4.

Table 4-5 Operating Conditions At Power-on and Power-down

Symbol	Parameter	Conditions	Min	Max	Unit
t_{VDD}	V_{DD} rising time rate	From 0 to V_{DD}	100	650	μs/V
	V_{DD} falling time rate	From V_{DD} to 0	100	∞	μs/V

4.3.3 Embedded Reset and Power Control Module Characteristics

The parameters given in the following table are based on the ambient temperature and V_{DD} supply voltage listed in Table 4-4.

Table 4-6 Embedded Reset And Power Control Module Features

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{PVD}	Rising	PLS[3:0]=0	1.78	1.88	1.98	V
	Falling	PLS[3:0]=0	1.68	1.78	1.88	
	Rising	PLS[3:0]=1	1.98	2.08	2.18	
	Falling	PLS[3:0]=1	1.88	1.98	2.08	
	Rising	PLS[3:0]=2	2.18	2.28	2.38	
	Falling	PLS[3:0]=2	2.08	2.18	2.28	
	Rising	PLS[3:0]=3	2.38	2.48	2.58	

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	Falling	PLS[3:0]=3	2.28	2.38	2.48	
	Rising	PLS[3:0]=4	2.58	2.68	2.78	
	Falling	PLS[3:0]=4	2.48	2.58	2.68	
	Rising	PLS[3:0]=5	2.78	2.88	2.98	
	Falling	PLS[3:0]=5	2.68	2.78	2.88	
	Rising	PLS[3:0]=6	2.96	3.08	3.2	
	Falling	PLS[3:0]=6	2.86	2.98	3.1	
	Rising	PLS[3:0]=7	3.16	3.28	3.4	
	Falling	PLS[3:0]=7	3.06	3.18	3.3	
	Rising	PLS[3:0]=8	3.36	3.48	3.6	
	Falling	PLS[3:0]=8	3.26	3.38	3.5	
	Rising	PLS[3:0]=9	3.56	3.68	3.8	
	Falling	PLS[3:0]=9	3.46	3.58	3.7	
	Rising	PLS[3:0]=10	3.76	3.88	4	
	Falling	PLS[3:0]=10	3.66	3.78	3.9	
	Rising	PLS[3:0]=11	3.92	4.08	4.24	
	Falling	PLS[3:0]=11	3.82	3.98	4.14	
	Rising	PLS[3:0]=12	4.12	4.28	4.44	
	Falling	PLS[3:0]=12	4.02	4.18	4.34	
	Rising	PLS[3:0]=13	4.32	4.48	4.64	
	Falling	PLS[3:0]=13	4.22	4.38	4.54	
	Rising	PLS[3:0]=14	4.52	4.68	4.84	
	Falling	PLS[3:0]=14	4.42	4.58	4.74	
	Rising	PLS[3:0]=15	4.72	4.88	5.04	
	Falling	PLS[3:0]=15	4.62	4.78	4.94	
$V_{PVDhyst}$(1)	PVD hysteresis	-	80	100	125	mV
$V_{POR/PDR}$	VDD power on/power down reset threshold	-	-	1.53	-	V
$T_{RSTTEMPO}$(1)	Reset temporization	-	-	150		us

Note:

(1)Guaranteed by design, not tested in production.

4.3.4 Internal Reference Voltage

The parameters given test conditions in the following table are based on the ambient temperature and V_{DD} supply voltage listed in Table 4-4.

Table 4-7 Internal Reference Voltage

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{REFINT}	Internal reference voltage	-40℃< T_A< +105℃	1.16	1.21	1.26	V

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$T_{S\_vrefint}$(1)	When reading the internal reference voltage, the sampling time of the ADC	PLS[2:0]=001 (Rising edge)	-	10	-	μs

Note:

(1The shortest sampling time is obtained through multiple loops in the application.

4.3.5 Power Supply Current Characteristics

The current consumption is a combination of several parameters and factors, including operating voltage, ambient temperaure, load of I/O pins, software configuration of the product, operating frequency, toggle rate of I/O pins , program location in memory, and code executed.

The measurement method of current consumption is illustrated in Figure 4-4.

All of the current consumption measurements given in this section are while executing a reduced set of code.

4.3.5.1 Maximum current consumption

The device is under the following conditions:

- All I/O pins are in input mode and connected to a static level-- V_{DD} or V_{SS} (no load).
- All peripherals are disabled except otherwise noted.
- The access time of Flash memory is adjusted to the frequency of f_{HCLK} (0~18MHz is 0 waiting period, 18~36MHz is 1 waiting period, and more than 36MHz is 2 waiting periods).
- Instruction prefetch is enabled (Note: this parameter must be set before setting the clock and bus divider).
- When the peripheral is enable: $f_{PCLK1} = f_{HCLK}$, $f_{PCLK2} = f_{HCLK}$.

The parameter given in Table 4-8, Table 4-9 and Table 4-10 are based on tests at the ambient temperature and VDD supply voltage listed in Table 4-4.

Table 4-8 Typical Current Consumption in RUN Mode During Code run from Embedded Flash

Symbol	Parameter	Conditions	f_{HCLK}	Typ (1) T_A = 105℃	Unit
I_{DD}	Supply current in Operating mode	External clock (2), Enable all peripherals	48MHz	9.04	mA
			24MHz	5.75	
			8MHz	3.03	
		External clock (2), Disable all peripherals	48MHz	5.38	
			24MHz	4.00	
			8MHz	2.60	

Note:

(1)Guaranteed by design and comprehensive evaluation, not tested in production.

(2)External clock, when f_{HCLK} is 24M or 48M, PLL needs to be enabled.

Table 4-9 Typical Current Consumption in RUN Mode, During Code Run in Embedded RAM

Symbol	Parameter	Conditions	f_{HCLK}	Typ (1) T_A = 105℃	Unit
I_{DD}	Supply current in RUN mode	External clock (2), Enable all peripherals	48MHz	10.14	mA
			24MHz	5.77	
			8MHz	2.62	
		External clock (2), Disable all peripherals	48MHz	6.21	
			24MHz	4.00	
			8MHz	2.10	

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Note:

(1)Guaranteed by design and comprehensive evaluation, Tested in production with maximal V_{DD} and maximal f_{HCLK}.

(2)External clock, when f_{HCLK} is 24M or 48M, PLL needs to be enabled.

Table 4-10 Typical Current Consumption in SLEEP Mode during Code Run in Embedded Flash Running

Symbol	Parameter	Conditions	f_{HCLK}	Typ (1) T_A = 105℃	Unit
I_{DD}	Supply current in SLEEP mode	External clock (2), Enable all peripherals	48MHz	7.06	mA
			24MHz	4.21	
			8MHz	2.14	
		External clock (2), Disable all peripherals	48MHz	3.08	
			24MHz	2.23	
			8MHz	1.41	

Note:

(1)Guaranteed by design and comprehensive evaluation, not tested in production.

(2)External clock, when f_{HCLK} is 24M or 48M, PLL needs to be enabled.

(3)When ADC is enabled, there is a current of 1.1mA (guaranteed by design).

Table 4-11 Typical Consumption in PD Mode and STOP Mode

Symbol	Parameter	Conditions	Typ (1)	Max	Unit
			V_{DD}=3.3V	V_{DD}=3.3V	
Low power mode	Current in SLEEP mode	The core is stopped, all peripherals including Cortex®-M0 core peripherals, such as NVIC, system tick clock (SysTick) is still running)	3.10	5	mA
	Current in STOP mode	Turn off RTC, SRAM data retention, all I/O status retention, register retention	2.60	25	uA
	Current in PD mode	V_{DD} power-down mode, 3 WAKEUP IO and NRST can wake up the chip	0.414	1	uA

Note:

(1)The typical value/maximum value is tested under T_A=25℃.

4.3.5.2 Typical current consumption

The device is under the following conditions:

- All I/O pins are in input mode and connected to a static level—V_{DD} or V_{SS} (no load).
- All peripherals are disabled except otherwise noted.
- The access time of Flash memory is adjusted to the frequency of f_{HCLK} (0~18MHz is 0 waiting period, 18~36MHz is 1 waiting period, and more than 36MHz is 2 waiting periods).
- Instruction prefetch is enabled (Note: this parameter must be set before setting the clock and bus divider).
- When the peripheral is enable: f_{PCLK1}= f_{HCLK}, f_{PCLK2} = f_{HCLK}, f_{ADCCLK} = f_{PCLK2}/3.

The parameter given in Table 4-12 and Table 4-13 are based on tests at the ambient temperature and VDD supply voltage listed in Table 4-4.

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Table 4-12 Typical Current Consumption in RUN Mode during Code execution from Embedded Flash

Symbol	Parameter	Conditions	f_{HCLK}	Typ(1)		Unit
				Enable all peripherals(2)	Disable all peripherals	
I_{DD}	Current in Operating mode	External high-speed clock (HSE), use AHB prescaler to reduce the frequency	48MHz	8.94	5.23	mA
			24MHz	5.35	3.49	
			8MHz	2.80	2.17	
		Internal high-speed RC oscillator (2) (HSI), using AHB prescaler to reduce the frequency	48MHz	8.21	4.57	mA
			24MHz	4.84	3.05	
			8MHz	2.27	1.65	

Note:

(1)The typical value is obtained by testing at T_A=25℃ V_{DD}=3.3V.

(2)The internal high-speed clock is 8MHz, and PLL is enabled when f_{HCLK} > 8MHz.

Table 4-13 Typical Current Consumption in SLEEP mode,during Code execution in Embedded Flash or RAM

Symbol	Parameter	Conditions	f_{HCLK}	Typ(1)		Unit
				Enable all peripherals(2)	Disable all peripherals	
I_{DD}	Current in SLEEP mode	External high-speed clock (HSE), use AHB prescaler to reduce the frequency	48MHz	6.92	3.00	mA
			24MHz	4.12	2.07	
			8MHz	1.93	1.27	
		Internal high-speed RC oscillator (2) (HSI), using AHB prescaler to reduce the frequency	48MHz	6.13	2.27	mA
			24MHz	3.37	1.45	
			8MHz	1.30	0.65	

Note:

(1)The typical value is obtained by testing at T_A=25℃ V_{DD}=3.3V.

(2)The internal high-speed clock is 8MHz, and PLL is enabled when f_{HCLK} > 8MHz.

4.3.6 External Clock Source Characteristics

4.3.6.1 High-speed External Clock Source (HSE)

The characteristic parameters in the following table are measured using a high-speed external clock source.

The ambient temperature and supply voltage meet the conditions specified in Table 4-4.

Table 4-14 High-speed External Clock Characteristics (Bypass Mode)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSE_ext}	External high-speed clock frequency	-	4	8	20	MHz
V_{HSEH}	OSC_IN input pin high level voltage (1)		$0.7V_{DD}$	-	V_{DD}	V
V_{HSEL}	OSC_IN input pin low-level voltage (1)		V_{SS}	-	$0.3V_{DD}$	
$t_{w(HSE)}$ $t_{w(HSE)}$	OSC_IN high or low time (1)		16	-	-	ns
$t_{r(HSE)}$ $t_{f(HSE)}$	OSC_IN rise or fall time (1)		-	-	20	
$C_{in(HSE)}$	OSC_IN input capacitive reactance (1)		-	5	-	pF
$DuCy_{(HSE)}$	Duty cycle		45	-	55	%
I_L	OSC_IN input leakage current (1)	$V_{SS} \le V_{IN} \le V_{DD}$	-	-	±1	μA

Note:

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(1)Guaranteed by design and comprehensive evaluation, not tested in production.

4.3.6.2 Low-speed External Clock Source (LSE)

The characteristic parameters in the following table are measured using a low-speed external clock source.

The ambient temperature and supply voltage meet the conditions specified in Table 4-4.

Table 4-15 Low-speed External Clock Characteristics (Bypass Mode)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSE_ext}	External low-speed clock frequency	-	0	32.768	1000	KHz
V_{LSEH}	OSC32_IN input pin high level voltage (1)		$0.7V_{DD}$	-	V_{DD}	V
V_{LSEL}	OSC32_IN input pin low-level voltage (1)		V_{SS}	-	$0.3V_{DD}$	
$t_{w(LSE)}$ $t_{w(LSE)}$	OSC32_IN high or low time (1)		450	-	-	ns
$t_{r(LSE)}t_{f(LSE)}$	OSC32_IN rise or fall time (1)		-	-	10	
$DuCy_{(LSE)}$	Duty cycle (1)		30	-	70	%
I_L	OSC32_IN input leakage current (1)	$V_{SS}\leq V_{IN}\leq V_{DD}$	-	-	±1	μA

Note:

(1)Guaranteed by design and comprehensive evaluation, not tested in production.

Figure 4-5 AC Timing Diagram Of External High-speed Clock Source

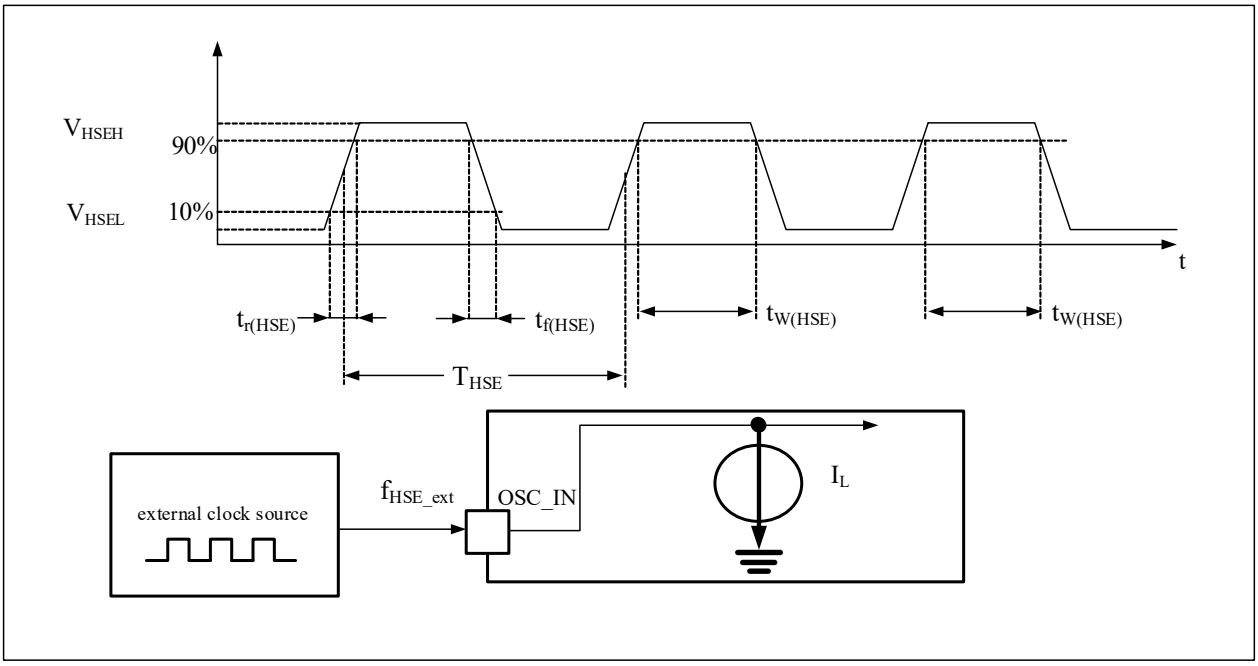

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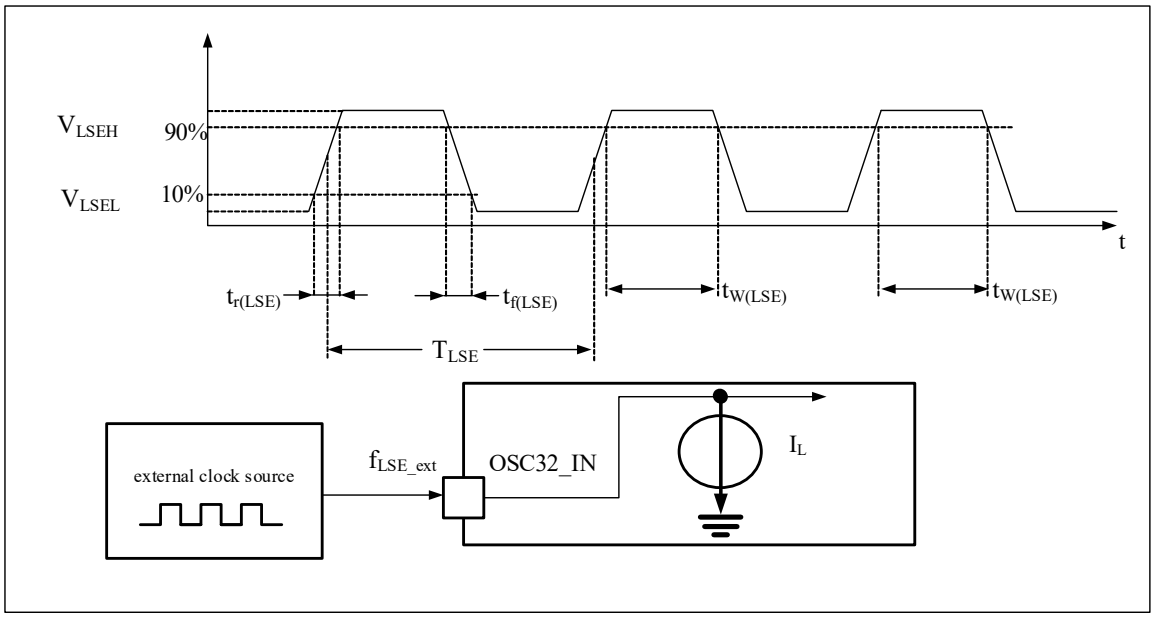
Figure 4-6 AC Timing Diagram of External Low-speed Clock Source



High-speed external clock generated by a crystal/ceramic resonator

The high-speed external clock (HSE) can be generated using a 4-20MHz crystal/ceramic resonator oscillator. The information presented in this section is based on a comprehensive feature evaluation using typical external components listed in the table below. In applications, the resonator and load capacitance must be as close to the oscillator pins as possible to reduce output distortion and stabilization time at startup. For detailed parameters (frequency, packaging, accuracy, etc.) of the crystal resonator, please consult the corresponding manufacturer. (The crystal resonator mentioned here is what we usually call passive crystal oscillator).

Table 4-16 HSE 4~20MHz Oscillator Characteristics (1)(2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{OSC_IN}	Oscillator frequency	-	4	8	20	MHz
$t_{SU(HSE)}$(3)	Startup Time	V_{DD} is stabilized, f_{out} = 20MHz	-	3	-	ms

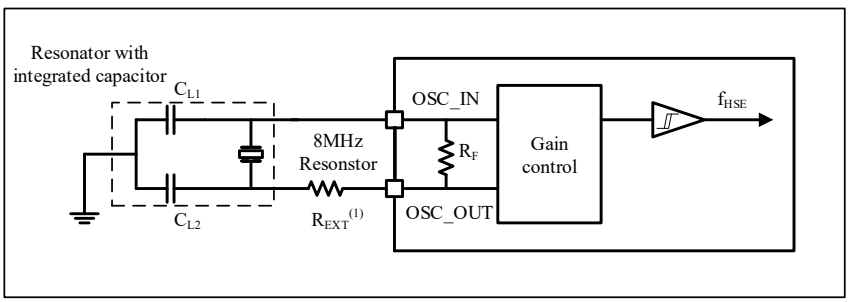
Note:

(1)The characteristic parameters of the resonator are given by the crystal/ceramic resonator manufacturer.

(2)Guaranteed by design and comprehensive evaluation, not tested in production.

(3)$t_{SU(HSE)}$ is the start-up time, which is the time from the software enabling HSE to start measurement until a stable 8MHz oscillation is obtained. This value is measured on a standard crystal resonator, and it may vary greatly depending on the crystal manufacturer.

Figure 4-7 Typical Application Using 8MHz Crystal



Note:

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(1)R_{EXT} value is determined by the characteristics of the crystal.

Low-speed external clock generated by a crystal/ceramic resonator

The Low-speed external clock (LSE) can be generated using a 32.768 kHz crystal/ceramic resonator oscillator. The information presented in this section is based on a comprehensive feature evaluation using typical external components listed in the table below. In applications, the resonator and load capacitance must be as close to the oscillator pins as possible to reduce output distortion and stabilization time at startup. For detailed parameters (frequency, packaging, accuracy, etc.) of the crystal resonator, please consult the corresponding manufacturer. (The crystal resonator mentioned here is what we usually call passive crystal oscillator).

Note: For C_{L1} and C_{L2}, it is recommended to use high-quality ceramic capacitors, and select a crystal or resonator that meets the requirements. Usually C_{L1} and C_{L2} have the same parameters. The crystal manufacturer usually gives the parameter of the load capacitance in the serial combination of C_{L1} and C_{L2}.

The load capacitance C_L is calculated by the following formula: $C_L = C_{L1} \times C_{L2} / (C_{L1} + C_{L2}) + Cstray$, where C_{stray} is the capacitance of the pin and the PCB or PCB-related capacitance.

Table 4-17 LSE Oscillator Characteristics (f_{LSE}=32.768 kHz) (1)

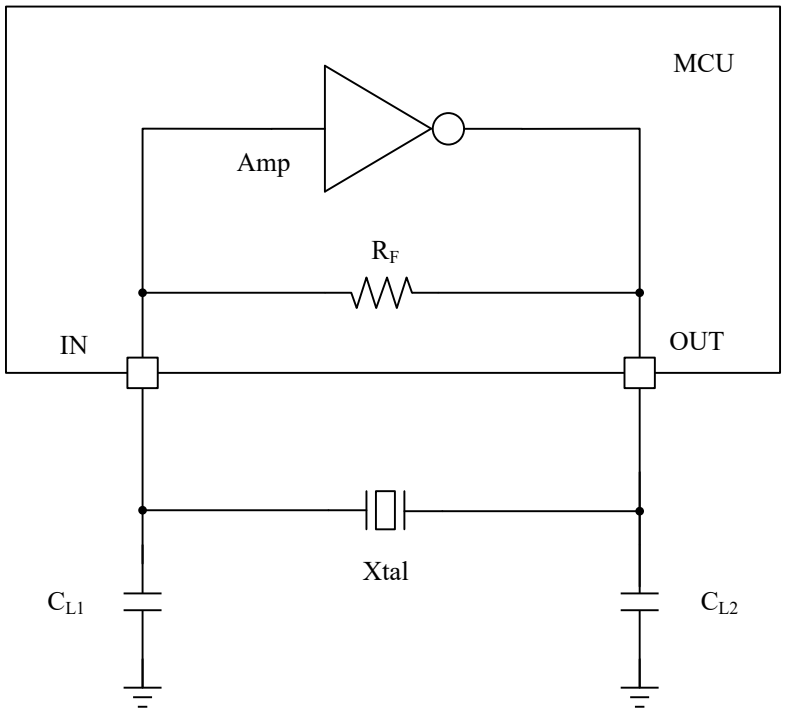
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{SU(LSE)}$(2)	Startup Time	V_{DD} is stabilized	-	2	-	s

Note:

(1)Guaranteed by design and comprehensive evaluation, not tested in production.

(2)$t_{SU(LSE)}$ is the start-up time, which is the time from the software enabling LSE to start measurement until a stable 32.768KHz oscillation is obtained. This value is measured on a standard crystal resonator, and it may vary greatly depending on the crystal manufacturer.

Figure 4-8 Typical Application Using 32.768kH Crystal



4.3.7 Internal Clock Source Characteristics

The parameter test conditions in the following table are based on Table 4-4.

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4.3.7.1 High-speed internal (HSI) RC oscillator

Table 4-18 HSI Oscillator Characteristics (1) (2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI}	Frequency	V_{DD}=3.3V, T_A = 25℃, After calibration	7.92(3)	8	8.08(3)	MHz
DuCy (HSI)	Duty cycle		45	-	55	%
ACC_{HSI}	The temperature drift of the HSI oscillator(4)	V_{DD}=3.3V, T_A = -40~105℃, Temperature drift	-3	-	3	%
		V_{DD}=3.3V, T_A = -10~85℃, Temperature drift	-1	-	1	%
		V_{DD}=3.3V, T_A = 0~70℃, Temperature drift	-1	-	1	%
$t_{SU(HSI)}$	HSI startup Time		1	-	3	μs
$I_{DD(HSI)}$	HSI power consumption		-	80	150	μA

Note:

(1)Unless otherwise specified, V_{DD} = 3.3V, T_A = -40~105℃.

(2)Guaranteed by design and comprehensive evaluation, not tested in production.

(3)Production calibration accuracy, excluding welding effects. Welding brings about 1% frequency deviation range.

(4)Frequency deviation includes the effect of welding, data is from sample testing, not tested in production.

4.3.7.2 Low-speed internal (LSI) RC oscillator

Table 4-19 LSI Oscillator Characteristics (1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSI}(2)	Frequency	V_{DD}=3.3V, T_A = 25℃, After calibration	29	30	31	KHz
		VDD =1.8V ~5.5V, TA = -40~105℃	24	30	36	KHz
$t_{SU(LSI)}$ (2)	LSI Startup Time		-	30	80	μs
$I_{DD(LSI)}$ (2)	LSI driving current		-	0.2	-	μA

Note:

(1)Unless otherwise specified, V_{DD} = 3.3V, T_A = -40~105℃.

(2)Guaranteed by design and comprehensive evaluation, not tested in production.

4.3.8 Low-power Mode Wake-up Time

The wake-up time listed in Table 4-20 is measured during the wake-up phase of an 8MHz HSI RC oscillator. The clock source used when waking up depends on the current operating mode:

- STOP or PD mode: the clock source is RC oscillator
- SLEEP mode: the clock source is the clock used when entering SLEEP mode

All times were measured using ambient temperature and supply voltage in accordance with Table 4-4.

Table 4-20 Low-power Mode Wake-up Time

Symbol	Parameter	Typ	Unit
$t_{WUSLEEP}$ (1)	Wake up from SLEEP mode	16	HCLK(2)
t_{WUSTOP} (1)	Wake up from STOP mode	20	us

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t_{WUPD} (1)	Wake up from PD mode	55	

Note:

(1)The measurement of the wake-up time is from the start of the wake-up event to the user program reading the first instruction.

(2)HCLK is the AHB frequency.

4.3.9 PLL Characteristics

The parameters listed in **Error! Reference source not found.** are measured when the ambient temperature and power s upply voltage meet the conditions in Table 4-4.

Table 4-21 PLL Characteristics

Symbol	Parameter	Num			Unit
		Min	Typ	Max(1)	
f_{PLL_IN}	PLL input clock(2)	4	8.0	20	MHz
	PLL input clock duty cycle	40	-	60	%
f_{PLL_OUT}	PLL multiplier output clock	48	-	72	MHz
t_{LOCK}	PLL Ready indicates signal output time	-	-	20	µs
Jitter	TIE RMS Jitter	-	40	-	pS
I_{pll}	Operating Current of PLL @48MHz VCO frequency.	-	300	500	uA

Note:

(1)Guaranteed by design and comprehensive evaluation, not tested in production.

(2)Need to pay attention to using the correct frequency multiplication factor, so that f_{PLL_OUT} is within the allowable range according to the PLL input clock frequency.

4.3.10 FLASH Characteristics

Unless otherwise specified, all characteristic parameters are obtained at T_A = -40~105℃.

Table 4-22 Flash Characteristics

Symbol	Parameter	Conditions	Min(1)	Typ(1)	Max(1)	Unit
tprog	Word programming time(32-bit)	T_A = -40~105℃	-	175	-	µs
t_{ERASE}	Page erase time(512Bytes)	T_A = -40~105℃	-	2.27	-	ms
t_{ME}	Mass erase time	T_A = -40~105℃;	-	34.1	-	ms
I_{DD}	Current(1)	Read, f_{HCLK}=48MHz, V_{DD}=3.3V	-	2	2.4	mA
		Write, f_{HCLK}=48MHz, V_{DD}=3.3V	-	-	1.2	mA
		Erase, f_{HCLK}=48MHz, V_{DD}=3.3V	-	-	0.6	mA
		Deep STANDBY mode, V_{DD}=3.3~3.6V	-	-	150	µA

Note:

(1)Guaranteed by design and comprehensive evaluation, not tested in production.

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Table 4-23 Flash Endurance and Data Retention Period

Symbol	Parameter	Conditions	Min(1)	Unit
N_{END}	Endurance(Note: erasing and writing cycle)	T_A = -40~105°C	100	kcycles
t_{RET}	Data retention	T_A = 105°C, after 1000 erasing cycle(1)	10	years

Note:

(1)Guaranteed by design and comprehensive evaluation, not tested in production.

4.3.11 Electrical Sensitivity

Based on three different tests (ESD, LU), a specific measurement method is used to test the strength of the chip to determine its performance in terms of electrical sensitivity.

Electrostatic Discharge (ESD)

Electrostatic discharge (a positive pulse followed by a negative pulse one second later) is applied to all pins of all samples.

Table 4-24 Absolute Maximum ESD Value

Symbol	Parameter	Conditions	Class	Max(1)	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A = +25 °C, In accordance with MIL-STD-883K Method 3015.9	2	4000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charging device model)	T_A = +25 °C, In accordance with ESDA/JEDEC JS-002-2018	II	1000	

Note:

(1) Guaranteed by design and comprehensive evaluation, not tested in production.

Static switch lock

To evaluate the locking performance, two complementary static latch-up tests were performed on six samples:

- Supply voltage exceeding limit for each power pin.
- Current is injected into each input, output, and configurable I/O pin.

This test conforms to EIA/JESD78E IC latch standard.

Table 4-25 Electrical Sensitivity

Symbol	Parameter	Conditions	Class
LU	Static locking classes	T_A = +105 °C, conforming to JESD78E	II level A

4.3.12 I/O Port Characteristics

General Input/Output Characteristics

Unless otherwise specified, the parameters listed in the following table are measured according to the conditions in Table 4-4. All I/O ports are CMOS and TTL compatible.

Table 4-26 I/O Static Characteristics

Symbol	Parameter	VDD	Conditions	Min	Max	Unit
V_{IL}	IO Low level input voltage	5	-	-	0.3×VDD	V
		3.3	-	-	0.8	
		1.8	-	-	0.2×VDD	

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V_{IH}	IO High level input voltage	5	-	0.7×VDD	-	
		3.3	-	2.0	-	
		1.8	-	0.8×VDD	-	
V_{hys}	I/O Schmitt trigger voltage hysteresis (1)	5/3.3/1.8	-	0.1×VDD	---	V
I_{lkg}(2)	Input leakage current IIH	5/3.3/1.8	-	---	+1	µA
	Input leakage current IIL	5/3.3/1.8	-	-1	-	
V_{OH}	Output high level voltage	5	High driving I_{min}=16mA low driving I_{min} =8mA	VDD-0.8	-	V
		3.3	High driving I_{min} =8mA low driving I_{min} =4mA	2.4	-	
		1.8	High driving I_{min} =4mA low driving I_{min} =2mA	VDD-0.45	-	
V_{OL}	Output low level voltage	5	High driving I_{min} =16mA low driving I_{min} =8mA	-	0.7	
		3.3	High driving I_{min} =8mA low driving I_{min} =4mA	-	0.45	
		1.8	High driving I_{min} =4mA low driving I_{min} =2mA	-	0.4	
R_{PU}	Weak pull-up equivalent resistor	5/3.3/1.8	-	50	100	kΩ
R_{PD}	Weak pull-down equivalent resistor	5/3.3/1.8	-	50	100	kΩ
C_{IO}	I/O pin capacitance	5/3.3/1.8	-	-	10	pF

Note:

(1) The hysteresis voltage of the Schmitt trigger switching level. Guaranteed by design and comprehensive evaluation, not tested in production.

(2)If there is negative current in the adjacent pin, the leakage current may be higher than the maximum value.

Input and Output AC Characteristics

Unless otherwise specified, the parameters listed in Table 4-27 were measured using ambient temperature and supply voltage in accordance with Table 4-4.

Table 4-27 I/O AC Characteristics

VDD	Conditions			Rise/Fall Time (ns)			Propagation Delay (ns)		
	Driving Strength	Slew Rate Control	$C_{Loading}$(pf)	Min	Typ	Max	Min	Typ	Max
5V (4.5~5.5)	Low (DR=1)	Slow (SR=1)	25	3.1	3.9	6.5	5	7.2	14
			50	5.7	6.5	11	6.5	8.8	16

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VDD	Conditions			Rise/Fall Time (ns)			Propagation Delay (ns)		
	Driving Strength	Slew Rate Control	$C_{Loading}$(pf)	Min	Typ	Max	Min	Typ	Max
3.3V (2.7~3.6)			100	11	13	20	10	12	21
		Fast (SR=0)	25	2.9	3.4	5.4	4.5	6.5	12
			50	5.6	6.3	10	6	8.1	14.2
			100	11	12.3	19.5	9	11.3	19.1
	High (DR=0)	Slow (SR=1)	25	1.8	2.5	4.1	4.2	6.7	13
			50	3	3.9	6.2	5	7.5	15
			100	5.6	6.5	10.2	6.4	9	17
		Fast (SR=0)	25	1.6	2.1	3.4	3.7	5.9	12
			50	2.9	3.5	5.5	4.4	6.6	13
			100	5.5	6.2	10	5.9	8	15
	Low (DR=1)	Slow (SR=1)	25	4	5.5	11	6.6	10	20
			50	7.5	9.5	18	8.5	12	24
			100	15	17	32	13	16	31
		Fast (SR=0)	25	3.8	4.9	9.2	5.9	8.8	18
			50	7.3	8.8	16.2	7.8	10.8	21.2
			100	14.2	16.7	30.5	12	15	29
	High (DR=0)	Slow (SR=1)	25	2.4	3.7	7.2	5.5	8.5	17.1
			50	3.9	5.5	10.5	6.5	9.6	19.2
			100	7.3	9.3	17.2	8.4	12	23
		Fast (SR=0)	25	2	3.1	5.9	4.9	7.6	16
			50	3.7	4.9	9.5	5.8	8.7	18
			100	7.2	8.8	17	7.7	11	22
1.8V (1.62~1.98)	Low (DR=1)	Slow (SR=1)	25	8	12	22	14	23	44
			50	15	20	36	18	27	52
			100	29	36	65	26	36	66
		Fast (SR=0)	25	7.5	10.5	16.4	12.25	20	40
			50	14.5	18.5	33	16.5	24.2	47
			100	28	35	62	24	33	62
	High (DR=0)	Slow (SR=1)	25	4.6	8	15.4	12	20.2	40
			50	7.6	11.8	22	14	22.5	44
			100	11.5	19.5	36	17.5	26.7	52
		Fast (SR=0)	25	4	6.9	14	10.5	18	36
			50	7.3	11	20	12.3	20	40

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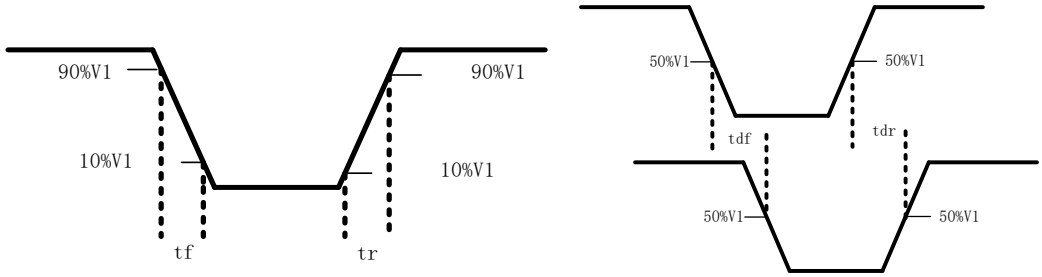
VDD	Conditions			Rise/Fall Time (ns)			Propagation Delay (ns)		
	Driving Strength	Slew Rate Control	$C_{Loading}$(pf)	Min	Typ	Max	Min	Typ	Max
			100	15	18.5	33	16	25	47

Figure 4-9 I/O AC Characteristic Definition



4.3.13 NRST Pin Characteristics

The NRST pin is integrated with pull-up resistor. Unless otherwise specified, the parameter test conditions in the following table are based on Table 4-4.

Table 4-28 NRST Pin Characteristics

Symbol	Parameter	VDD	Min	Typ	Max	Unit
$V_{IL(NRST)}$(1)	NRST low level input voltage	1.8V~5.5V	-	-	0.3VDD	V
$V_{IH(NRST)}$(1)	NRST high level input voltage	1.8V~5.5V	0.75VDD	-	-	
$V_{hys(NRST)}$	NRST schmitt trigger voltage hysteresis	1.8V~5.5V	115	220	315	mV
R_{PU}	Weak pull-up equivalent resistor (2)	1.8V~5.5V	30	40	50	kΩ
$V_{F(NRST)}$(1)	NRST input filter pulse	1.8V~2V	-	-	100	ns
		3V~3.6V	-	-	100	
		4.5V~5.5V	-	-	50	
$V_{NF(NRST)}$(1)	NRST input unfiltered pulse	1.8V~2V	650	-	-	ns
		3V~3.6V	300	-	-	
		4.5V~5.5V	200	-	-	

Note:

(1)Guaranteed by design, note tested in production

(2)The pull-up resistor is designed as true resistor for a not switchable PMOS implementation, the resistance of this PMOS switch is very small (about 10%).

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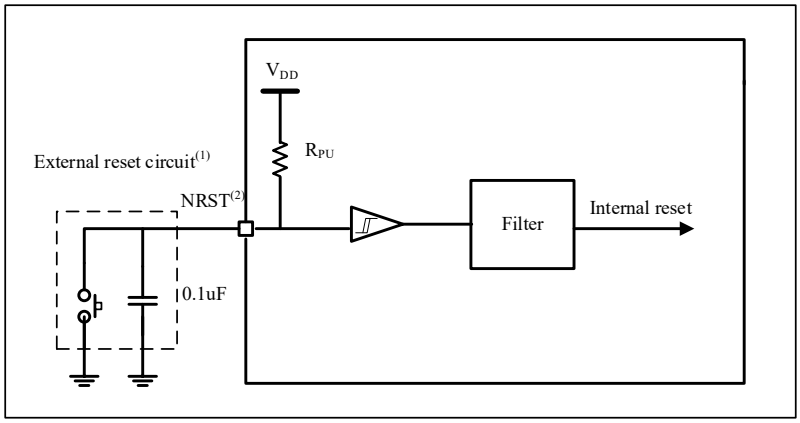
Figure 4-10 NRST Pin Protection Recommended Circuit Design



Note:

(1)The reset network is to prevent parasitic reset.

(2)The user must ensure that the potential of the NRST pin can be lower than the maximum $V_{IL\ (NRST)}$, otherwise the MCU cannot be reset.

4.3.14 Timer Characteristics

Table 4-29 Timer (1) Characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{res(TIM)}$	Timer resolution time	$f_{TIMxCLK}$= 48MHz	1	-	$t_{TIMxCLK}$
		$f_{TIMxCLK}$= 48MHz	20.8	-	ns
f_{EXT} (2)	Timer external clock frequency on CH1 to CH4	-	0	$f_{TIMxCLK}$/2	MHz
		$f_{TIMxCLK}$= 48MHz	0	24	MHz
Res_{TIM}	Timer resolution	$f_{TIMxCLK}$= 48MHz	-	16	bit
$t_{COUNTER}$	Select the internal clock, 16-bit counter clock cycle	$f_{TIMxCLK}$= 48MHz	1	65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$= 48MHz	0.0208	1365	μs
t_{MAX_COUNT}	Maximum count	$f_{TIMxCLK}$= 48MHz	-	65536x65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$= 48MHz	-	89.478	s

Note:

(1)Timer is generic name, representing TIM~TIM8

(2)Only applicable to advanced timers and general-purpose timers, not applicable to basic timers.

4.3.15 I2C Interface Characteristics

Unless otherwise specified, the parameters listed in **Error! Reference source not found.30** were measured using a mbient temperature, f_{PCLK1} frequency, and V_{DD} supply voltage in accordance with Table 4-4.

The I2C interface complies with the standard I2C communication protocol.

But SDA and SCL are not "true" open-drain pins. When configured as open-drain output, the PMOS tube between the pin and VDD is turned off, but it still exists.

Table 4-30 I2C Interface Characteristics

Symbol	Parameter	Standard model		Fast mode		Fast+ mode		Unit
		Min	Max	Min	Max	Min	Max	
f_{SCL}	I2C interface frequency	0	100	0	400	0	1000	KHz

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$th_{(STA)}$	Start condition holding time (1)	4.0	-	0.6	-	0.26	-	μs
$tw_{(SCLL)}$	SCL Clock Low Time (1)	4.7	-	1.3	-	0.5	-	μs
$tw_{(SCLH)}$	SCL clock high time (1)	4.0	-	0.6	-	0.26	-	μs
$tsu_{(STA)}$	Setup time of repeated starting conditions (1)	4.7	-	0.6	0.6	0.26	-	μs
$th_{(SDA)}$	SDA data hold time (1)	-	3.4	-	0.9	-	0.4	μs
$tsu_{(SDA)}$	Setup time of SDA (1)	250.0	-	100	-	50	-	ns
$tr_{(SDA)}$ $tr_{(SCL)}$	SDA and SCL rising time (1)	-	1000	20+0.1 Cb	300	-	120	ns
$tf_{(SDA)}$ $tf_{(SCL)}$	SDA and SCL falling time (1)	-	300	20+0.1 Cb	300	-	120	ns
$tsu_{(STO)}$	Stop condition setup time(1)	4.0	-	0.6	-	0.26	-	μs
$tw_{(STO:STA)}$	Time from stop condition to start condition (bus idle) (1)	4.7	-	1.3	-	0.5	-	μs
C_b	Capacity load per bus (1)	-	400	-	400	-	100	pf
$tv_{(SDA)}$	Data validity time(1)	3.45	-	0.9	-	0.45	-	μs
$tv_{(ACK)}$	Response validity time (1)	3.45	-	0.9	-	0.45	-	μs

Note:

(1)Guaranteed by design and comprehensive evaluation, not tested in production.

(2)To achieve the maximum frequency of standard mode I2C, f_{PCLK1} must be greater than 2MHz.To achieve the maximum frequency of fast mode I2C, f_{PCLK1} must be greater than 4MHz.

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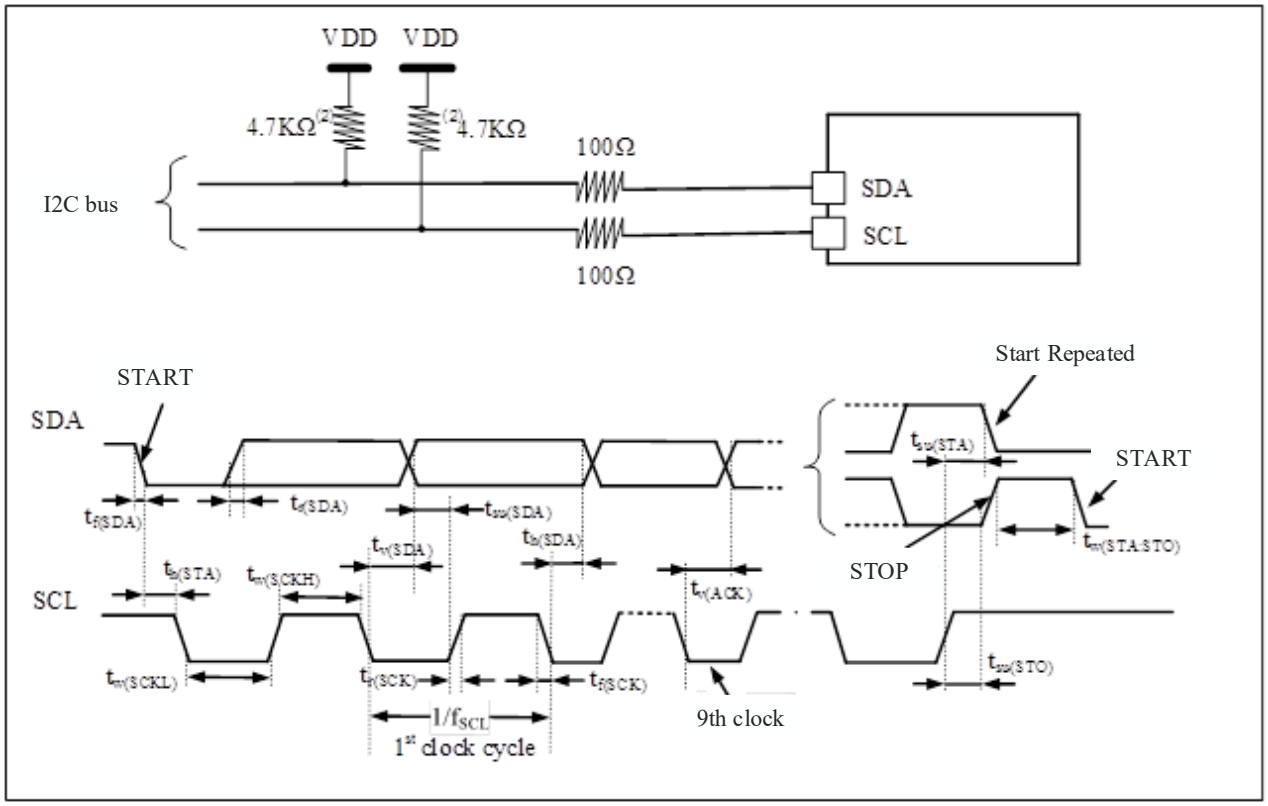
Figure 4-11 I2C Bus AC Waveform and Measurement Circuit (1)



Note:

(1)The measuring point is set at the CMOS level: $0.3V_{DD}$ and $0.7V_{DD}$.

4.3.16 SPI/I2S Interface Characteristics

Unless otherwise specified, the SPI parameters listed in Table 4-31 is measured using ambient temperature, fPCLKx frequency, and VDD supply voltage in accordance with Table 4-4.

Table 4-31 SPI Characteristics (4)

Symbol	Parameter	Conditions		Min	Max	Unit
f_{SCLK} $1/t_{c(SCLK)}$	SPI clock frequency	Master mode		-	18	MHz
		Slave mode		-	18	
$t_{r(SCLK)}t_{f(SCLK)}$	SPI clock rising and falling time	Load capacitance: C = 30pF		-	15	ns
DuCy(SCK)	SPI slave input clock duty cycle	SPI Slave mode		45	55	%
$t_{su(NSS)}$ (1)	NSS setup time	Slave mode		$4t_{PCLK}$	-	ns
$t_{h(NSS)}$(1)	NSS hold time	Slave mode		$2t_{PCLK}$	-	ns
$t_{w(SCLKH)}$(1) $t_{w(SCLKL)}$(1)	SCLK high and low time	Master mode		t_{PCLK}	t_{PCLK} + 2	ns
$t_{su(MI)}$(1)	Data entry setup time	Master mode	SPI1	19.84	-	ns
			SPI2	20.5	-	
$t_{su(SI)}$(1)		Slave mode	SPI1	4.16	-	
			SPI2	4.16	-	
$t_{h(MI)}$(1)	Data entry hold time	Master mode		0	-	ns

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$t_{h(SI)}^{(1)}$		Slave mode	4	-	
$t_{a(SO)}^{(1)(2)}$	Data output access time	Slave mode, f_{PCLK} = 18MHz	0	$3t_{PCLK}$	ns
$t_{dis(SO)}^{(1)(3)}$	Disabled time for data output	Slave mode	2	10	ns
$t_{v(SO)}^{(1)}$	Valid time of data output	Slave mode (after the enabled edge) SPI1	-	32	ns
		Slave mode (after the enabled edge) SPI2	-	30	
$t_{v(MO)}^{(1)}$		Master mode (after the enabled edge) SPI1	-	28	
		Master mode (after the enabled edge) SPI2	-	28	
$t_{h(SO)}^{(1)}$	Data output hold time	Slave mode (after the enabled edge)	0	-	ns
$t_{h(MO)}^{(1)}$		Master mode (after the enabled edge)	0	-	

Note:

(1)Guaranteed by design and comprehensive evaluation, not tested in production.

(2)The minimum value means the minimum time to drive the output, and the maximum value means the maximum time to get the data correctly.

(3)The minimum value means the minimum time to turn off the output, and the maximum value means the maximum time to put the data wire in the high resistance state.

(4)Test voltage is 3.3V.

Figure 4-12 SPI Sequence Diagram - Slave Mode and CPHA=0

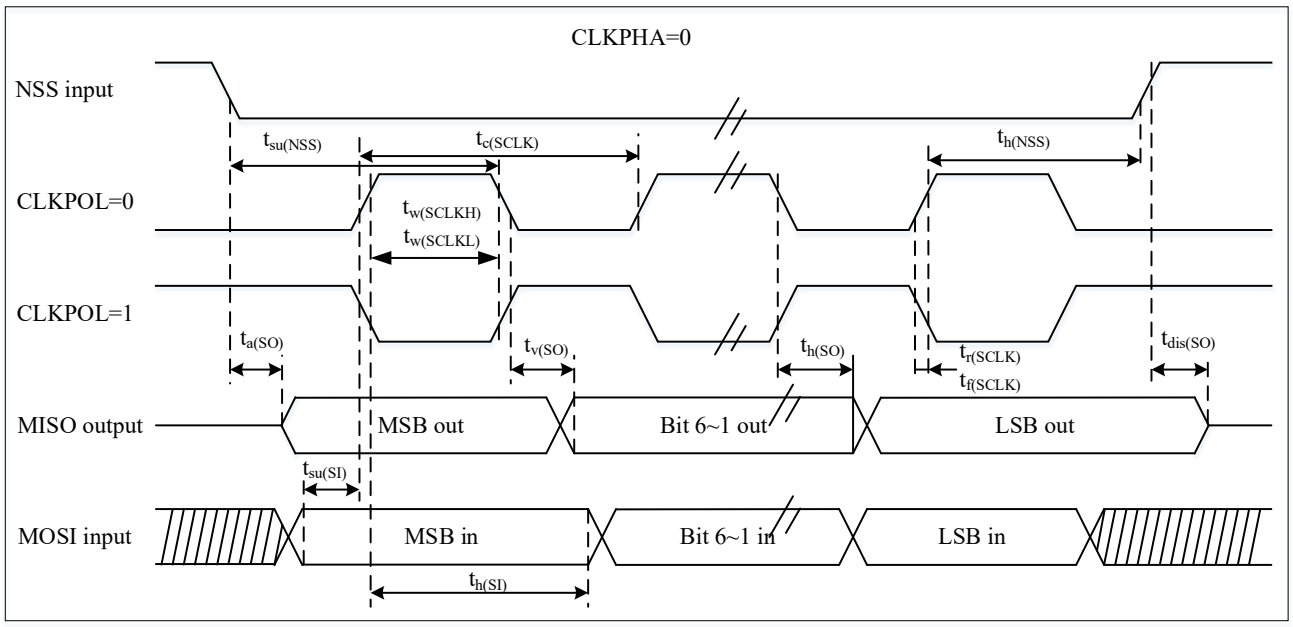

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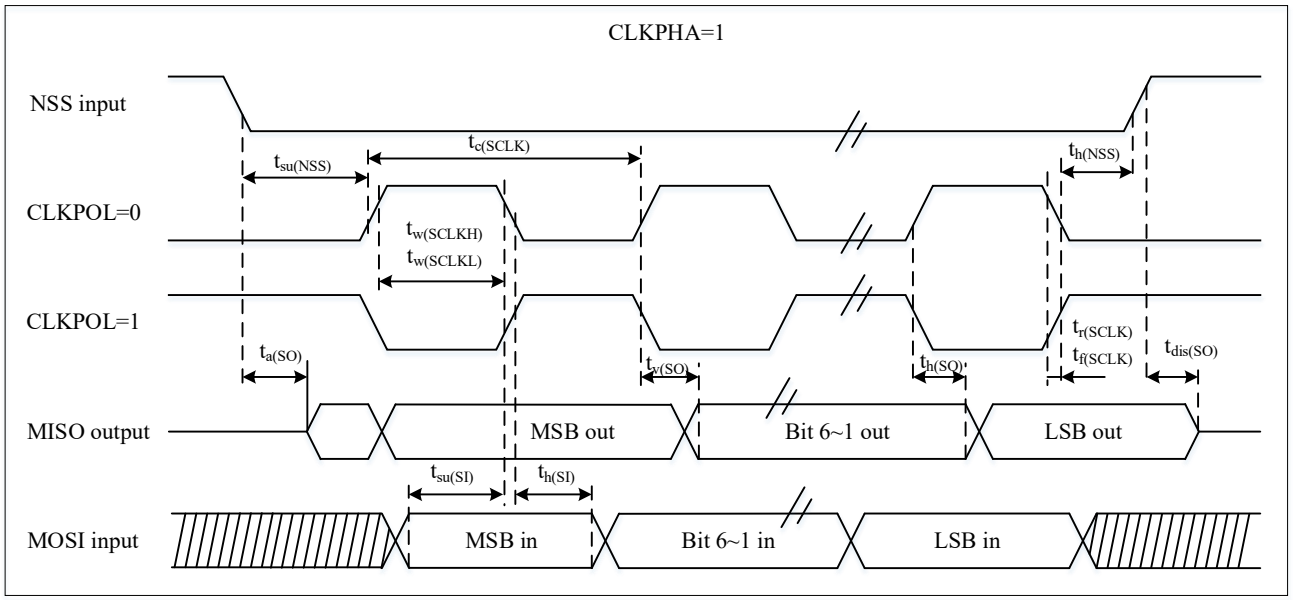
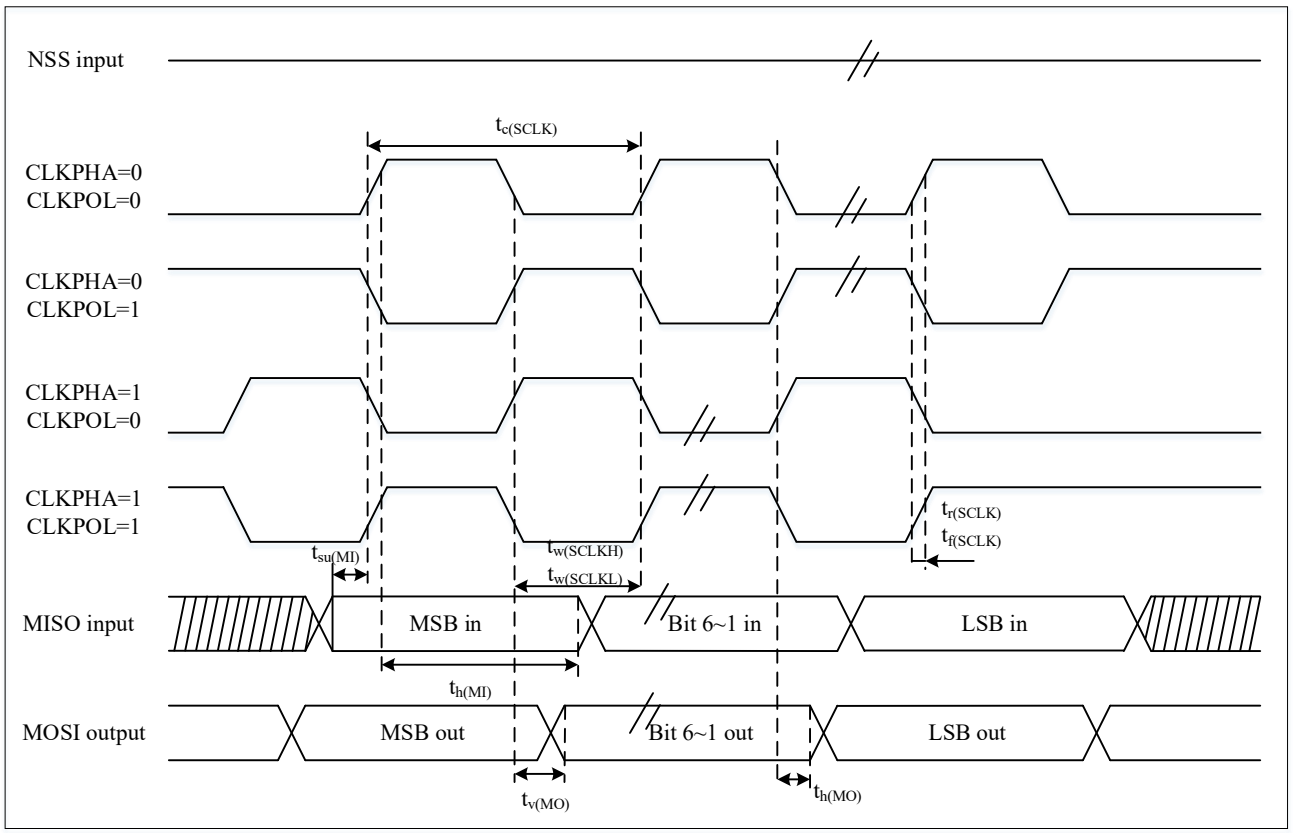
Figure 4-13 SPI Timing Diagram - Slave Mode and CPHA=1(1)



Note:

(1)The measurement points were set at the CMOS level of 0.3 V_{DD} and 0.7 V_{DD}.

Figure 4-14 SPI Timing Diagram-Master Mode (1)



Note:

(1)The measurement points are set at CMOS level: 0.3 V_{DD} and 0.7 V_{DD}.

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Table 4-32 I2S Characteristics (1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
DuCy(SCK)	I2S clock duty cycle	I2S Slave mode	30	50	70	%
f_{CLK} $1/t_{c(CLK)}$	I2S clock frequency	Master mode (16bit)	-	2*Fs(3)*16	-	Hz
		Slave mode (16bit)	-	2*Fs(3)*16	-	
		Master mode (32bit)	-	2*Fs(3)*32	-	
		Slave mode (32bit)	-	2*Fs(3)*32	-	
$t_{r(CLK)}$	I2S clock rising and falling time	Load capacitance: C_L = 50pf	-	-	8	ns
$t_{v(WS)}$ (1)	WS validity time	Master mode	13.5	-	-	
$t_{h(WS)}$(1)	WS hold time	Master mode	0	-	-	
$t_{su(WS)}$ (1)	WS setup time	Slave mode	4	-	-	
$t_{h(WS)}$(1)	WS hold time	Slave mode	0	-	-	
$t_{w(CLKH)}$(1)	CLK high and low time	Master mode, fpclk = 16mhz, audio 48khz	312.5	-	-	
$t_{w(CLKL)}$(1)			345	-	-	
$t_{su(SD\_MR)}$(1)	Data entry setup time	Master receiver	3.6	-	-	
$t_{su(SD\_SR)}$(1)		Slave receiver	3.5	-	-	
$t_{h(SD\_MR)}$(1)(2)	Data entry hold time	Master receiver	0	-	-	
$t_{h(SD\_SR)}$(1)(2)		Slave receiver	0	-	-	
$t_{v(SD\_ST)}$(1)(2)	Valid time of data output	Slave transmitter (after the enabled edge)	-	-	29.76	ns
$t_{h(SD\_ST)}$(1)	Data output hold time	Slave generator(after the enabled edge)	0	-	-	
$t_{v(SD\_MT)}$(1)(2)	Valid time of data output	Master generator(after the enabled edge)	-	-	13.6	
$t_{h(SD\_MT)}$(1)	Data output hold time	Master generator(after the enabled edge)	-6.5	-	-	

Note:

(1)Guaranteed by design and comprehensive evaluation, not tested in production.

(2)Relying on f_{PCLK}.For example, if f_{PCLK}=8MHz, then T_{PCLK}=1/ f_{PCLK} =125ns.

(3)F_S value audio sampling frequency, frequency range 8 KHz ~ 96 KHz.

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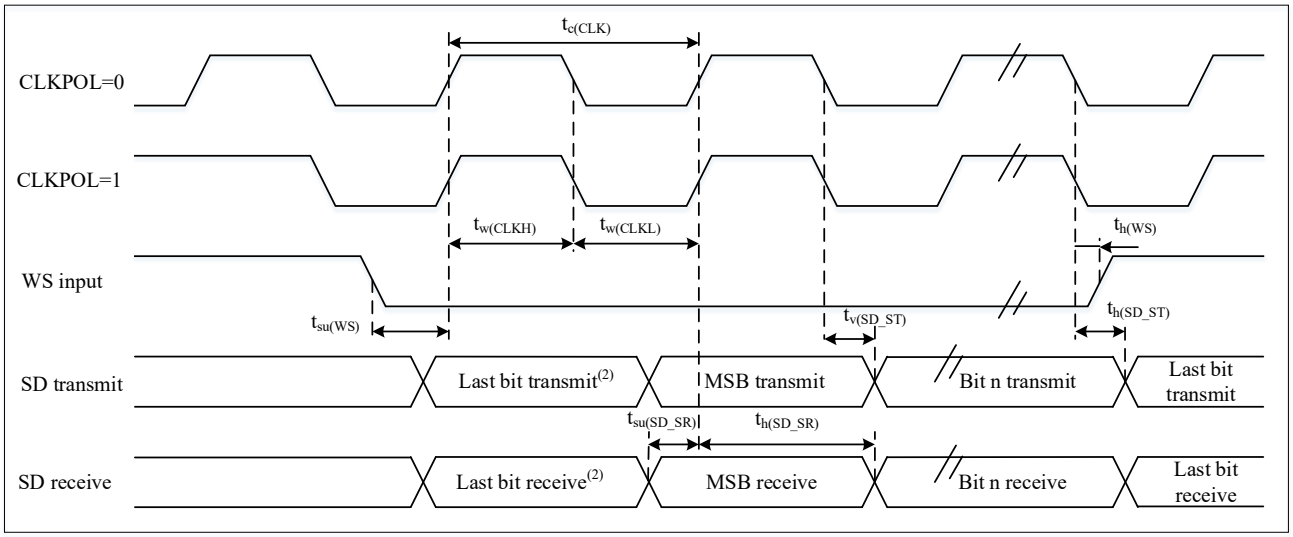
Figure 4-15 I2S Slave Mode Timing Diagram (Philips Protocol) (1)

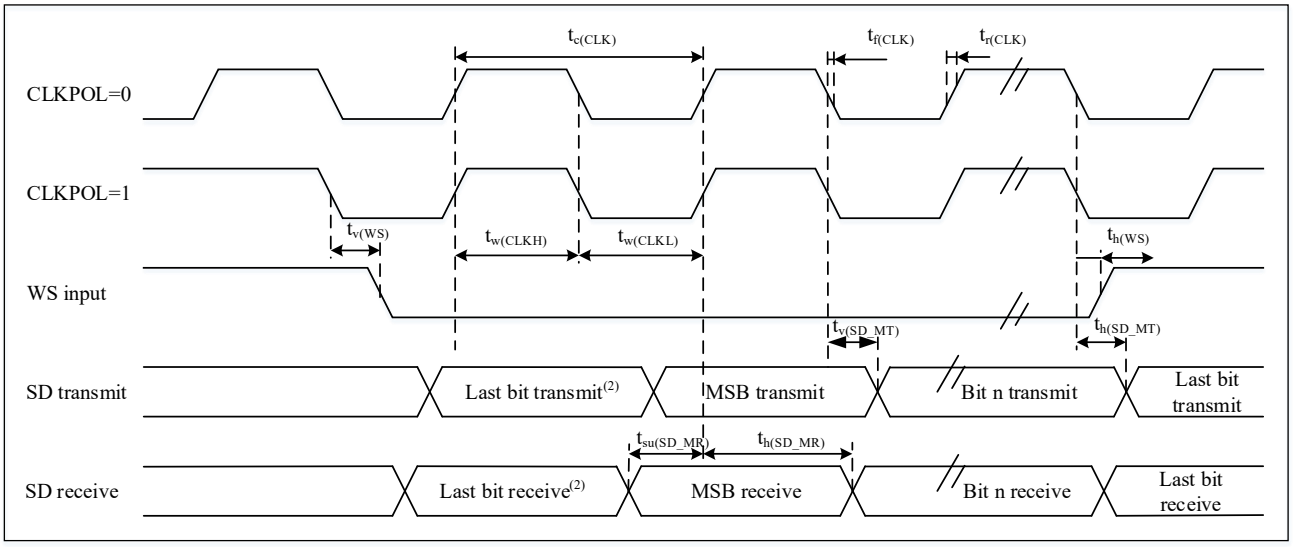


Note:

(1)The measuring point is set at the CMOS level: 0. 3V_{DD} and 0. 7V_{DD}.

(2)Transmit/receive of the last byte. There is no transmit/receive of this least significant bit before the first byte.

Figure 4-16 I2S Master Mode Timing Diagram (Philips Protocol) (1)



Note:

(1)The measuring point is set at the CMOS level: 0. 3V_{DD} and 0. 7V_{DD}.

(2)Transmit/receive of the last byte. There is no transmit/receive of this last bit before the first byte.

4.3.17 ADC Characteristics

Unless otherwise specified, the parameters in Table 4-33 are measured using ambient temperature, f_{HCLK} frequency, and V_{DDA} supply voltage in accordance with the conditions in Table 4-4.

Table 4-33 ADC Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}(1)	Supply voltage	-	2.4	3.3	5.5	V
V_{REF+}	Positive reference voltage	-	2.4	-	V_{DDA}	V

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f_{ADC}	ADC clock frequency	-	-	-	18	MHz
f_s(1)	Sampling rate	-	0.03	-	1	Msps
V_{AIN}	Conversion voltage range	-	0	-	V_{REF+}	V
R_{AIN}(1)	External input impedance	-	See formula 1			Ω
R_{ADC}(1)	ADC input resistance	V_{DDA} =3.0v	-	1500	-	Ω
C_{ADC}(1)	Internal sample and hold capacitor	-	-	13	15	pF
SNDR	Signal noise distortion ration	V_{DDA} =3.3v	-	68	-	dB
T_S (1)	Sampling cycle	-	6	-	-	$1/f_{ADC}$
t_{STAB} (1)	Power-on time	-	32	-	-	$1/f_{ADC}$
t_{CONV} (1)	Conversion time	-	12			$1/f_{ADC}$

Note:

(1)Guaranteed by design and comprehensive evaluation, not tested in production.

Formula 1: Maximum R_{AIN} formula

$$R_{AIN} < \frac{T_S}{f_{ADC} \times C_{ADC} \times \ln(2^{N+2})} - R_{ADC}$$

The above formula (Formula 1) is used to determine the maximum external impedance so that the error can be less than 1/4 LSB. Where N=12 (representing 12-bit resolution).

Table 4-34 ADC Accuracy (1)

Symbol	Parameter	Conditions	Typ	Max(2)	Unit
EG	Gain error	V_{REF+} = 3.3V, T_A = 25 °C, sample rate = 1MSPS, Vin = 0.05V_{DDA} ~ 0.95V_{DDA}	±2	±5	LSB
EO	Offset error		±0.5	±2.0	
ED	Differential linearity error		±0.6	1.5	
EL	Integral linearity error		±1.5	2.5	
ENOB	Effective number of bits		11	-	Bits

Note:

(1)The relationship between the negative injection current and ADC accuracy: the need to avoid negative current is injected on any standard analog input pin, as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (between the pin and ground) on the standard analog pin that may produce negative injection current.

(2)Guaranteed by design and comprehensive evaluation, not tested in production.

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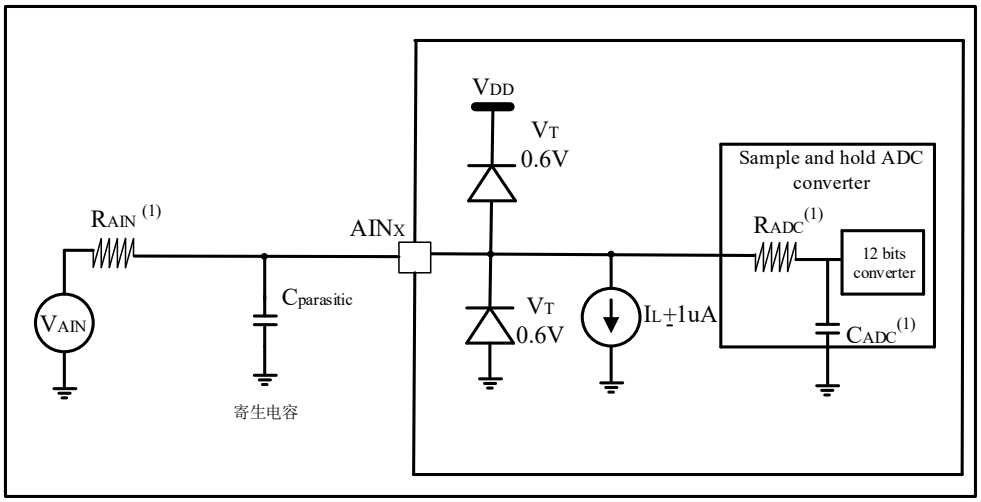
Figure 4-17 ADC Typical Connection Diagram



4.3.18 Internal Reference Source (VREFP) Characteristics

Unless otherwise specified, the parameters in Table 4-35 are measured using ambient temperature, f_{HCLK} frequency and V_{DDA} supply voltage in accordance with the conditions in Table 4-4.

Table 4-35 V_{REFP} Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage	Normal mode	2.7	-	5.5	V
V_{REFP}	Voltage reference source	Normal mode	2.364	2.4	2.436	V
I_{DDA}(1)	V_{REFP} consumption from V_{DDA}	I_{load} = 0 μA	-	1000	-	μA
Load cap(1)	Load capacitance				25	pF
t_{START}(1)	Start-up time	-	5	-	-	μs

Note:

(1)Guaranteed by design, not tested in production.

4.3.19 OPAMP Characteristics

Unless otherwise specified, the parameters in Table 4-36 are measured using ambient temperature, f_{HCLK} frequency, and V_{DDA} supply voltage in accordance with the conditions in Table 4-4.

Table 4-36 OPAMP Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VDDA	Analog supply voltage	-	2.9	-	5.5	V
CMIR	Common mode voltage input range	-	0	-	V_{DDA}	V
$V_{IOFFSET}$	Input offset voltage	-	-10	4	10	mV
I_{LOAD}	Drive current	-	-	0.5	-	mA
I_{DDA}	OPAMP current consumption	No load, quiescent mode	-	0.5	-	mA
CMMR	Common mode rejection ratio	-	-	70	-	dB
PSRR	Power supply rejection ratio	-	-	60	-	dB
GBW	Gain bandwidth	-	-	2.5	-	MHz

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SR	Slew rate	-		3	-	V/us
R_{LOAD}	Minimum impedance load	-	10	-	-	KΩ
C_{LOAD}	Maximum capacitive load	-	-	-	25	pF
$T_{STARTUP}$	Startup time	CLOAD ≤ 25 pf, RLOAD ≥ 10 kΩ, Follower configuration	-	3	5	μs
PGA BW	PGA bandwidth for different non inverting gain	PGA Gain = 2, Cload = 25pF, Rload = 10 KΩ	-	1	-	MHz
		GA Gain = 4, Cload = 25pF, Rload = 10 KΩ	-	0.5	-	
		GA Gain = 16, Cload = 25pF, Rload = 10 KΩ	-	0.125	-	
		GA Gain = 32, Cload = 25pF, Rload = 10 KΩ	-	0.0625	-	

Note:

(1)Guaranteed by design and comprehensive evaluation, not tested in production.

4.3.20 COMP Characteristics

Unless otherwise specified, the parameters in Table 4-37 are measured using ambient temperature, f_{HCLK} frequency, and V_{DDA} supply voltage in accordance with the conditions in Table 4-4.

Table 4-37 COMP characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage	-		2.2	-	5.5	V
V_{IN}	Input voltage range	-		0	-	V_{DDA}	
T_{START}	Comparator startup time	normal mode		-	-	5	us
		low speed mode				15	
t_d	Propagation delay for 200 mV step with 100 mV overdrive	V_{DDA}>=2.2Vnormal mode		-	100		ns
		low speed mode			520		
V_{OFFSET}	Comparator input offset error	Full common mode range		-	±4	±20	mV
V_{hys}	Comparison of hysteresis voltage (high speed/low power consumption)	No hysteresis		-	0	-	mV
		Low hysteresis		-	10/8	-	
		Medium hysteresis		-	20/15	-	
		High hysteresis		-	30/25	-	
I_{DDA}	Comparator current consumption	High speed mode. Comparator is turned on, reference input compare voltage source is turned off(2)	Static	-	35	-	μA
			With 50 kHz ±100 mV overdrive square signal	-	36	-	
		Low speed	Static	-	5	-	

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		mode. Comparator is turned on, reference input compare voltage source is turned off[2]	With 50 kHz ±100 mV overdrive square signal	-	6	-	

Notes:

[1]Guaranteed by design and comprehensive evaluation, not tested in production.

[2]For reference input compare voltage source, the static power is 671μA (guaranteed by design), the maximum configurable voltage is V_{DDA}

4.3.21 Temperature Sensor Characteristics

Unless otherwise specified, the parameters in Table 4-38 are measured using ambient temperature, f_{HCLK} frequency, and V_{DDA} supply voltage in accordance with the conditions in Table 4-4.

Table 4-38 Temperature Sensor Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
T_L[1]	Linearity of V_{SENSE} with respect to temperature	-	±2	-	ºC
Avg_Slope[1]	Average slope	-	3.9	-	mV/ºC
V_{25}[1]	Voltage at 25ºC	-	1.3	-	V
t_{START}[1]	Startup time	-	11	22	μs
T_{S_temp}[1][2]	ADC sampling time when reading the temperature	-	1.87	6.43	μs

Notes:

[1]Guaranteed by design and comprehensive evaluation, not tested in production.

[2]The shortest sampling time is obtained through multiple loops in the application.

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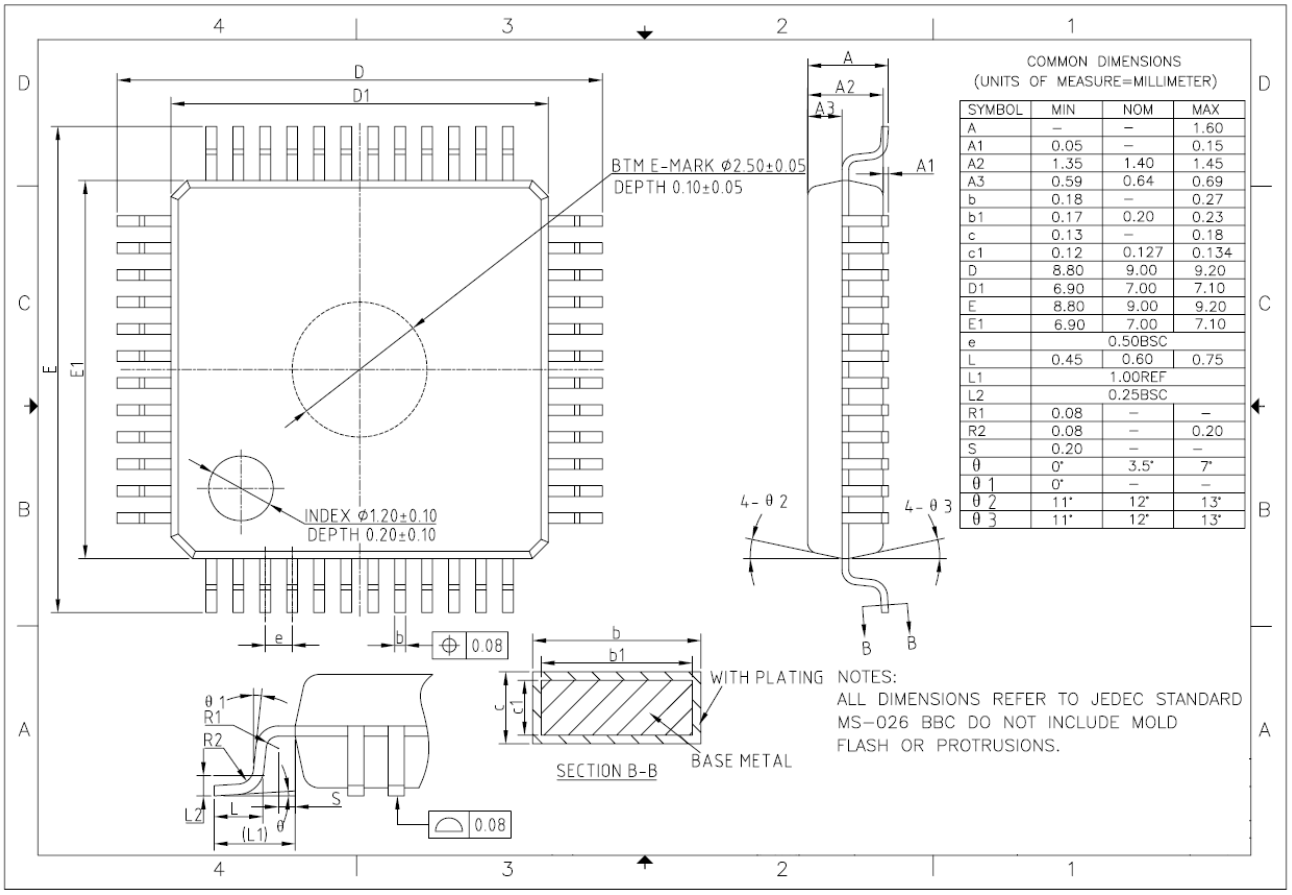
5 Packages

5.1 LQFP48(7mm x 7mm)

Figure 5-1 LQFP48(7mm x 7mm) Package Dimensions



SYMBOL	MIN	NOM	MAX
A	–	–	1.60
A1	0.05	–	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.18	–	0.27
b1	0.17	0.20	0.23
c	0.13	–	0.18
c1	0.12	0.127	0.134
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
e		0.50BSC	
L	0.45	0.60	0.75
L1		1.00REF	
L2		0.25BSC	
R1	0.08	–	–
R2	0.08	–	0.20
S	0.20	–	–
θ	0°	3.5°	7°
θ1	0°	–	–
θ2	11°	12°	13°
θ3	11°	12°	13°

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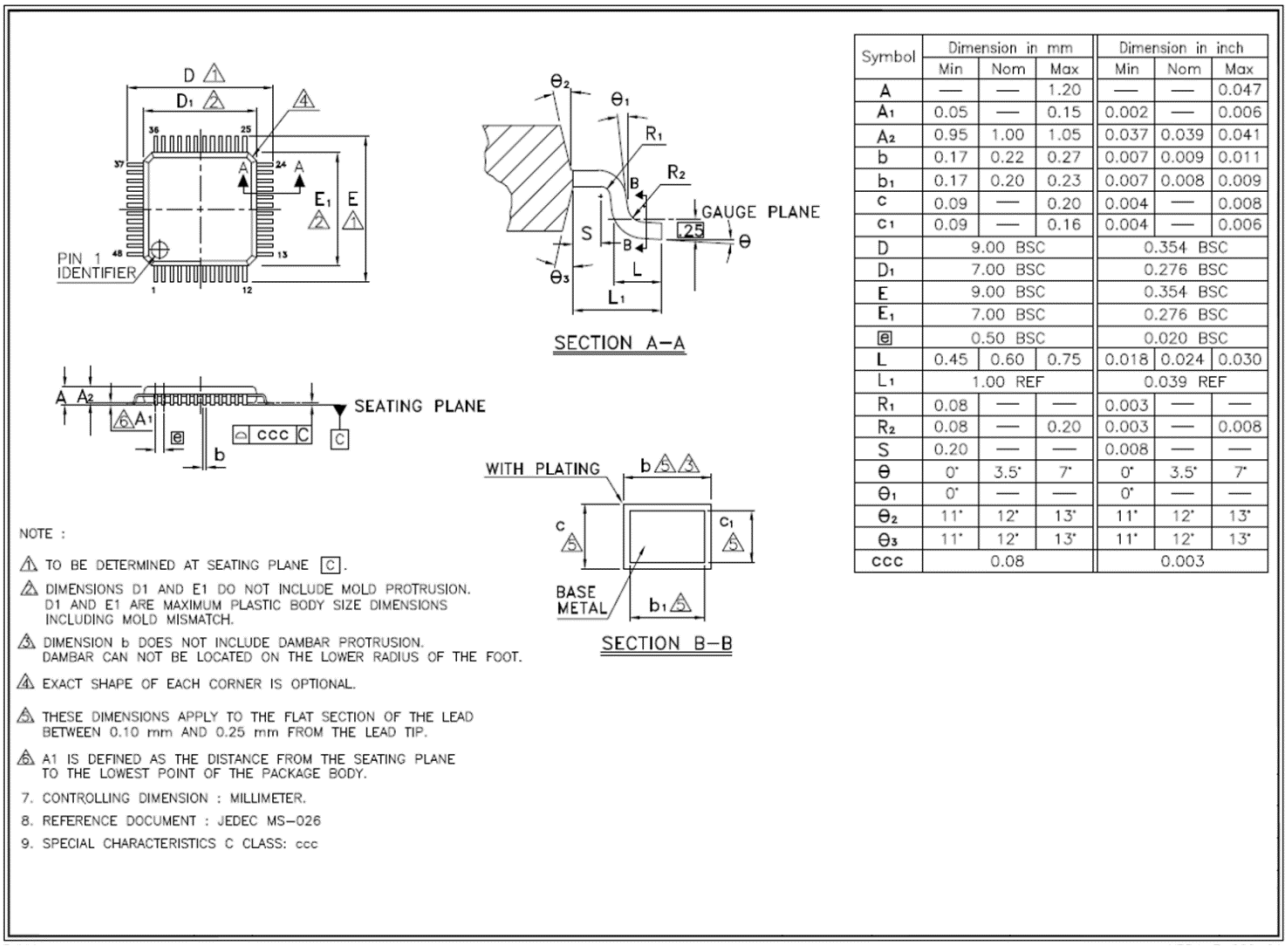
5.2 TQFP48(7mm x 7mm)

Figure 5-2 TQFP48(7mm x 7mm) Package Dimensions



Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	—	—	1.20	—	—	0.047
A_1	0.05	—	0.15	0.002	—	0.006
A_2	0.95	1.00	1.05	0.037	0.039	0.041
b	0.17	0.22	0.27	0.007	0.009	0.011
b_1	0.17	0.20	0.23	0.007	0.008	0.009
c	0.09	—	0.20	0.004	—	0.008
c_1	0.09	—	0.16	0.004	—	0.006
D	9.00 BSC			0.354 BSC		
D_1	7.00 BSC			0.276 BSC		
E	9.00 BSC			0.354 BSC		
E_1	7.00 BSC			0.276 BSC		
e	0.50 BSC			0.020 BSC		
L	0.45	0.60	0.75	0.018	0.024	0.030
L_1	1.00 REF			0.039 REF		
R_1	0.08	—	—	0.003	—	—
R_2	0.08	—	0.20	0.003	—	0.008
S	0.20	—	—	0.008	—	—
θ	0°	3.5°	7°	0°	3.5°	7°
$θ_1$	0°	—	—	0°	—	—
$θ_2$	11°	12°	13°	11°	12°	13°
$θ_3$	11°	12°	13°	11°	12°	13°
ccc	0.08			0.003		

NOTE :

1. TO BE DETERMINED AT SEATING PLANE C.
2. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT.
4. EXACT SHAPE OF EACH CORNER IS OPTIONAL.
5. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 mm AND 0.25 mm FROM THE LEAD TIP.
6. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.
7. CONTROLLING DIMENSION : MILLIMETER.
8. REFERENCE DOCUMENT : JEDEC MS-026
9. SPECIAL CHARACTERISTICS C CLASS: ccc

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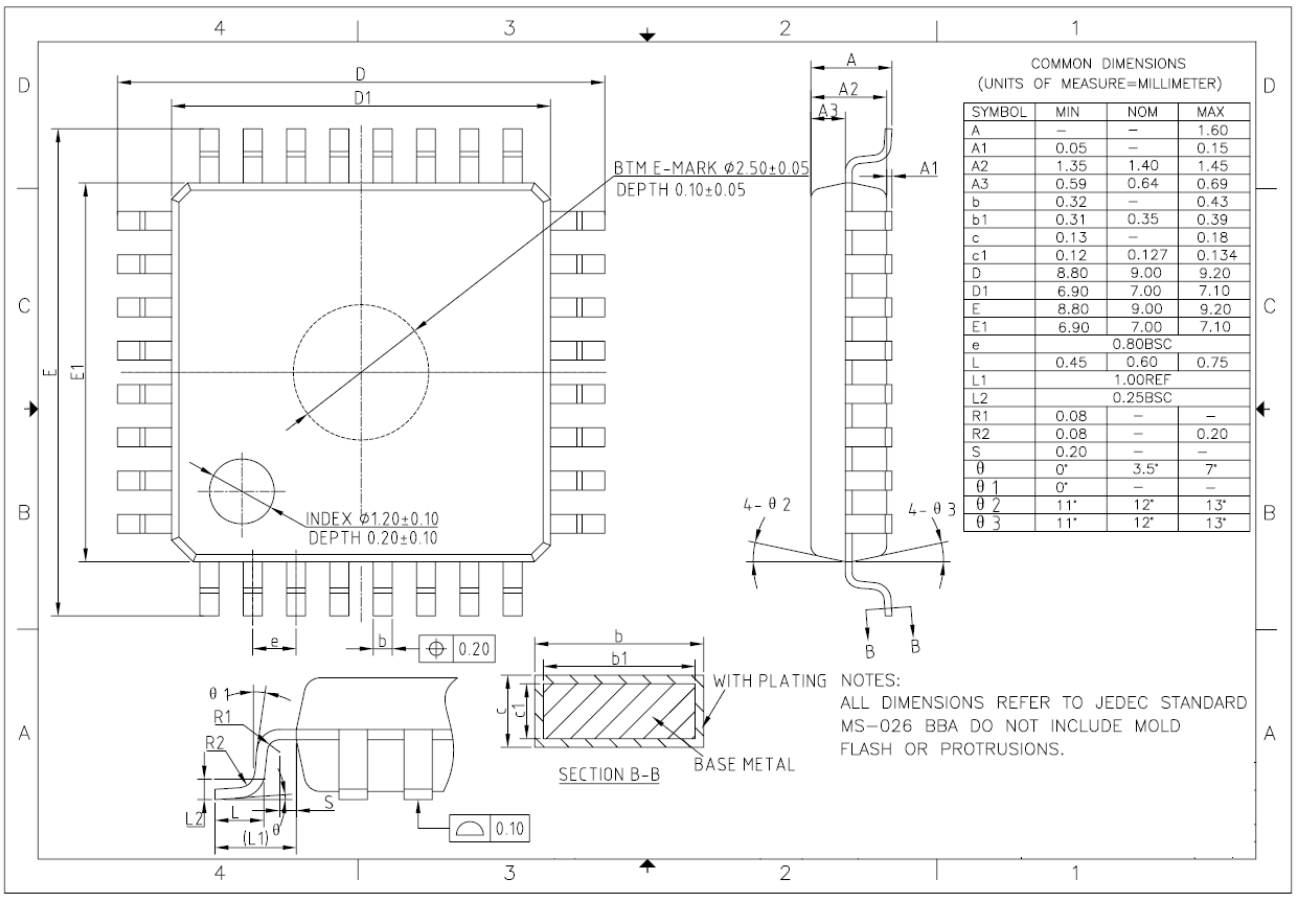
5.3 LQFP32(7mm x 7mm)

Figure 5-3 LQFP32(7mm x 7mm) Package Dimensions



SYMBOL	MIN	NOM	MAX
A	–	–	1.60
A1	0.05	–	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.32	–	0.43
b1	0.31	0.35	0.39
c	0.13	–	0.18
c1	0.12	0.127	0.134
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
e		0.80BSC	
L	0.45	0.60	0.75
L1		1.00REF	
L2		0.25BSC	
R1	0.08	–	–
R2	0.08	–	0.20
S	0.20	–	–
θ	0°	3.5°	7°
θ1	0°	–	–
θ2	11°	12°	13°
θ3	11°	12°	13°

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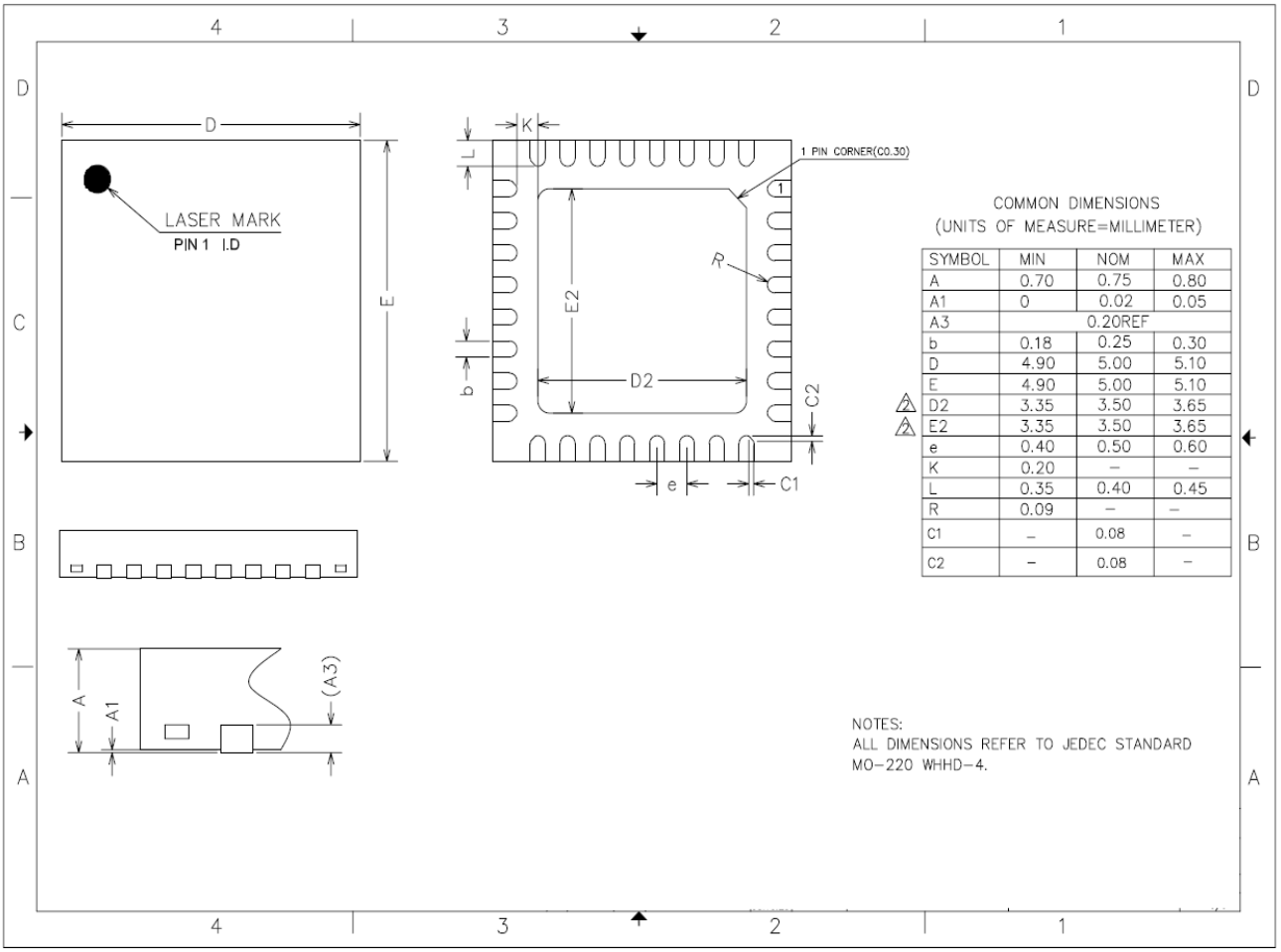
5.4 QFN32(5mm x 5mm)

Figure 5-4 QFN32 (5mm x 5mm) Package Dimensions



SYMBOL	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0	0.02	0.05
A3		0.20REF	
b	0.18	0.25	0.30
D	4.90	5.00	5.10
E	4.90	5.00	5.10
D2	3.35	3.50	3.65
E2	3.35	3.50	3.65
e	0.40	0.50	0.60
K	0.20	–	–
L	0.35	0.40	0.45
R	0.09	–	–
C1	–	0.08	–
C2	–	0.08	–

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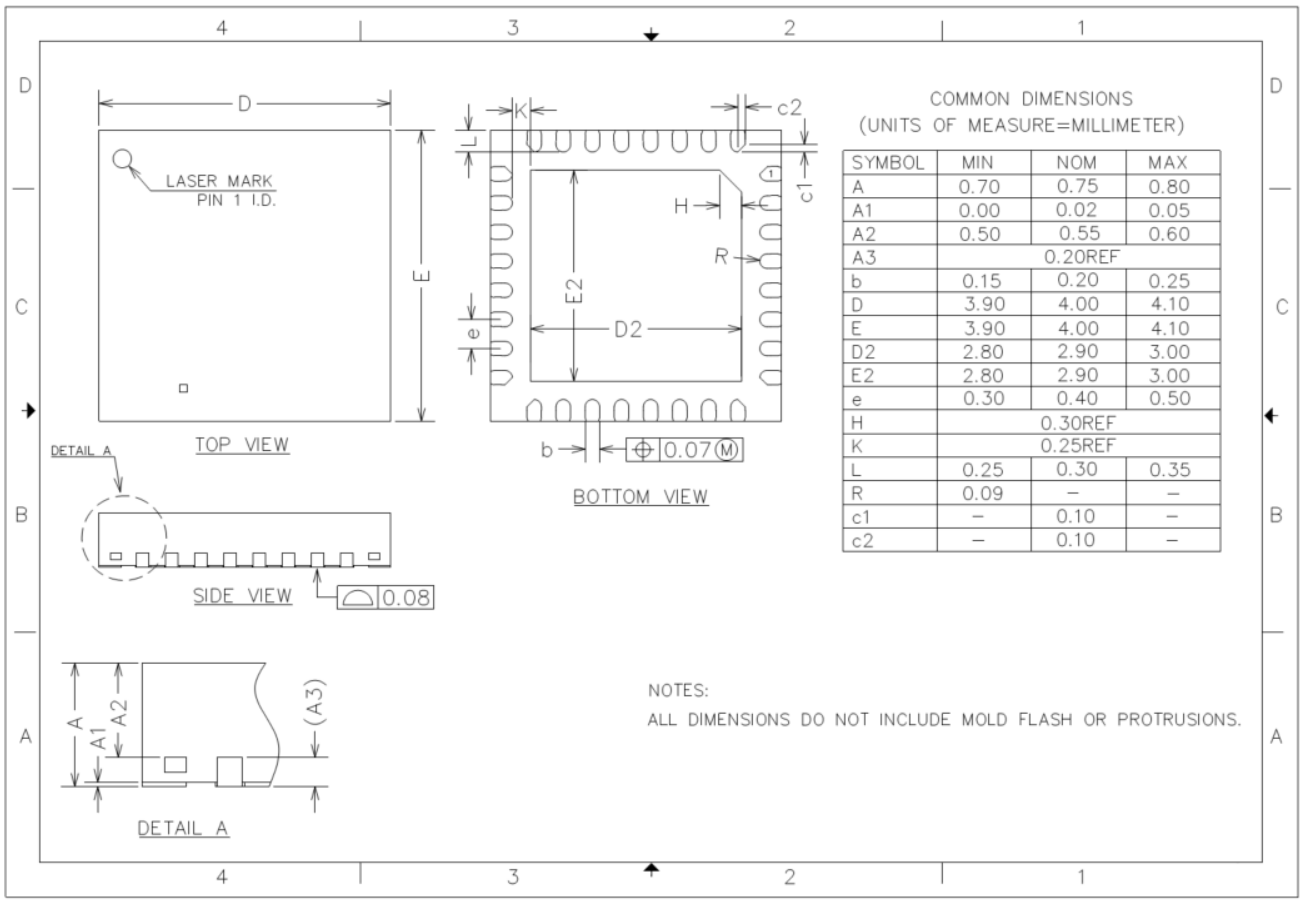
5.5 QFN32(4mm x 4mm)

Figure 5-5 QFN32 (4mm x 4mm) Package Dimensions



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A2	0.50	0.55	0.60
A3		0.20REF	
b	0.15	0.20	0.25
D	3.90	4.00	4.10
E	3.90	4.00	4.10
D2	2.80	2.90	3.00
E2	2.80	2.90	3.00
e	0.30	0.40	0.50
H		0.30REF	
K		0.25REF	
L	0.25	0.30	0.35
R	0.09	–	–
c1	–	0.10	–
c2	–	0.10	–

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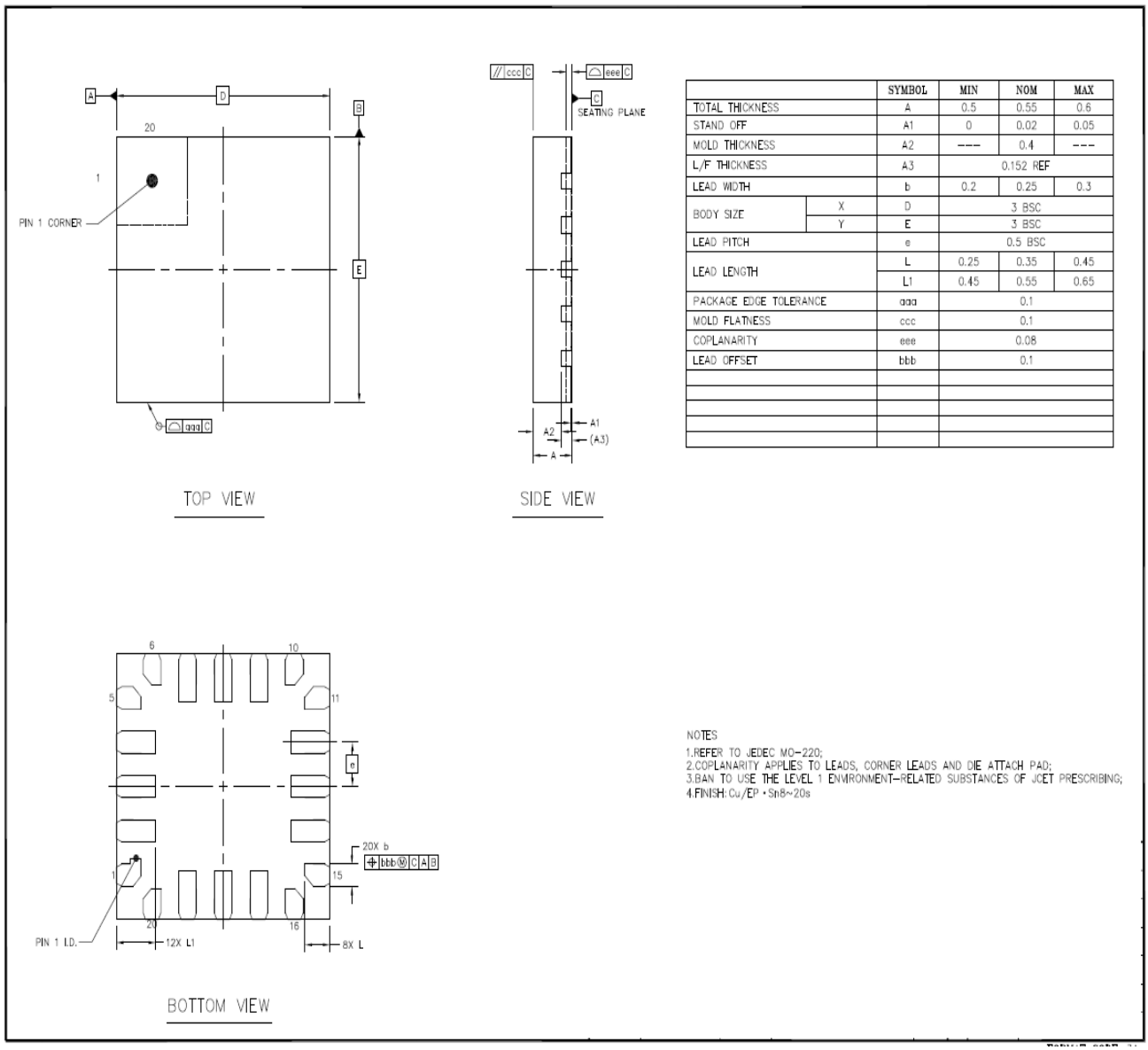
5.6 UFQFPN20(3mm x 3mm)

Figure 5-6 UFQFPN20(3mm x 3mm) Package Dimensions



		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.5	0.55	0.6
STAND OFF		A1	0	0.02	0.05
MOLD THICKNESS		A2	---	0.4	---
L/F THICKNESS		A3		0.152 REF	
LEAD WIDTH		b	0.2	0.25	0.3
BODY SIZE	X	D		3 BSC	
	Y	E		3 BSC	
LEAD PITCH		e		0.5 BSC	
LEAD LENGTH		L	0.25	0.35	0.45
		L1	0.45	0.55	0.65
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		ccc		0.1	
COPLANARITY		eee		0.08	
LEAD OFFSET		bbb		0.1	

NOTES
1.REFER TO JEDEC MO-220;
2.COPLANARITY APPLIES TO LEADS, CORNER LEADS AND DIE ATTACH PAD;
3.BAN TO USE THE LEVEL 1 ENVIRONMENT-RELATED SUBSTANCES OF JCET PRESCRIBING;
4.FINISH: Cu/EP • Sn8~20s

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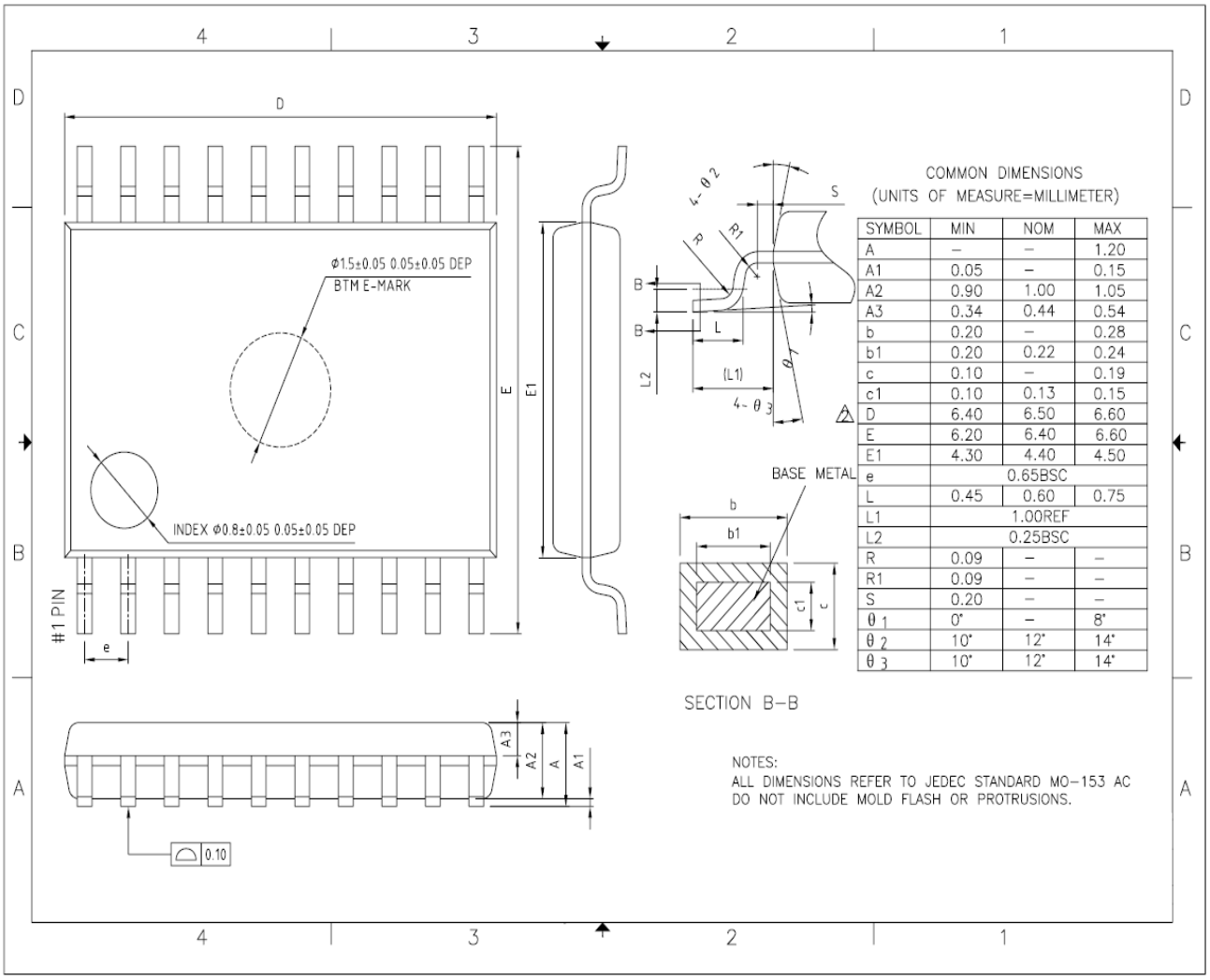
5.7 TSSOP20(6.5mm x 4.4mm)

Figure 5-7 TSSOP20(6.5mm x 4.4mm) Package Dimensions



SYMBOL	MIN	NOM	MAX
A	–	–	1.20
A1	0.05	–	0.15
A2	0.90	1.00	1.05
A3	0.34	0.44	0.54
b	0.20	–	0.28
b1	0.20	0.22	0.24
c	0.10	–	0.19
c1	0.10	0.13	0.15
D	6.40	6.50	6.60
E	6.20	6.40	6.60
E1	4.30	4.40	4.50
e	0.65BSC		
L	0.45	0.60	0.75
L1	1.00REF		
L2	0.25BSC		
R	0.09	–	–
R1	0.09	–	–
S	0.20	–	–
θ1	0°	–	8°
θ2	10°	12°	14°
θ3	10°	12°	14°

NOTES:
ALL DIMENSIONS REFER TO JEDEC STANDARD MO-153 AC
DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.

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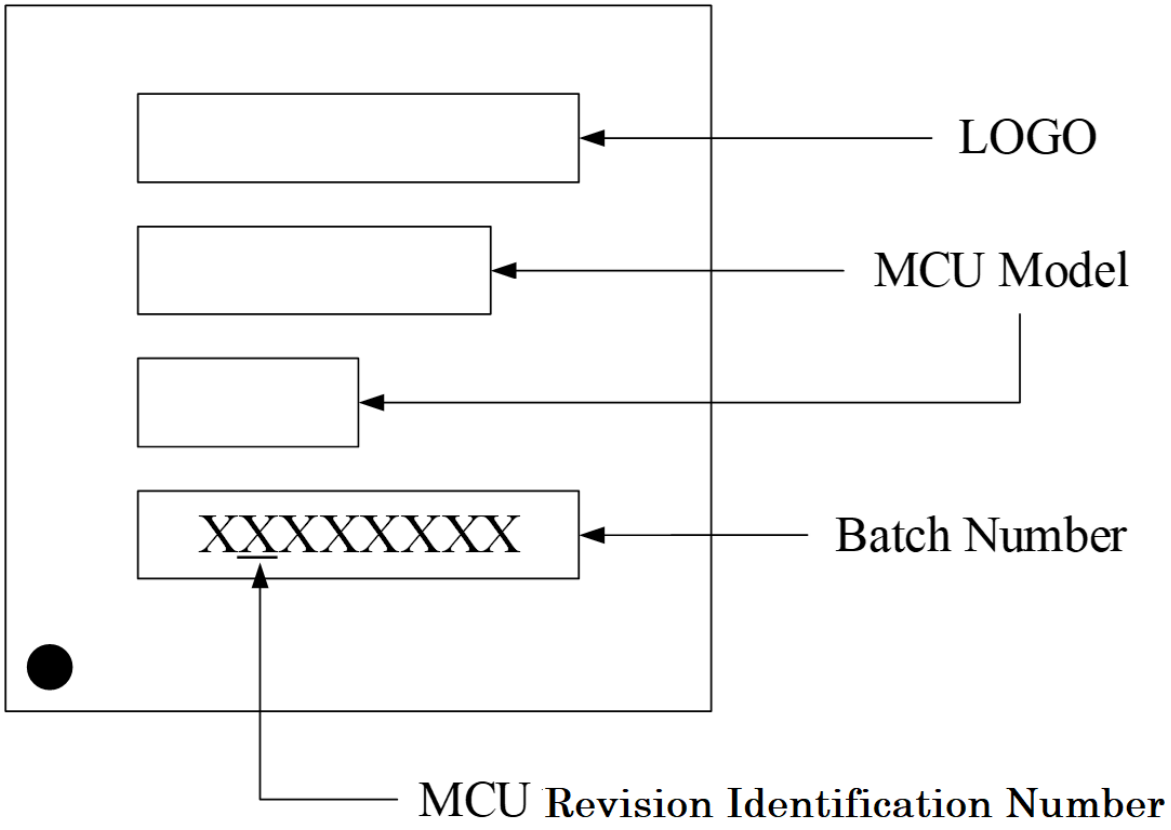
5.8 Marking Information

Figure 5-8 Marking Information



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6 Version History

Version	Date	Changes
V1.0	2021.2.1	Modify some descriptions
V1.1	2021.4.29	Modify ADC and IO VOL parameters
V1.2	2021.8.16	1. Table 4 -32 Modify I2S parameters. 2. Section 2.17 ADC , delete division factor 3; 3. Table 2-1 Timer function comparison LPTIM, the number of capture/compare channels is changed to 2 ; 4. Add TQFP48 package information; 5. PA0 cannot be multiplexed to OSC_IN;
V1.3	2022.3.3	1. Modify the mode configuration table in Section 2.13 2. Modify the number of I2S pins in chapter 2.15 , and increase the main clock output function 3. Modify section 3.2. Modify LPUART mapping and add MCO mapping. 4. 4-37 in Section 4.3.20 , the linearity of V SENSE with respect to temperature, deleted the maximum value, and increased the typical value
V 1.4	2022.6.26	1. Chapter 2.11 LPTIM capture / compare channel to count changed to 0 2. Section 2.17 , ADC internal channel changed to 4 3. 4.3.6 , modify the figure 4-8 , in the figure f HSE is changed to fLSE 4. Section 4.3.1 , Table 4-1 , delete two notes 5. Section 2.17 , ADC uses PLL and AHB_CLK as the clock source, add the division factor 3 6. Section 4.3.11. Table 4-24 , the minimum value is changed to the maximum value 7. Section 4.3.13 , Figure 4-10 , the filter is at the back, the resistor is a fixed resistor 8. Section 4.3.10 , Table 4-22 , changed "Power Down / Shutdown" to "Deep STANDBY Mode" 9. Section 4.3.17 , Modify Table 4-33 10. Modified Section 4.1.6, Figure 4-3. VDDA is connected to a capacitor of 100nf+ 1uf 11. Table 4-1 , remove input voltage on 5V tolerant pins, remove original note 2

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		12. Table 4-2 , remove total injected current on all I/O and control pins, remove original note 2, Modify the injection current of NRST to 0/-5 13. Section 4.3.5 , delete "Able to get results equivalent to Dhrystone 2.1 code" 14. Section 4.3.11 , Modified standards to follow 15. Added Figure 4-10 , IO port propagation delay graph 16. Modify Table 4-29, change fext to CH1 ~ CH4, note that fext does not apply to basic timers 17. Modify Table 4-30 , modify the capacitive load of each bus of I2C to 100pf 18. Modify Figure 4-14 , MOSI and MISO are written inversely, and one output is written as input 19. Modify Figure 2-1 , change Flash to Main Flash 20. Section 2.24 , delete " can also be used to activate the bootloader with security function (Secure Bootloader) " 21. Table 4-16 and Table 4-17, delete the description of load capacitance and drive curren. and add the qualification fout = 20MHz to Table 4-16 22. Modify Figure 4-8 23. Table 4-18 , HSI electrical characteristics add duty cycle 24. Table 4-28, delete Vol 25. Section 4.1.1 and 4.1.2. Delete description about standard distribution 26. Table 4-10. Add note “When ADC enabled, there is 1.1 mA current” 27. Table 4-21, Modify maximum of PLL ready time to 20us 28. Table 4-36, Add note2. Static power of reference input voltage source. 29. Modify description about MCO in Key feature 30. Table 4-31 , Modification slave input clock duty cycle, modification of data output access time constraints 31. Section 2.4, Add LSI to drive RTC and IWDG 32. Section 4.3.6. Table 4-14 and Table 4-15 add Bypass mode. Modify Figure 4-5 and Figure 4-6 33. Modify Figure 4-16, the diagram of I2S master.
V1.5	2022.9.13	1. Table 4-6, modify max and min. Gear 0-5, max ±100mv, gear 6-10, max ±120mv, gear 11-15, max ±160mv. 2. Section 2.11.6, modify IWDG 8-bits prescaler to 3-bit prescaler 3. Key feature, delete programmable low voltage detection and reset、

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		4. Section 2.18, delete(or both internal amplification and external filtering) 5. Add 4.3.18，VREFP characteristics
V1.6.0	2023.08.11	1. Table 4-5, Modify max VDD rising time rate to 650 2. Table 4-36, Minimum operating voltage of OPA is adjusted from 2.4V to 2.9V , and modify OPA Vinoffset min to -10mv, max to 10mv 3. Section 5.5. Modify package dimension of QFN32(4mx4m)

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