N32G435x8/xB Product Brief

N32G435 series uses 32-bit ARM Cortex-M4F core, operating frequency up to 108MHz, supporting floating-point unit and DSP instructions. The devices integrate up to 128KB of encrypted Flash, and 32KB of SRAM. The series features rich of high-performance interfaces, including one built-in 12-bit 5Msps ADC, two independent rail-to-rail operational amplifiers, two high-speed comparators, one 1Msps 12-bit DAC, multi-channel U(S)ART, I^2C, SPI, USB, CAN, and other communication interfaces, allowing a built-in hardware acceleration engine for cryptographic algorithms.

Key Features

- CPU core
  - 32-bit ARM Cortex-M4F core with FPU, supporting single-cycle multiplication and hardware division, DSP instructions and MPU
  - Built-in 2KB instruction Cache, supporting 0-wait-state execution from Flash memory
  - Frequency up to 108MHz with 135DMIPS
- Memories
  - Up to 128KByte of embedded Flash with ECC
    1. Supports encryption, multi-user partition and data protection
    2. 100,000 erase/write cycles, and 10 years data retention
  - Up to 32KByte of SRAM with hardware parity check, including 24Kbyte SRAM1(SRAM1 can be configured to data retention in STOP2 mode) and 8 Kbyte SRAM2(both in Standby and Stop2 modes, SRAM2 can be configured to data retention)
- Low power management
  - STANDBY mode: 2.5uA, all backup registers retained, all IOs retained, optional RTC Run, 8KByte Retention SRAM retained, supports fast wake up.
  - STOP2 mode: 6uA, RTC Run, 8KByte SRAM2 and 24KByte SRAM1 retained, CPU registers retained, all IOs retained, supports fast wake up.
  - RUN mode: 90uA/MHz@108MHz
  - LPRUN mode: The PLL is off, MSI is used as the system master clock. MR off, LPR on. USB/CAN/CRYE power off, other peripherals are optional.
  - SLEEP mode: only CPU is stopped, all peripherals are optional.
  - LP-SLEEP mode: CPU is stopped, the PLL is off, USB/CAN/CRYE module are disabled, all IOs remained, other peripherals are optional.
- High Performance Analog Interfaces

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- 1x 12bit 5Msps ADC
    1. Multiple precision configuration
    2. Up to 16 external single-ended input channels
    3. Supports differential mode
- 2x rail-to-rail operational amplifiers with built-in up to 32 times programmable gain amplifier (PGA)
- 2x high-speed analog comparators with internal 64-level adjustable comparison reference. COMP1 can operate in low-power STOP2 mode
- 1 x 12bit 1Msps DAC
- Internal 2.048V independent reference voltage source
- Analog voltage operation from 1.8~3.6V

- Clock
    - 4MHz~32MHz high-speed external crystal oscillator
    - 32.768KHz low-speed external crystal oscillator
    - High-speed internal RC (HSI) 16MHz
    - Multi-speed internal RC (MSI) 100K~4MHz
    - Low-speed internal RC (LSI) 40KHz
    - Built-in high-speed PLL
    - Supports one clock output, which can be configured as low-speed or high-speed clock
- Reset
    - Supports power on, brown-out, and external pin reset
    - Supports watchdog reset, software reset
- GPIOs
    - Up to 52 GPIOs
    - Supports multiplexed functions
    - Maximum toggle speed of 50 MHz
- Communication interfaces
    - 5x U(S)ART interfaces
        1. 3x USART interfaces (support 1xISO7816, 1xIrDA, LIN)
        2. 2x UART interfaces

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- 1x LPUART, supports waking up MCU from low-power STOP2 mode
- 2x SPI interfaces, the rate is up to 27 Mbps, support I^2S communication
- 2x I^2C interfaces, the rate is up to 1 MHz, which can be configured in master/slave mode and support dual address response in slave mode
- 1x USB2.0 FS Device interface
- 1x CAN 2.0A/B bus interface

- DMA controller
  - 1x high-speed DMA controller
  - Each controller supports 8 channels
  - Channel source address and destination address can be configured arbitrarily
- RTC real-time clock
  - Supports leap year perpetual calendar, alarm event, periodic wake up
  - Supports internal and external clock calibration
- Timers
  - 2x 16bit advanced control timers with maximum control precision of 9.25ns
    1. Supports input capture, complementary output, quadrature encoding input
    2. Each timer has four independent channels, with 3 channels support 6 complementary PWM outputs
  - 5x 16bit general-purpose timers
    1. Supports input capture/output comparison /PWM output
    2. Each timer has 4 independent channels
  - 2x 16bit basic timers
  - 1x 16bit low power timer, supports double pulse counting function, can work in STOP2 mode
  - 1x 24bit SysTick timer
  - 1x 7bit window Watchdog (WWDG)
  - 1x 12bit independent Watchdog (IWDG)
- Programming methods
  - Supports SWD/JTAG online debugging interface
  - Supports UART and USB Bootloader
- Security features

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- Built-in hardware acceleration engine for cryptographic algorithms
- Supports AES, DES, TDES, SHA1/224/256 and SM7 algorithms
- Flash encryption, multi-user partition management (MMU)
- True random number generator(TRNG)
- CRC16/32 calculation
- Supports write protection (WRP), multiple read protection (RDP) levels (L0/L1/L2)
- Supports secure boot, program encryption download, secure update
- Supports external clock failure detection, anti-tamper detection

- 96-bit UID and 128-bit UCID
- Operating conditions
  - Operating voltage range: 1.8V~3.6V
  - Operating temperature range: -40°C ~ 105°C
  - ESD: ±4KV (HBM model), ±1KV (CDM model)
- Packages
  - QFN28 (4mm x 4mm)
  - LQFP32 (7mm x 7mm)
  - LQFP48 (7mm x 7mm)
  - LQFP64 (10mm x 10mm)
  - LQFP64 (7mm x 7mm)
- Ordering information

Reference	Part Number
N32G435x8	N32G435G8Q7, N32G435K8L7, N32G435C8L7, N32G435R8L7
N32G435xB	N32G435KBL7, N32G435CBL7, N32G435GBQ7, N32G435RBL7[1], N32G435RBL7-1[2]

Notes:

[1] LQFP64 (10mm × 10mm)

[2] LQFP64 (7mm × 7mm)

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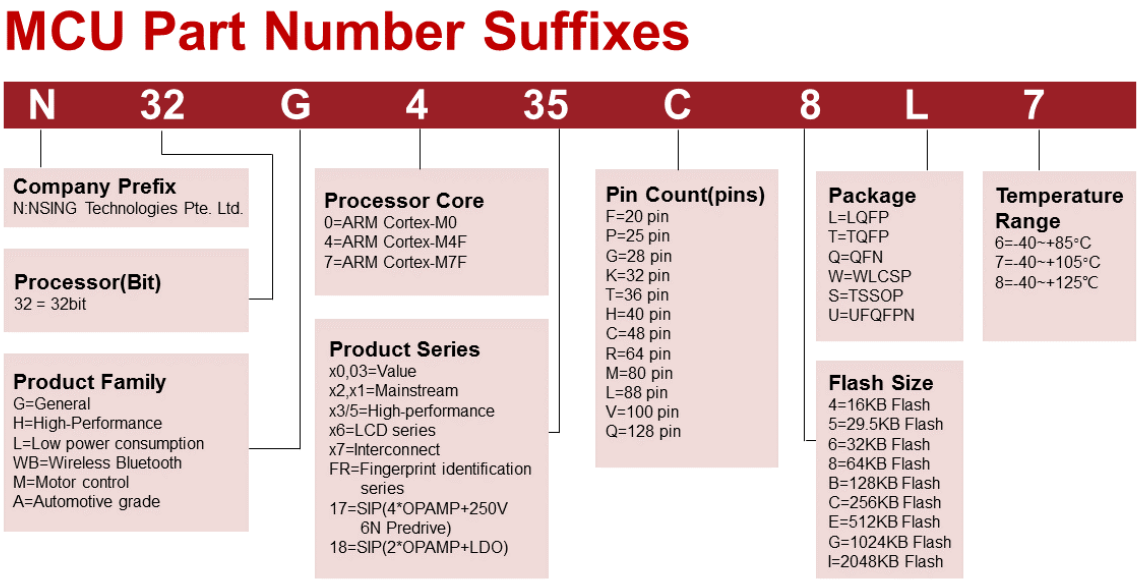
1 Naming Convention

Figure 1-1 N32G435 Series Part Number Information



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2 Product Configurations

Table 2-1 N32G435 Series Resource Configuration

Device		N32G435G8/B		N32G435K8/B		N32G435C8/B		N32G435R8/B	
Flash capacity (KB)		64	128	64	128	64	128	64	128
SRAM (KB)		16	32	16	32	16	32	16	32
CPU frequency		ARM Cortex-M4F @ 108MHz, 135DMIPS							
Operating conditions		1.8~3.6V/-40~105℃							
Timers	General	5							
	Advanced	2							
	Basic	2							
	LPTIM	1							
Communication interface	SPI	1		2					
	I^2S	1		2					
	I^2C	2							
	UART	2							
	USART	2		2		3			
	LPUART	1							
	USB	No(1)		1					
	CAN	No(1)		1					
GPIO		24		26		38		52	
DMA Number of channels		1x 8 Channel							
12bit ADC Number of channels		1x 10 Channel						1x 16 Channel	
12bit DAC Number of channels		1x 1 Channel							
OPAMP/COMP		2/2							
Algorithm support		DES/TDES, AES, SHA1/SHA224/SHA256 CRC16/CRC32, TRNG							
Security protection		Read-Write protection (RDP/WRP), storage encryption, partition protection, secure boot							
Package		QFN28		LQFP32		LQFP48		LQFP64	

Note: (1) It is not supported.

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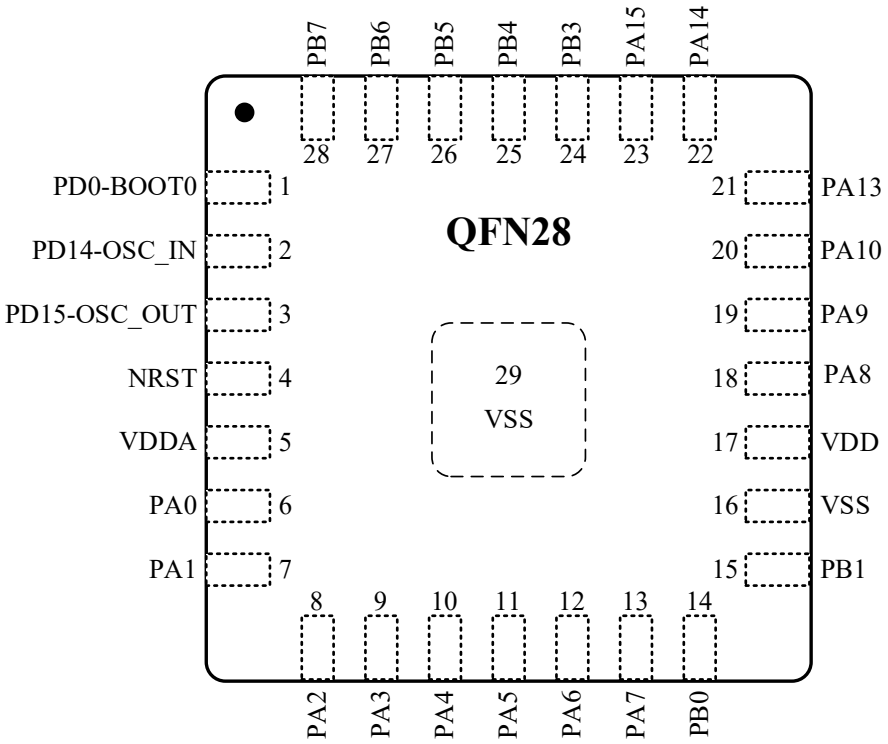
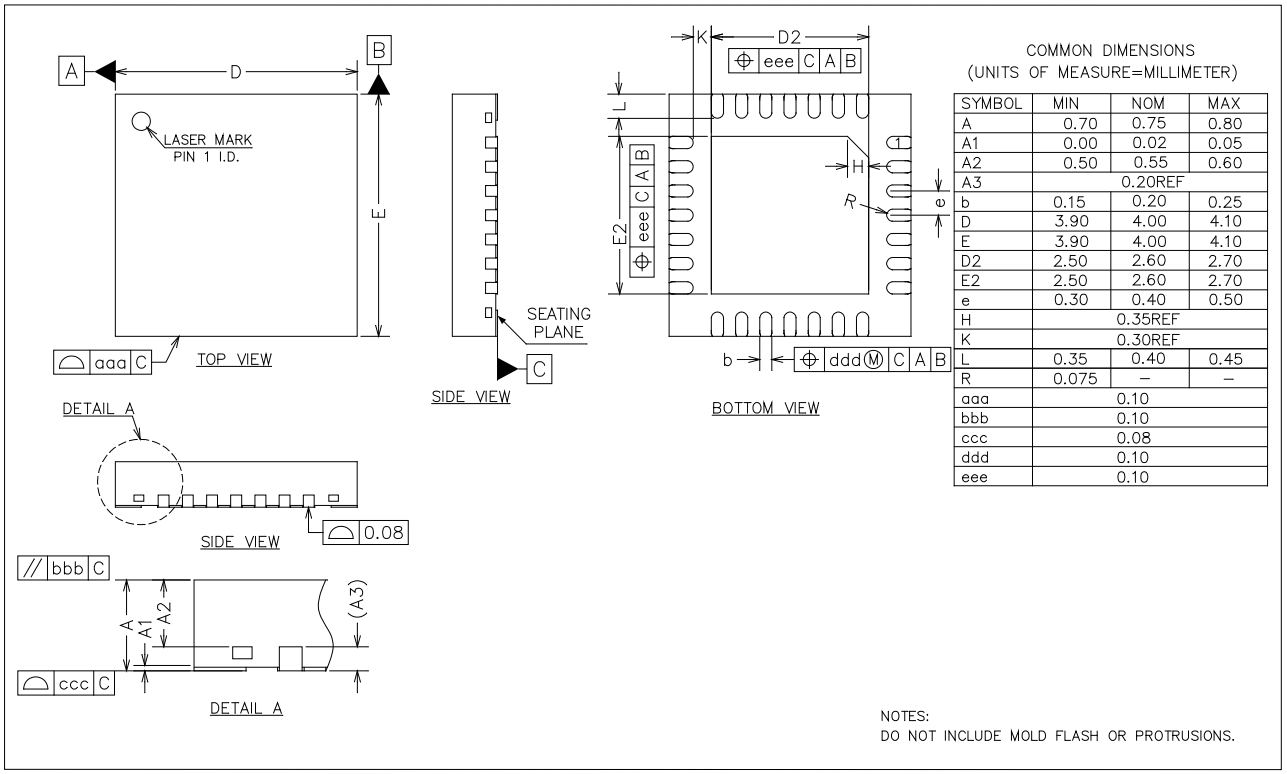
3 Packages

3.1 QFN28 Package

3.1.1 QFN28 Pin Assignment



3.1.2 QFN28(4mm x 4mm) Package Dimensions



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A2	0.50	0.55	0.60
A3		0.20REF	
b	0.15	0.20	0.25
D	3.90	4.00	4.10
E	3.90	4.00	4.10
D2	2.50	2.60	2.70
E2	2.50	2.60	2.70
e	0.30	0.40	0.50
H		0.35REF	
K		0.30REF	
L	0.35	0.40	0.45
R	0.075	–	–
aaa		0.10	
bbb		0.10	
ccc		0.08	
ddd		0.10	
eee		0.10	

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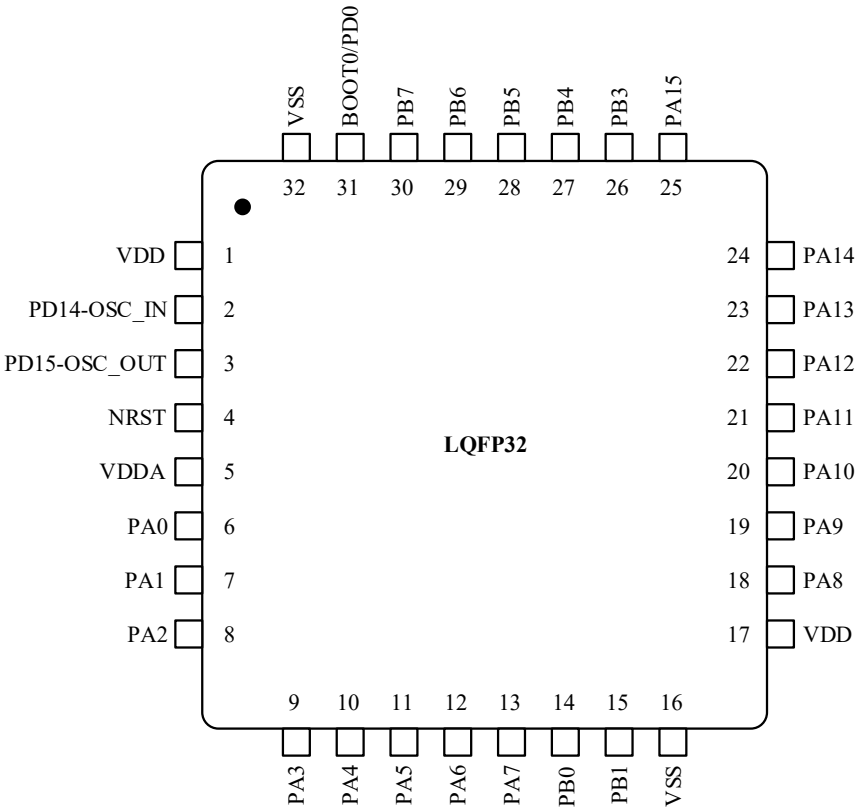
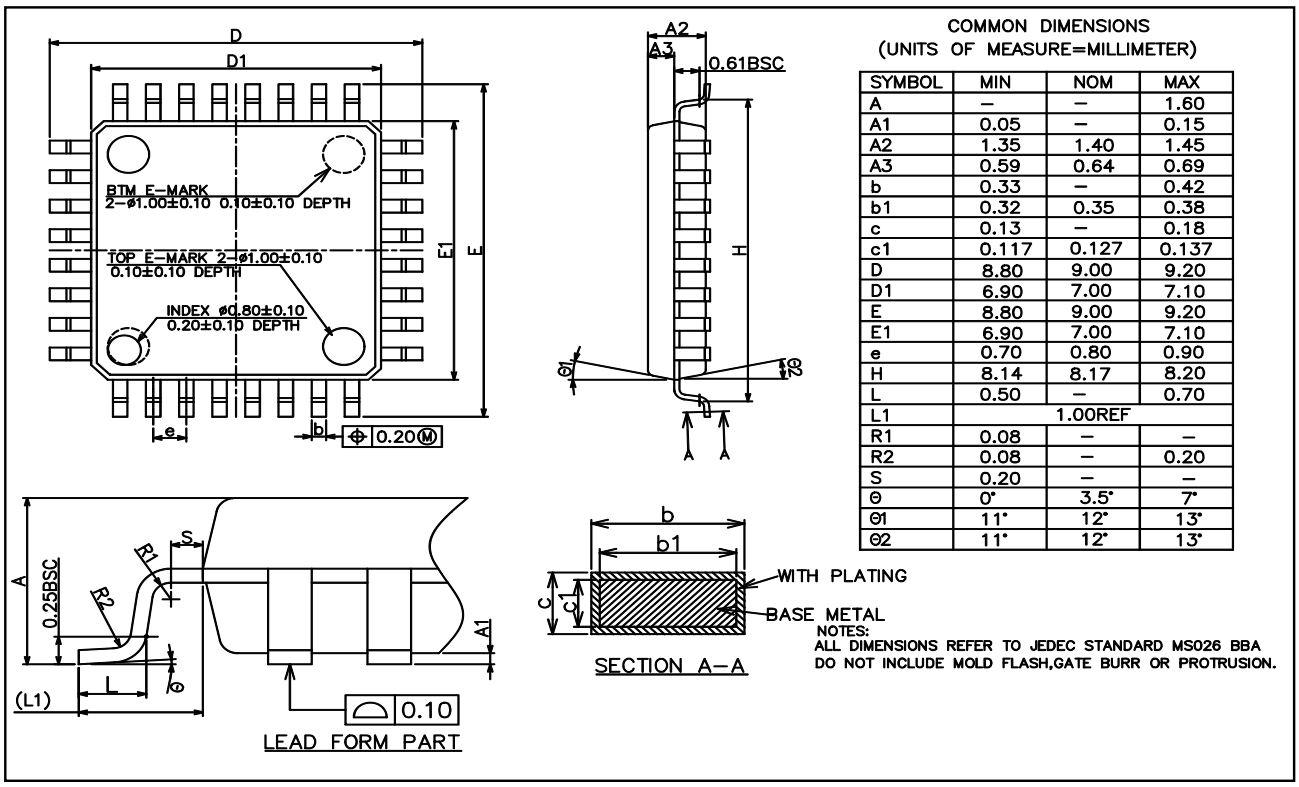
3.2 LQFP32 Package

3.2.1 LQFP32 Pin Assignment



3.2.2 LQFP32(7mm x 7mm) Package Dimensions



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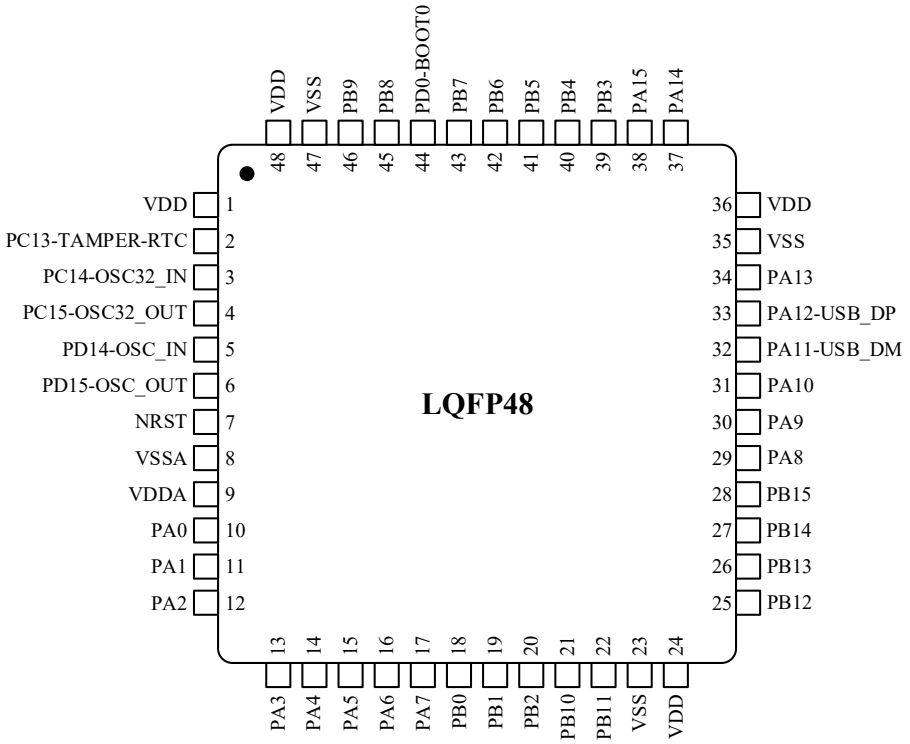
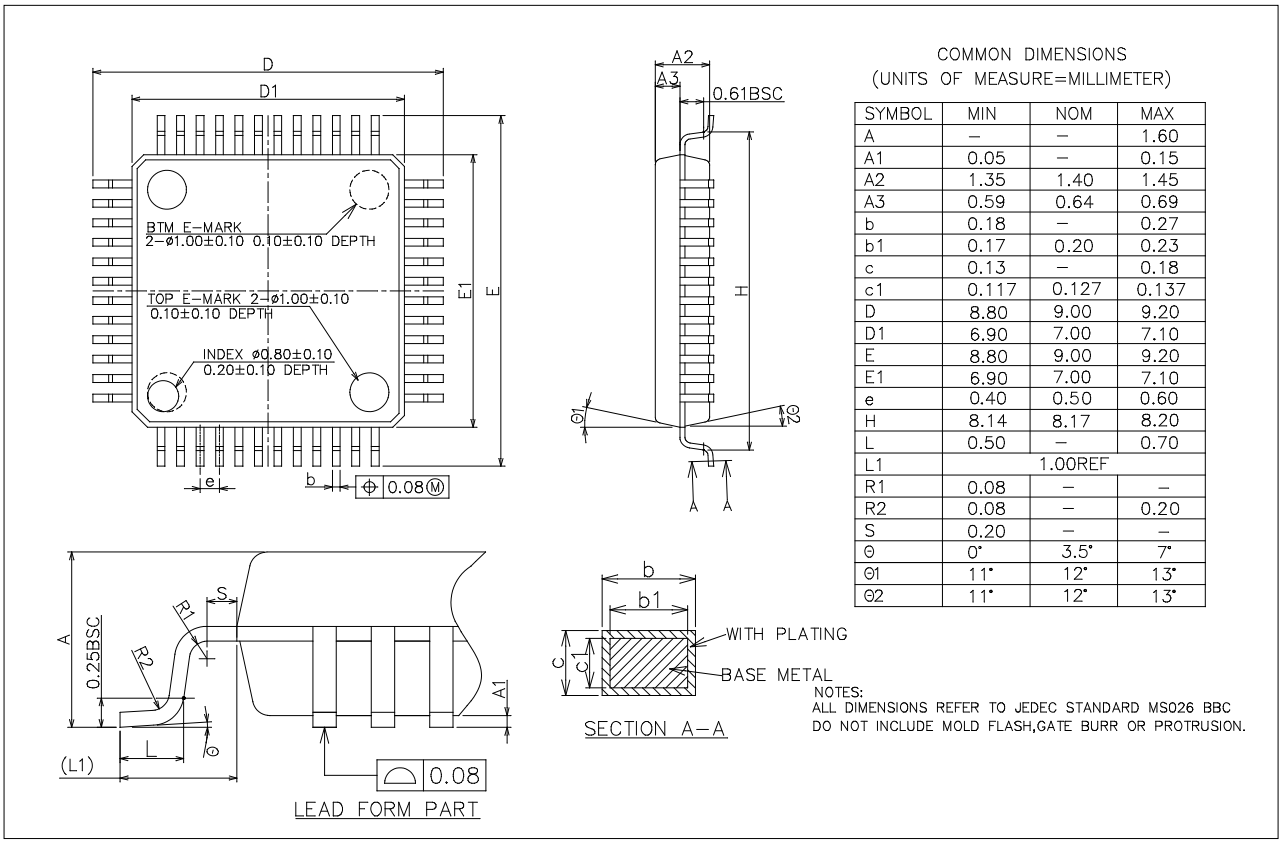
3.3 LQFP48 Package

3.3.1 LQFP48 Pin Assignment



3.3.2 LQFP48(7mm x 7mm) Package Dimensions



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	–	–	1.60
A1	0.05	–	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.18	–	0.27
b1	0.17	0.20	0.23
c	0.13	–	0.18
c1	0.117	0.127	0.137
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
e	0.40	0.50	0.60
H	8.14	8.17	8.20
L	0.50	–	0.70
L1	1.00REF		
R1	0.08	–	–
R2	0.08	–	0.20
S	0.20	–	–
θ	0°	3.5°	7°
θ1	11°	12°	13°
θ2	11°	12°	13°

NOTES:
ALL DIMENSIONS REFER TO JEDEC STANDARD MS026 BBC
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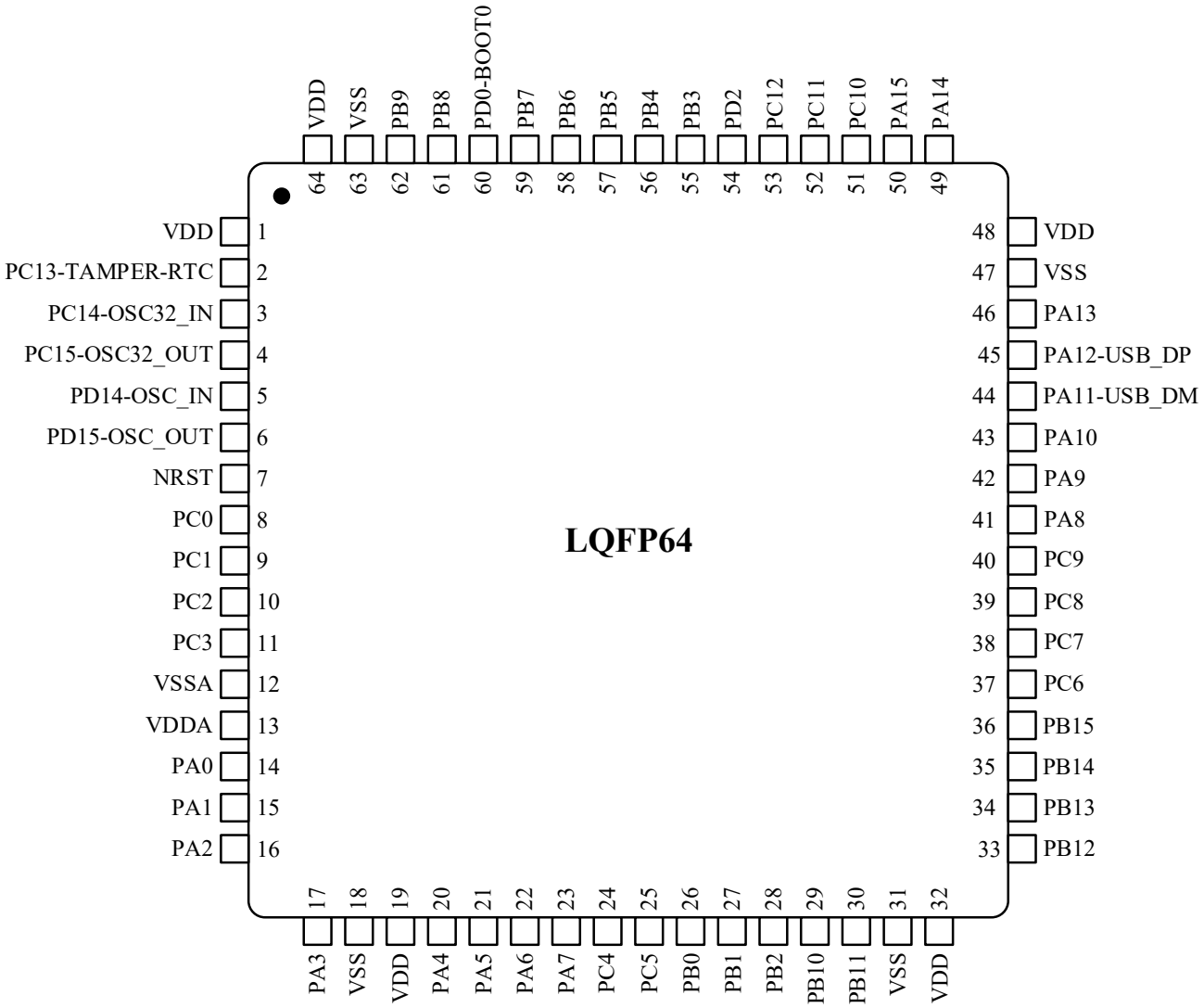
3.4 LQFP64 Package

3.4.1 LQFP64 Pin Assignment



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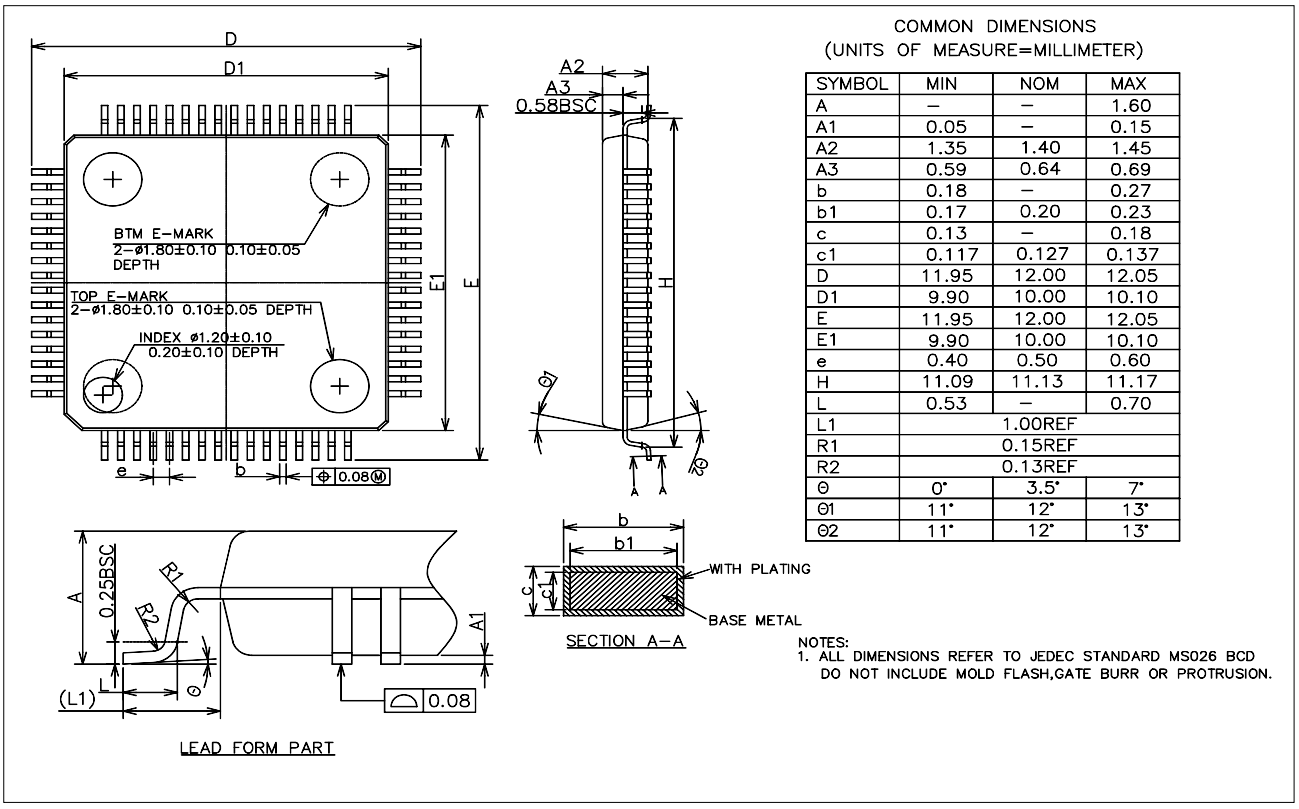
3.4.2 LQFP64(10mm x 10mm) Package Dimensions



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	–	–	1.60
A1	0.05	–	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.18	–	0.27
b1	0.17	0.20	0.23
c	0.13	–	0.18
c1	0.117	0.127	0.137
D	11.95	12.00	12.05
D1	9.90	10.00	10.10
E	11.95	12.00	12.05
E1	9.90	10.00	10.10
e	0.40	0.50	0.60
H	11.09	11.13	11.17
L	0.53	–	0.70
L1	1.00REF		
R1	0.15REF		
R2	0.13REF		
Θ	0°	3.5°	7°
Θ1	11°	12°	13°
Θ2	11°	12°	13°

NOTES:
1. ALL DIMENSIONS REFER TO JEDEC STANDARD MS026 BCD
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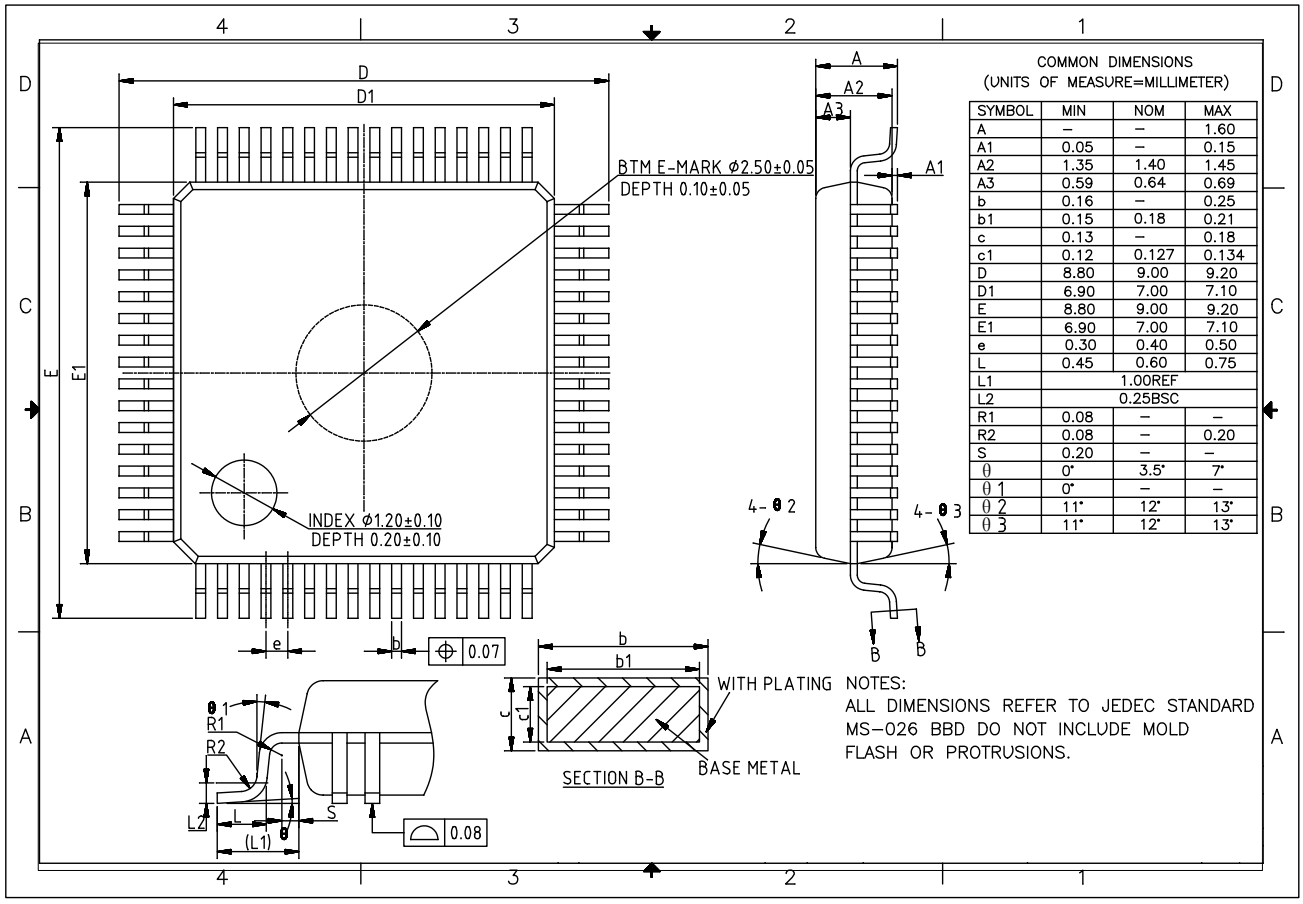
3.4.3 LQFP64(7mm x 7mm) Package Dimensions



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	–	–	1.60
A1	0.05	–	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.16	–	0.25
b1	0.15	0.18	0.21
c	0.13	–	0.18
c1	0.12	0.127	0.134
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
e	0.30	0.40	0.50
L	0.45	0.60	0.75
L1	1.00REF		
L2	0.25BSC		
R1	0.08	–	–
R2	0.08	–	0.20
S	0.20	–	–
θ	0°	3.5°	7°
θ1	0°	–	–
θ2	11°	12°	13°
θ3	11°	12°	13°

NOTES:
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4 Version History

Version	Date	Changes
V1.0	2020.6.12	Initial release
V1.1	2020.9.12	Updated product model resource configuration
V1.2	2021.4.14	1) Added N32G435G8Q7 model 2) Added LQFP64 (7mmx7mm) model and package size
V1.3	2021.7.6	Modified the description of low power

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