N32G401x6/x8 Datasheet

N32G401 series use 32-bit ARM Cortex-M4F kernel, operating frequency up to 72MHz, supporting floating-point unit and DSP instructions. The devices integrates up to 64KB of encrypted flash, and 8KB of SRAM. The series feature rich of high-performance interfaces, including 1 built-in 12bit 4.7Msps ADC, 3 high-speed comparators, multi-channel U(S)ART, I2C, SPI and other communication interfaces.

Key Features

- CPU Core
  - 32-bit ARM Cortex-M4F with FPU, supporting DSP instruction
  - Built-in 1KB instruction Cache, supporting zero-wait state execution from Flash memory.
  - Frequency up to 72MHz, with 90DMIPS
- **Memory**
  - Up to 64KByte of embedded Flash memory
  - Supports encryption, multi-user partition and data protection
  - 10,000 erase/write cycling and 10-years data retention.
  - Up to 8KByte of SRAM.it is retained in Stop2 mode and can be configured in Standby mode.
- **Low Power Management**
  - Sleep mode: The CPU is turned off, all peripherals remain active and can wake up the CPU when needed.
  - Stop0 mode: PLL, HSI and HSE are disabled, LSE/LSI can keep running, RTC can keep running, SRAM and all register contents retained, all IOs retained.
  - Stop2 mode: PLL, HSI and HSE are disabled, LSE/LSI can keep running, RTC can keep running, SRAM and all register contents retained, all IOs retained, CPU registers and backup registers contents retained.
  - Standby mode: Internal voltage regulator is turned off, PLL, HSI and HSE are disabled, LSE/LSI can keep running, RTC and IWDG can keep running, SRAM can be configured to retention, all IOs retained.
  - Standby mode: Internal voltage regulator is turned off, PLL, HSI and HSE are disabled, LSE/LSI can keep running, RTC and IWDG can keep running, SRAM can be configured to retention, all IOs retained.
- **High-Performance Analog Interface**
  - 1x 12bit 4.2Msps ADC with 12/10/8/6 bits configurable resolution, up to 16 external single-ended input channels, 3 internal single-ended input channels, supporting differential mode.
  - 3 x high-speed analog comparators with internal 64-level adjustable comparison reference
- **Clock**
  - HSE: 4MHz~32MHz high-speed external crystal oscillator
  - LSE: 32.768KHz External low-speed external crystal oscillator
  - HSI: High-speed internal RC 8MHz
  - LSI: Low-speed internal RC 40KHz
  - Built-in high-speed PLL

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  - MCO: Support 2-channels clock output, configurable as SYSCLK, HSI, HSE, LSI, LSE, and PLL division output

- **Reset**
  - Supports power-on/power-down/external pin reset.
  - Supports watchdog reset, software reset.
  - Supports programmable low voltage detection and reset.
- **GPIOs**
  - Up to 39+1 GPIOs
- **Communication Interface**
  - 4x U(S)ART interfaces
  - 2x USART interfaces (support ISO7816, IrDA, LIN)
  - 2x UART interfaces
  - 2x SPI interfaces
  - Speed up to 28Mbps (without CRC) and 20Mbps (with CRC) in master mode
  - Speed up to 32Mbps in slave mode
  - Supports I2S
  - 2x I2C interfaces (Master/Slave) with speedup to 1 MHz, support dual address responses in slave mode
- **DMA controller**
  - 1 x high-speed DMA controller supports 8 channels, with arbitrarily configurable channel sources and destination addresses
- **RTC real-time clock**
  - Supports leap year calendar, alarm event, periodic wake up
  - Supports internal and external clock calibration.
- **Beeper**
  - Supports complementary output, 12mA output driving capability.
- **Timer**
  - 2x 16-bit advanced timers with maximum control precision of 7.8ns
  - Supports input capture, complementary output, quadrature encoder input, etc.
  - Each timer has four independent channels, of which Timer1 supports 8 channels complementary PWM output, and Timer8 supports 6 channels complementary PWM output.
  - 4x 16-bit general purpose timers
  - Each timer has 4 independent channels
  - Supports input capture/output comparison /PWM output.
  - 1x 16-bit basic timer
  - 1x 16-bit low power timer
  - Supports single pulse and double pulse counting function
  - Supports operating in STOP2 mode.

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- 1x 24-bit SysTick timer
- 1x 14-bit Window Watchdog (WWDG)
- 1x 12-bit Independent Watchdog (IWDG)

- **Programming Methods**
  - Supports SWD/JTAG debugging interface.
  - Supports UART Bootloader
- **Security Features**
  - Flash storage encryption, Multi-user partition Management Unit (MMU)
  - CRC16/32
  - Supports write protection (WRP), multiple level (L0/L1/L2) of read protection (RDP)
  - Supports secure boot, encrypted program download, secure firmware updates.
  - Supports external clock failure detection, anti-tamper detection.
- **96-bit UID and 128-bit UCID**
- **Operating Conditions**
  - Operating voltage range: 2.4V~3.6V
  - Operating temperature range: -40℃ ~ 105℃
  - ESD: ±4KV (HBM model), ±2KV (CDM model)
- **Packages**
  - LQFP32(7mm x 7mm)
  - LQFP48(7mm x 7mm)
  - QFN20(3mm x 3mm)
  - QFN28(4mm x 4mm)
  - QFN32(4mm x 4mm)
  - QFN48(6mm x 6mm)
  - TSSOP20(6.5mm x 4.4mm)
- **Ordering Information**

Reference	Part Number
N32G401x6	N32G401C6L7, N32G401K6L7 N32G401C6Q7, N32G401K6Q7, N32G401G6Q7, N32G401F6Q7, N32G401F6S7-1
N32G401x8	N32G401C8L7, N32G401K8L7 N32G401C8Q7, N32G401K8Q7, N32G401G8Q7, N32G401F8Q7, N32G401F8S7-1

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1 Product Introduction

The N32G401 microcontrollers series features a high-performance 32-bit ARM Cortex™-M4F core with an integrated floating point operation unit (FPU) and digital signal processing (DSP). It supports parallel computing instructions and operates at a maximum frequency of 72MHz. The embedded encrypted memory Flash can hold up to 64KB, supporting multi-user partition permission management. Additionally, it includes up to 16KB of embedded SRAM.

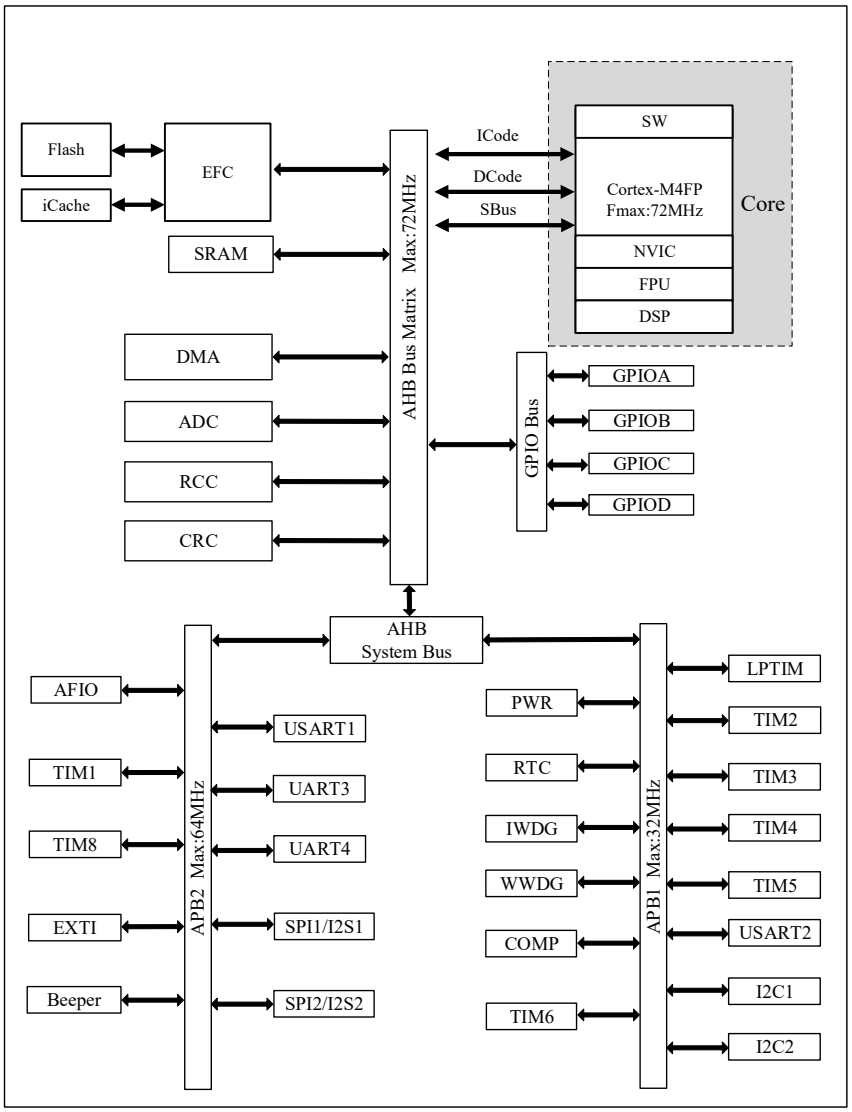
The device is equipped with internal high speed AHB bus, along with two low speed peripherals clock bus APB and bus matrix. It supports up to 40 alternate I/Os and features a diverse range of high-performance analog interfaces. These include a 12-bit 4.2Msps ADC, with up to 16 external input channels and 3 internal channels.

For digital communication, the N32G401 provides 4x U(S)ART, 2x I2C, 2x SPI/ I2S communication interface.

The N32G401 series operates reliably in the temperature range of -40°C to +105°C and supply voltage from 2.4V to 3.6V. It offers multiple power modes to cater to low-power applications. Available in 20/28/32/48 pin package, the device in the peripheral configuration is different.

Figure 1-1 N32g401 Series Block Diagram

Figure 1-1 N32g401 Series Block Diagram



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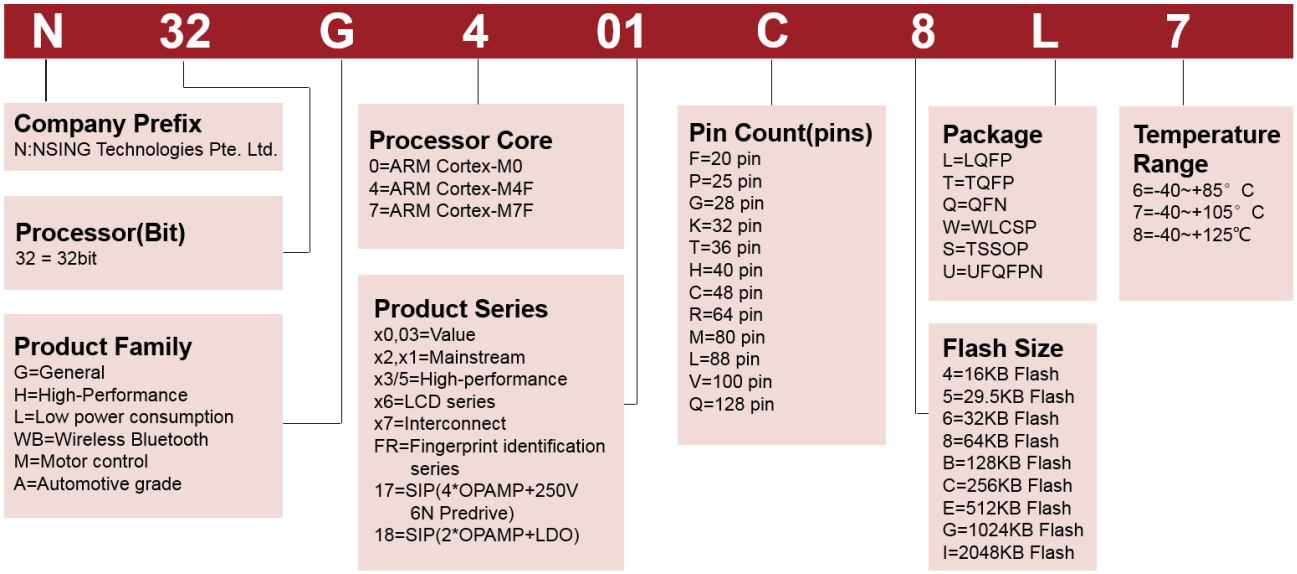
1.1 Naming Convention

Figure 1-2 N32g401 Series Part Naming Conversion



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1.2 Product Configurations

Table 1-1 N32G401 Series Resource Configuration (1)

Device		N32G401F6S7-1	N32G401F8S7-1	N32G401F6Q7	N32G401F8Q7	N32G401G6Q7	N32G401G8Q7
Flash capacity (KB)		32	64	32	64	32	64
SRAM capacity (KB)		8	8	8	8	8	8
CPU frequency		ARM Cortex-M4F @72MHz，90DMIPS					
Operating Conditions		2.4~3.6V/-40~105℃					
Timers	General	4					
	Advanced	2(1)					
	Basic	1					
	LPTIM	1					
Communication Interfaces	SPI	2					
	I2S	2					
	I2C	2					
	UART	1				2	
	USART	2					
BEEPER		1					
GPIO		15+1				23+1	
DMA Number of Channels		1 8 Channel					
12bit ADC Number of Channels		1 9Channel		1 7Channel		1 10Channel	
COMP		0		3			
Security Protection		Read and Write Protection (RDP/WRP), Memory Encryption, Partition Protection, Secure Boot					
Package		TSSOP20		QFN20		QFN28	

Note: (1) Timer1 supports 4 channels and 8 complementary output, Timer8 supports 3 channels and 6 complementary output.

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Table 1-2 N32G401 Series Resource Configuration (2)

Device		N32G401K6L7 N32G401K6Q7	N32G401K8L7 N32G401K8Q7	N32G401C6L7 N32G401C6Q7	N32G401C8L7 N32G401C8Q7
Flash capacity (KB)		32	64	32	64
SRAM capacity (KB)		8	8	8	8
CPU frequency		ARM Cortex-M4F @72MHz，90DMIPS			
Operating Conditions		2.4~3.6V/-40~105℃			
Timers	General	4			
	Advanced	2(1)			
	Basic	1			
	LPTIM	1			
Communication Interfaces	SPI	2			
	I2S	2			
	I2C	2			
	UART	2			
	USART	2			
BEEPER		1			
GPIO		25+1		39+1	
DMA Number of Channels		1 8 Channel			
12bit ADC Number of Channels		1 10Channel		1 16Channel	
COMP		3			
Security Protection		Read and Write Protection (RDP/WRP), Memory Encryption, Partition Protection, Secure Boot			
Package		LQFP32 QFN32		LQFP48 QFN48	

Note: (1) Timer1 supports 4 channels and 8 complementary output, Timer8 supports 3 channels and 6 complementary output.

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2 Functional overview

2.1 Processor Core

The N32G401 series integrates the latest generation of embedded ARM Cortex™-M4F processors. It features a floating point processing unit (FPU), DSP and parallel computing instructions, providing excellent performance of 1.25DMIPS/MHz. At the same time, its efficient signal processing capabilities combined with low power consumption, low cost, and ease of use. It can be used in application scenarios that require a blend of control and signal processing capabilities while being user-friendly.

The ARM Cortex™-M4F 32-bit reduced instruction set processor offers exceptional code efficiency.

Note: Cortex-M4F is backward compatible with Cortex-M3 code.

2.2 Memories

The N32G401 series include embedded encrypted Flash memory and embedded SRAM.

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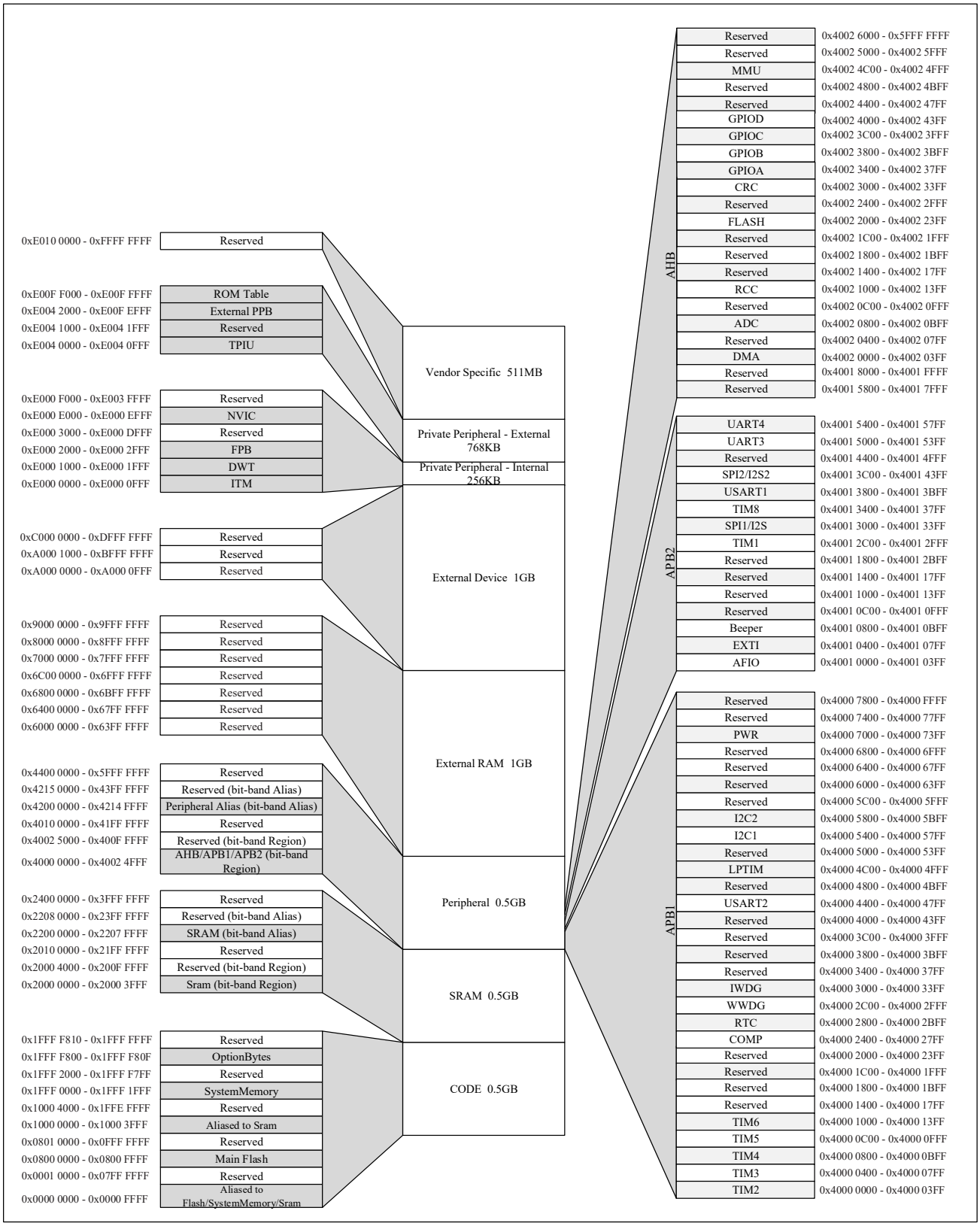
Figure 2-1 Memory Map



2.2.1 Embedded FLASH Memory

The integrated encrypted FLASH (FLASH) memory range from 32K to 64K bytes, utilized for storing programs and data. The page size is 2K byte, supporting page erasing, word writing, word reading, half-word reading, and byte read operations.

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It supports storage encryption protection, enabling automatic encryption during writing and encryption during reading (including program execution operation).

User partition management is supported, allowing for a maximum of 2 user partitions, different users cannot access each other's data (only executable code can be accessed).

2.2.2 Embedded SRAM

The chip integrates a built-in SRAM of up to 8K bytes. In operating、SLEEP、STOP0、STOP2 and STANDBY mode, SRAM data can be retained.

2.2.3 Nested Vector Interrupt Controller (NVIC)

The built-in Nested Vector Interrupt Controller, can handle up to 53 maskable interrupt channels (excluding the 16 Cortex™-M4F interrupts) and 16 priorities.

- The tightly coupled NVIC ensures low-latency interrupt response processing
- Interrupt vector entry address directly access the kernel
- Allows early processing of interrupts
- Processing late arriving higher-priority interrupts
- Support interrupt tail chaining functionality.
- Automatically saves processor state
- Automatically resumes when interrupt returns with no instruction overhead

This module offers flexible interrupt management with minimal interrupt latency.

2.3 Extended Interrupt/Event Controller (EXIT)

The external interrupt/event controller contains 24 edge detectors used for generating interrupt/event requests. Each interrupt line can be independently configured with its trigger event (rising edge, falling edge or both) and can be individually masked. A pending register maintains the state of all interrupt requests. The EXTI can detect clock pulse with widths smaller than internal APB2 clock cycle. Up to 40 general-purpose I/O ports are connected to 16 external interrupts lines.

2.4 Clock System

The device offers various clock options for users to choose from, including:

- High speed internal RC oscillator (his) at 8MHz.
- Low speed internal clock (LSI) at 40KHz.
- High speed external crystal oscillator (HSE) ranging from4MHz to32MHz.
- Low speed external crystal oscillator (LSE) at 32.768kHz.
- Phase-Locked Loop (PLL).

Upon reset, the internal HSI clock is set as the default CPU clock. User can choose the external HSE clock with fail function. When an external clock failure is detected, it will be isolated, and the system will automatically switch to his. If interrupts are enabled, software can receive the corresponding interrupts. Similarly, the system will automatically switch back to HIS when the PLL clock was adopted and external oscillator fails.

There is a built-in clock security system. When enabled by the user, it can detect in real-time whether the external HSE or LSE has fails. Once an external clock failure is detected, the system automatically switches back to internal clock and generates an interrupt alert.

Multiple prescalers are used to adjust the AHB frequency, high speed APB (APB2) and low speed APB (APB1) domains. The AHB has a maximum frequency of 72MHz, APB2 has a maximum frequency of 64MHz and APB1

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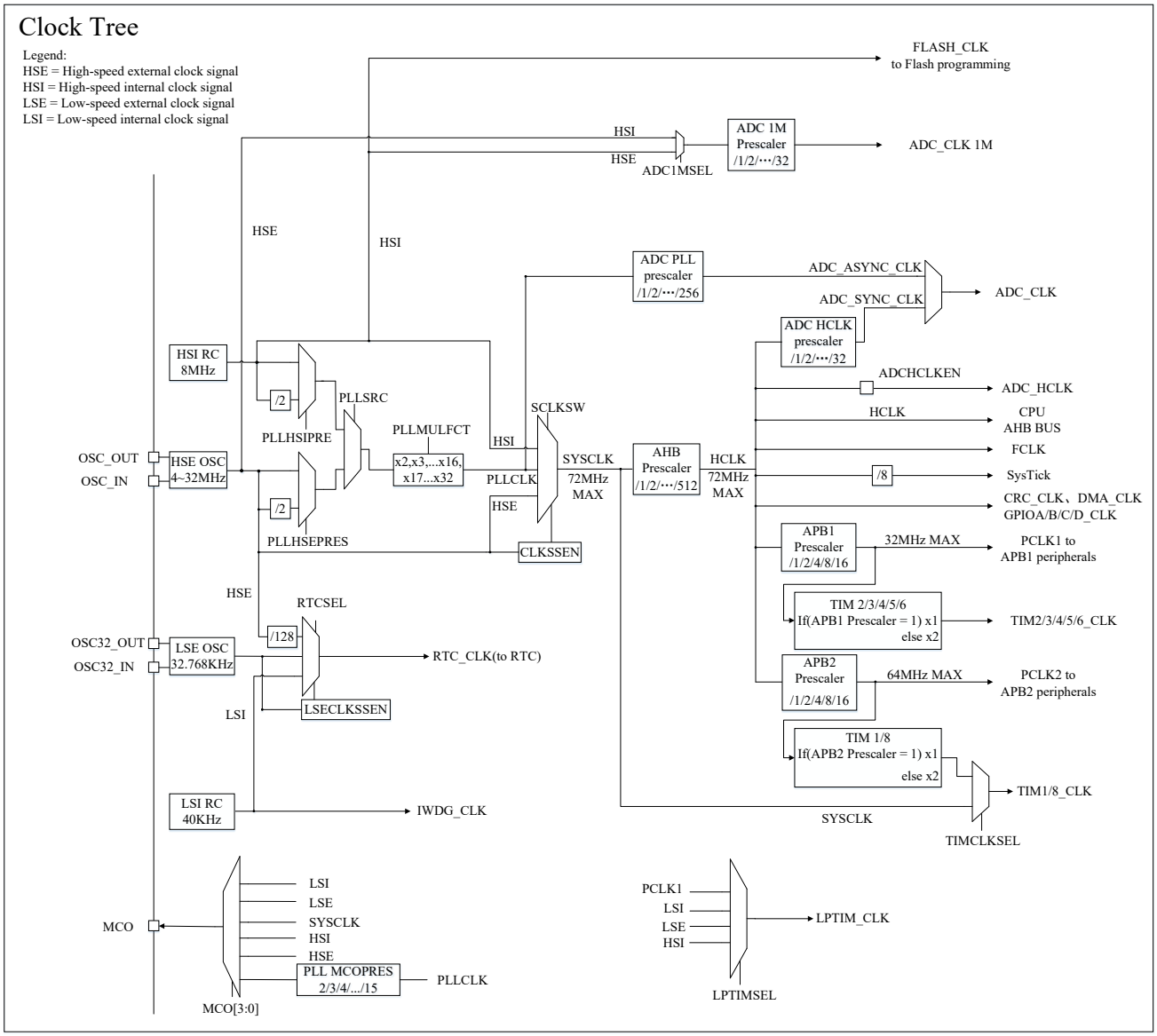
has a maximum frequency of 32MHz.

Note: If APB1 and APB2 are running at the maximum frequency, the system clock needs to be reduced to 64MHz.

Figure 2-2 Clock Tree



2.5 Boot Modes

At startup, the BOOT mode after reset can be selected through the BOOT0 pin and option byte BOOT configuration (USER2).

- Boot from FLASH memory
- Boot from system memory
- Boot from embedded SRAM

The Bootloader is stored in the system memory and can program the Flash memory through USART1 interface.

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2.6 Power Supply Schemes

- V_{DD} = 2.4~3.6V: The V_{DD} pin supplies power to the I/O pin and the internal voltage regulator.
- V_{DDA} = 2.4V~3.6V: The V_{DDA} provides power supply for ADC, COMP.
- V_{DDA} and V_{SSA} must be connected to V_{DD} and V_{SS} respectively. See Figure 4-3 Power supply scheme.

2.7 Reset

POR circuit is integrated inside the device. This part of the circuit ensure that the system works stably when the power supply exceeds 2.4V.When V_{DD} falls below a set threshold ($V_{POR/PDR}$), the device goes into reset state without using an external reset circuit.

2.8 Programmable Voltage Detector

The device has a built-in programmable voltage detector (PVD), which monitors the power supply of V_{DD} and compares it with the threshold V_{PVD}. When V_{DD} is lower or higher than the threshold V_{PVD}, an interrupt will be generated. The interrupt handler can send a warning message, and the PVD function needs to be enabled through the program. See Table 4-6 for values of $V_{POR/PDR}$ and V_{PVD}.

2.9 Voltage Regulator

The voltage regulator has 3 control modes:

- Main mode: The MCU operates in operating, SLEEP, STOP0 modes.
- Low power mode: The MCU operates in STOP0 mode.
- Turn off mode: The MCU run in STOP2, STANDBY modes.

The voltage regulator is always in the main mode after the MCU reset.

2.10 Low Power Modes

The N32G401 series supports four low-power modes.

- SLEEP mode.

In SLEEP mode, only the CPU is stopped and all peripherals remain operational. They can wake up the CPU when an interrupt/event occurs.

- STOP0 mode

In STOP0 mode, the voltage regulator can be configured in main mode or low power mode, and most clocks in the main domain are disabled, such as PLL, HSI and HSE. The SRAM and all register contents are retained.

All I/O pins remain in the same state as in operating mode.

- STOP2 mode

In STOP2 mode, all the core digital logic areas are powered off.

  - The Main voltage regulator (MR) is turned off.
  - HSE/HSI/PLL is turned off.
  - CPU registers are retained.
  - LSE/LSI can be configured to operate.
  - GPIOs are retained.
  - SRAM is retained.

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- 80-byte backup register are retained.
- RET and Backup domains operate normally.

Wake up: The microcontroller can be woken up from STOP2 mode by any of the 16 external EXTI signals (I/O related), WKUP pin wakeup, RTC periodic wake up, RTC alarm, RTC tamper, RTC timestamp, NRST reset, IWDG reset.

- STANDBY mode

In STANDBY mode, the device can achieve a lower current consumption. The internal voltage regulator is turned off, as well as PLL, HSI RC oscillator and HSE crystal oscillator. Only LSE and LSI can be configured to operate; Upon entering STANDBY mode, the contents of the main domain registers will be lost, I/Os are retained, SRAM can optionally be retained, and the STANDBY circuitry continues to function.

In STANDBY mode, if PA13 and PA14 are used as non-debug pins and configured as input mode, it is necessary to add external strong pull-up and pull-down resistances on PA13 and PA14 pins. The resistance is recommended to be within 10KΩ.

External reset signal on the NRST, IWDG reset, rising/falling edge on three WKUP pins, RTC periodic wake up, RTC alarm, RTC timestamp and RTC tamper can wake up the microcontroller from STANDBY mode.

Note: RTC, IWDG and corresponding clock cannot be stopped when entering standby mode.

2.11 Direct Memory Access (DMA)

The device integrates a flexible general-purpose DMA controller that supports eight DMA channels. It can manage data transfers from memory to memory, peripherals to memory, and memory to peripherals. The DMA controller supports the management of circular buffers, thus avoiding interrupts when the controller reaches the end of the buffer.

Each channel has dedicated hardware DMA request logic, and each channel can be triggered by software. The transmission length, source address and destination address of each channel can be set separately by software.

DMA can be used with major peripherals: SPI, I2C, USART, TIMx (Advanced/General/Basic), I2S, ADC.

2.12 Real Time Clock (RTC)

The RTC is a set of continuously running counters integrated with a built-in calendar clock module that provides a perpetual calendar functionality, as well as alarm interrupt and periodic interrupt (with a minimum 2 clock cycles). The RTC will not be reset by the system reset, nor will it be reset when wake up from STANDBY mode.

The RTC can be driven by either a 32.768 kHz external crystal oscillator, an internal low-power 40 KHz RC oscillator, or a high-speed external clock with 128 frequency divisions.

For application scenarios requiring very high timing accuracy, it is recommended to use an external 32.768 kHz clock as the clock source, to compensate for the clock deviation of natural crystal, a 256Hz signal can be output to calibrate the clock of RTC.

The RTC features a 22-bit prescaler for a time-based clock. By default, when the clock is set to 32.768 kHz, it generates a 1-second time reference. In addition, the RTC can be used to trigger wake up in low-power mode.

2.13 Timers And Watchdogs

Up to 2 advanced control timers, 4 general-purpose timers and 1 basic timer, 1 low power timer, 2 watchdog timers and 1 system tick timer.

The following table compares the functions of advanced control timer, general-purpose timer and basic timer:

Table 2-1 Comparison Of Timer Functions

Timer	Counter Resolution	Counter Type	Prescaler Factor	Generate DMA	Capture/ Compare	Complementary Output

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				Requests	Channels	
TIM1 TIM8	16	Up, down, up/down	Any integer between 1 and 65536	Y	4	Y
TIM2 TIM3 TIM4 TIM5	16	Up, down, up/down	Any integer between 1 and 65536	Y	4	N
TIM6	16	up	Any integer between 1 and 65536	Y	0	N

2.13.1 Low Power Timer (LPTIM)

The LPTIM is a 16-bit timer with multiple clock sources, it can keep running in all power modes except for Standby mode. LPTIM can run without internal clock source as a "Pulse Counter". Also, the LPTIM can wake up the system from low-power modes, to realize "Timeout functions" with extremely low power consumption.

Main features:

- 16-bit upcounter
- 3-bit prescaler with prescaler factors (1,2,4,8,16,32,64,128)
- Multiple clock sources
    - Internal clock source: LSE, LSI, HSI or APB1 clock
    - External clock source: External clock source through LPTIM Input1 (operating without LP oscillator, for pulse counter applications)
- 16-bit auto-reload register (LPTIM_ARR)
- 16-bit compare register (LPTIM_COMP)
- Continuous or One-shot counting mode
- Programmable software or hardware input trigger
- Programmable digital filter for filtering glitch
- Configurable output: Pulse, PWM
- Configurable I/O polarity
- Encoder mode
- Pulse counting mode, support single pulse counting, double pulse counting (quadrature and non-quadrature)

2.13.2 Basic Timer (TIM6)

The basic timer contains a 16-bit counter.

Main features:

- 16-bit auto-reload up-counting counters.
- 16-bit programmable prescaler. (The prescaler factor can be configured with any value between 1 and 65536)
- Events that generate the interrupt/DMA is as follows:
    - Update event

2.13.3 General-Purpose Timer (TIMX)

The general-purpose timers (TIM2, TIM3, TIM4 and TIM5) is mainly used in the following occasions: counting the

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input signal, measuring the pulse width of the input signal and generating the output waveform, etc.

Main features:

- 16-bit auto-reload counters. (It can realize up-counting, down-counting, up/down counting)
- 16-bit programmable prescaler. (The prescaler factor can be configured with any value between 1 and 65536)
- TIM2, TIM3, TIM4 and TIM5 up to 4 channels.
- Channel's working modes: PWM output, output compare, one-pulse mode output, input capture.
- The events that generate the interrupt/DMA are as follows:
  - Update event.
  - Trigger event.
  - Input capture.
  - Output compare
- Timer can be controlled by external signal.
- Timer can be linked together internally for timer synchronization or chaining.
- Incremental (quadrature) encoder interface: used for tracking motion and resolving rotation direction and position.
- Hall sensor interface: used to do three-phase motor control.

2.13.4 Advanced Control Timer (TIM1 And TIM8)

The advanced control timers (TIM1 and TIM8) is mainly used in the following purposes: counting the input signal, measuring the pulse width of the input signal and generating the output waveform, etc.
Advanced timers have complementary output function with dead-time insertion and break function. They are suitable for motor control.

Main features:

- 16-bit auto-reload counters. (It can realize up-counting, down-counting, up/down counting). TIM1 support center-aligned asymmetric counting mode.
- 16-bit programmable prescaler. (The prescaler factor can be configured with any value between 1 and 65536)
- Programmable Repetition Counter
- TIM1 up to 9 channels, TIM8 up to 6 channels.
- Up to 4 capture/compare channels
  - PWM output
  - Output compare
  - One-pulse mode output
  - Input capture
- The events that generate the interrupt/DMA are as follows:
  - Update event.
  - Trigger event.
  - Input capture.
  - Output compare.
  - Break input.

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- Complementary outputs with programmable dead-time.
  - For TIM1, channel 1,2,3,4 support this feature.
  - For TIM8, channel 1,2,3 support this feature.
- TIM can be controlled by external signal.
- TIM can be linked together for TIM synchronization or chaining.
- TIM1_CC5 and TIM8_CC5 for COMP blanking.
- For TIM1, channels 4/7/8/9 can output pulse signals, which can be configured to trigger the ADC on either the rising or falling edge of clock.
- Incremental (quadrature) encoder interface: used for tracking motion and resolving rotation direction and position.
- Hall sensor interface: used to do three-phase motor control.

2.13.5 SysTick Timer (SysTick)

This timer is dedicated to real-time operating systems and can also be used as a standard down-counter.

Main features:

- 24-bit down-counter
- Automatic reloading function
- A maskable system interrupt is generated when the counter is 0
- Programmable clock source

2.13.6 Watchdog (WDG)

Support for two watchdog independent watchdog (IWDG) and window watchdog (WWDG). Two watchdogs provide increased security, time accuracy, and flexibility in use.

Independent Watchdog (IWDG)

The independent watchdog is based on a 12-bit down-counter and a 3-bit prescaler. It is driven by a separate low-speed RC oscillator that remains active even if the master clock fails and can operate in STOP and STANDBY modes. Once activated, if the watchdog is not fed (clears the watchdog counter) within the set time, the IWDG generates a reset when the counter counts to 0x000. It can be used to reset the entire system in the event of an application problem, or as a free timer to provide time-out management for applications. It is hardware or software configurable through the option bytes. Reset and low power wake up are available.

Window Watchdog (WWDG)

A window watchdog is usually used to detect software failures caused by an application deviating from the normal running sequence due to external interference or unforeseen logical conditions. Unless the down-counter value is flushed before the T6 bit becomes zero, the watchdog circuit generates an MCU reset when the preset time period is reached. If the 14-bit down-counter value (in the control register) is flushed before the down-counter reaches the window register value, then an MCU reset will also occur. This indicates that the down-counter needs to be refreshed in a finite time window.

Main features:

- The WWDG is driven by a clock divided from the APB1 clock.
- Programmable free-running down-counter.
- Reset condition:
  - When the down-counter is less than 0x40, a reset occurs (if the watchdog is started);
  - A reset occurs when the down-counter is reloaded outside the window (if the watchdog is started);

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- If the watchdog is enabled and interrupts are allowed, an early wake up interrupt (EWINT) occurs when the down-counter equals 0x40, which can be used to reload the counter to avoid WWDG reset.

2.14 I²C Bus Interface

The device integrates up to two independent I2C bus interfaces, which provide multi-host function and control all I2C bus-specific timing, protocol, arbitration, and timeout. I2C bus interface supports multiple communication rate modes (up to 1MHz), supports DMA operations and is compatible with SMBus 2.0. The I2C module provides multiple functions, including CRC generation and verification, System Management Bus (SMBus), and Power Management Bus (PMBus).

Main features:

- Multi-master function: this module can be used as master device or slave device
- I2C master device function
  - Generate a clock
  - Generate start and stop signals
- I2C slave device function:
  - Programmable address detection
  - The I2C interface supports 7-bit or 10-bit addressing and dual-slave address response capability in 7-bit slave mode
  - Stop bit detection
- Generate and detect 7-bit / 10-bit addresses and broadcast calls
- Support different communication speeds
  - Standard speed (up to 100 kHz)
  - Fast (up to 400 kHz)
  - Fast + (up to 1MHz)
- Status flags:
  - Transmitter/receiver mode flag
  - Byte transfer complete flag
  - I2C bus busy flag
- Error flags:
  - Arbitration loss in master mode
  - Acknowledge (ACK) fail after address/data transfer
  - Error start or stop condition detected.
  - Overrun or underrun when clock extending is disable
- Two interrupt vectors:
  - 1 interrupt for address/data communication success
  - 1 interrupt for an error
- Optional extend clock function.
- DMA of single-byte buffers
- Generation or verification of configurable PEC (Packet error checking)

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- In transmit mode, the PEC value can be transmitted as the last byte.
- PEC error check for the last received byte.
- SMBus 2.0 compatible
  - Timeout delay for 25ms clock low
  - 10 ms accumulates low clock extension time of master device.
  - 25 ms accumulates low clock extension time of slave device.
  - PEC generation/verification of hardware with ACK control
  - Support address resolution protocol (ARP)
- Compatible with the PMBus

2.15 Universal Synchronous/Asynchronous Transceiver (USART)

The N32G401 series products integrate up to 4 serial transceiver interfaces, including 2 universal synchronous/ asynchronous transceivers (USART1 and USART2) and 2 universal asynchronous transceivers (UART3 and UART4).All four interfaces provide asynchronous communication, support for IrDA SIR ENDEC transmission codec, multi-processor communication mode, single wire half-duplex communication mode, and LIN master/slave function.

The USART1 and USART2 interfaces have hardware CTS and RTS signal management, ISO7816-compatible Smartcard mode, and like SPI communication mode, all of which can use DMA operations.

Main features of USART are as follows:

- Full duplex, asynchronous communication.
- NRZ standard format.
- Fractional baud rate generator system, baud rate programmable, used for sending and receiving.
- Programmable data word length (8 or 9 bits)
- Configurable stop bit, supporting 1 or 2 stop bits.
- LIN master's ability to send synchronous interrupters and LIN slave's ability to detect interrupters. When USART hardware is configured as LIN, it generates 13-bit interrupters and detects 10/11 bit interrupters
- Output clock for synchronous transmission.
- IRDA SIR encoder decoder, supports 3/16-bit duration in normal mode;
- Smart card simulation function.
  - The smart card interface supports the asynchronous smart card protocol defined in ISO7816-3.
  - 0.5 and 1.5 stop bits for smart cards.
- Single-wire half duplex communication.
- Configurable multi-buffer communication using DMA, receiving/sending bytes in SRAM using centralized DMA buffer.
- Independent transmitter and receiver enable bits.
- Detect flag.
  - Receive buffer is full.
  - Send buffer empty.
  - Transmission complete

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- Parity control
  - Send parity bit.
  - Verify the received data.
- Four error detection flags.
  - Overflow error.
  - Noise error
  - Frame error.
  - Parity error
- 10 USART interrupt sources with flags
  - CTS change
  - LIN break detection
  - Send data register is empty.
  - Send complete.
  - Received data register is full.
  - Bus was detected to be idle.
  - Overflow error.
  - Frame error.
  - Noise error
  - Parity error
- Multi-processor communication, if the address does not match, then enter the silent mode.
- Wake up from silent mode (via idle bus detection or address flag detection)
- There are two ways to wake up the receiver: address bit (MSB, bit 9), bus idle.
- Mode configuration:

USART modes	USART1	USART2	UART3	UART4
Asynchronous mode	support	support	support	support
Hardware flow control	support	support	Does not support	Does not support
Multiple buffer communication (DMA)	support	support	support	support
Multiprocessor communication	support	support	support	support
Synchronous mode	support	support	Does not support	Does not support
Smartcard mode	support	support	Does not support	Does not support
Half Duplex (Single wire mode)	support	support	support	support
IrDA	support	support	support	support
LIN	support	support	support	support

2.16 Serial Peripheral Interface (SPI)

The device integrates two SPI interfaces, which are multiplexed with I2S interface. SPI shares resources with I2S.

SPI allows the chip to communicate with peripheral devices in a half/full duplex, synchronous, serial manner. This interface can be configured in master mode and provides a communication clock (SCK) for external slave devices. Interfaces can also work in a multi-master configuration. It can be used for a variety of purposes, including two-line

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simplex synchronous transmission using a two-way data line, and reliable communication using CRC checks.

The main features of SPI interfaces are as follows:

- 3-wire full-duplex synchronous transmission
- Two-wire simplex synchronous transmission with or without a third bidirectional data line
- 8- or 16-bit transmission frame format selection
- Master or slave operations
- Support multi-master mode
- 8 master mode baud rates prescaler coefficient (maximum $f_{PCLK}/2$)
- Slave mode frequency (maximum f_{PCLK} /2)
- Fast communication between master mode and slave mode
- NSS can be managed by software or hardware in both master and slave modes: dynamic change of master/slave modes
- Programmable clock polarity and phase
- Programmable data order, MSB before or LSB before
- Dedicated send and receive flags that trigger interrupts
- SPI bus busy flag
- Hardware CRC for reliable communication
  - In send mode, the CRC value can be sent as the last byte
  - In full-duplex mode, CRC is automatically performed on the last byte received
- Master mode failures, overloads, and CRC error flags that trigger interrupts.
- Single byte send and receive buffer with DMA capability: generates send and receive requests
- Maximum interface speed: master mode 28Mbps (without CRC), 20Mbps(with CRC), slave mode 32Mbps

2.17 Serial Audio Interface (I^2S)

I^2S is a 3-pin synchronous serial interface communication protocol. The device integrates two standard I^2S interfaces (multiplexed with SPI) and can operate in master or slave mode. The two interfaces can be configured for 16-bit, 24-bit or 32-bit transmission, or as input or output channels, supporting audio sampling frequencies from 8 KHz to 96KHz. It supports four audio standards, including Philips I^2S, MSB and LSB alignment, and PCM.

In half duplex communication, it can work in master and slave. When it acts as a master device, it provides clock signals to external slave devices through an interface.

The main features of I^2S interface are as follows:

- Simplex communication (send or receive only)
- Master or slave operations
- 8-bit linear programmable prescaler for accurate audio sampling frequencies (8 KHZ to 96KHz)
- The data format can be 16, 24, or 32 bits
- Audio channel fixed packet frame is 16 bits (16-bit data frame) or 32 bit (16, 24 or 32 bit data frame)
- Programmable clock polarity (steady state)
- The overflows flag bit in slave sending mode and the overflows flag bit in master/slave receiving mode
- 16-bit data registers are used for sending and receiving, with one register at each end of the channel

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- Supported I²S protocols:
  - I²S Philips standard
  - MSB alignment standard (left aligned)
  - LSB alignment standard (right aligned)
  - PCM standard (16-bit channel frame with long or short frame synchronization or 16-bit data frame extension to 32-bit channel frame)
- The data direction is always MSB first
- Both send and receive have DMA capability
- The master clock can be output to external audio devices at a fixed rate of 256xFs(Fs is the audio sampling frequency)

2.18 General Purpose Input/Output Interface (GPIO)

Up to 39+1 GPIO, which can be divided into four groups (GPIOA/GPIOB/GPIOC/GPIOD). Each group of GPIOA, GPIOB has 16 ports, GPIOC has 3 ports and GPIOD has 4+1 ports. Each GPIO pin can be configured by software as an output (push pull or open drain), input (with or without pull-up/pull-down), or multiplexing peripheral function port. Most GPIO pins are shared with digital or analog alternate peripherals, and some I/O pins are multiplexed with clock pins. All GPIO pins have high current passing capability except ports with analog input capability.

Main features:

- Each bit of the GPIO port can be configured separately by the software into multiple modes:
  - Input floating
  - Input pull up (weak pull up)
  - Input pull down (weak pull down)
  - Analog input
  - Open drain output
  - Push-pull output
  - Push-pull alternate function
  - Open drain alternate function.
- General I/O (GPIO)
  - During and just after reset, the alternate function is not enabled, except for BOOT0 (which is an input pull-down) and NRST pin, the I/O port is configured to analog input mode.
  - After reset, the default state of pins associated with the debug system is enable SWD-JTAG, the JTAG pin is placed in input pull-up or pull-down mode:
    - JTDI in pull-up mode
    - JTCK in drop down mode
    - JTMS in pull-up mode
    - NJTRST is placed in pull-up mode
  - When configured as output, values written to the output data registers are output to the appropriate I/O pins. Can be output in push pull mode or open drain mode
- Separate bit setting or bit clearing functions

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- External interrupt/wake up: All ports have external interrupt capability. In order to use external interrupts, ports must be configured in input mode
- Alternate function :(port configuration registers must be programmed before using default alternate function)
- GPIO lock mechanism, which freezes I/O configurations. When a LOCK is performed on a port bit, the configuration of the port bit cannot be changed until the next reset
- Precautions for using GPIO
  - When VDD and VDDA are not powered on, the voltage applied to GPIO must not exceed 3.6V
  - When the voltage applied to GPIO is 5.5V, VDD and VDDA must not be lower than 2.4V
  - If you do not want the MCU have leakage, you need to ensure that the voltage applied to the GPIO is less than or equal to VDD and VDDA
  - When the voltage applied on GPIO is greater than VDD and VDDA, if you want to reduce the leakage current of MCU, you need to connect a resistor in series with the GPIO

2.19 Analog/Digital Converter (ADC)

The device supports a 12-bit Successive Approximation Register ADC with a sampling rate of 4.7 Msps. It supports both single-ended and differential inputs, capable of measuring 16 external and 3 internal sources.

Main features:

- Support 12/10/8/6 - bit resolution configurable.
  - The maximum sampling rate at 12bit resolution is 4.2MSPS
  - The maximum sampling rate at 10bit resolution is 5.5MSPS
  - The maximum sampling rate at 8bit resolution is 6.5MSPS
  - The maximum sampling rate at 6bit resolution is 8MSPS.
- ADC clock source is divided into operating clock source, sampling clock source and timing clock source.
  - AHB_CLK can be configured as the operating clock source, up to 72MHz
  - PLL can be configured as a sampling clock source, up to 72MHZ, supports 1,2,4,6,8,10,12,16,32, 64,128,256 frequency division.
  - The AHB_CLK can be configured as the sampling clock source, up to 72MHz, and supports 1,2,4,6,8,10,12,16,32 frequency division.
  - The timing clock is used for internal timing functions and the frequency must be configured to 1MHz
- Supports timer trigger ADC sampling
- Interrupts when conversion ends, injection conversion ends, and analog watchdog events occur
- Single and continuous conversion modes
- Automatic scan mode from channel 0 to channel N
- Support for self-calibration.
- Data alignment with embedded data consistency
- Sampling intervals can be programmed separately by channel
- Both regular conversions and injection conversions have external triggering options

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- Continuous mode
- ADC power supply requirements: 2.4V to 3.6V
- ADC input range: VREF- ≤ VIN ≤ VREF+
- ADC can use DMA operations, and DMA requests are generated during regular channel conversion.
- Analog watchdog function can monitor one, multiple, or all selected channels with great precision. When the monitored signal exceeds the preset threshold, an interruption will occur.

2.20 Analog Comparator (Comp)

The device integrates up to 3 comparators. It can be used as a separate device (all ports of the comparator are plugged into the I/O) or in combination with a timer. In the case of motor control, it can be combined with the PWM output from the timer to form periodic current control.

Main features:

- Rail to rail comparators are supported
- The reverse and forward sides of the comparator support the following inputs
  - Optional I/O
  - DAC channel output
  - 64 level adjustable internal reference voltage input
- Programmable hysteresis can be configured as no hysteresis, low hysteresis, medium hysteresis, and high hysteresis
- The comparator can output to I/O or timer input for triggering
  - Capture events
  - OCREF_CLR events (for periodic current control)
  - The brake events
- The comparator supports output filtering, including analog and digital filtering
- Support comparator output with blanking, you can choose forbidden energy blanking or Timer1_OC5/Timer8_OC5 as blanking input;
- Each comparator can have interrupt wake up capability, support from Sleep mode and Stop0 mode wake up;

2.21 Temperature Sensor (TS)

The temperature sensor generates a voltage that varies linearly with temperature in the range of 2.4V <V< 3.6V. The temperature sensor is internally connected to the ADC_IN17 input channel for converting the output of the temperature sensor to digital values.

2.22 Beeper

The beeper module supports complementary outputs and can generate periodic signals to drive external passive buzzers. Used to generate a beep or the alarm.

2.23 Cyclic Redundancy Check Calculation Unit (CRC)

The device integrated CRC32 and CRC16 functthenalities. The cyclic redundancy check (CRC) calculation unit is

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based on a fixed generation polynomial to obtain arbitrary CRC calculation results. In many applications, CRC-based techniques are used to verify data transfer or storage consistency. Within the scope of the EN/IEC 60335-1 standard, it provides a means of detecting flash memory errors. The CRC unit can be used to calculate signatures of software in real time and compare them with signatures generated during the link time and generating of the software.

Main features:

- CRC16: supports polynomials $X^{16} + X^{15} + X^2 + X^0$
- CRC32: supports polynomials $X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$
- CRC16 calculation time: 1 AHB clock cycle (HCLK)
- CRC32 calculation time: 1 AHB clock cycle (HCLK)
- The initial value for cyclic redundancy computing is configurable
- Support DMA mode

2.24 Unique Device Serial Number (UID)

The N32G401 series products have two built-in unique device serial numbers of different lengths, which are 96-bit Unique Device ID (UID) and 128-bit Unique Customer ID (UCID). These two device serial numbers are stored in the system configuration block of Flash memory. The information they contain is written at the time of delivery and is guaranteed to be unique to any of the N32G401 series microcontrollers under any circumstances and can be read by user applications or external devices through the CPU or JTAG/SWD interface and cannot be modified.

The 96-bit UID is usually used as a serial number or password. When writing Flash memory, this unique identifier is combined with software encryption and decryption algorithm to further improve the security of code in Flash memory.

The UCID is 128-bit, which complies with the definition of national technology chip serial number. It contains information related to chip production and version.

2.25 Serial Single-Wire JTAG Debug Port (SWJ-DP)

The device has an embedded ARM SWJ-DP interface, which is a combination of JTAG and serial single-line debugging interface, can achieve serial single-line debugging interface or JTAG interface connection. The JTMS and JTCK signals of JTAG share pins with SWDIO and SWCLK respectively, and a special signal sequence on the JTMS pin is used to switch between JTAG-DP and SW-DP.

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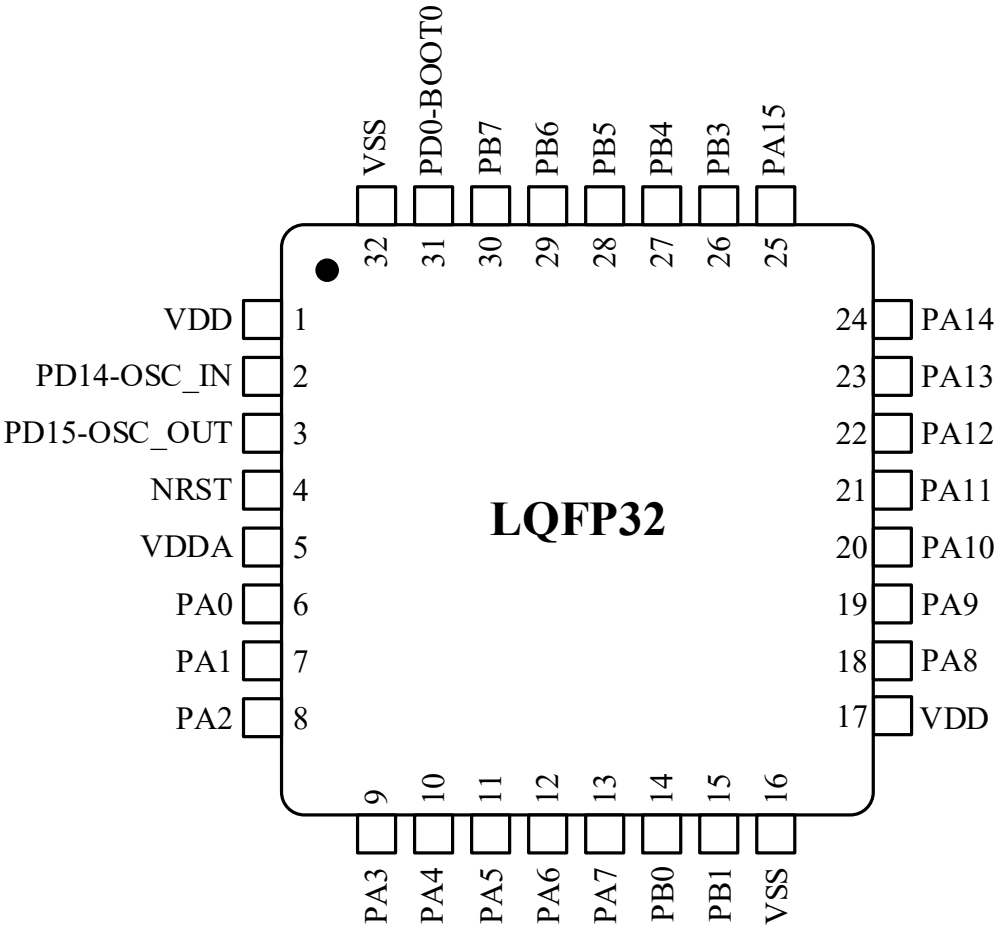
3 Pinouts And Pin Description

3.1 Pinouts

3.1.1 LQFP32

Figure 3-1 N32g401 Series LQFP32 Pinout



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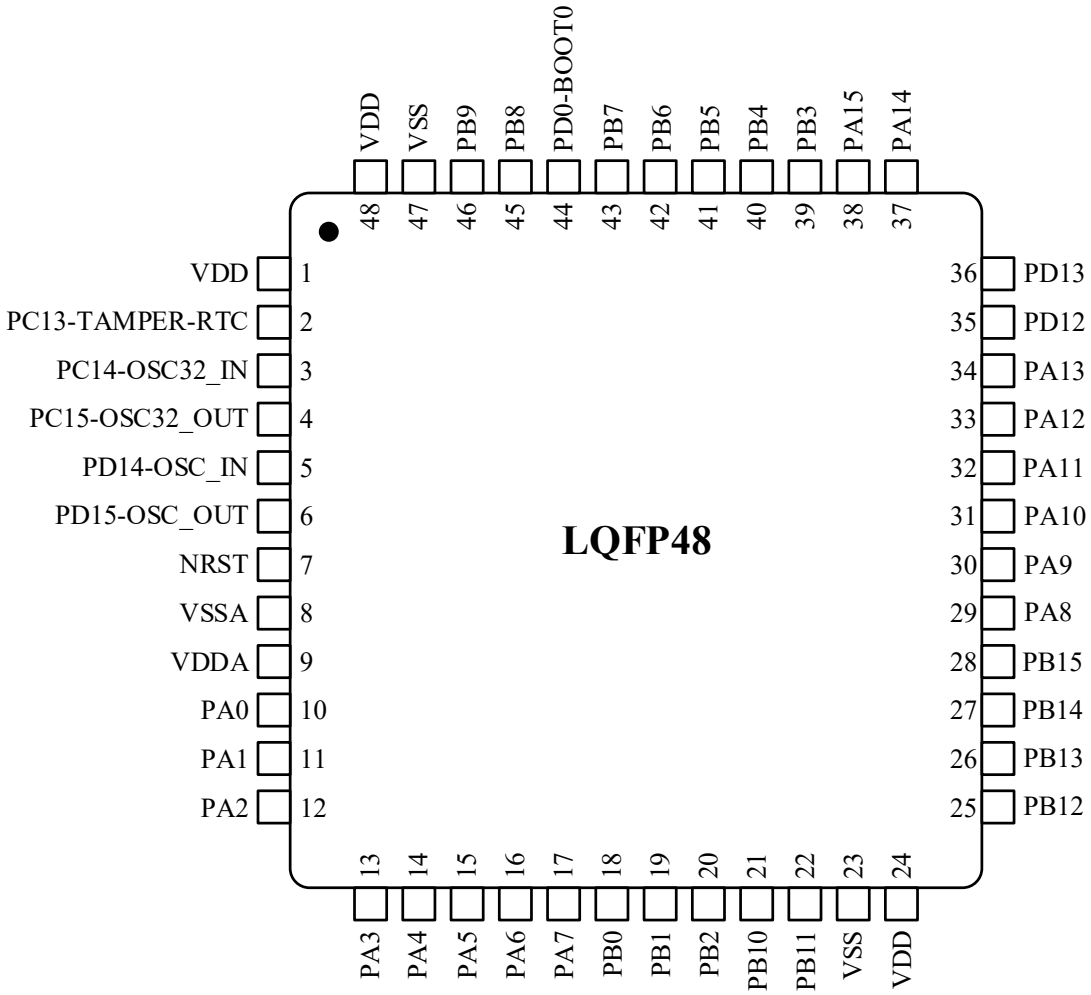
3.1.2 LQFP48

Figure 3-2 N32g401 Series LQFP48 Pinout



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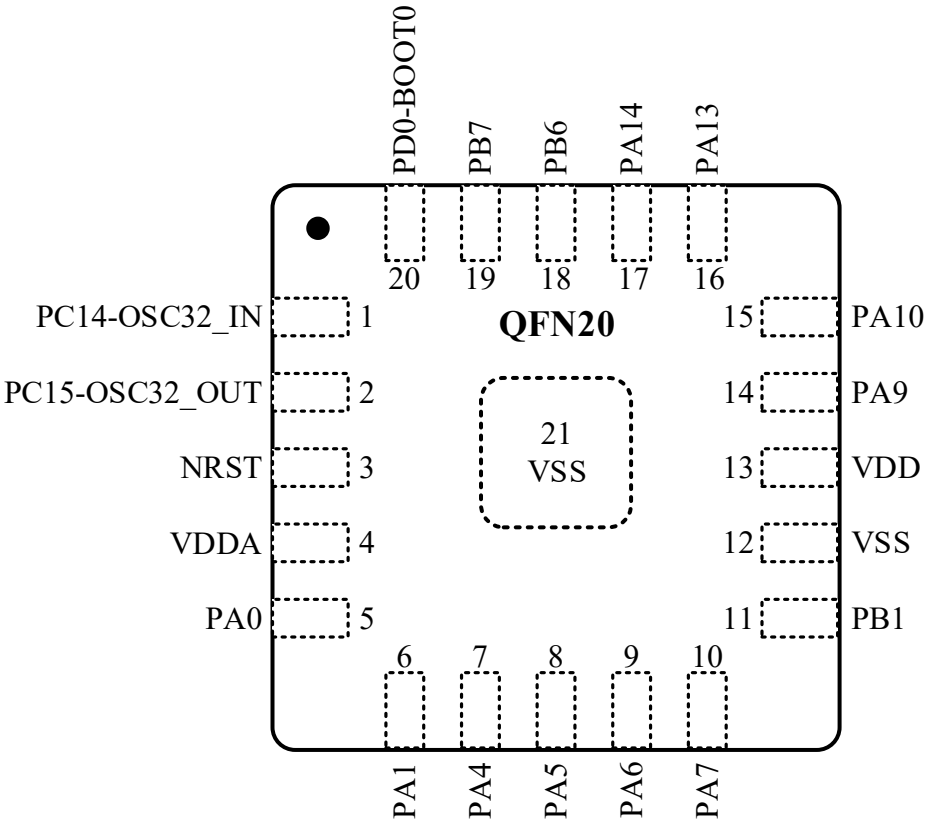
3.1.3 QFN20

Figure 3-3 N32g401 Series QFN20 Pinout



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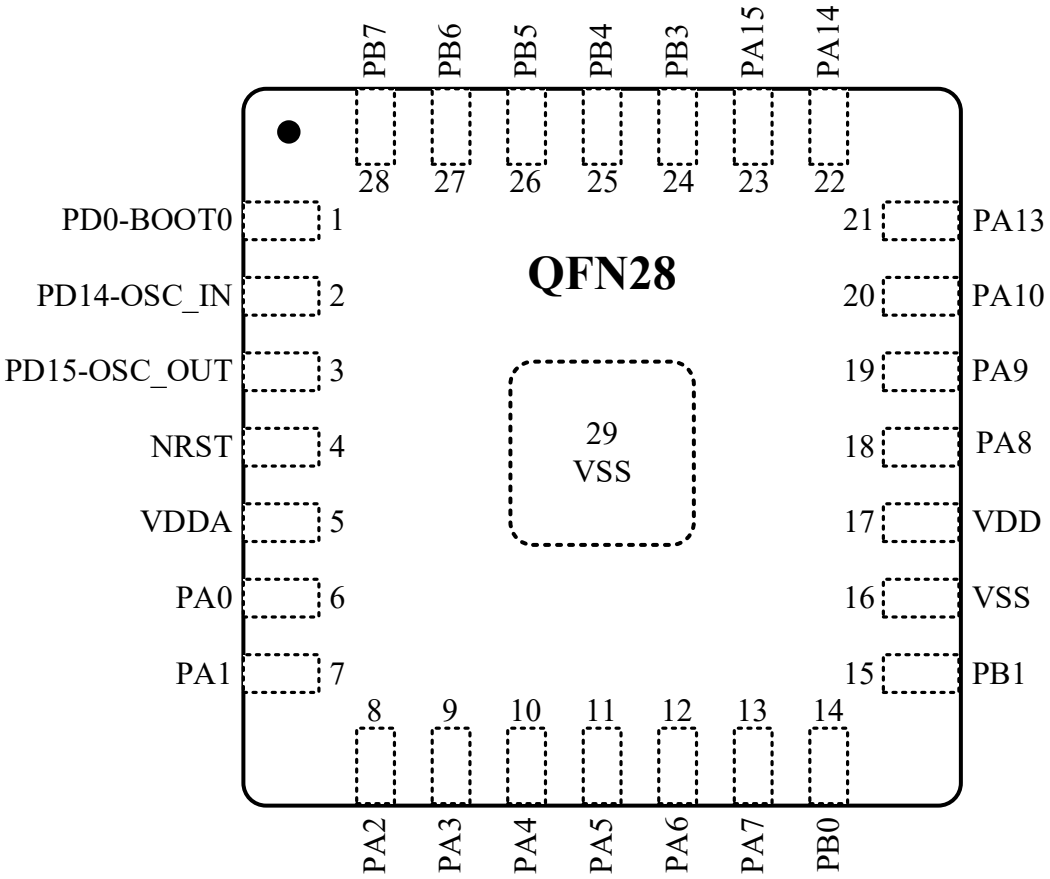
3.1.4 QFN28

Figure 3-4 N32g401 Series QFN28 Pinout



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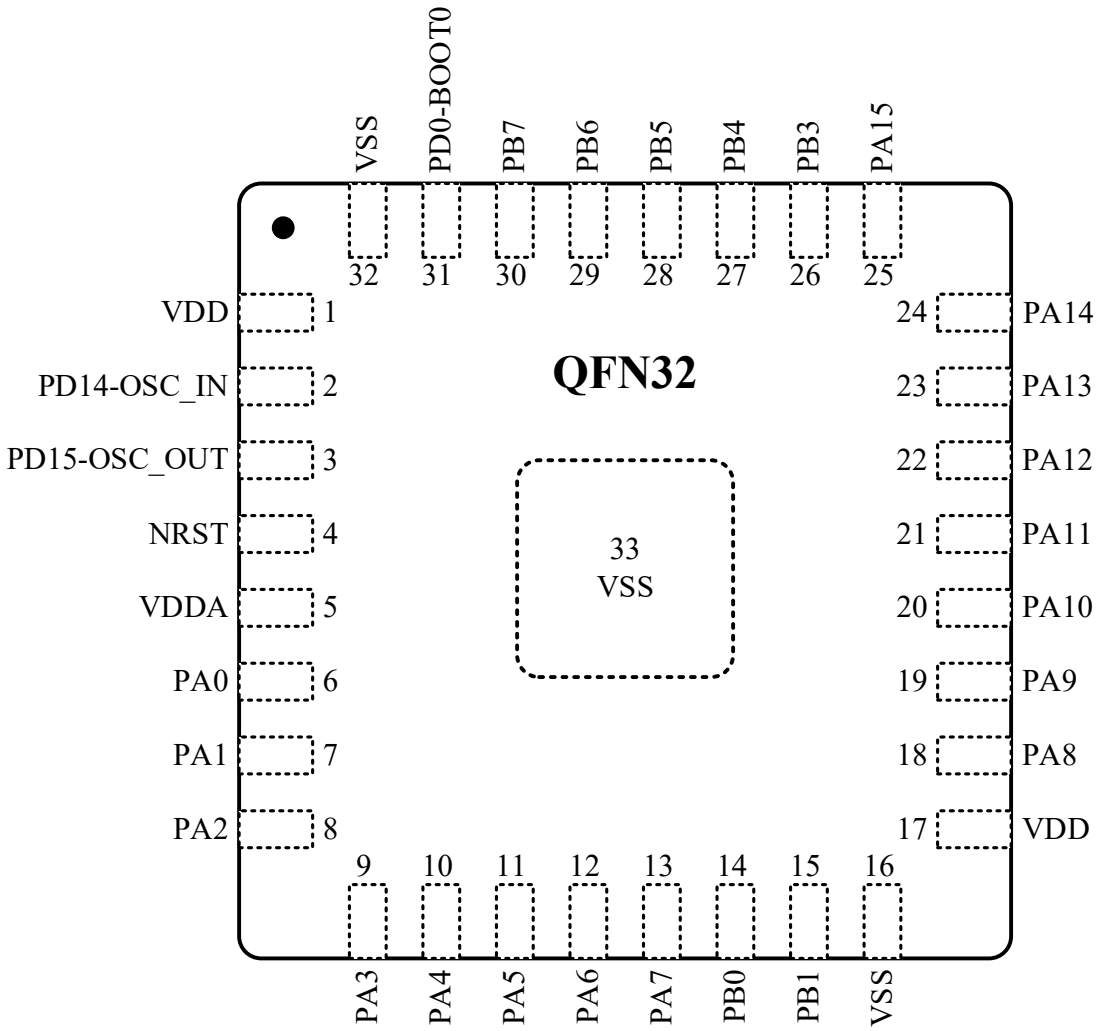
3.1.5 QFN32

Figure 3-5 N32g401 Series QFN32 Pinout



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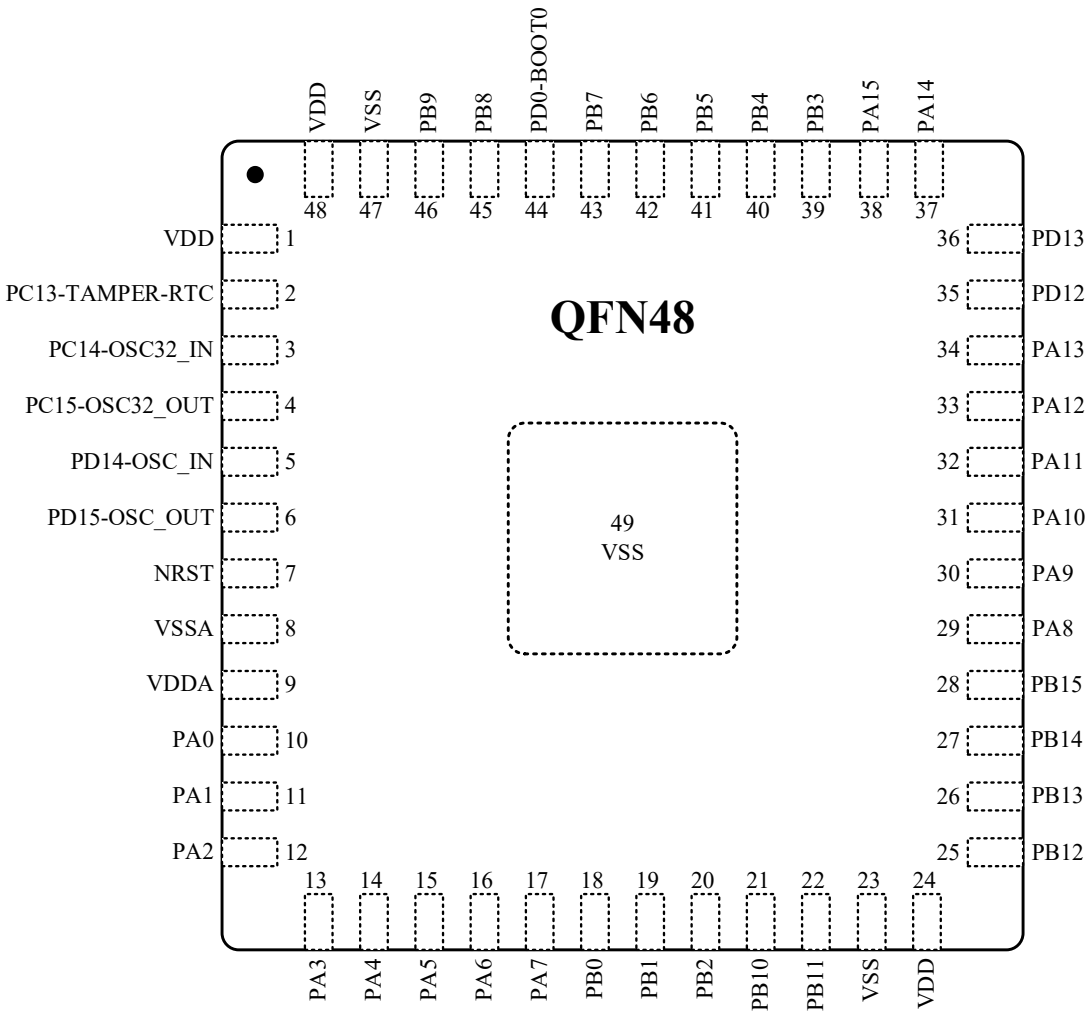
3.1.6 QFN48

Figure 3-6 N32g401 Series QFN48 Pinout



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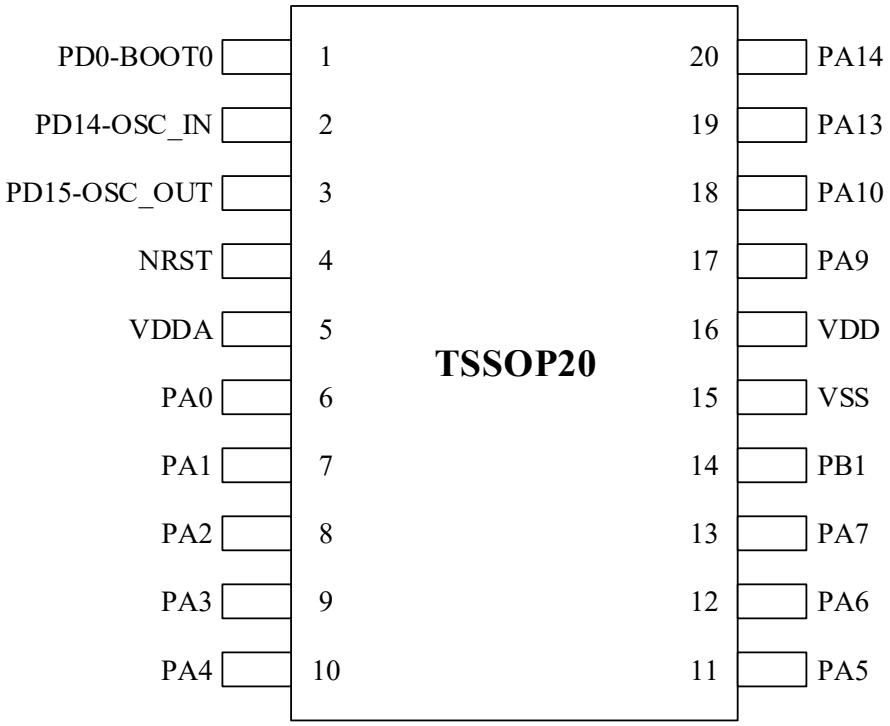
3.1.7 TSSOP20

Figure 3-7 N32g401 Series TSSOP20 Pinout



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3.2 Pin Description

Table 3-1 Pin Description

TSSOP20[8]	QFN20	QFN28	QFN32 LQFP32	QFN48 LQFP48	Pin name (after reset)	Type[1]	I/O[2]	Fail-safe[4]	Alternate functions[3]	Optional functions
-	-	-	1	1	VDD	S	-	-	-	-
-	-	-	-	2	PC13_TAMPER-RTC	I/O	FT	Y	TIM1_CH1N EVENTOUT	RTC-TAMP1 RTC_OUT WKUP3
-	1	-	-	3	PC14-OSC32_IN	I/O	FTa	Y	-	OSC32_IN
-	2	-	-	4	PC15-OSC32_OUT	I/O	FTa	Y	-	OSC32_OUT
2	-	2	2	5	PD14-OSC_IN	I/O	FTa	Y	USART2_TX I2C2_SDA TIM1_CH3N	OSC_IN
3	-	3	3	6	PD15-OSC_OUT	I/O	FTa	Y	USART2_RX I2C2_SCL TIM1_CH2N	OSC_OUT
4	3	4	4	7	NRST	I	-	-	-	-
-	-	-	-	8	VSSA/VREF-	S	-	-	-	-
5	4	5	5	9	VDDA/VREF+	S	-	-	-	-
6	5	6	6	10	PA0	I/O	FTa	Y	USART2_CTS TIM2_CH1 TIMER2_ETR TIM5_CH1 TIM8_ETR SPI1_MISO I2S1_MCK EVENTOUT COMP1_OUT TIM1_CH1 UART4_TX	ADC_IN1[5] COMP1_INM COMP1_INP WKUP2 RTC-TAMP2 COMP3_INP
7	6	7	7	11	PA1	I/O	FTa	Y	USART2_RTS TIM5_CH2 TIM2_CH2 EVENTOUT SPI1_NSS TIM1_CH1N	ADC1_IN2[5] COMP1_INP
8	-	8	8	12	PA2	I/O	FTa	Y	USART2_TX TIM5_CH3 TIM2_CH3 I2C2_SDA COMP2_OUT EVENTOUT TIM8_BKIN TIM8_CH1	ADC_IN3[5] COMP2_INM COMP1_INP
9	-	9	9	13	PA3	I/O	FTa	Y	USART2_RX TIM5_CH4 I2C2_SCL EVENTOUT TIM8_CH2	ADC_IN4[5] COMP2_INP COMP3_INM

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TSSOP20[8]	QFN20	QFN28	QFN32 LQFP32	QFN48 LQFP48	Pin name (after reset)	Type[1]	I/O[2]	Fail-safe[4]	Alternate functions[3]	Optional functions
10	7	10	10	14	PA4	I/O	FTa	Y	USART2_CK I2C1_SCL SPI1_NSS I2S1_WS USART1_TX EVENTOUT LPTIM_OUT SPI2_NSS TIM8_CH3 I2S2_WS TIM4_CH3	ADC_IN5[5] COMP1_INM COMP2_INM
11	8	11	11	15	PA5	I/O	FTa	Y	SPI1_SCK I2C1_SDA I2S1_CK USART1_RX EVENTOUT LPTIM_IN1 TIM8_CH4 TIM4_CH4	ADC_IN6[6] COMP1_INM COMP2_INM
12	9	12	12	16	PA6	I/O	FTa	Y	SPI1_MISO I2S1_MCK TIM8_BKIN TIM3_CH1 TIM1_BKIN COMP2_OUT EVENTOUT BEEPER_OUT P TIM8_CH3 USART2_TX COMP3_OUT TIM1_CH2N	ADC_IN7[6] COMP2_INM COMP2_INP
13	10	13	13	17	PA7	I/O	FTa	Y	SPI1_MOSI I2S1_SD TIM1_CH1N TIM8_CH1N TIM3_CH2 COMP2_OUT EVENTOUT USART2_RX BEEPER_OUT _N TIM1_CH4 TIM4_CH1	ADC_IN8[6] COMP2_INP COMP3_INM
-	-	14	14	18	PB0	I/O	FTa	Y	TIM1_CH2N TIM3_CH3 TIM8_CH2N UART4_TX EVENTOUT	ADC_IN9[6]
14	11	15	15	19	PB1	I/O	FTa	Y	TIM1_CH3N TIM3_CH4 TIM8_CH3N UART4_RX EVENTOUT	ADC_IN10[6] COMP3_INP

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TSSOP20[8]	QFN20	QFN28	QFN32 LQFP32	QFN48 LQFP48	Pin name (after reset)	Type[1]	I/O[2]	Fail-safe[4]	Alternate functions[3]	Optional functions
									SPI1_SCK SPI2_MOSI I2S2_SD TIM4_CH2	
-	-	-	-	20	PB2	I/O	FTa	Y	LPTIM_OUT EVENTOUT TIM3_ETR TIM1_CH4N	ADC_IN11[6] COMP3_INM
-	-	-	-	21	PB10	I/O	FTa	Y	UART3_TX I2C2_SCL TIM2_CH3 EVENTOUT COMP3_OUT TIM4_ETR	COMP1_INP ADC_IN12[6]
-	-	-	-	22	PB11	I/O	FTa	Y	UART3_RX I2C2_SDA TIM2_CH4 EVENTOUT	ADC_IN13[6] COMP3_INP
15	12	16	16	23	VSS	S	-	-	-	-
16	13	17	-	24	VDD	S	-	-	-	-
-	-	-	-	25	PB12	I/O	FTa	Y	SPI2_NSS I2S2_WS I2C2_SMBA TIM1_BKIN EVENTOUT TIM5_CH1	ADC_IN14[6]
-	-	-	-	26	PB13	I/O	FTa	Y	SPI2_SCK I2S2_CK I2C2_SCL TIM1_CH1N EVENTOUT TIM5_CH2	ADC_IN15[6]
-	-	-	-	27	PB14	I/O	FTa	Y	SPI2_MISO I2S2_MCK TIM1_CH2N I2C2_SDA EVENTOUT UART4_TX TIM8_CH1 TIM1_CH1	ADC_IN16[6] COMP3_INM
-	-	-	-	28	PB15	I/O	FTa	Y	UART4_RX SPI2_MOSI I2S2_SD TIM1_CH3N EVENTOUT RTC_REFIN TIM8_CH2 TIM8_CH1N TIM1_CH2N	COMP3_INP
-	-	-	17	-	VDD	S	-	-	-	-

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TSSOP20[8]	QFN20	QFN28	QFN32 LQFP32	QFN48 LQFP48	Pin name (after reset)	Type[1]	I/O[2]	Fail-safe[4]	Alternate functions[3]	Optional functions
-	-	18	18	29	PA8	I/O	FT	Y	USART1_CK I2C2_SMBA TIM1_CH1 I2C2_SDA SPI1_NSS I2S1_WS MCO EVENTOUT COMP3_OUT TIM1_CH2	WKUP1 RTC-TAMP3
17	14	19	19	30	PA9	I/O	FT	Y	USART1_TX I2C2_SCL TIM1_CH2 EVENTOUT TIM8_BKIN SPI2_MISO I2S2_MCK TIM1_CH3N	LPTIM_IN2 MCO
18	15	20	20	31	PA10	I/O	FT	Y	USART1_RX I2C2_SDA SPI1_SCK SPI2_SCK I2S1_CK I2S2_CK TIM1_CH3 EVENTOUT TIM1_BKIN	COMP3_OUT LPTIM_ETR RTC_REFIN
-	-	-	21	32	PA11	I/O	FTa	Y	USART1_CTS SPI2_MISO I2S2_MCK TIM1_CH4 COMP1_OUT EVENTOUT TIM4_ETR	COMP2_INP
	-	-	22	33	PA12	I/O	FTa	Y	USART1_RTS SPI2_MOSI I2S2_SD TIM1_ETR COMP2_OUT EVENTOUT	COMP1_INP
19	16	21	23	34	PA13[7]	I/O	FT	Y	SWDIO-JTMS SPI2_NSS I2S2_WS EVENTOUT SPI2_MISO	-
-	-	-	-	35	PD12	I/O	FT	Y	UART4_RX I2C1_SDA SPI2_SCK I2S2_CK EVENTOUT	-

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TSSOP20[8]	QFN20	QFN28	QFN32 LQFP32	QFN48 LQFP48	Pin name (after reset)	Type[1]	I/O[2]	Fail-safe[4]	Alternate functions[3]	Optional functions
-	=	-	-	36	PD13	I/O	FT	Y	UART4_TX I2C1_SCL EVENTOUT	-
20	17	22	24	37	PA14[7]	I/O	FT	Y	SWCLK-JTCK USART2_CK I2C1_SDA COMP2_OUT EVENTOUT SPI2_MOSI I2S2_SD	-
-	-	23	25	38	PA15	I/O	FTa	Y	JTDI USART2_CTS I2C1_SCL SPI2_NSS I2S2_WS TIM2_CH1 TIM2_ETR EVENTOUT SPI1_NSS TIM8_CH1N	COMP2_INP
-	-	24	26	39	PB3	I/O	FTa	Y	USART2_RTS SPI1_SCK I2S1_CK TIM2_CH2 JTDO EVENTOUT TIM8_CH2N	COMP1_INP COMP2_INM COMP3_INP
-	-	25	27	40	PB4	I/O	FTa	Y	USART2_TX SPI1_MISO I2S1_MCK TIM3_CH1 UART3_TX EVENTOUT TIM8_CH3 TIM1_BKIN NJTRST	COMP1_INP COMP3_OUT
-	-	26	28	41	PB5	I/O	FTa	Y	USART2_RX I2C1_SMBA SPI1_MOSI I2S1_SD TIM3_CH2 UART3_RX LPTIM_IN1 EVENTOUT TIM8_CH4 TIM8_BKIN	COMP1_INM COMP3_INP

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TSSOP20[8]	QFN20	QFN28	QFN32 LQFP32	QFN48 LQFP48	Pin name (after reset)	Type[1]	I/O[2]	Fail-safe[4]	Alternate functions[3]	Optional functions
-	18	27	29	42	PB6	I/O	FT	Y	USART1_TX I2C1_SCL SPI1_NSS I2S1_WS TIM1_CH2N TIM4_CH1 SPI2_SCK I2S2_CK LPTIM_ETR COMP1_OUT EVENTOUT TIM1_CH4 TIM8_CH3N	BEEPER_OUT_P
-	19	28	30	43	PB7	I/O	FTa	Y	USART1_RX I2C1_SDA TIM4_CH2 EVENTOUT LPTIM_IN2 BEEPER_OUT_N TIM8_ETR TIM1_CH4N SPI2_MISO I2S2_MCK	COMP2_INP
1	20	1	31	44	BOOT0/PD0	I/O	FT	Y	-	-
-	-	-	-	45	PB8	I/O	FT	Y	I2C1_SCL TIM4_CH3 USART1_TX UART3_TX COMP1_OUT EVENTOUT TIM8_CH3	-
-	-	-	-	46	PB9	I/O	FT	Y	I2C1_SDA TIM4_CH4 UART3_RX COMP2_OUT EVENTOUT TIM1_CH4	-
-	-	-	32	47	VSS	S	-	-	-	-
-	-	-	-	48	VDD	S	-	-	-	-

Notes:

1. *I = input, O = output, S = power supply*
2. *FT: 5V tolerant, FTa: 5V tolerant, with Analog function*
3. *This alternate function can be configured by the software to other pins (if the corresponding package model has such pins). For details, refer to the I/O and debugging Settings sections of the alternate function in the N32G401xx user Reference manual.*
4. *Fail-safe indicates that when the chip has no power input, a high input level is added to the IO. The high input level does not flood into the chip, resulting in a certain voltage on the power supply and current consumption.*

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5. *The corresponding ADC channel is a fast channel and supports a maximum sampling rate of 4.2MSPS(12Bit).*
6. *The corresponding ADC channel is a slow channel, supporting a maximum sampling rate of 3.6MSPS(12Bit).*
7. *If MCU will enter STANDBY mode, before entering the STANDBY mode, if pins PA13 and PA14 are used as non-debug pins ,and configured as input mode, it is necessary to add strong pull-down resistance on pins PA13 and PA14. The pull-down resistance is recommended to be within 10KΩ.*
8. *TSSOP20 package dose not support COMP module.*

For the FT and FTa ports in the table, it is necessary to ensure that the voltage difference between the IO voltage and the power supply voltage is less than 3.6V

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4 Electrical Characteristics

4.1 Parameter Conditions

All voltages are based on V_{SS} unless otherwise specified.

4.1.1 Minimum And Maximum Values

Unless otherwise specified, all minimums and maximums will be guaranteed under the worst ambient temperature, supply voltage and clock frequency conditions by performing tests on 100% of the product on the production line at ambient temperatures T_A=25°C.

Note at the bottom of each form that data obtained through characterization results, design simulation and/or process characteristics will not be tested on the production; based on characterization, the minimum and maximum values are obtained by taking the average of the samples tested and adding or subtracting three times the standard distribution (mean ±3σ).

4.1.2 Typical Numerical Values

Unless otherwise specified, typical data are based on T_A=25°C and V_{DD}=3.3V (2.4V ≤ V_{DD} ≤ 3.6V voltage range). These data are for design guidance only and not tested.

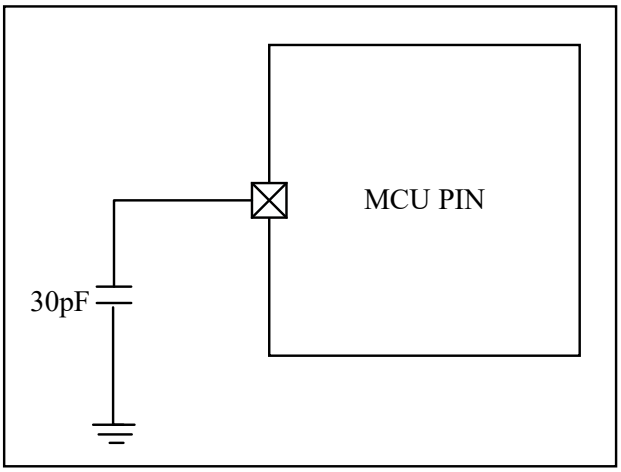
4.1.3 Typical Curve

Unless otherwise specified, typical curves are for design guidance only and not tested.

4.1.4 Loading Capacitor

The load conditions for measuring pin parameters are shown in Figure 4-1.

Figure 4-1 Pin Loading Conditions



4.1.5 Pin Input Voltage

The measurement of the input voltage on the pin is shown in Figure 4-2.

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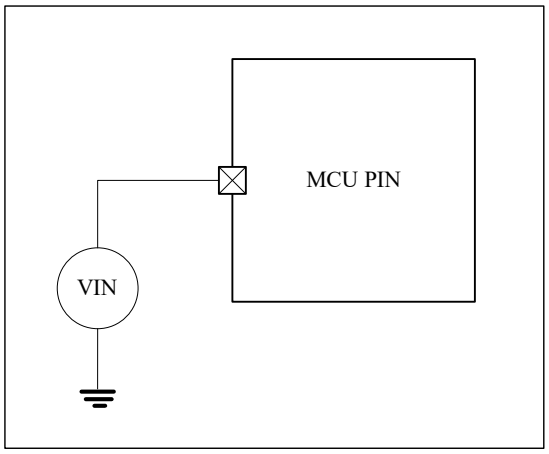
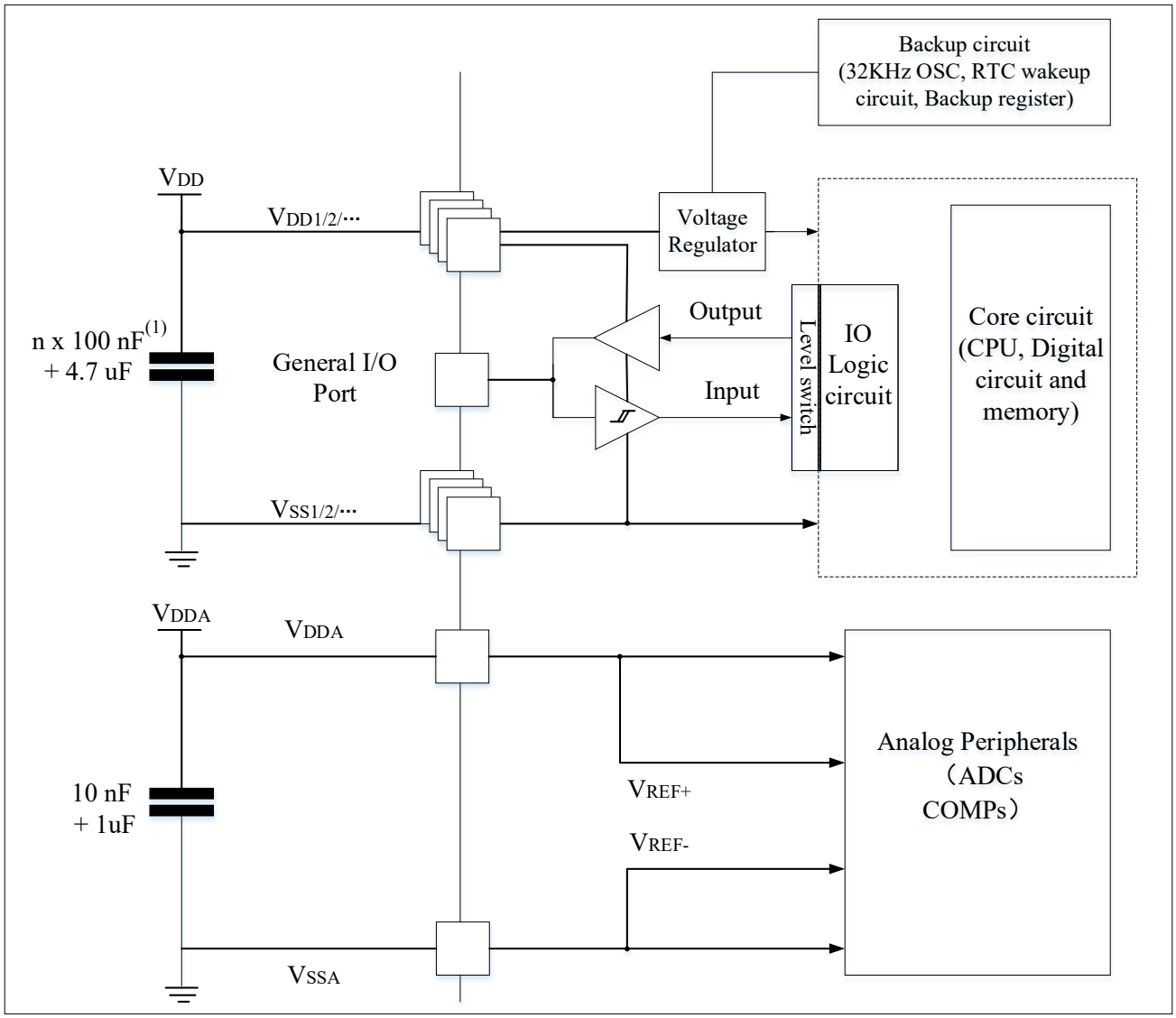
Figure 4-2 Pin Input Voltage



4.1.6 Power Supply Scheme

Figure 4-3 Power Supply Scheme



Note: (1) n is the count of V_{DD}.

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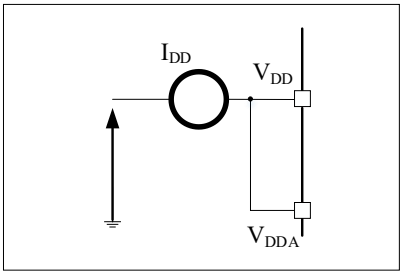
Please refer to the hardware design guide for the capacitor connection method.

4.1.7 Current Consumption Measurement

Figure 4-4 Current Consumption Measurement Scheme



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4.2 Absolute Maximum Rating

The load applied to the device may permanently damage the device if it exceeds the values given in the Absolute maximum rating list (Table 4-1, Table 4-2, Table 4-3). The maximum load that can be sustained is only given here, and it does not mean that the functional operation of the device under such conditions is correct. The reliability of the device will be affected when the device works for a long time under the maximum condition.

Table 4-1 Voltage Characteristics

Symbol	Describe	Min	Max	Unit
V_{DD}- V_{SS}	External main supply voltage (including V_{DD} and V_{DDA})(1)	-0.3	4.0	V
V_{IN}	Input voltage on 5V tolerant pins(3)	V_{SS} - 0.3	5.5	
	Input voltage on other pins(2)	V_{SS} - 0.3	V_{DD} + 0.3	
$\|\Delta V_{DDx}\|$	Voltage difference between different supply pins	-	50	mV
$\|V_{SSX}- V_{SS}\|$	Voltage difference between different ground pins	-	50	
$V_{ESD(HBM)}$	ESD Electrostatic discharge voltage (human body model)	See section 4.3.11		

Note:

(1) All power (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply system within permissible limits.

(2) V_{IN} shall not exceed its maximum value. Refer to Table 4-2 for current characteristics.

(3) When 5.5V is applied to the 5V tolerant pin, V_{DD} cannot be less than 2.25V.

Table 4-2 Current Characteristics

Symbol	Describe	Max (1)	Unit
I_{VDD}	Total current through V_{DD}/V_{DDA} power line (supply current) (1) (4)	150	mA
I_{VSS}	Total current through V_{SS} ground line (outflow current) (1) (4)	150	
I_{IO}	Output current sunk by I/O and control pin	12	
	Output current source by I/O and control pin	-12	
$I_{INJ(PIN)}$(2)(3)	Injection current on NRST pin	-5/0	
	Injection current on other pins	±5	

Notes:

(1) All power (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply system within permissible limits.

(2) When $V_{IN}>V_{DD}$, there is a forward injection current; when $V_{IN}<V_{SS}$, there is a reverse injection current. $I_{INJ(PIN)}$ should not exceed its maximum value. Voltage characteristics refer to Table 4-1.

(3) Reverse injection current can interfere with the analog performance of the device. See section 4.3.17.

(4) When the maximum current occurs, the maximum allowable voltage drop of V_{DD} is 0.1V_{DD}.

Table 4-3 Temperature Characteristics

Symbol	Describe	Value	Unit
T_{STG}	Storage temperature range	- 40 ~ + 150	℃
T_J	Maximum junction temperature	125	℃

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4.3 Operating Conditions

4.3.1 General Operating Conditions

Table 4-4 General Operating Conditions

Symbol	Parameter	Condition	Min	Max	Unit
f_{HCLK}	Internal AHB clock frequency	-	0	72	MHz
f_{PCLK1}	Internal APB1 clock frequency	-	0	32(2)	
f_{PCLK2}	Internal APB2 clock frequency	-	0	64(2)	
V_{DD}	Standard operating voltage	-	2.4	3.6	V
V_{DDA}	Analog operating voltage	Must be the same potential as V_{DD}(1)	2.4	3.6	V
T_A	Ambient temperature(temperature number 7)	7 suffix version	- 40	105	℃
T_J	Junction temperature range	7 suffix version	- 40	125	℃

Notes:

(1) It is recommended that the same power supply be used to power the V_{DD} and V_{DDA}. During power-on and normal operation, a maximum of 300mV difference is allowed between the V_{DD} and V_{DDA}.

(2) If APB1 and APB2 are running at the highest frequency, the system clock needs to be reduced to 64MHz.

4.3.2 Operating Conditions at Power-On and Power-Off

The parameters given in the following table are based on the ambient temperatures listed in Table 4-4.

Table 4-5 Operating Conditions at Power-On And Power-Off

Symbol	Parameter	Condition	Min	Max	Unit
t_{VDD}	V_{DD} rise time rate	Supply voltage goes from 0 to V_{DD}	20	∞	μs/V
	V_{DD} fall time rate	Supply voltage drops from V_{DD} to 0	80	∞	

4.3.3 Embedded Reset and Power Control Module Characteristics

The parameters given in the following table are based on the ambient temperature and V_{DD} supply voltage listed in Table 4-4.

Table 4-6 Features of Embedded Reset And Power Control Modules

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{PVD}	Programmable voltage detector level selection (PWR_CTRL.MSB = 0)	PRS[2:0]=011 (rising)	2.38	2.48	2.58	V
		PRS[2:0]=011 (falling)	2.28	2.38	2.48	V
		PRS[2:0]=100 (rising)	2.47	2.58	2.69	V
		PRS[2:0]=100 (falling)	2.37	2.48	2.59	V
		PRS[2:0]=101 (rising)	2.57	2.68	2.79	V
		PRS[2:0]=101 (falling)	2.47	2.58	2.69	V
		PRS[2:0]=110 (rising)	2.66	2.78	2.9	V
		PRS[2:0]=110 (falling)	2.56	2.68	2.8	V
		PRS[2:0]=111 (rising)	2.76	2.88	3	V
		PRS[2:0]=111 (falling)	2.66	2.78	2.9	V
	Programmable voltage	PRS[2:0]=100 (rising)	3.15	3.28	3.41	V

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Symbol	Parameter	Conditions	Min	Typ	Max	Unit
	detector level selection (PWR_CTRL.MSB = 1)	PRS[2:0]=100 (falling)	3.05	3.18	3.31	V
		PRS[2:0]=101 (rising)	3.24	3.38	3.52	V
		PRS[2:0]=101 (falling)	3.15	3.28	3.41	V
		PRS[2:0]=110 (rising)	3.34	3.48	3.62	V
		PRS[2:0]=110 (falling)	3.24	3.38	3.52	V
		PRS[2:0]=111 (rising)	3.44	3.58	3.72	V
		PRS[2:0]=111 (falling)	3.34	3.48	3.62	V
$V_{PVDhyst}$(1)	PVD hysteresis	-	-	100	-	mV
$V_{POR/PDR}$	VDD Power on/down Reset threshold	Falling edge	1.625	1.856	2.179	V
		Rising edge	1.648	1.893	2.236	
$V_{PDRhyst}$(1)	PDR hysteresis	-	22	36	58	mV
$T_{RSTTEMPO}$(1)	Reset temporization	-	-	0.8	4	ms

Note: (1)Guaranteed by design, not tested in production.

4.3.4 Embedded Reference Voltage

The parameters given in the following table are based on the ambient temperature and V_{DD} supply voltage listed in Table 4-4.

Table 4-7 Built-In Reference Voltage

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{REFINT}	Internal reference voltage	-40 ℃ < T_A < + 105 ℃	1.164	1.2	1.236	V
$T_{S\_vrefint}$(1)	The sampling time of the ADC when reading the internal reference voltage	-	-	5	17(2)	µs
V_{RERINT}(2)	Internal reference voltage spread over the temperature range	V_{DD}=3.3V±10mV	-	-	10	mV
T_{Coeff}(2)	Temperature coefficient	-	-	-	48	ppm/℃

Note:

(1) The shortest sampling time is obtained through multiple loops in the application.

(2) Guaranteed by design, not tested in production.

4.3.5 Power Supply Current Characteristics

The current consumption is a combination of several parameters and factors, including operating voltage, ambient temperature, load of I/O pins, software configuration of the product, operating frequency, I/O pin toggle rate, program location in memory, and code executed.

The measurement method of current consumption is described in Figure 4-4.

All of the current consumption measurements given in this section are while executing a reduced set of code.

4.3.5.1 Maximum current consumption

The device is under the following conditions:

- All I/O pins are in input mode and are connected to a static level -- V_{DD} or V_{SS} (no load).
- All peripherals are disabled except otherwise noted.
- The access time of the Flash memory is adjusted to the fastest operating frequency (0 waiting periods from 0 to

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32MHz, 1 waiting period from 32 to 64MHz, 2 waiting periods from 64MHz to 72MHz)(1), (0 waiting periods from 0 to 39MHz, 1 waiting period from 39 to 72MHz)(2).

- Instruction prefetch is enabled (note: this parameter must be set before setting the clock and bus divider).
- When the peripheral is enable: $f_{PCLK1} = f_{HCLK}$ /4, $f_{PCLK2} = f_{HCLK}$ /2.
- V_{DD}=3.63V, ambient temperature equal to 105℃

Notes:

(1) Applicate to C version

(2) Applicate to D version

The parameters given in Table 4-8 and Table 4-Typical Current Consumption in Sleep Mode when executing code in Embedded Flash Memory are based on the test at ambient temperature and VDD supply voltage listed in Table 4-4.

Table 4-8 Typical Current Consumption in Operating Mode when executing code in Embedded Flash Memory

Symbol	Parameter	Conditions	f_{HCLK}	Typ(1)	Unit
				VDD=3.63V, T_A = 105℃	
I_{DD}(2)	Supply current in operating mode Supply current in operatingmode	External clock, enable all peripherals	72MHz	9.58	mA
			64MHz	8.92	
			32MHz	6.25	
			16MHz	4.92	
			8MHz	4.30	
		External clock, disable all peripherals	72MHz	7.92	
			64MHz	7.43	
			32MHz	5.51	
			16MHz	4.55	
			8MHz	4.02	
I_{DD}(2)	Supply current in operating mode	Internal clock, enable all peripherals	72MHz	7.25	mA
			64MHz	6.54	
			32MHz	3.73	
			16MHz	2.34	
			8MHz	1.69	
		Internal clock, disable all peripherals	72MHz	5.49	
			64MHz	4.98	
			32MHz	2.95	
			16MHz	1.95	
			8MHz	1.39	

Notes:

(1) Evaluated by characterization, not tested in production.

(2) PLL is enabled when f_{HCLK} >8MHz.

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Table 4-Typical Current Consumption in Sleep Mode when executing code in Embedded Flash Memory

Symbol	Parameter	Conditions	f_{HCLK}	Typ (1)	Unit
				VDD=3.63V, T_A = 105℃	
I_{DD}(2)	Supply current in sleep mode	External clock, enable all peripherals	72MHz	7.59	mA
			64MHz	7.14	
			32MHz	5.35	
			16MHz	4.47	
			8MHz	4.08	
		External clock, disable all peripherals	72MHz	5.74	
			64MHz	5.50	
			32MHz	4.54	
			16MHz	4.06	
			8MHz	3.77	
I_{DD}(2)	Supply current in sleep mode	Internal clock, enable all peripherals	72MHz	5.15	mA
			64MHz	4.68	
			32MHz	2.80	
			16MHz	1.87	
			8MHz	1.45	
		Internal clock, disable all peripherals	72MHz	3.21	
			64MHz	2.96	
			32MHz	1.94	
			16MHz	1.44	
			8MHz	1.14	

Notes:

(1) Based on characterization, not tested in production.

(2) PLL is enabled when f_{HCLK}>8MHz.

4.3.5.2 Typical current consumption

MCU is under the following conditions:

- All I/O pins are in input mode and are connected to a static level -- V_{DD} or V_{SS} (no load).
- All peripherals are disabled unless otherwise noted.
- The access time of the Flash memory is adjusted to the fastest operating frequency (0 waiting periods from 0 to 32MHz, 1 waiting period from 32 to 64MHz, 2 waiting periods from 64MHz to 72MHz) (1), (0 waiting periods from 0 to 39MHz, 1 waiting period from 39 to 72MHz)(2).
- Ambient temperature and V_{DD} supply voltage conditions are listed in Table 4-4.
- Instruction prefetch is enabled (note: this parameter must be set before setting the clock and bus divider).When the peripheral is turned on: $f_{PCLK1} = f_{HCLK}$ /4, $f_{PCLK2} = f_{HCLK}$ /2, $f_{ADCCLK} = f_{HCLK}$ /2.

Notes:

1. *Applicate to C version*
2. *Applicate to D version*

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Table 4-9 Typical Current Consumption in Operating Mode when executing code in Embedded Flash Memory

Symbol	Parameter	Conditions	f_{HCLK}	Typ(1)		Unit
				Enable all peripherals	Disable all peripherals	
I_{DD}(2)	Supply current in operation mode	External clock	72MHz	8.08	6.38	mA
			64MHz	7.40	5.92	
			32MHz	4.75	4.02	
			16MHz	3.45	3.05	
			8MHz	2.81	2.52	
I_{DD}(2)	Supply current in operation mode	Internal clock	72MHz	6.75	4.98	mA
			64MHz	6.04	4.47	
			32MHz	3.25	2.51	
			16MHz	1.92	1.52	
			8MHz	1.29	0.97	

Note:

(1) Typical values are measured at T_A = 25℃ and V_{DD} = 3.3V.

(2) PLL is enabled when f_{HCLK} > 8MHz.

Table 4-10 Typical Current Consumption In Sleep Mode

Symbol	Parameter	Condition	f_{HCLK}	Typ (1)		Unit
				Enable all peripherals(2)	Disable all peripherals	
I_{DD}(3)	Supply current in sleep mode	External clock	72MHz	6.07	4.25	mA
			64MHz	5.64	4.01	
			32MHz	3.86	3.05	
			16MHz	2.98	2.57	
			8MHz	2.58	2.28	
I_{DD}(3)	Supply current in sleep mode	Internal clock	72MHz	4.65	2.75	mA
			64MHz	4.19	2.53	
			32MHz	2.36	1.54	
			16MHz	1.45	1.01	
			8MHz	1.03	0.72	

Note:

(1) Typical values are measured at T_A = 25℃ and V_{DD} = 3.3V.

(2) When ADC is on, 0.2mA (1MSPS) additional current consumption is added. In the application environment, this part of the current is increased only when the ADC is turned ON (set ADC_CTRL2.ON bit).

(3) PLL is enabled when F_{HCLK} > 8MHz.

4.3.5.3 Low power mode current consumption

The device is under the following conditions:

- All I/O pins are in input mode and are connected to a static level of --V_{DD} or V_{SS} (no load).
- All peripherals are off unless otherwise noted.

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Table 4-11 Typical Current Consumption In Shutdown And Standby Mode

Symbol	Parameter	Condition	Typ(1)			Unit
			V_{DD} = 3.3 V T_A = -40 ℃	V_{DD} = 3.3 V T_A = 25 ℃	V_{DD} = 3.3 V T_A = 105℃	
I_{DD_STOP0}	Supply current in Stop mode 0 (STOP0)	The voltage regulator is in operation mode, low-speed and high-speed internal RC oscillators and high-speed external oscillators are off (Independent watchdog is off)	180	212.3	700	μA
		The voltage regulator is in low power consumption mode, and the low-speed and high-speed internal RC oscillators and high-speed external oscillators are off (Independent watchdog is off)	42	52.7	420	
I_{DD_STOP0}	Supply current in Stop mode 2 (STOP2)	Low-speed external RC oscillator is on, RTC is running, SRAM retention, all I/O states retention, and the independent watchdog is off	2.01	6.0	63.11	
		Low-speed internal RC oscillator is on, RTC is running, SRAM retention, all I/O states retention, and the independent watchdog is off	1.76	5.77	62.77	
$I_{DD\_STANDBY}$	Supply current in STANDBY mode	Low-speed external RC oscillator and independent watchdog are on, RTC is running , SRAM retention	1.28	2.42	20.51	
		Low-speed external RC oscillator is on, RTC is running , SRAM retention, independent watchdog is off	1.23	2.33	20.4	
		Low-speed external RC oscillator is on, RTC is running , SRAM not retention, independent watchdog is off	0.94	1.96	19.89	
		Low-speed external RC oscillator is on, RTC is off , SRAM not retention, independent watchdog is off	0.81	1.78	19.62	

Note: (1) Based on comprehensive evaluation result, not tested in production.

4.3.6 External Clock Source Characteristics

4.3.6.1 High-speed external clock source (HSE)

The characteristic parameters in the following table are measured using a high-speed external clock source, and the ambient temperature and supply voltage refer to the conditions specified in Table 4-4.

Table 4-12 High-Speed External User Clock Features

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSE_ext}	User external clock frequency(1)	-	4	8	32	MHz
V_{HSEH}	OSC_IN Input pin high level voltage(1)		0.8V_{DD}	-	V_{DD}	V
V_{HSEL}	OSC_IN Input pin low level voltage(1)		V_{SS}	-	0.2V_{DD}	
$t_{w(HSE)}$	Time when OSC_IN is high or low(1)		16	-	-	ns
$t_{r(HSE)}$ $t_{f(HSE)}$	OSC_IN rise or fall time(1)		-	-	20	

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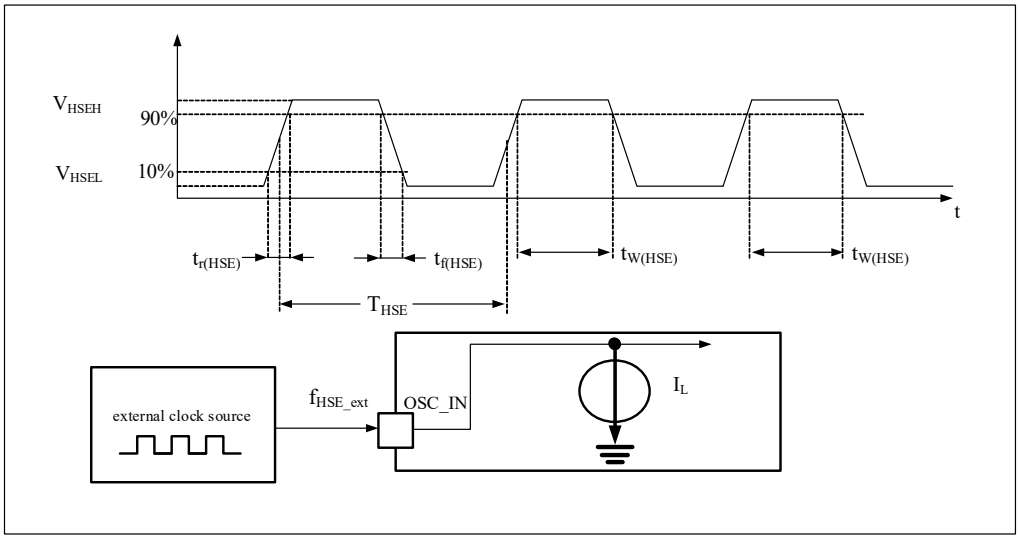
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$DuCy_{(HSE)}$	Duty cycle(1)	-	45	-	55	%
I_L	OSC_IN Input leakage current(1)	$V_{SS} \leq V_{IN} \leq V_{DD}$	-1	-	+1	μA

Note: (1) Guaranteed by design, not tested in production.

Figure 4-5 Ac Timing Diagram Of An High-Speed External Clock Source



4.3.6.2 Low-speed external clock source (LSE)

The characteristic parameters given in the following table are measured using a low-speed external clock source, and the ambient temperature and supply voltage refer to the conditions specified in Table 4-4.

Table 4-13 Features Of A Low-Speed External User Clock

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSE_ext}	User external clock frequency(1)	-	0	32.768	1000	KHz
V_{LSEH}	OSC32_IN input pin high level voltage(1)		$0.5V_{DD}$	-	V_{DD}	V
V_{LSEL}	OSC32_IN input pin low level voltage(1)		V_{SS}	-	200	mV
$t_{w(LSE)}$ $t_{w(LSE)}$	OSC32_IN high or low time(1)		450	-	-	ns
$t_{r(LSE)}$ $t_{f(LSE)}$	OSC32_IN rise or fall time(1)		-	-	50	
$DuCy_{(LSE)}$	Duty cycle(1)	-	30	-	70	%
I_L	OSC32_IN input leakage current(1)	$V_{SS} \leq V_{IN} \leq V_{DD}$	-1	-	+1	μA

Note: (1) Guaranteed by design, not tested in production.

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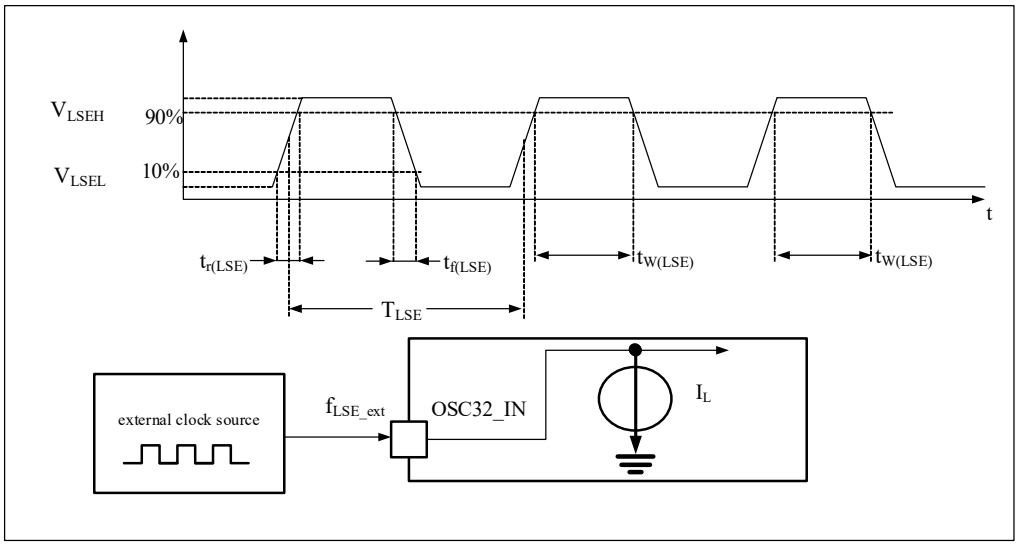
Figure 4-6 Ac Timing Diagram of an External Low Speed Clock Source



High-speed external clock generated using a crystal/ceramic resonator

High speed external clocks (HSE) can be generated using an oscillator consisting of a 4~32MHz crystal/ceramic resonator. The information presented in this section is based on a comprehensive feature evaluation using typical external components listed in the table below. In applications, the resonator and load capacitance must be as close to the oscillator pins as possible to reduce output distortion and stabilization time at startup. For detailed crystal resonator parameters (frequency, package, accuracy, etc.), please consult the appropriate manufacturer. (The crystal resonator mentioned here is usually referred to as passive crystal oscillator)

Table 4-14 HSE 4~32mhz Oscillator Characteristics (1)(2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{OSC_IN}	Oscillator frequency		4	8	32	MHz
R_F	Feedback resistor		-	160	-	K Ω
i_2	HSE driving current	V_{DD} = 3.3 V, V_{IN} = V_{SS} 30 pF load	-	1.7	-	mA
g_m	Oscillator transconductance	Startup	-	10	-	mA/V
$t_{SU(HSE)}$ (3)	Startup time (8M crystal)	V_{DD} is stabilized	-	7	-	ms

Notes:

(1) The characteristic parameters of the resonator are given by the crystal/ceramic resonator manufacturer.

(2) Guaranteed by design, not tested in production.

(3) $t_{SU(HSE)}$ is the start time, from the time when HSE is enabled by the software to the time when a stable 8MHz oscillation is obtained. This value is measured on a standard crystal resonator and can vary widely depending on the crystal manufacturer.

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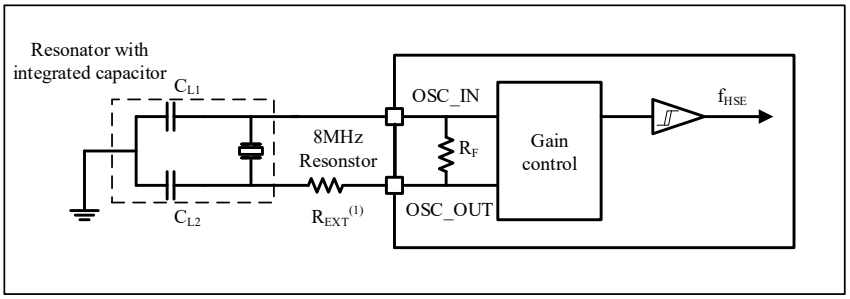
Figure 4-7 Typical Application Using 8mhz Crystal



Note: (1) The R_{EXT} value depends on the properties of the crystal.

Low-speed external clock generated by a crystal/ceramic resonator

The low speed external clock (LSE) can be generated using an oscillator consisting of a 32.768 KHz crystal/ceramic resonator. The information presented in this section is based on a comprehensive feature evaluation using typical external components listed in Table 4-15. In applications, the resonator and load capacitance must be as close to the oscillator pins as possible to reduce output distortion and stabilization time at startup. For detailed crystal resonator parameters (frequency, package, accuracy, etc.), please consult the appropriate manufacturer. (The crystal resonator mentioned here is usually referred to as passive crystal oscillator)

Note: For C_{L1} and C_{L2}, it is recommended to use high quality ceramic dielectric containers. Usually C_{L1} and C_{L2} have the same parameters. Crystal manufacturers usually give parameters for load capacitance as serial combinations of C_{L1} and C_{L2}.

Load capacitance C_L is calculated by the following formula: $C_L = C_{L1} \times C_{L2} / (C_{L1} + C_{L2}) + C_{stray}$, where C_{stray} is the capacitance of the pin and the PCB or PCB-related capacitance.

For example: If a resonator with load capacitance C_L=6pF is selected and C_{stray}=2pF, then C_{L1}=C_{L2}=8pF.

Table 4-15 LSE Oscillator Characteristics (F_{lse} =32.768 Khz) (1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R_F	Feedback resistor	-	-	5	-	MΩ
g_m	Oscillator transconductance	-	-	15	-	μA/V
$t_{SU(LSE)}$(2)	Startup time	V_{DD} is stabilized	-	1	-	s

Note:

(1) Guaranteed by design, not tested in production.

(2) $t_{SU(LSE)}$ is the startup time, which is the period from the LSE enabled by the software to the stable 32.768kHz oscillation. This value is measured on a standard crystal resonator and can vary widely depending on the crystal manufacturer.

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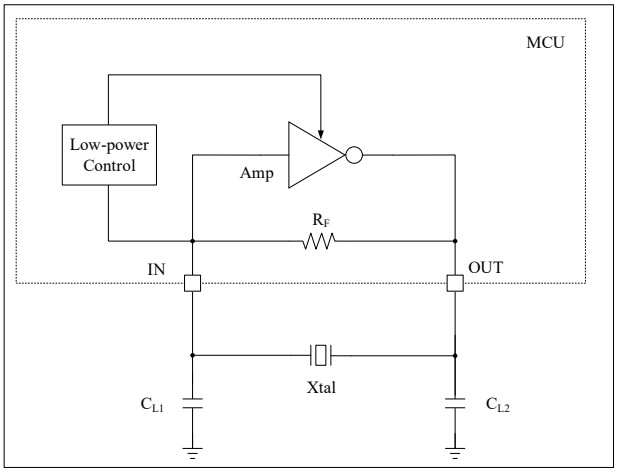
Figure 4-8 Typical Application Of 32.768khz Crystal(1)



Note: (1) Please refer to the Crystal Selection Guide.

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4.3.7 Internal Clock Source Characteristics

The characteristic parameters given in the following table were measured using ambient temperature and supply voltage in accordance with Table 4-4.

4.3.7.1 High speed internal (HSI) RC oscillator

Table 4-16 Hsi Oscillator Characteristics (1)(2)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{HSI}	frequency	V_{DD}=3.3V, T_A = 25℃, after calibration	7.96(3) (5)	8	8.04(5)	MHz
			7.94(3) (6)	8	8.04(3) (6)	
$DuCy_{(HSI)}$	Duty cycle	-	45	-	55	%
ACC_{HSI}	Accuracy of HSI oscillator(4)	V_{DD}=3.3V, T_A = -40~105℃	-1.5	-	2	%
		V_{DD}=3.3V, T_A = -10~85℃	-1.2	-	1.6	%
		V_{DD}=3.3V, T_A = 0~70℃	-1	-	1.2	%
$t_{SU(HSI)}$	HSI oscillator startup time	-	-	-	6	μs
$I_{DD(HSI)}$	HSI oscillator power consumption	-	-	120	-	μA

Notes:

(1) V_{DD} = 3.3V, T_A = -40~105 ℃ unless otherwise specified.

(2) Guaranteed by design, not tested in production.

(3) Production calibration accuracy, excluding welding effects. Welding brings about 1% frequency deviation range.

(4) Frequency deviation includes the effect of welding, data is from sample testing, not tested in production.

(5) Suitable for packages other than TSSOP20.

(6) Suitable for TSSOP20 package.

4.3.7.2 Low speed internal (LSI) RC oscillator

Table 4-17 LSI Oscillator Characteristics (1)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{LSI}(2)	Output frequency	25℃ calibration, V_{DD} =3.3V	38.8	40	41.2	KHz
		V_{DD} = 2.4 V to 3.6 V, T_A = - 40 ~ 105 ℃	28	40	60	KHz
$t_{SU(LSI)}$ (2)	LSI oscillator startup time	-	-	80	130	μs
$I_{DD(LSI)}$ (2)	LSI oscillator power consumption	-	-	0.1	-	μA

Notes:

(1) V_{DD} = 3.3V, T_A = -40~105 ℃ , unless otherwise specified.

(2) Guaranteed by design, not tested in production.

4.3.8 Wakeup Time From Low Power Mode

The wake-up time listed in Table 4-18 is measured during the wake-up phase of an 8MHz HSI RC oscillator. The clock source used when waking up depends on the current operating mode:

- Stop or standby mode: clock source is RC oscillator
- Sleep mode: The clock source is the clock used when entering sleep mode

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All times were measured using ambient temperature and supply voltage in accordance with Table 4-4.

Table 4-18 Wakeup Time In Low Power Mode

Symbol	Parameter	Typ	Unit
$t_{WUSLEEP}$(1)	Wake up from SLEEP mode	7	HCLK
$t_{WUSTOP0}$(1)	Wake up from STOP0 mode	15	μs
$t_{WUSTOP2}$(1)	Wake up from STOP2 mode	33	μs
$t_{WUSTDBY}$(1)	Wake up from STANDBY mode	75	μs

Note: (1) The wake up time is measured from the start of the wake up event until the first instruction is read by the user program.

4.3.9 PLL Characteristics

The parameters listed in Table 4-19 are measured when the ambient temperature and power supply voltage refer to the conditions in Table 4-4.

Table 4-19 PLL Features

Symbol	Parameter	Value			Unit
		Min	Typ	Max (1)	
f_{PLL_IN}	PLL input clock	4	8	32	MHz
	PLL Input clock duty cycle	40	50	60	%
f_{PLL_OUT}	PLL output clock(2)	32	-	72	MHz
t_{LOCK}	PLL ready indicates signal output time(3)	-	-	150	μs
Jitter	RMS cycle-to-cycle jitter @72MHz	-	8	-	ps
Ipll	Operating Current of PLL @72MHz VCO frequency. (1)	-	600	-	μA

Notes:

(1) Guaranteed by characterization results, not tested in production.

(2) Care needs to be taken to use the correct frequency doubling factor to input the clock frequency according to PLL so that f_{PLL_OUT} is within the allowable range.

(3) Guaranteed by design, not tested in production.

4.3.10 FLASH Characteristics

Unless otherwise specified, all characteristic parameters are obtained at T_A = -40~105℃.

Table 4-20 Flash Characteristics

Symbol	Parameter	Condition	Min (1)	Typ (1)	Max (1)	Unit
tprog	32-bit programming time	T_A = - 40 ~ 105 ℃	-	60	-	μs
t_{ERASE}	Page (2K bytes) erase time	T_A = - 40 ~ 105 ℃	-	12.5	-	ms
t_{ME}	Mass erase time	T_A = - 40 ~ 105 ℃	-	-	20	ms
I_{DD}	The power supply current	Read mode, f_{HCLK}=72MHz, 2 waiting cycles, V_{DD}=3.3V	-	-	3.231	mA
		Write mode, f_{HCLK} =72MHz, V_{DD} = 3.3 V	-	-	6.5	mA
		Erase mode, f_{HCLK} =72MHz, V_{DD} = 3.3 V	-	-	4.5	mA

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Symbol	Parameter	Condition	Min (1)	Typ (1)	Max (1)	Unit
		Power-down mode, V_{DD}= 3.0 to 3.6V	-	-	4.63	uA
Vprog	Programming voltage	-	2.4	-	3.6	V

Note: (1) Guaranteed by design, not tested in production.

Table 4-21 Flash Endurance And Data Retention

Symbol	Parameter	Condition	Min (1)	Unit
N_{END}	Endurance (note: erase times)	T_A = -40~105°C(7 suffix versions)	10	Kcycle
t_{RET}	Data retention	T_A = 125℃	10	Years

Note: (1) Guaranteed by characterization results, not tested in production.

4.3.11 Absolute Maximum (Electrical Sensitivity)

Based on three different tests (ESD, LU), a specific measurement method is used to test the strength of the chip to determine its performance in terms of electrical sensitivity.

Electrostatic discharge (ESD)

Electrostatic discharge (a positive pulse followed by a negative pulse one second later) is applied to all pins of all samples.

Table 4-22 Absolute Maximum ESD Value

Symbol	Parameter	Condition	Type	Max (1)	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A = +25 °C, In accordance with MIL-STD-883K Method 3015.9	3A	4000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charging device model)	T_A = +25 °C, In accordance with ESDA/JEDEC JS-002-2018	C3	2000	

Note: (1) Guaranteed by characterization results, not tested in production.

Static Latch up

To evaluate the locking performance, two complementary static locking tests were performed on six samples:

- Supply voltage exceeding limit for each power pin.
- Current is injected into each input, output, and configurable I/O pin.

This test conforms to EIA/JESD78E IC latch standard.

Table 4-23 Electrical Sensitivity

Symbol	Parameter	Condition	Type
LU	Static locking classes	T_A = +105 °C, in accordance with JESD78E	II class A

4.3.12I/O Port Characteristics

General input/output characteristics

Unless otherwise specified, the parameters listed in the following table are measured according to the conditions in Table 4-4. All I/O ports are CMOS and TTL compatible.

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Table 4-24 I/O Static Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{IL}	Input low level voltage	TTL port	Vss	-	0.8	V
V_{IH}	Input high level voltage		2	-	5.5	
V_{IL}	Input low level voltage	CMOS port	Vss	-	$0.35V_{DD}$	
V_{IH}	Input high level voltage		$0.65V_{DD}$	-	$V_{DD}+0.5$	
V_{hys}	Schmitt trigger voltage lag(1)	V_{DD} = 3.3 V / 2.5 V	200	-	-	mV
I_{lkg}	Input leakage current(2)	V_{DD}=Maximum V_{PAD} = 0 or V_{PAD} = V_{DD}(4)	-1	-	1	μA
R_{PU}	Weak pull-up equivalent resistance(3)	V_{DD} = 3.3 V, V_{IN} = V_{SS}	80	-	220	KΩ
		V_{DD} = 2.5V, V_{IN} = V_{SS}	90	-	300	KΩ
R_{PD}	Weak pull-down equivalent resistance(3)	V_{DD} = 3.3 V, V_{IN} = V_{DD}	80	-	220	KΩ
		V_{DD} = 2.5V, V_{IN} = V_{DD}	90	-	300	KΩ
C_{IO}	Capacitance of I/O pins	-	-	5	-	pF

Notes:

(1) The hysteresis voltage of Schmitt trigger switching level. Guaranteed by characterization results, not tested in production.

(2) The leakage current may be higher than the maximum if there is reverse current in adjacent pins.

(3) Pull-up and pull-down resistors are implemented with a switchable PMOS/NMOS.

(4) V_{PAD} refers to the input voltage of the IO pin.

All I/O ports are CMOS and TTL compatible (no software configuration required) and their features take into account most of the strict CMOS process or TTL parameters:

- For V_{IH}:
  - If V_{DD} is between [2.4V~3.08V]; Use CMOS features but include TTL.
  - If V_{DD} is between [3.08V~3.6V]; Use TTL features but include CMOS.
- For V_{IL}:
  - If V_{DD} is between [2.4V~3.6V]; Use CMOS features but include TTL.

Output drive current

GPIO (universal input/output port) can absorb or output up to +/-12mA current.

Output voltage

Unless otherwise specified, guaranteed by design, not tested in production. The parameters listed in Table 4-25 were measured using ambient temperature and V_{DD} supply voltage in accordance with Table 4-4. All I/O ports are CMOS and TTL compatible.

Table 4-25 Io Output Drive Capability Characteristics

Drive class	I_{OH}(1), V_{DD}=3.3V	I_{OL}(1), V_{DD}=3.3V	I_{OH}(1), V_{DD}=2.5V	I_{OL}(1), V_{DD}=2.5V	Unit
2	-2	2	-1.5	1.5	mA
4	-4	4	-3	3	mA
8	-8	8	-7	7	mA
12	-12	12	-11	11	mA

Note: (1) Guaranteed by design, not tested in production.

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Table 4-26 Output voltage characteristics

Symbol	Parameter	Condition	Min	Max	Unit
V_{OL}(1)	Output low level	V_{DD} = 3.3 V, I_{OL}(3)= 2mA, 4mA, 8mA, and 12mA	V_{SS}	0.4	V
		V_{DD} = 2.5 V, I_{OL}(3)= 1.5mA, 3mA, 7mA, and 11mA	V_{SS}	0.4	
V_{OH}(2)	Output high level	V_{DD} = 3.3 V, I_{OH}(3)= -2mA, -4mA, -8mA, and -12mA	2.4	V_{DD}	
		V_{DD} = 2.5 V, I_{OH}(3)= -1.5mA, -3mA, -7mA, and -11mA	1.8	V_{DD}	

Notes:

(1) The current I_{IO} absorbed by the chip must always follow the absolute maximum rating given in Table 4-2, and the sum of I_{IO} (all I/O pins and control pins) must not exceed I_{VSS}.

(2) The current I_{IO} output from the chip must always follow the absolute maximum rating given in Table 4-2, and the sum of I_{IO} (all I/O pins and control pins) must not exceed I_{VDD}.

(3) Actual drive capability see Table 4-25.

Input/output AC characteristics

The definitions and values of the input and output AC characteristics are given in Figure 4-9 and Table 4-27 respectively.

Unless otherwise specified, the parameters listed in Table 4-27 were measured using ambient temperature and supply voltage in accordance with Table 4-4.

Table 4-27 Input/Output AC Characteristics (1)

GPIOx_DS.DSy[1:0] Configuration	Symbol	Parameter	Condition	Min	Max	Unit
00 (2mA)	$f_{max(IO)out}$	Maximum frequency(2)	C_L = 5 pF, V_{DD} = 3.3 V	-	75	MHz
			C_L = 5 pF, V_{DD} = 2.5 V	-	50	
	$t_{(IO)out}$	Output delay (A to pad)	C_L = 5 pF, V_{DD} = 3.3 V	-	3.66	ns
			C_L = 5 pF, V_{DD} = 2.5 V	-	4.72	
	$t_{(IO)in}$	Input delay (pad to Y)	C_L = 50 fF, V_{DD} = 2.97 V, V_{DDD} = 0.81 V Input characteristics at 1.8V and 2.5V are derated	-	2	ns
10 (4mA)	$f_{max(IO)out}$	Maximum frequency(2)	C_L = 10 pF, V_{DD} = 3.3 V	-	90	MHz
			C_L = 10 pF, V_{DD} = 2.5 V		60	
	$t_{(IO)out}$	The output delay (A to pad)	C_L = 10 pF, V_{DD} = 3.3 V	-	3.5	ns
			C_L = 10 pF, V_{DD} = 2.5 V		4.5	
	$t_{(IO)in}$	Input delay (pad to Y)	C_L = 50 fF, V_{DD} = 2.97 V, V_{DDD} = 0.81 V Input characteristics at 1.8V and 2.5V are derated	-	2	
01 (8mA)	$f_{max(IO)out}$	Maximum frequency(2)	C_L = 20 pF, V_{DD} = 3.3 V	-	100	MHz
			C_L = 20 pF, V_{DD} = 2.5 V		75	
	$t_{(IO)out}$	The output delay (A to pad)	C_L = 20 pF, V_{DD} = 3.3 V	-	3.42	ns
			C_L = 20 pF, V_{DD} = 2.5 V		4.37	
	$t_{(IO)in}$	Input delay (pad to Y)	C_L = 50 fF, V_{DD} = 2.97 V, V_{DDD} = 0.81 V Input characteristics at 1.8V and 2.5V are derated	-	2	
11 (12mA)	$f_{max(IO)out}$	Maximum frequency(2)	C_L = 30 pF, V_{DD} = 3.3 V	-	120	MHz
			C_L = 30 pF, V_{DD} = 2.5 V	-	90	
	$t_{(IO)out}$	The output delay	C_L = 30 pF, V_{DD} = 3.3 V	-	3.34	ns

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GPIOx_DS.DSy[1:0] Configuration	Symbol	Parameter	Condition	Min	Max	Unit
		(A to pad)	C_L = 3 pF, V_{DD} = 2.5 V	-	4.26	
	$t_{(IO)in}$	Input delay (pad to Y)	C_L = 50 fF, V_{DD} = 2.97 V, V_{DDD} = 0.81 V Input characteristics at 1.8V and 2.5V are derated	-	2	
-	t_{EXTIpw}	Pulse width of external signals detected by the EXTI controller	-	10	-	ns

Notes:

(1) The I/O port drive capability can be configured via GPIOx_DS.DSy[1:0]. Refer the description of the GPIO port drive capability configuration register in N32G401 user manual.

(2) The maximum frequency is defined in Figure 4-9.

(3) Propagation delay is defined in Figure 4-10.

Figure 4-9 Definition of Input/Output AC Characteristics

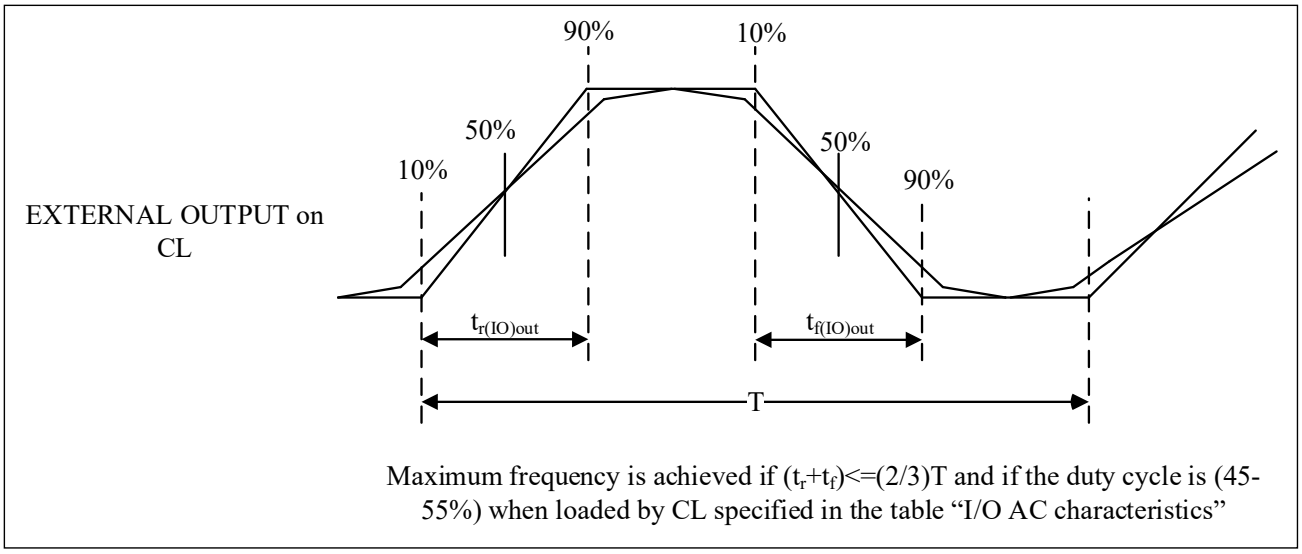

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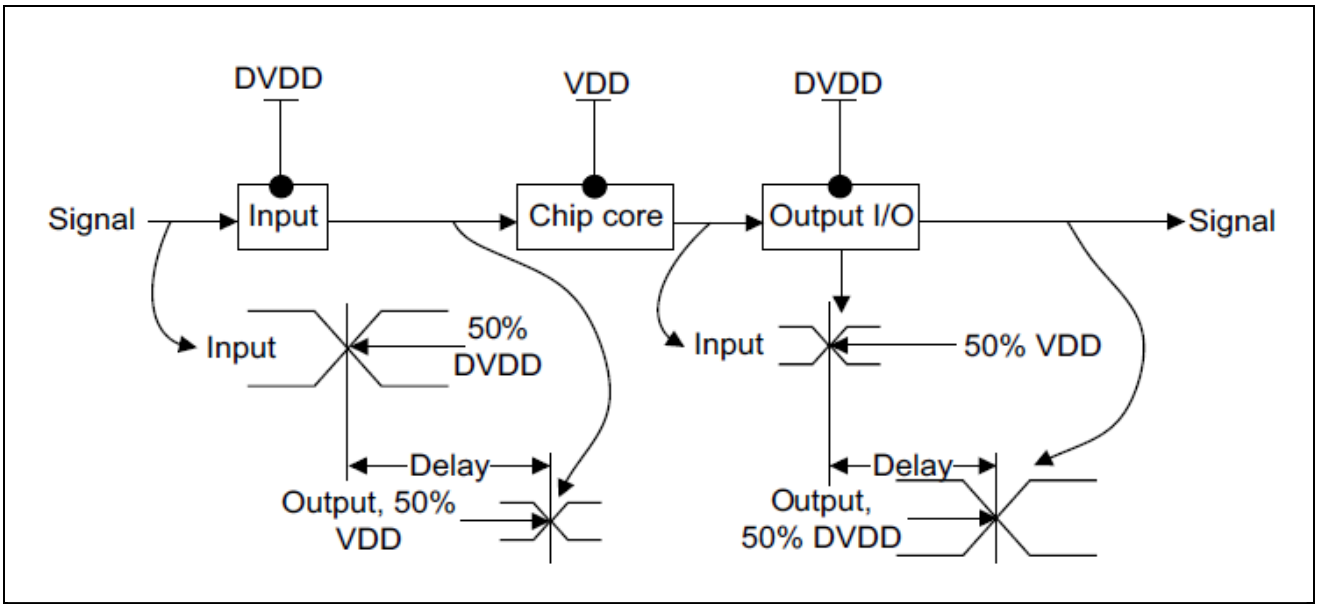
Figure 4-10 Propagation Delay



4.3.13 NRST Pin Characteristics

The NRST pin is integrated with pull-up resistor, R_{PU} (see Table 4-24). Unless otherwise specified, the parameters listed in Table 4-28 were measured using ambient temperature and supply voltage in accordance with Table 4-4.

Table 4-28 NRST Pin Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$V_{IL(NRST)}$(1)	NRST input low level voltage	V_{DD} = 3.3 V	Vss	-	0.8	V
$V_{IH(NRST)}$(1)	NRST input high level voltage	V_{DD} = 3.3 V	2	-	VDD	
$V_{hys(NRST)}$	NRST schmitt trigger voltage hysteresis	-	-	100	-	mV
R_{PU}	Weak pull-up equivalent resistor(2)	V_{DD} = 3.3 V	30	50	70	KΩ
$V_{F(NRST)}$(1)	NRST input filtered pulse	-	-	-	100	ns
$V_{NF(NRST)}$(1)	NRST input not filtered pulse	-	300	-	-	ns
T_{NRST_OUT}	Generated reset pulse duration	Internal reset source	10	13	-	µs

Notes:

(1) Guaranteed by design, not tested in production.

(2) The pull-up resistor is designed as a true resistor in series for a not switchable PMOS implementation. The resistance of this PMOS switch is very small (about 10%).

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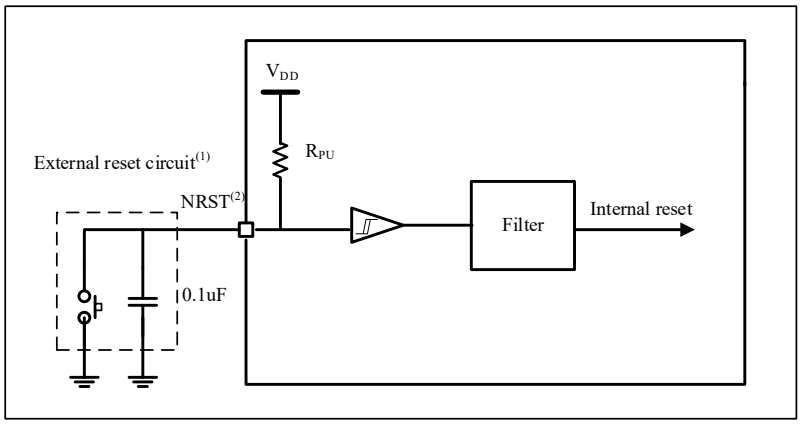
Figure 4-11 Recommended NRST Pin Protection



Notes:

(1) Filter action.

(2) The user must ensure that the NRST pin potential is below the maximum $V_{IL(NRST)}$ listed in Table 4-28, otherwise the MCU cannot be reset.

4.3.14 Timer And Watchdog Characteristics

The parameters listed in Table 4-29 and Table 4-30 are guaranteed by design.

See section 4.3.12 for details on the features of the I/O alternate function pins (output comparison, input capture, external clock, PWM output).

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Table 4-29 TIM1/8 Characteristics

Symbol	Parameter	Condition	Min	Max	Unit
$t_{res(TIM)}$	Timer resolution time	-	1	-	t_{TIMCLK}
		f_{TIMCLK}= 72MHz	13.9	-	ns
f_{EXT}	Timer CH1 to CH2 external clock frequency	-	0	f_{TIMCLK}/2	MHz
		f_{TIMCLK}= 72MHz	0	36	MHz
Res_{TIM}	Timer resolution	-	-	16	bits
$t_{COUNTER}$	16 bit counter clock cycle when internal clock is selected	-	1	65536	t_{TIMCLK}
		f_{TIMCLK}= 72MHz	0.0139	910	µs
t_{MAX_COUNT}	Maximum count	-	-	65536 x 65536	t_{TIMCLK}
		f_{TIMCLK}= 72MHz	-	59.625	s

Table 4-30 TIM2/3/4/5 Characteristics

Symbol	Parameter	Condition	Min	Max	Unit
$t_{res(TIM)}$	Timer time resolution	-	1	-	t_{TIMCLK}
		f_{TIMCLK}= 64MHz	15.62	-	ns
f_{EXT} (1)	Timer CH1 to CH2 external clock frequency	-	0	f_{TIMCLK} /2	MHz
		f_{TIMCLK}= 64MHz	0	32	MHz
Res_{TIM}	Timer resolution	-	-	16	bits
$t_{COUNTER}$	16 bit counter clock cycle when internal clock is selected	-	1	65536	t_{TIMCLK}
		f_{TIMCLK}= 64MHz	0.01562	1024	µs
t_{MAX_COUNT}	Maximum count with 32-bit counter	-	-	65536 x 65536	t_{TIMCLK}
		f_{TIMCLK}= 64MHz	-	67.108	s

Note: If f_{TIMCLK} is running at the highest frequency, the system clock needs to be reduced to 64MHz.

Table 4-31 LPTIM Characteristics

Symbol	Parameter	Condition	Min	Max	Unit
$t_{res(LPTIM)}$	Timer time resolution	-	1	-	$t_{LPTIMCLK}$
		$f_{LPTIMCLK}$= 32MHz	31.25	-	ns
f_{EXT} (1)	IN2 and OUT external clock frequency	-	0	32	MHz
		$f_{LPTIMCLK}$= 32MHz	0	32	MHz
Res_{LPTIM}	Timer resolution	-	-	16	bits
$t_{COUNTER}$	16 bit counter clock cycle when internal clock is selected	-	1	65536	$t_{LPTIMCLK}$
		$f_{LPTIMCLK}$= 32MHz	0.03125	2048	µs
t_{MAX_COUNT}	Maximum count with 32-bit counter	-	-	65536 x 65536	$t_{LPTIMCLK}$
		$f_{LPTIMCLK}$= 32MHz	-	134.217	s

Note: If $f_{LPTIMCLK}$ is running at the highest frequency, the system clock needs to be reduced to 64MHz.

Table 4-32 IWDG Counting Maximum and Minimum Reset Time (Lsi = 40 Khz)

Prescaler	IWDG_PREDIV.PD[2:0]	Min(1) IWDG_RELV.REL[11:0]=0	Max(1) IWDG_RELV.REL[11:0]=0xFFF	Unit
/4	000	0.1	409.6	ms
/8	001	0.2	819.2	
/16	010	0.4	1638.4	
/32	011	0.8	3276.8	

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/64	100	1.6	6553.6	
/128	101	3.2	13107.2	
/256	11x	6.4	26214.4	

Note: (1) Guaranteed by design, not tested in production.

Table 4-33 WWDG Counting Maximum and Minimum Reset Time (APB1 PCLK1 = 32mhz)

Prescaler	WWDG_CFG.TIMERB[1:0]	Min(1) WWDG_CGF.W[13:0]=0x3F	Max(1) WWDG_CFG.W[13:0]=0x3FFF	Unit
/1	00	0.128	2089	ms
/2	01	0.256	4178	
/3	10	0.512	8356	
/4	11	1.024	16712	

Note: (1) Guaranteed by design, not tested in production.

4.3.15 I²C Interface Characteristics

Unless otherwise specified, the parameters listed in Table 4-34 were measured using ambient temperature, f_{PCLK1} frequency, and V_{DD} supply voltage in accordance with Table 4-4.

The I²C interface of the N32G401 product conforms to the standard I²C communication protocol, but has the following limitations: SDA and SCL are not "true" open leak pins, and when configured for open leak output, the PMOS tube between the pin and V_{DD} is closed, but still exists.

I²C interface features are listed in Table 4-34. See Section 4.3.12 for details about the features of the input/output multiplexing function pins (SDA and SCL).

Table 4-34 I²C Interface Characteristics

Symbol	Parameter	Standard Mode(1) (2)		Fast Mode(1) (2)		Fast + Mode(1) (2)		Unit
		Min	Max	Min	Max	Min	Max	
f_{SCL}	I2C interface frequency	0.0	100	0	400	0	1000	KHz
$t_{h(STA)}$	Start condition hold time	4.0	-	0.6	-	0.26	-	µs
$t_{w(SCLL)}$	SCL clock low time	4.7	-	1.3	-	0.50	-	µs
$t_{w(SCLH)}$	SCL clock high time	4.0	-	0.6	-	0.26	-	µs
$t_{su(STA)}$	Repeat start condition setup time	4.7	-	0.6	-	0.26	-	µs
$t_{h(SDA)}$	SDA data hold time	0	3.4	0	0.9	0	0.4	µs
$t_{su(SDA)}$	SDA setup time	250	-	100	-	50	-	ns
$t_{r(SDA)}$ $t_{r(SCL)}$	SDA and SCL rise time	-	1000	20+0.1Cb	300	-	120	ns
$t_{f(SDA)}$ $t_{f(SCL)}$	SDA and SCL fall time	-	300	20+0.1Cb	300	-	120	ns
$t_{su(STO)}$	Stop condition setup time	4.0	-	0.6	-	0.26	-	µs
$t_{w(STO:STA)}$	Time from stop condition to start condition (bus idle)	4.7	-	1.3	-	0.50	-	µs
C_b	Capacitive load for per bus	-	400	-	400	-	100	pf
t_{SP}	Pulse width of the spikes that are suppressed by the analog filter for standard and fast mode	0	35	0	35	0	35	µs
$t_{v(SDA)}$	Data validity time	-	3.45	-	0.9	-	0.45	

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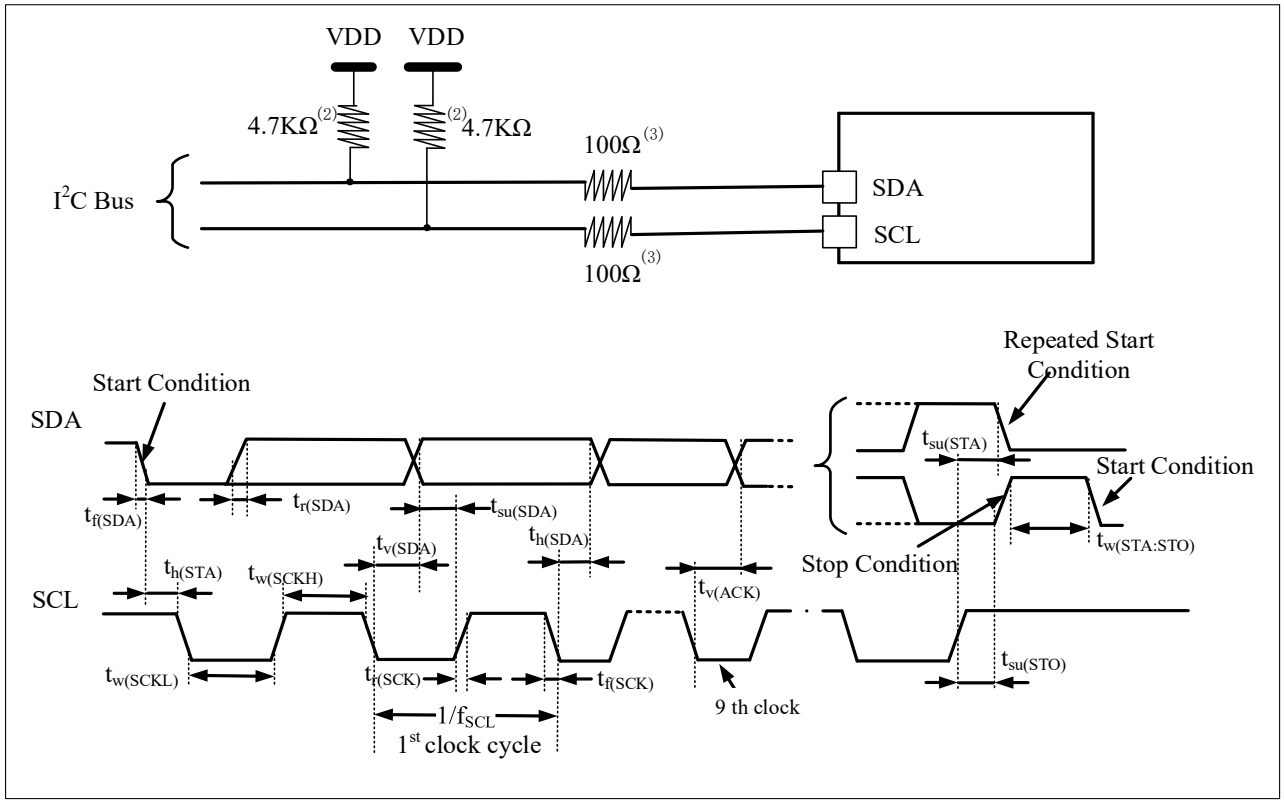
Symbol	Parameter	Standard Mode(1) (2)		Fast Mode(1) (2)		Fast + Mode(1) (2)		Unit
		Min	Max	Min	Max	Min	Max	
$t_{v\,(ACK)}$	Response time	-	3.45	-	0.9	-	0.45	

Notes:

(1) Guaranteed by design, not tested in production.

(2) To achieve the maximum frequency of standard mode I2C, f_{PCLK1} must be greater than 2MHz. To achieve the maximum frequency of fast mode I2C, f_{PCLK1} must be greater than 4MHz.

Figure 4-12 I²C Bus AC Waveform and Measuring Circuit (1)



Notes:

(1) The measuring point is set at $0.3V_{DD}$ and $0.7V_{DD}$.

(2) The pull-up resistance depends on the I2C interface speed.

(3) The resistance value depends on the actual electrical characteristics. The signal line can be directly connected without serial resistance.

4.3.16 SPI/I²S Interface Characteristics

Unless otherwise specified, the SPI parameters listed in Table 4-35 and the I²S parameters listed in Table 4-36 are measured using ambient temperature, f_{PCLKx} frequency, and V_{DD} supply voltage in accordance with Table 4-4.

See section 4.3.12 for details on the characteristics of the I/O multiplexed pins (NSS, SCLK, MOSI, MISO for SPI, WS, CLK, SD for I²S).

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Table 4-35 SPI Characteristics [1]

Symbol	Parameter	Condition		Min	Max	Unit
f_{SCLK} $1/t_{c(SCLK)}$	SPI clock frequency	Master mode		-	18[4]/20[5]/28[6]	MHz
		Slave mode		-	32	
$t_{r(SCLK)}$ $t_{f(SCLK)}$	SPI clock rise and fall time	Load capacitance: C = 30pF		-	8	ns
DuCy(SCK)	SPI from the input clock duty cycle	Slave mode		45	55	%
$t_{su(NSS)}$ [1]	NSS setup time	Slave mode		$4t_{PCLK}$	-	ns
$t_{h(NSS)}$[1]	NSS hold time	Slave mode		$2t_{PCLK}$	-	ns
$t_{w(SCLKH)}$[1] $t_{w(SCLKL)}$[1]	SCLK high and low time	Master mode		t_{PCLK} - 2	t_{PCLK} + 2	ns
$t_{su(MI)}$[1]	Data input setup time	Master mode	SPI1	14	-	ns
			SPI2	13[4] /12[5]	-	
$t_{su(SI)}$[1]		Slave mode	SPI1	4.5[4]/4[5]	-	
			SPI2	4.5	-	
$t_{h(MI)}$[1]	Data input hold time	Master mode	SPI1	2.5[4]/4.5[5]	-	ns
			SPI2	2[4]/4.5[5]	-	
$t_{h(SI)}$[1]		Slave mode	SP1	2.5[4]/4.5[5]	-	
			SP2	2.5[4]/4.5[5]	-	
$t_{a(SO)}$[1][2]	Data output access time	Slave mode, f_{PCLK} = 32MHz		0	$3t_{PCLK}$	ns
$t_{dis(SO)}$[1][3]	Disable time of data output	Slave mode		2	10	ns
$t_{v(SO)}$[1]	Valid time of data output	Slave mode (after enable edge)	SPI1	-	15	ns
			SPI2	-	15	
$t_{v(MO)}$[1]		Master mode (after enabling edge)	SPI1	-	5.5	
			SPI2	-	5.0	
$t_{h(SO)}$[1]	Data output hold time	Slave mode (after enable edge)	SPI1	4.5	-	ns
			SPI2	4.0	-	
$t_{h(MO)}$[1]		Master mode (after enabling edge)	SPI1	-1.0	-	
			SPI2	-0.5[4]/-1.0[5]	-	

Notes:

[1] Guaranteed by design, not tested in production.

[2] The minimum value represents the minimum time to drive the output, and the maximum value represents the maximum time to get the data correctly.

[3] The minimum value represents the minimum time for turning off the output and the maximum value represents the maximum time for placing the data line in a high resistance state.

[4] Applicate to C version

[5] Applicate to D version, with CRC

[6] Applicate to D version, without CRC

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Figure 4-13 SPI Timing Diagram-Slave Mode and CLKPHA=0

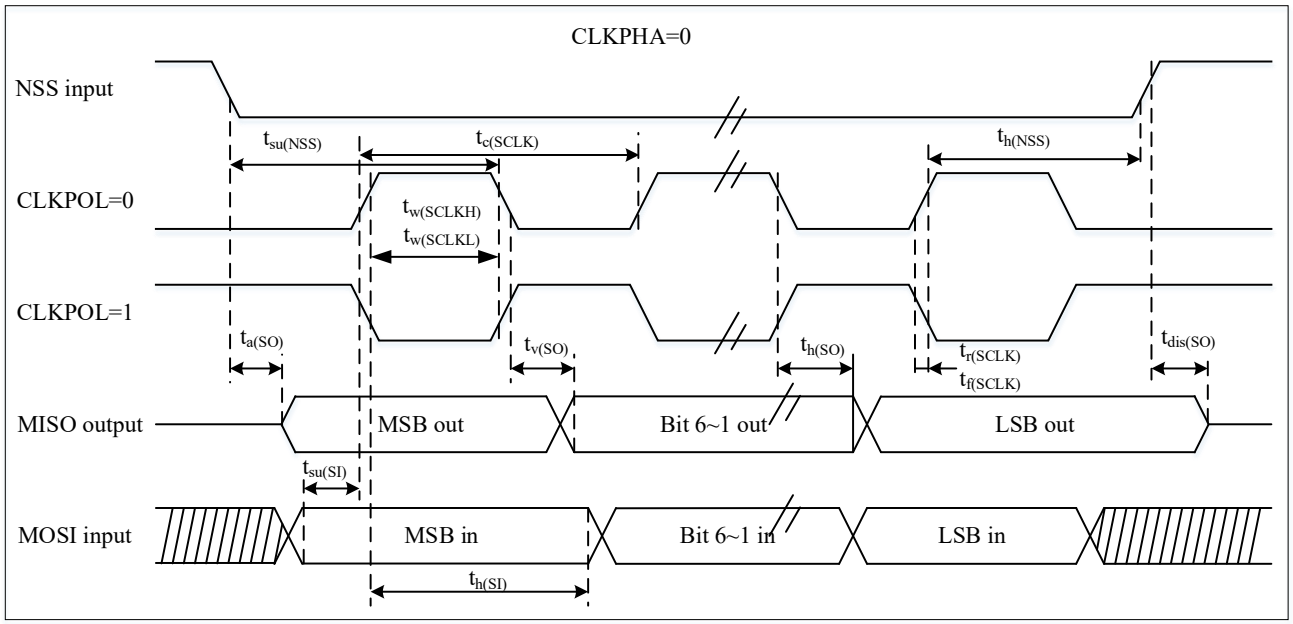
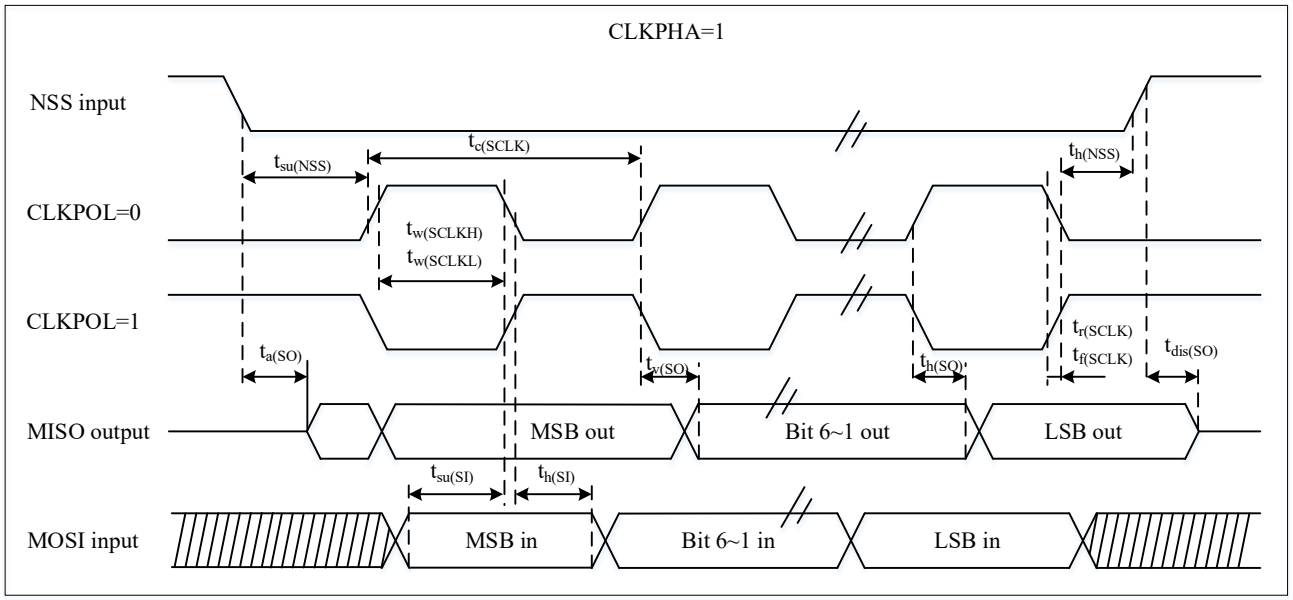


Figure 4-14 SPI Timing Diagram-Slave Mode and CLKPHA=1 (1)



Note: (1) The measuring point is set at $0.3V_{DD}$ and $0.7V_{DD}$.

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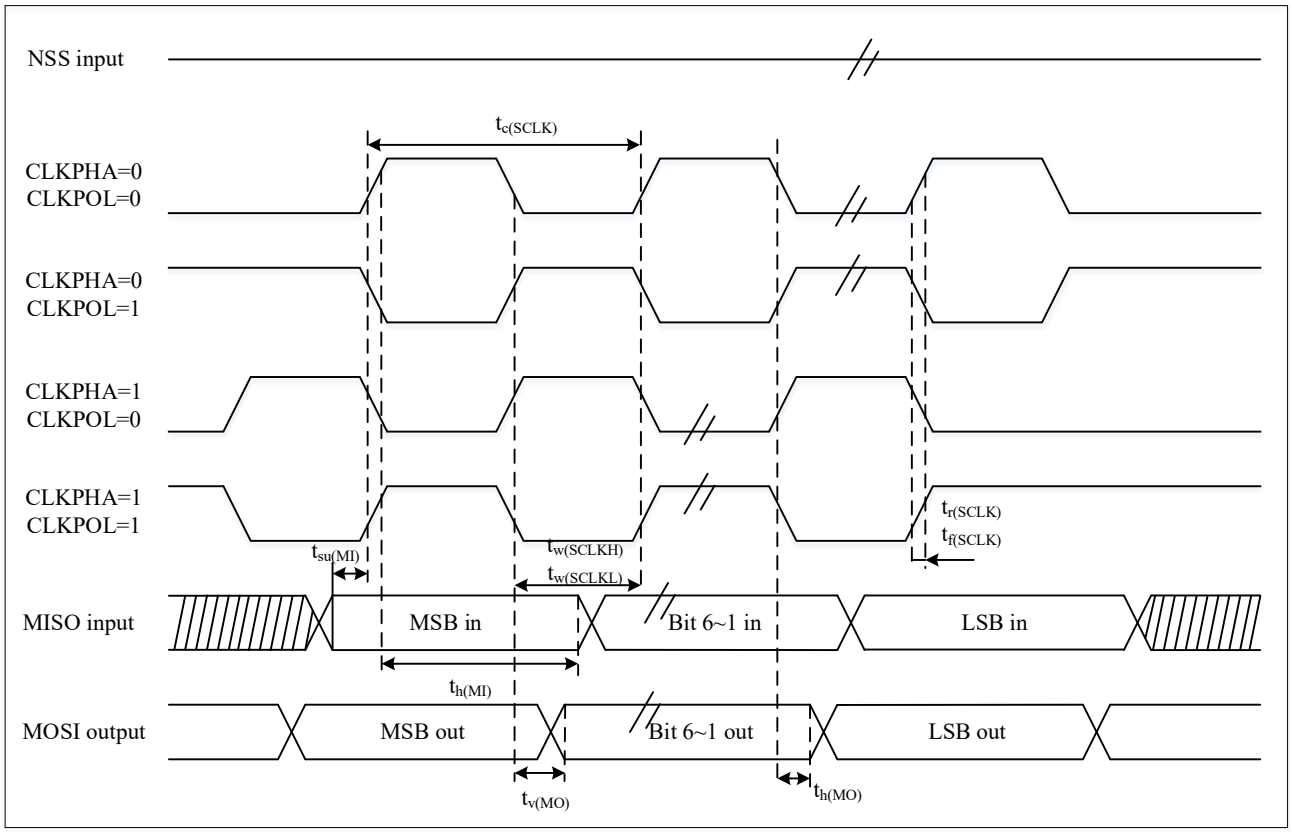
Figure 4-15 SPI Timing Diagram- Master Mode (1)



Note: (1) The measuring point is set at 0.3V and 0.7V.DDDD

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Table 4-36 I²s Characteristics (1)

Symbol	Parameter	Condition		Min	Max	Unit
f_{MCLK}	I²S master clock	Master mode		-	256*Fs(3)	MHz
f_{CLK} $1/t_{c(CLK)}$	I²S clock frequency	Master mode (32 bit)		-	64*Fs(3)	MHz
		Slave mode (32 bit)		-	64*Fs(3)	
DuCy(SCK)	I²S clock frequency duty cycle	I2S Slave mode		30	70	%
$t_{r(CLK)}$ $t_{f(CLK)}$	I²S clock rise and fall time	Load capacitance: CL = 50pF		-	8	ns
$t_{v(WS)}$ (1)	WS valid time	Master mode	I2S1	7.5	-	
			I2S2	6.0	-	
$t_{h(WS)}$(1)	WS hold time	Master mode	I2S1	0	-	
			I2S2	0	-	
$t_{su(WS)}$ (1)	WS setup time	Slave mode	I2S1	4.5	-	
			I2S2	4.5	-	
$t_{h(WS)}$(1)	WS hold time	Slave mode	I2S1	2.5	-	
			I2S2	2.5	-	
$t_{w(CLKH)}$(1)	CLK high and low times	Master mode, f_{PCLK} = 16MHz, audio 48kHz		312.5	-	
$t_{w(CLKL)}$(1)				345	-	
$t_{su(SD\_MR)}$(1)	Data input setup time	Master receiver	I2S1	5.0	-	
			I2S2	5.0	-	
$t_{su(SD\_SR)}$(1)		Slave receiver	I2S1	4.5	-	
			I2S2	4.5	-	
$t_{h(SD\_MR)}$(1)(2)	Data input hold time	Master receiver	I2S1	1.5	-	
			I2S2	1.5	-	
$t_{h(SD\_SR)}$(1)(2)		Slave receiver	I2S1	1.5	-	
			I2S2	1.5	-	
$t_{v(SD\_ST)}$(1)(2)	Data output valid time	Slave transmitter (after the enabled edge)	I2S1	-	16.0	
			I2S2	-	15.5	
$t_{h(SD\_ST)}$(1)	Data output hold time	Slave generator (after enable edge)	I2S1	4.5	-	
			I2S2	4.5	-	
$t_{v(SD\_MT)}$(1)(2)	Data output valid time	Master generator (after enabling edge)	I2S1	-	5.5	
			I2S2	-	5.5	
$t_{h(SD\_MT)}$(1)	Data output hold time	Master generator (after enabling edge)	I2S1	1	-	
			I2S2	1	-	

Notes:

(1) Guaranteed by design, not tested in production.

(2) Depends on f_{PCLK}. For example, if f_{PCLK}=16MHz, then T_{PCLK}=1/f_{PCLK} =125ns.

(3) Audio signal sampling frequency.

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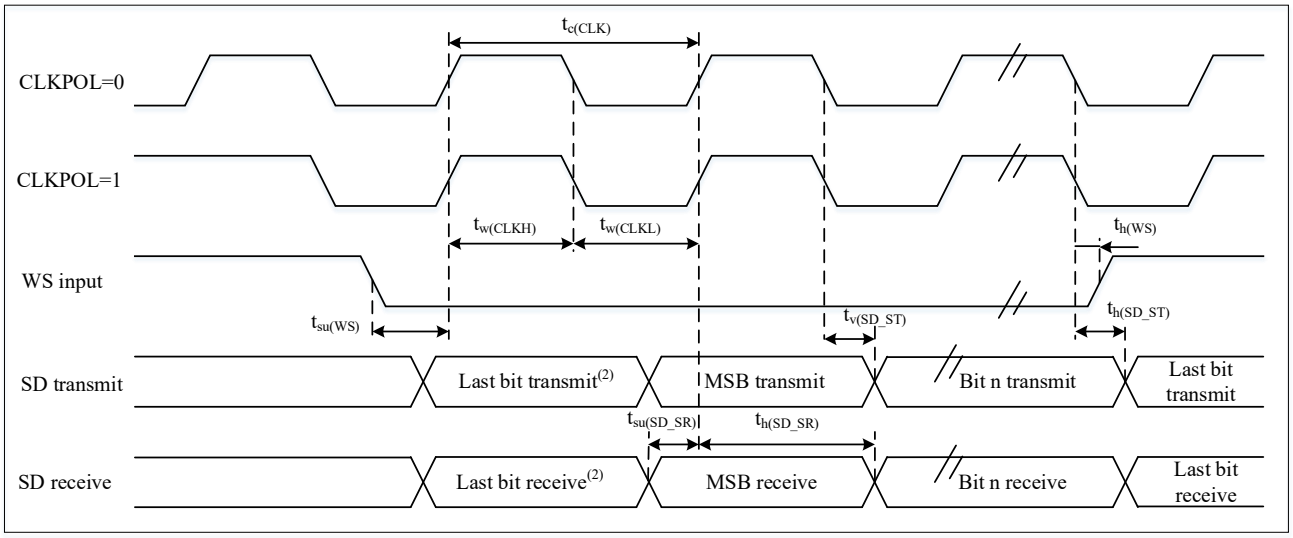
Figure 4-16 I²S Slave Mode Timing Diagram (Philips Protocol) (1)

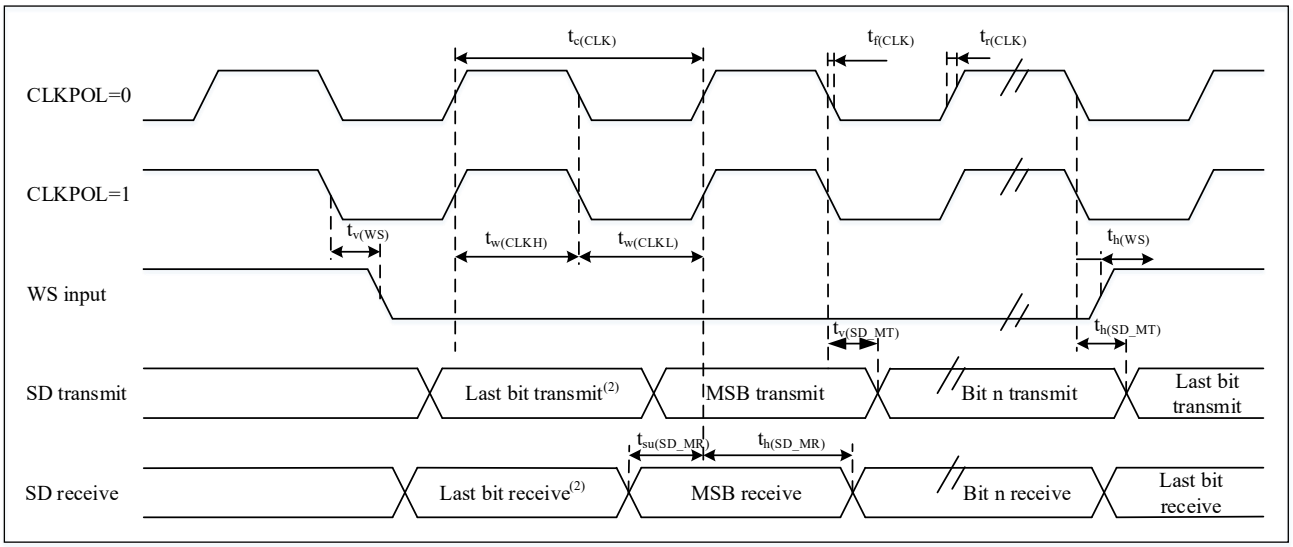


Notes:

(1) The measuring point is set at $0.3V_{DD}$ and $0.7V_{DD}$.

(2) Transmit/receive of the last byte. There is no transmit/receive of this least significant bit before the first byte.

Figure 4-17 I²S Master Mode Timing Diagram (Philips Protocol) (1)



Notes:

(1) The measuring point is set at $0.3V_{DD}$ and $0.7V_{DD}$.

(2) Transmit/receive of the last byte. There is no transmit/receive of this last bit before the first byte.

4.3.17 Electrical Parameters of 12-bit Analog-to-Digital Converter (ADC)

Unless otherwise specified, the parameters in Table 4-37 are measured using ambient temperature, f_{HCLK} frequency, and V_{DDA} supply voltage in accordance with the conditions in Table 4-4.

Note: It is recommended to perform a calibration at each power-on.

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Table 4-37 ADC Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{DDA}	The power supply voltage	Use an external reference voltage	2.4	-	3.6	V
V_{REF+}	Positive reference voltage	-	2.4	-	V_{DDA}	V
V_{REF-}	Negative reference voltage	-		0		V
f_{ADC}	ADC clock frequency	-	-	-	72	MHz
f_s(2)	Sampling rate	Resolution = 12bits Fast channel	-	-	4.2	Msps
		Resolution = 10bits Fast channel	-	-	5.5	
		Resolution = 8bits Fast channel	-	-	6.5	
		Resolution = 6bits Fast channel	-	-	8	
f_{TRIG}(2)	External trigger frequency(3)	f_{ADC}=72MHz Resolution = 12bits	-	-	4.2	MHz
		Resolution = 12bits	-	-	17	$1/f_{ADC}$
V_{AIN}	Switching voltage range	-	0 (V_{SSA} or V_{REF-} Connect to ground)	-	V_{REF+}	V
R_{AIN}(2)	External input impedance	-	-	-	100(1)	KΩ
R_{ADC}(2)	Sampling switch resistance	Fast channel, VDD=3.3V	-	-	0.4	KΩ
		Slow channel, VDD=3.3V	-	-	0.65	
C_{ADC}(2)	Internal sampling and holding capacitor		-	5	-	pF
t_{cal}(2)	The calibration time			82		$1/f_{ADC}$
t_{lat}(2)	Injection trigger conversion latency	f_{ADC} = 72 MHz	-	-	8.35	µs
		-	-	-	601.5	$1/f_{ADC}$
t_{latr}(2)	Regular trigger conversion latency	f_{ADC} = 72MHz	-	-	8.35	µs
		-	-	-	601.5	$1/f_{ADC}$
SNDR	Signal noise distortion ration		-	65	-	dB
t_S(2)	Sampling time	f_{ADC} = 72MHz(fast channel) Resolution = 12bits	0.0625(1)	-	7.528.35	us
		f_{ADC} = 72MHz(fast channel) Resolution = 10bits	0.0347(1)	-	8.35	
		f_{ADC} = 72MHz(fast channel) Resolution = 8bits	0.0347(1)	-	8.35	
		f_{ADC} = 72MHz(fast channel) Resolution = 6bits	0.0347(1)	-	8.35	
		f_{ADC} = 72MHz(slow channel) Resolution = 12bits	0.1042(1)	-	8.35	
		f_{ADC} = 72MHz(slow channel) Resolution = 10bits	0.1042(1)	-	8.35	
		f_{ADC} = 72MHz(slow channel) Resolution = 8bits	0.0625(1)	-	8.35	
		f_{ADC} = 72MHz(slow channel) Resolution = 6bits	0.0625(1)	-	7.528.35	

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T_S[2]	Sampling cycles	The fast channel Resolution = 12bits	4.5[1]	-	601.5	$1/f_{ADC}$
		The slow channel Resolution = 12bits	7.5[1]	-	601.5	
t_{STAB}[2]	Power-up time	-	6	10	20	μs
t_{CONV}[2]	Total conversion time (including sampling time)	-	9 ~ 614 (Sampling T_S + 6.5/8.5/10.5/12.5 for successive approximation)			$1/f_{ADC}$

Notes:

[1] Guaranteed by design, not tested in production.，please refer to Table 4-38 for details.

[2] Guaranteed by design, not tested in production.

[3] Suitable for ADC continuous conversion mode.

Formula 1: maximum R_{AIN} formula

$$R_{AIN} < \frac{T_S}{f_{ADC} \times C_{ADC} \times \ln(2^{N+2})} - R_{ADC}$$

The above formula (Formula 1) is used to determine the maximum external impedance so that the error can be less than 1/4 LSB. Where N=12(representing 12-bit resolution).

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Table 4-38 ADC Sampling Time(1)

Input	Resolution	Rin(kΩ)	Minimum sampling time (ns)	Input	Resolution	Rin(kΩ)	Minimum sampling time (ns)
fast channel	12-bit	0	39.6	slow channel	12-bit	0	79.2
		0.05	43.5			0.05	83.1
		0.1	47.4			0.1	86.9
		0.2	55.1			0.2	94.7
		0.5	78.4			0.5	118.0
		1	117.2			1	156.8
		10	815.9			10	855.5
		20	1592.2			20	1631.8
		50	3921.2			50	3960.8
		100	7802.8			100	7842.4
fast channel	10-bit	0	33.9	slow channel	10-bit	0	67.9
		0.05	37.3			0.05	71.2
		0.1	40.6			0.1	74.5
		0.2	47.2			0.2	81.2
		0.5	67.2			0.5	101.1
		1	100.5			1	134.4
		10	699.4			10	733.3
		20	1364.8			20	1398.7
		50	3361.0			50	3395.0
		100	6688.1			100	6722.1
fast channel	8-bit	0	28.3	slow channel	8-bit	0	56.6
		0.05	31.1			0.05	59.3
		0.1	33.8			0.1	62.1
		0.2	39.4			0.2	67.7
		0.5	56.0			0.5	84.3
		1	83.7			1	112.0
		10	582.8			10	611.1
		20	1137.3			20	1165.6
		50	2800.9			50	2829.1
		100	5573.5			100	5601.7
fast channel	6-bit	0	22.6	slow channel	6-bit	0	45.2
		0.05	24.8			0.05	47.5
		0.1	27.1			0.1	49.7
		0.2	31.5			0.2	54.1
		0.5	44.8			0.5	67.4
		1	67.0			1	89.6
		10	466.2			10	488.9
		20	909.9			20	932.5
		50	2240.7			50	2263.3
		100	4458.8			100	**4.4**

Note: (1) Guaranteed by design, not tested in production.

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Table 4-39 ADC Accuracy-Limited Test Conditions [1][2]

Symbol	Parameter	Condition	Max [3]	Unit
ET	Comprehensive error[4]	f_{ADC} = 72MHz, sample rate = 4.2MSPS, V_{DDA} = 2.4V~3.3V, T_A = 25 °C, Single-ended mode	±4.5	LSB
		f_{ADC} = 72MHz, sample rate = 4.2MSPS, V_{DDA} = 2.4V~3.3V, T_A = 25 °C, Differential mode	±4.5	
EO	Offset error	f_{ADC} = 72MHz, sample rate = 4.2MSPS, V_{DDA} = 2.4V~3.3V, T_A = 25 °C, Single-ended mode	±1.5	
		f_{ADC} = 72MHz, sample rate = 4.2MSPS, V_{DDA} = 2.4V~3.3V, T_A = 25 °C, Differential mode	±1.5	
ED	Differential linearity error	f_{ADC} = 72MHz, sample rate = 1MSPS, V_{DDA} = 2.4V~3.3V, T_A = 25 °C, Single-ended mode	±2.0	
		f_{ADC} = 72MHz, sample rate = 1MSPS, V_{DDA} = 2.4V~3.3V, T_A = 25 °C, Differential mode	±1.5	
EL	Integral linearity error	f_{ADC} = 72MHz, sample rate = 1MSPS, V_{DDA} = 2.4V~3.3V, T_A = 25 °C, Single-ended mode	±1.5	
		f_{ADC} = 72MHz, sample rate = 1MSPS, V_{DDA} = 2.4V~3.3V, T_A = 25 °C, Differential mode	±1.0	

Notes:

[1] The ADC accuracy of the ADC is measured after internal calibration.

[2] ADC accuracy versus reverse injection current: It is necessary to avoid injecting reverse current on any standard analog input pin, as this can significantly reduce the accuracy of the conversion being performed on the other analog input pin. It is recommended to add a Schottky diode (between pin and ground) to standard analog pins that may generate reverse injection current. The forward injection current does not affect the ADC accuracy as long as it is within the range of $I_{INJ(PIN)}$ given in Table 4-2

[3] Guaranteed by characterization results, not tested in production.

[4] Guaranteed by design, not tested in production.

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Figure 4-18 ADC Precision Characteristics

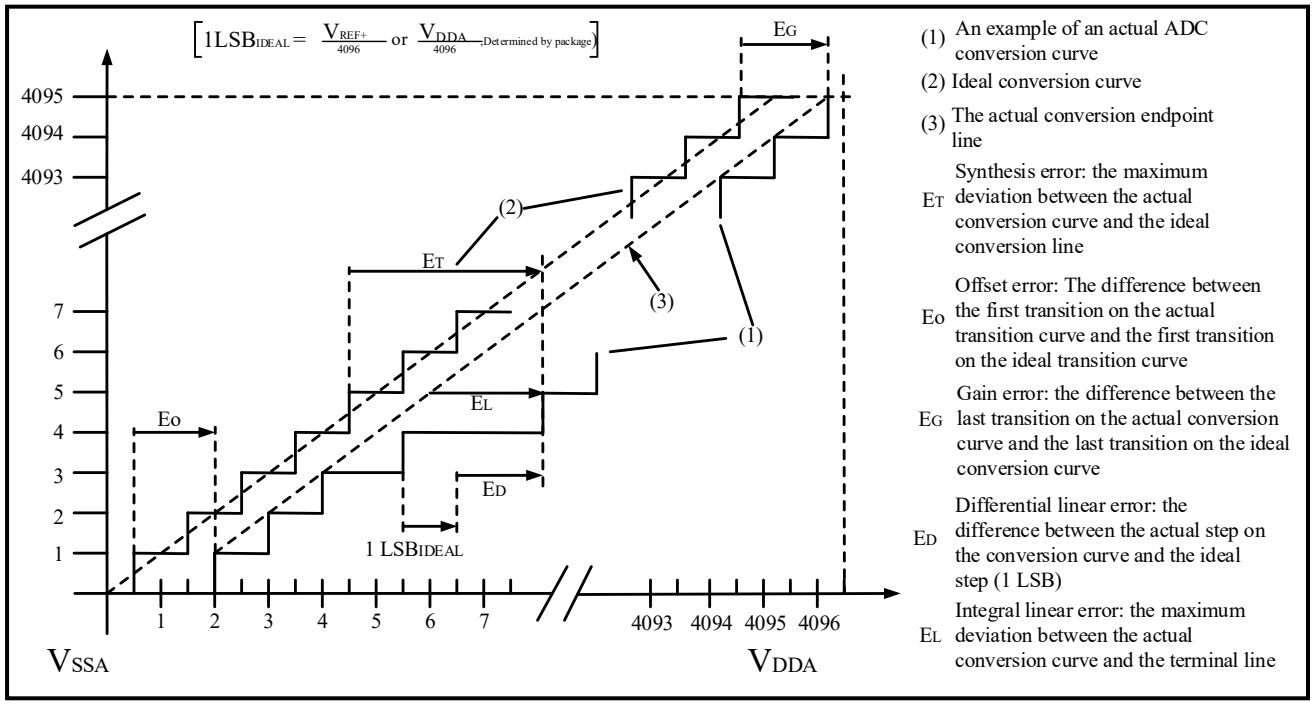
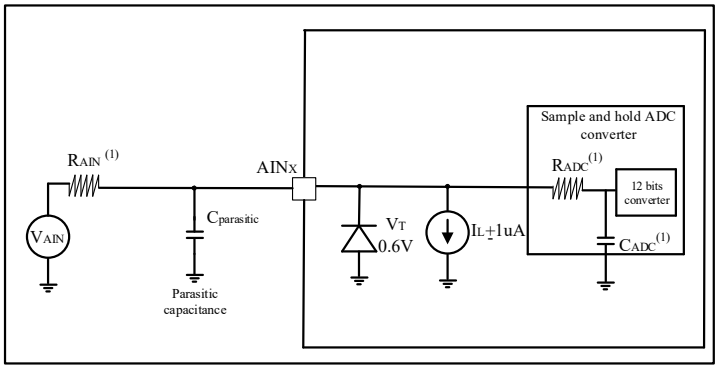


Figure 4-19 Typical Connection Diagram Using ADC



Notes:

(1) For values of R_{AIN}, R_{ADC}, and C_{ADC}, see Table 4-37.

(2) Cparasitic indicates parasitic capacitance on PCB (related to welding and PCB layout quality) and pads (approximately 7pF).A larger Cparasitic value would reduce the accuracy of the conversion and the solution was to reduce f_{ADC}.

PCB Design Suggestions

The decoupling of the power supply must be connected in accordance with Figure 4-20. The 10nF capacitors in the picture must be ceramic capacitors (good quality), and they should be as close as possible to the MCU chip.

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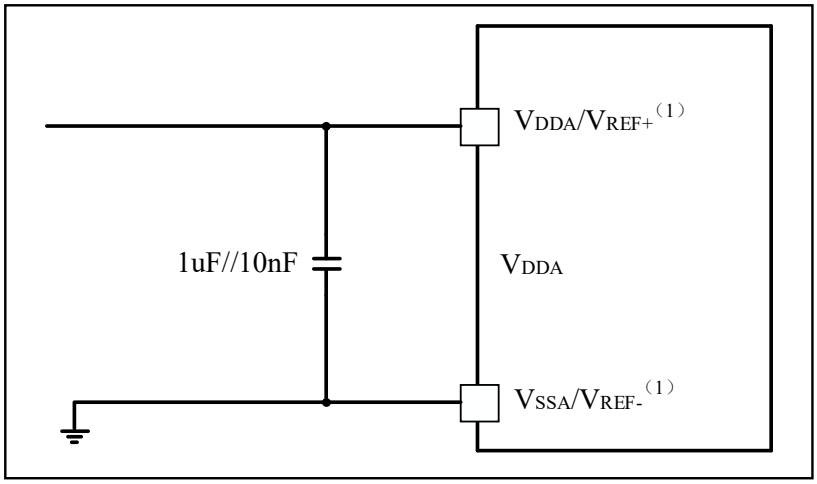
Figure 4-20 Decoupling Circuit of Power Supply And Reference Power Supply (V_{REF+} is Connected to V_{DDA})



Note: (1) V_{REF+} and V_{REF-} are internally connected to VDDA and VSSA.

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4.4.1 Comparator (COMP) Electrical Parameters

Unless otherwise specified, the parameters in Table 4-40 are measured using ambient temperature, f_{HCLK} frequency, and V_{DDA} supply voltage in accordance with the conditions in Table 4-4.

Table 4-40 COMP Characteristics (1)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DDA}	Analog Supply voltage	-		2.4	-	3.6	V
V_{IN}	Input voltage range	-		0	-	V_{DDA}	
$I_{DDA(SCALER)}$	Scaler static consumption from V_{DDA}	Sel = 100000 'b		-	-	350	µA
T_{START_SCALER}	Scaler starup time	-		-	1	2	µs
t_{START}(1)	Comparator startup time to reach propagation delay	High speed mode	2.4V≤V_{DDA}≤3.6V	-	-	6	µs
t_D	Propagation delay for 200 mV step with 100 mV overdrive	High speed mode	2.4V≤V_{DDA}≤3.6V	-	72	200	ns
V_{OFFSET}	Comparator offset error	Full common mode range		-	±10	±20	mV
Vhys	Comparator hysteresis	Low hysteresis		-	10	-	mV
		Medium hysteresis		-	20	-	
		High hysteresis		-	30	-	
I_{DDA}	Comparator consumption from V_{DDA}	High speed mode: one comparator is turned on, the internal reference is turned off	Static	-	45	-	µA
			With 50 kHz ±100 mV overdrive square signal	-	50	-	

Note: (1) Guaranteed by design, not tested in production.

4.4.2 Temperature Sensor (TS) Characteristics

Unless otherwise specified, the parameters in Table 4-41 are measured using ambient temperature, f_{HCLK} frequency, and V_{DDA} supply voltage in accordance with the conditions in Table 4-4.

Table 4-41 Temperature Sensor Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
T_L(1)	Linearity of V_{SENSE} with respect to temperature	-	±1	±4	ºC
Avg_Slope(1)	Average slope	-3.7	-4	-4.3	mV/ºC
V_{25}(1)	Voltage at 25ºC	-	1.32	-	V
t_{START}(1)	Startup time	-	-	10	µs
T_{S_temp}(2)(3)	When reading temperature, the ADC sampling time	8.2	-	17.1	µs

Notes:

(1) Guaranteed by characterization result, not tested in production.

(2) Guaranteed by design, not tested in production.

(3) The minimum sampling time can be determined by the application through multiple loops.

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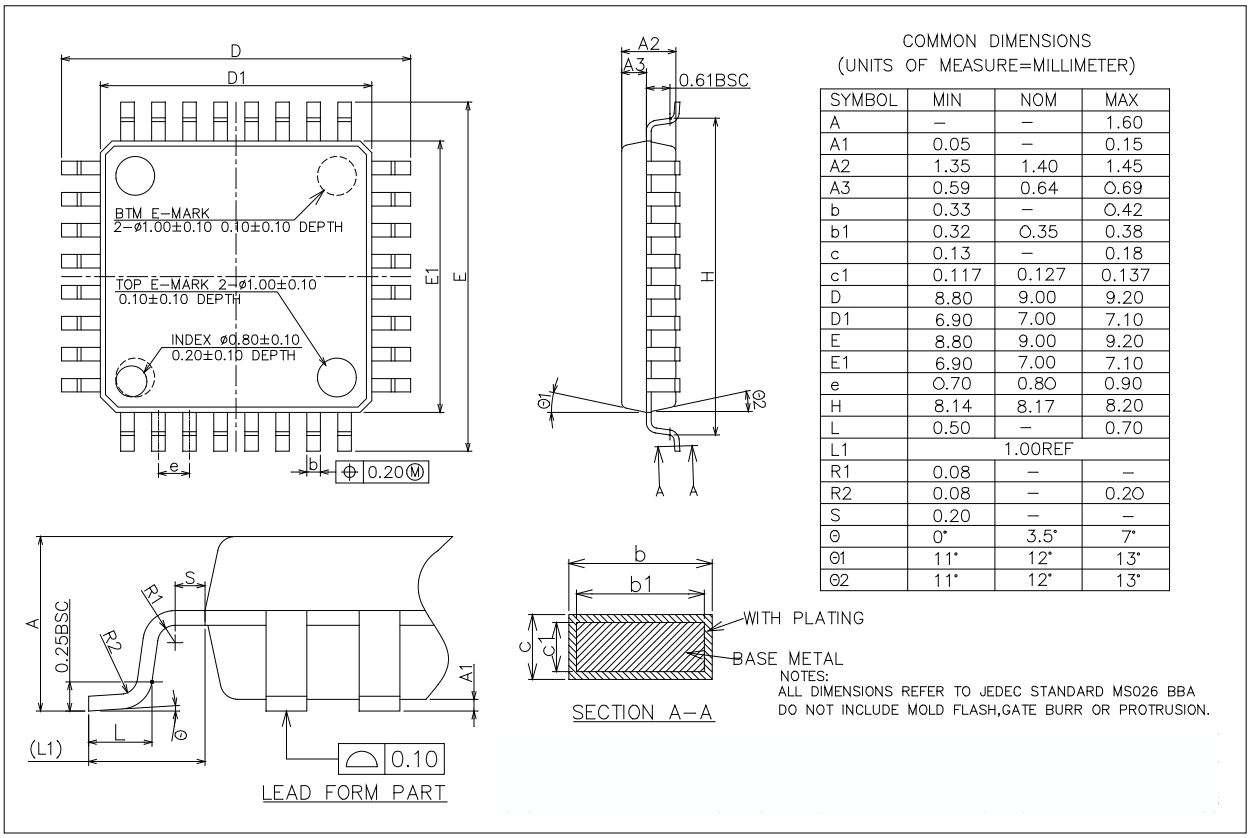
5 Package Information

5.1 LQFP32 (7mm x 7mm)

Figure 5-1 LQFP32 Package Dimensions



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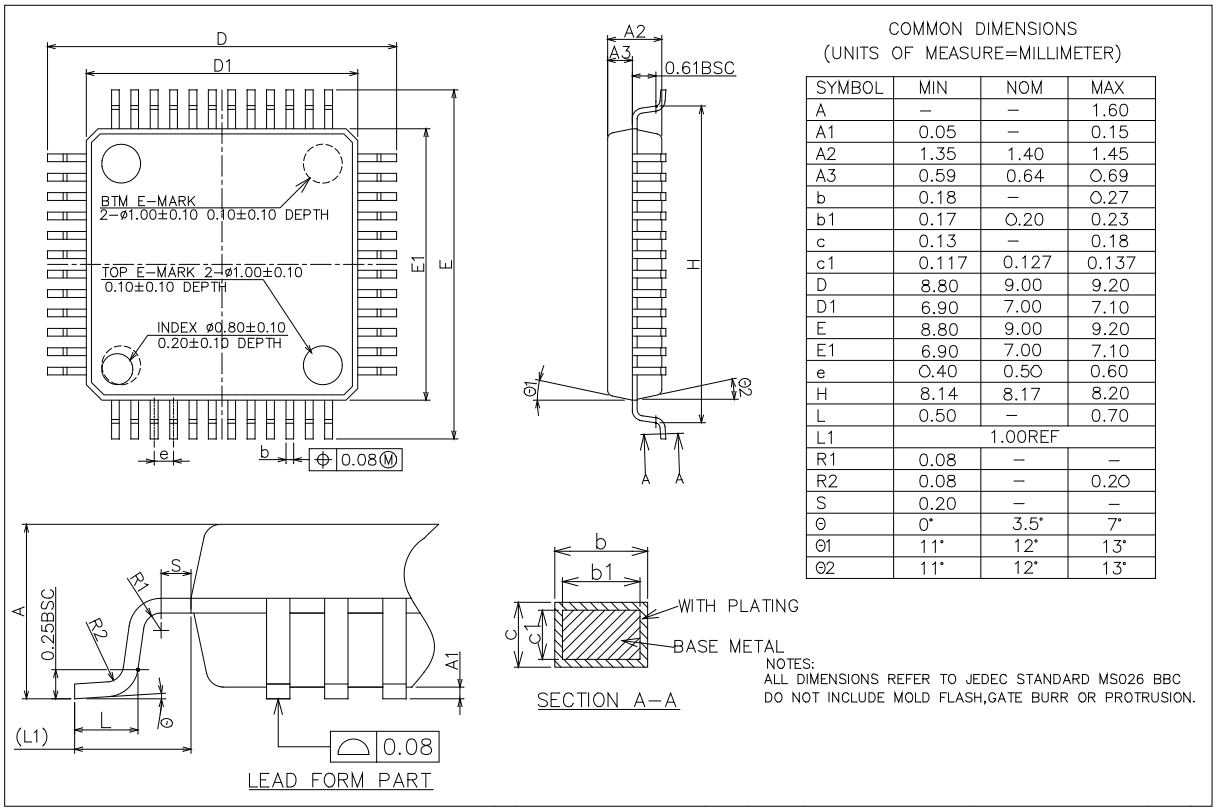
5.2 LQFP48 (7mm x 7mm)

Figure 5-2 LQFP48 Package Dimensions



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	–	–	1.60
A1	0.05	–	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.18	–	0.27
b1	0.17	0.20	0.23
c	0.13	–	0.18
c1	0.117	0.127	0.137
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
e	0.40	0.50	0.60
H	8.14	8.17	8.20
L	0.50	–	0.70
L1		1.00REF	
R1	0.08	–	–
R2	0.08	–	0.20
S	0.20	–	–
θ	0°	3.5°	7°
θ1	11°	12°	13°
θ2	11°	12°	13°

NOTES:
ALL DIMENSIONS REFER TO JEDEC STANDARD MS026 BBC
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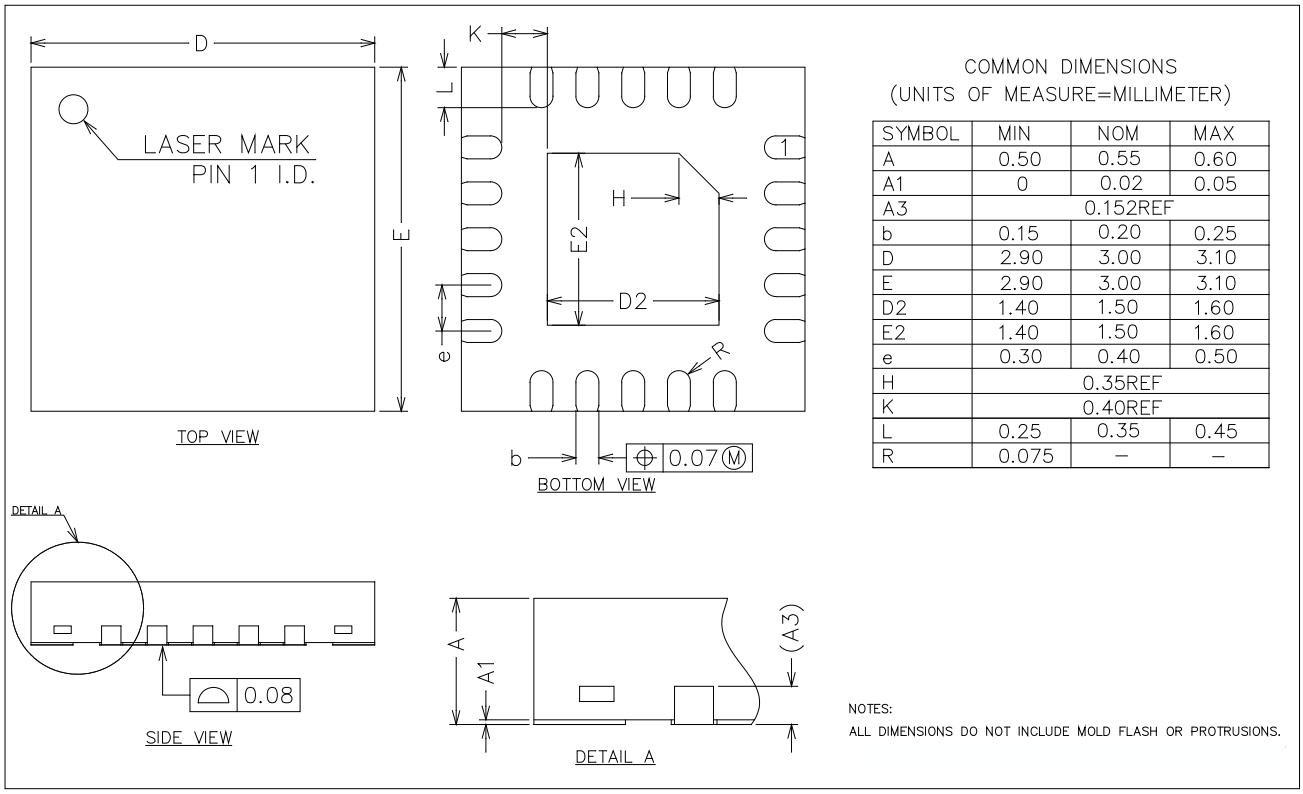
5.3 QFN20 (3mm x 3mm)

Figure 5-3 QFN20 Package Dimensions



SYMBOL	MIN	NOM	MAX
A	0.50	0.55	0.60
A1	0	0.02	0.05
A3		0.152REF	
b	0.15	0.20	0.25
D	2.90	3.00	3.10
E	2.90	3.00	3.10
D2	1.40	1.50	1.60
E2	1.40	1.50	1.60
e	0.30	0.40	0.50
H		0.35REF	
K		0.40REF	
L	0.25	0.35	0.45
R	0.075	–	–

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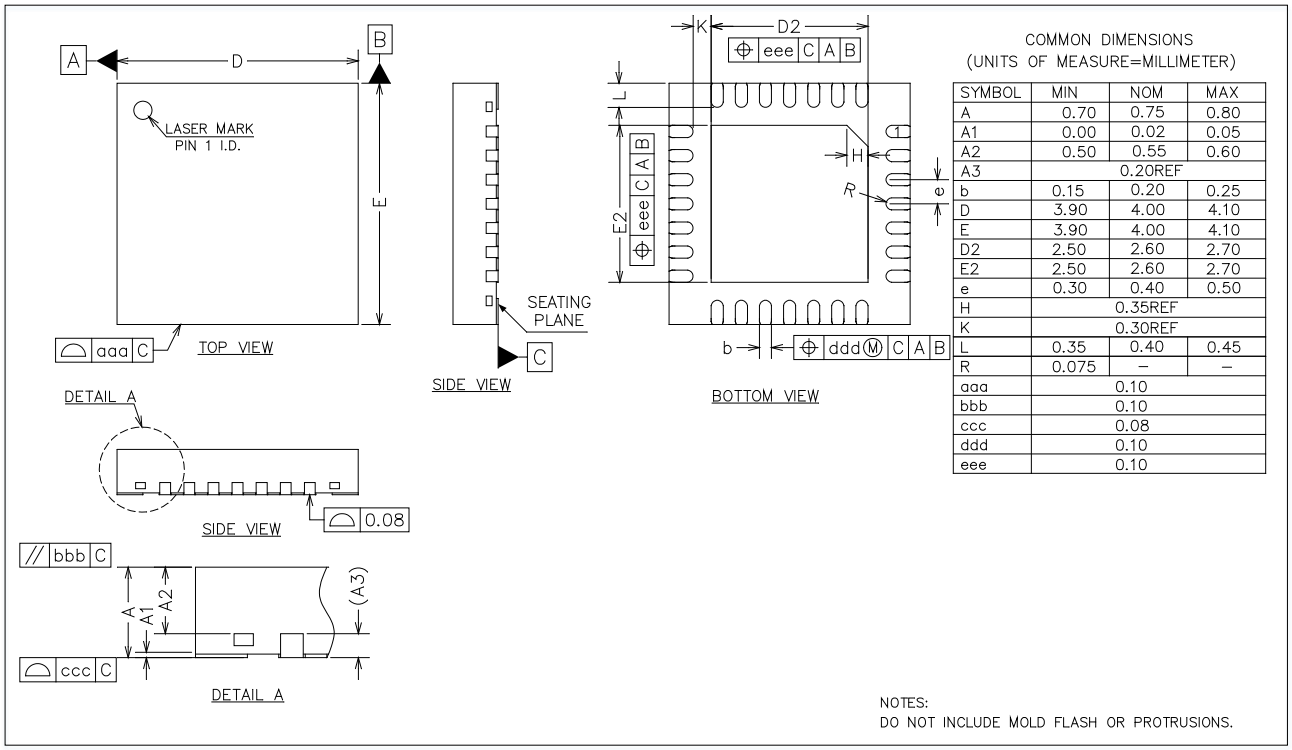
5.4 QFN28 (4mm x 4mm)

Figure 5-4 QFN28 Package Dimensions



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A2	0.50	0.55	0.60
A3		0.20REF	
b	0.15	0.20	0.25
D	3.90	4.00	4.10
E	3.90	4.00	4.10
D2	2.50	2.60	2.70
E2	2.50	2.60	2.70
e	0.30	0.40	0.50
H		0.35REF	
K		0.30REF	
L	0.35	0.40	0.45
R	0.075	–	–
aaa		0.10	
bbb		0.10	
ccc		0.08	
ddd		0.10	
eee		0.10	

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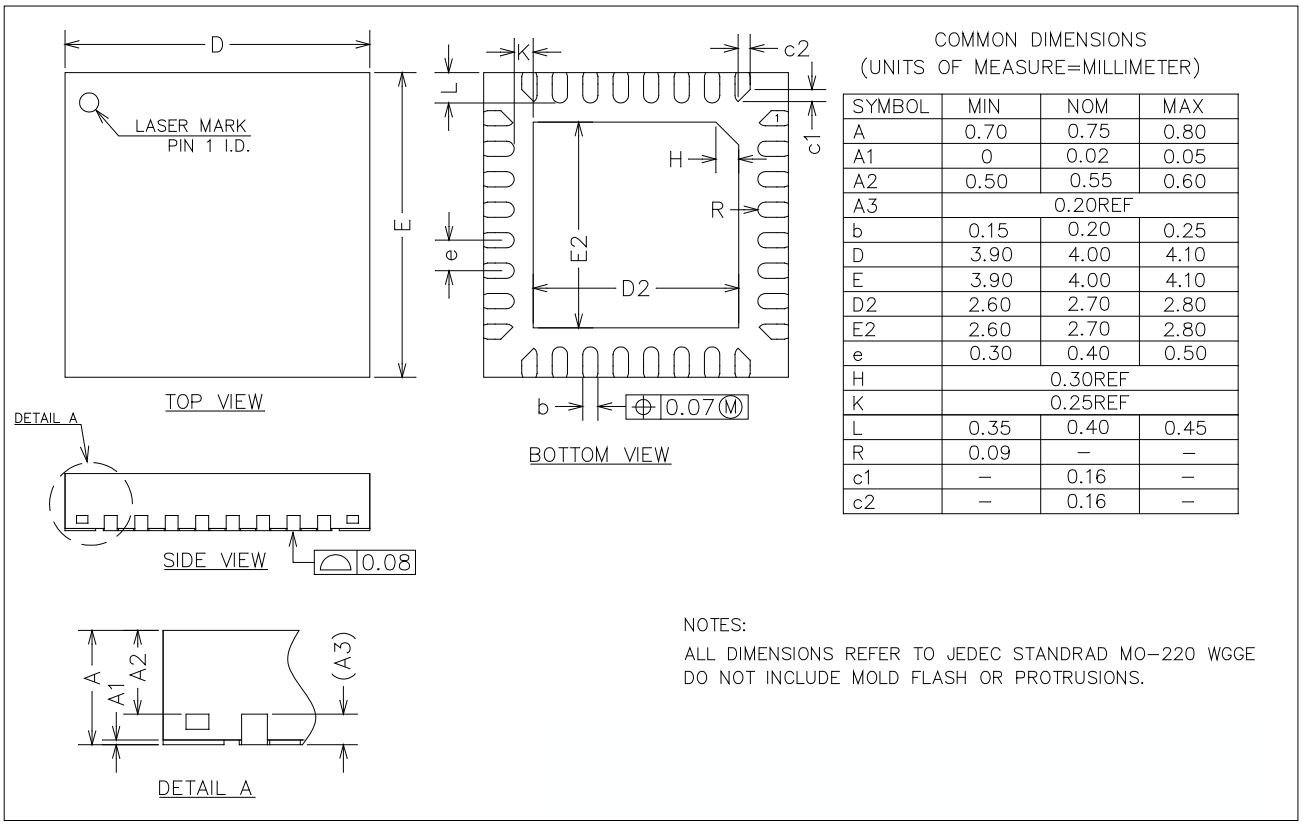
5.5 QFN32 (4mm x 4mm)

Figure 5-5 QFN32 Package Dimensions



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0	0.02	0.05
A2	0.50	0.55	0.60
A3		0.20REF	
b	0.15	0.20	0.25
D	3.90	4.00	4.10
E	3.90	4.00	4.10
D2	2.60	2.70	2.80
E2	2.60	2.70	2.80
e	0.30	0.40	0.50
H		0.30REF	
K		0.25REF	
L	0.35	0.40	0.45
R	0.09	–	–
c1	–	0.16	–
c2	–	0.16	–

NOTES:
ALL DIMENSIONS REFER TO JEDEC STANDRAD MO-220 WGGE
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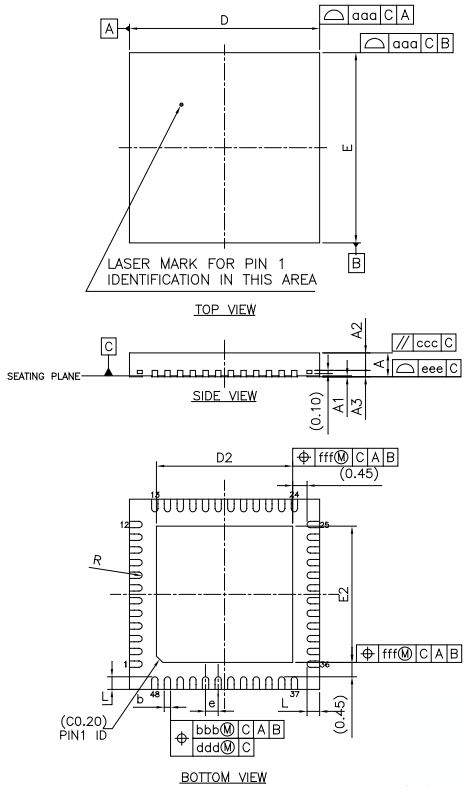
5.6 QFN48 (6mm x 6mm)

Figure 5-6 QFN48 Package Dimensions



Item		Symbol	MIN.	NOM.	MAX.
total height		A	0.70	0.75	0.80
stand off		A1	0.00	0.02	0.05
mold thickness		A2	0.50	0.55	0.60
leadframe thickness		A3		0.20 REF.	
lead width		b	0.15	0.20	0.25
package size	X	D	5.90	6.00	6.10
	Y	E	5.90	6.00	6.10
E-PAD size	X	D2	4.20	4.30	4.40
	Y	E2	4.20	4.30	4.40
lead length		L	0.30	0.40	0.50
lead pitch		e		0.40 bsc	
lead arc		R	0.075	---	---
Package profile of a surface		aaa		0.10	
Lead position		bbb		0.07	
Parallelism		ccc		0.10	
Lead position		ddd		0.05	
Lead profile of a surface		eee		0.08	
Epad position		fff		0.10	

NOTES:
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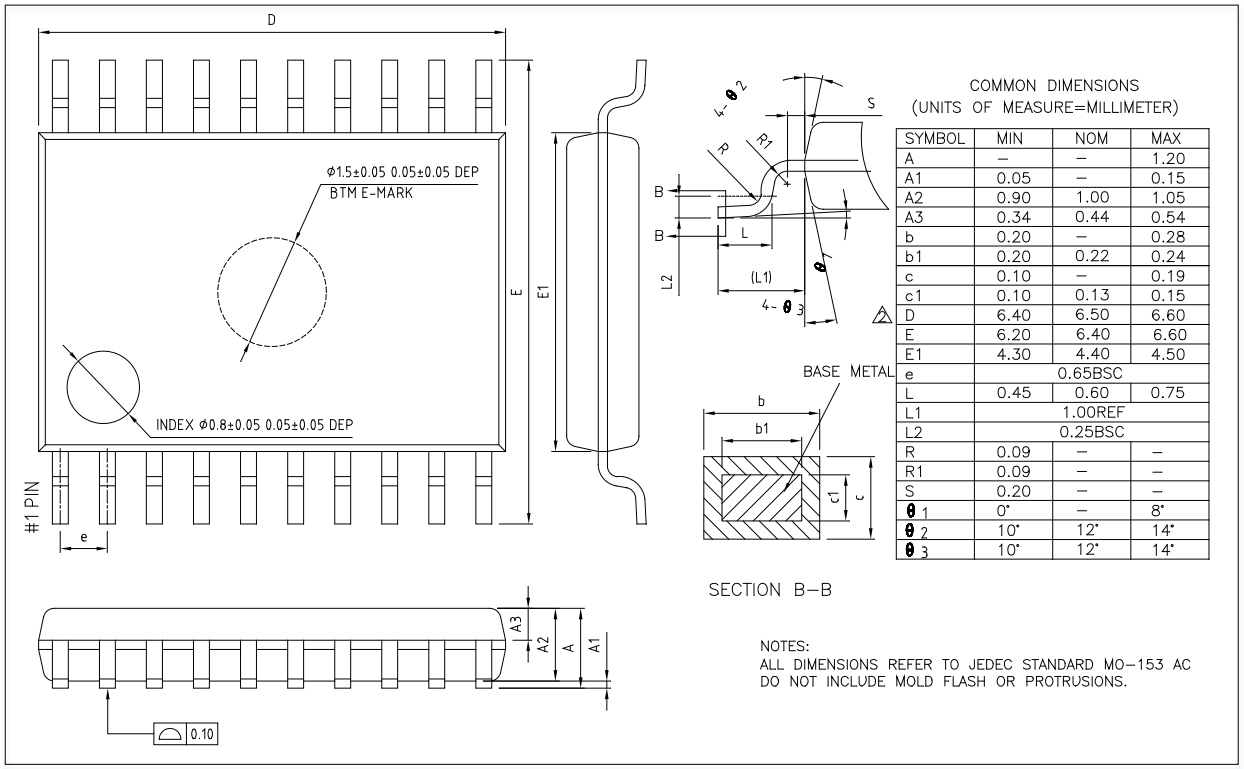
5.7 TSSOP20 (6.5mm x 4.4mm)

Figure 5-7 TSSOP20 Package Dimensions



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	–	–	1.20
A1	0.05	–	0.15
A2	0.90	1.00	1.05
A3	0.34	0.44	0.54
b	0.20	–	0.28
b1	0.20	0.22	0.24
c	0.10	–	0.19
c1	0.10	0.13	0.15
D	6.40	6.50	6.60
E	6.20	6.40	6.60
E1	4.30	4.40	4.50
e	0.65BSC		
L	0.45	0.60	0.75
L1	1.00REF		
L2	0.25BSC		
R	0.09	–	–
R1	0.09	–	–
S	0.20	–	–
θ1	0°	–	8°
θ2	10°	12°	14°
θ3	10°	12°	14°

NOTES:
ALL DIMENSIONS REFER TO JEDEC STANDARD MO–153 AC
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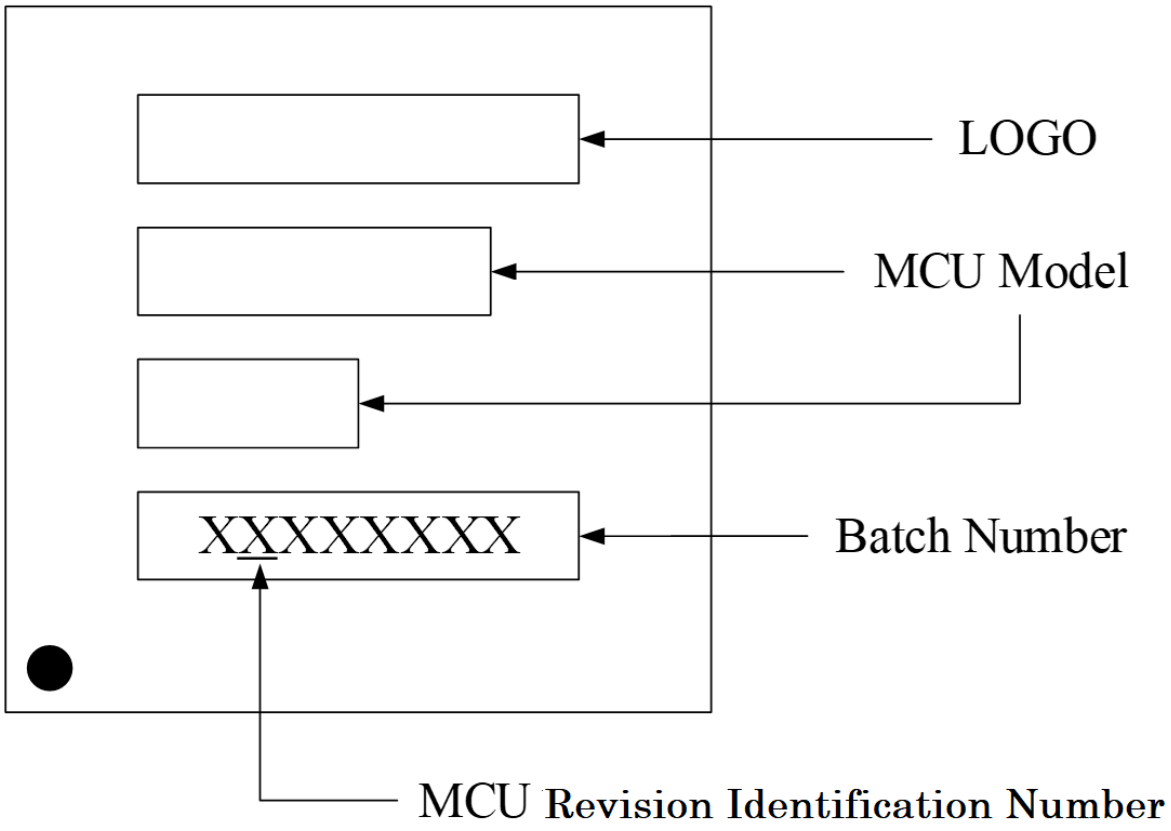
5.8 Marking Information

Figure 5-8 Marking Information



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6 Version History

Version	Date	Changes
V1.0.0	2023.6.6	Initial release

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NSING Technologies Pte. Ltd.
Add: NSING, Teletech Park #02-28, 20 Science Park Road, Singapore 117674
Tel: +65 69268090
Email: sales@nsing.com.sg