User Guide

Crystal Selection Guide

Introduction

This document details the crystal selection guide to provide users with a reference.

This document is only applicable to NSING MCU products. Currently, the supported product series includes N32G430 series.

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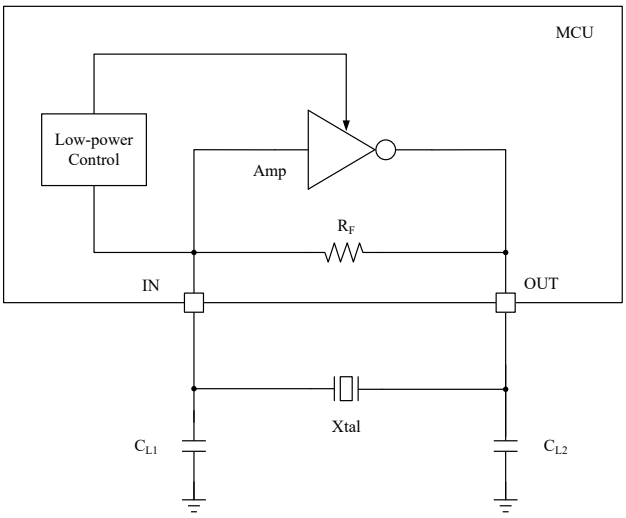
1. Description for Crystal Selection

1.1 Application Circuit for Crystal

Figure 1-1 is the typical application circuit for crystal. Feedback resistor (R_F) is embedded in the oscillator circuitry, no external resistance is required.

Figure 1-1 Typical Application with a 32.768 kHz Crystal



1.2 Selection of Capacitors

The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal/ceramic resonator oscillator. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

For C_{L1} and C_{L2}, it is recommended to use high-quality ceramic capacitors to match the requirements of the crystal. Usually, C_{L1} and C_{L2} have the same capacitance value.

Load capacitance C_L has the following formula:

$$C_L = \frac{C_{L1} \times C_{L2}}{C_{L1} + C_{L2}} + C_{stray}$$

C_{stray} is stray capacitance, sum of the device pin and the PCB (a parasitic) capacitances.

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For example: if you choose a crystal with a load capacitance of C_L =7 pF, and C_{stray} = 2 pF,

$$C_L - C_{stray} = \frac{C_{L1} \times C_{L2}}{C_{L1} + C_{L2}} = 5 \text{ pF}$$

hence C_{L1} = C_{L2} = 10 pF.

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1.3 Crystal Test

1.3.1 LSE Parameter Configuration

When using a low-speed external crystal (LSE), call the void RCC_LSE_Config (uint32_t RCC_LSE, uint16_t LSE_Trim) function to configure the LSE parameters through the input parameter uint16_t LSE_Trim. For details, see the following code example:

Figure 1-2 Example to Call RCC_LSE_Config Function

```
/**
 *\*\name    RCC_LSE_Config.
 *\*\fun     Configures the External Low Speed oscillator (LSE).
 *\*\param   RCC_LSE(the new state of the LSE):
 *\*\         - RCC_LSE_DISABLE    LSE oscillator OFF
 *\*\         - RCC_LSE_ENABLE     LSE oscillator ON
 *\*\         - RCC_LSE_BYPASS     LSE oscillator bypassed with external clock
 *\*\param   LSE_Trim(LSE Driver Trim Level):
 *\*\         - 0x00~0x1FF
 *\*\return  none
 **/
void RCC_LSE_Config(uint32_t RCC_LSE,uint16_t LSE_Trim)
{
    /* Enable PWR Clock */
    RCC_APB1_Peripheral_Clock_Enable(RCC_APB1_PERIPH_PWR);
    /* PWR DBKP set 1 */
    PWR->CTRL |=  PWR_CTRL_DBKP;

    /* Reset LSEEN LSEBP bits before configuring the LSE */
    *(__IO uint32_t*)RCC_BDCTRL_ADDR &= (~(RCC_LSE_ENABLE | RCC_LSE_BYPASS));
    /* Configure LSE (RCC_LSE_DISABLE is already covered by the code section above) */
    switch (RCC_LSE)
    {
        case RCC_LSE_ENABLE:
            /* Set LSEON bit */
            *(__IO uint32_t*)RCC_BDCTRL_ADDR |= RCC_LSE_ENABLE;
            RCC_LSE_Trim_Config(LSE_Trim);
            break;
        case RCC_LSE_BYPASS:
            /* Set LSEBYP and LSEON bits */
            *(__IO uint32_t*)RCC_BDCTRL_ADDR |= (RCC_LSE_BYPASS | RCC_LSE_ENABLE);
            break;
        default:
            break;
    }
}
```

Different configuration values have a great influence on the characteristics of the final crystal. The recommended LSE configuration parameter value is set to 0x1D7.

1.3.2 Crystal Frequency Test

1.3.2.1 Crystal frequency test @ 25℃

Referring to the peripheral hardware design in Figure 1-1, select a crystal and connect an external capacitor to test the crystal frequency. The crystal signal can be output to a frequency meter or other frequency testing instruments through the MCO.

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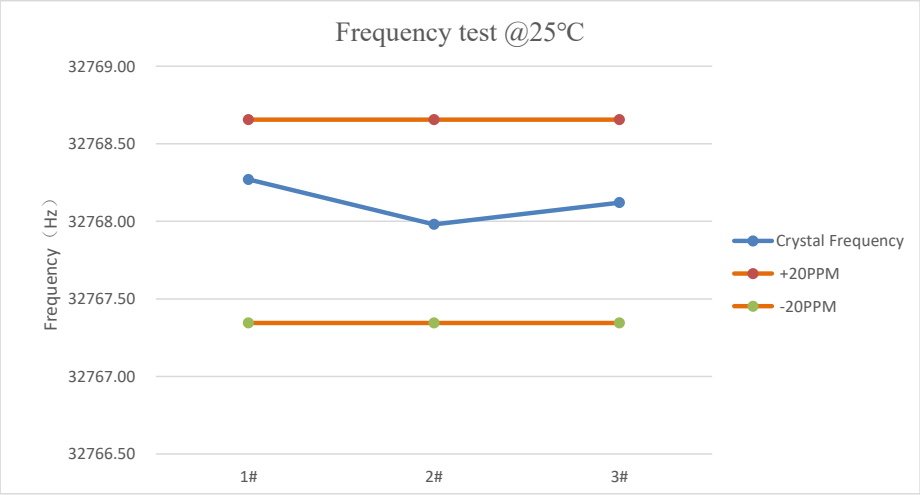
- For example

The selected crystal load capacitance C_L=9 pF, with the frequency tolerance is ±20ppm. Assuming C_{stray} is 4 pF, then C_{L1}=C_{L2}=10pF.

Note: C_{stray} is related to different test board hardware. Users can fine-tune the external capacitors C_{L1} and C_{L2} based on the test frequency.

Refer to Figure 1-3, is the crystal output frequency at normal temperature (25℃) when the LSE configuration parameter value is set to 0x1D7.

Figure 1-3 Crystal Output Frequency (25℃, C_{L1} = C_{L2} = 10 pF, LSE Configuration Parameter = 0x1D7)



As can be seen from Figure 1-3, the output frequencies of the three test boards are all within ±20ppm at 25℃ temperature condition.

1.3.2.2 Crystal frequency test @-40~85℃

Refer to Figure 1-4 is the crystal output frequency at the operating temperature (-40~85℃) when the LSE configuration parameter value is set to 0x1D7.

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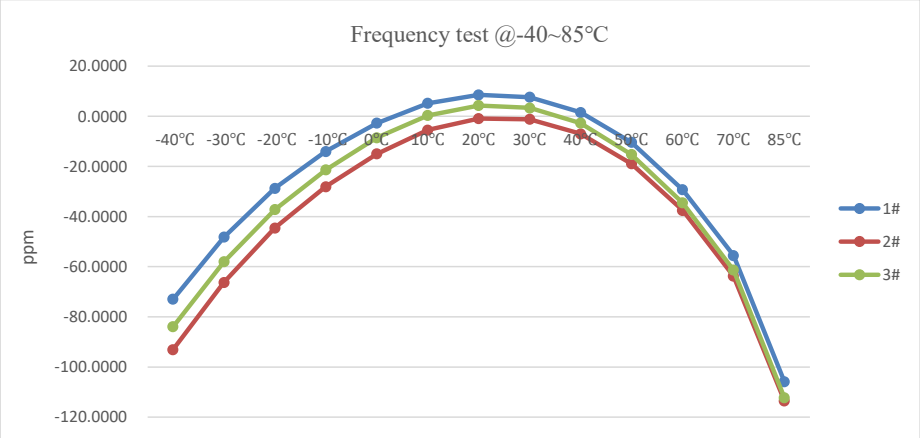
Figure 1-4 Crystal Output Frequency (-40~85℃, C_{L1} = C_{L2} = 10 pF, LSE Configuration Parameter = 0x1D7)



1.3.3 Crystal Compatibility List

When selecting a 32.768kHz external crystal for the N32G430 chip, it is important to ensure that the selected crystal can operate within the full temperature range.
The LSE configuration parameters are different, and the compatible crystal models are also different. Refer to Table 1-1, is the crystal full temperature test compatibility list, with the LSE configuration parameter set to 0x1D7.

Table 1-1 Crystal Compatibility List

No.	Product Name/Part Number	Package	Manufacturer	CL (pF)	CO (pF)	ESR(max) (kΩ)	Temp Range (℃)
1	TFX-04-32.768K(7PF)	1610	RIVER	7	1.3	90	-40~85
2	TFX-04-32.768K			12.5	1.3	90	
3	1TJH090DR1A0086		KDS	9	1.3	90	
4	DST1610A 32.768KHz			12.5	1.3	90	
5	X1A0001210005		EPSON	12.5	1.2	90	
6	SC-16S 32.768kHz 20PPM 12.5pF		SEIKO	12.5	1.2	90	
7	ABS06-32.768KHZ-T	2012	ABRACON	12.5		90	
8	SC-20S,32.768kHz,20PPM,7pF		SEIKO	7	1.3	90	
9	FC-12M 32.768000 kHz 7.0+20.0-20.0/X1A0000610006		EPSON	7	1.3	90	
10	TJXM32768K2TGDCNT2T		TAE	12.5		70	
11	1TJG125DR1A0019		KDS	12.5	1.3	80	
12	FC-135R 32.768KHz 9PF 20PPM/ X1A0001410002	3215	EPSON	9	1.1	50	
13	FC-135 32.768KHz 9PF 20PPM/ Q13FC13500003			9	1	70	

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14	FC-135 32.768KHz 7PF 20PPM/ Q13FC13500002			7	1	70	
15	FC-135 32.768kHz 6PF 20PPM/ Q13FC1350004900			6	1	70	
16	FC-135 32.768KHz 12.5PF 20PPM/ Q13FC13500004			12.5	1.2	70	
17	FC-135 32.768KHz 9PF 20PPM			9	1	70	
18	SC-32S 32.768kHz 7pF 20ppm		SEIKO	7	1	70	
19	SC-32S 32.768kHz 12.5pF 20ppm			12.5	1	70	
20	SC-32S 32.768kHz 9pF 20ppm			9	1	70	
21	SC-32S 32.768kHz 6pF 20ppm			6	1	70	
22	1TJF125DP1A000A		KDS	12.5	1.3	80	
23	NX3215SA-32.768kHz-EXS00A-MU00202		NDK	7	1	70	
24	7LC32768F12UC		SJK	12.5	1.2	70	
25	7LC32768F07UC			7	1.2	70	
26	SF32WK32768D71T005		TKD	7	1.1	70	
27	SF32WK32768D61T002			6	1.1	70	
28	FC31M2-32.768-NTLLLDT		HCI	12.5	1.5	70	
29	FC31M2-32.768-N09LLDT			9	1.5	70	
30	X321532768KGD2SI		YXC	12.5	1.2	70	
31	ETST00327000JE		HOSONIC	12.5	2	70	
32	TCXM32768K2NGDCZT2T		TAE	12.5	2	80	
33	XDMCZLNDDF-0.032768MHZ		TAITIEN	12.5			
34	KFC3276812520		KYX	12.5	1.2	70	
35	F3K232768PWQAC		JYJE	12.5		70	
36	26S-32.768-12.5-10-10/B	DT26	LIMING	12.5		90	
37	MC-146 32.768KHz 9PF 20PPM/ Q13MC14610004		EPSON	9	0.8	65	
38	MC-146 32.768KHz 12.5PF 20PPM/ Q13MC14620002			12.5	0.8	65	
39	SSP-T7-F 32.768kHz 20PPM 12.5pF	MC-146	SEIKO	12.5	0.8	65	
40	SSP-T7-F 32.768kHz 20PPM 7pF			7	0.8	65	
41	FR07S4-32.768-N07LLDT		HCI	7	0.8	65	
42	FR07S4-32.768-NTLLLDT			12.5	0.8	65	
43	TSXM32768K4KGDCZT3T		TAE	12.5	0.8	65	
44	7MC32768F12UC		SJK	12.5	1.2	70	
45	6LC32768F12UC		SJK	12.5	1.2	50	
46	6LC32768F06UC			6	1.2	50	
47	MC-306 32.768kHz 6PF 20PPM/ Q13MC3062000600	MC-306	EPSON	6	0.9	50	
48	X803832768KID4GI		YXC	6		70	
49	FR08S4-32.768-N06LLDT		HCI	6	0.9	50	

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50	CD01K032768FEPBAEAE	DT26	TKD	8	1.4	40	-20~70
51	CD01K032768ACNBAEAE			12.5	1.4	40	
52	Y26003271C2040DYJY		JGHC	12.5		40	
53	X206032768KGB2SC		YXC	12.5		40	
54	WTL2T45292LZ		WTL	12.5	1.5	40	
55	146-32.768-12.5-20-20/A	MC-146	LIMING	12.5			
56	7L032768NW2		HD	12.5	0.8	65	
57	X308032768KGB2SC	DT38	YXC	12.5		40	
58	CD02K032768AEPBAEAE		TKD	12.5	1.8	30	
59	38-32.768-12.5-10/A		LIMING	12.5			
60	S3132768092070	3215	JGHC	9	1	65	-10~60
61	SMD31327681252090			12.5	1	65	
62	S3132768072070			7	1	65	
63	DT-26-32.768K 6pF 20PPM	DT26	KDS	6	1.1	40	
64	DT-26 32.768KHz			12.5	1.1	40	
65	DT-38 32.768KHz	DT38	KDS	12.5	1.3	30	
66	Y308327681252075		JGHC	12.5	1.1	40	

Notes:

(1) The chip power supply voltage for the above crystal compatibility test is VDD=3.3V.

(2) It is recommended that customers use the crystals from the compatible list above, and customers need to confirm the availability of these crystals through production testing.

(3) If the crystal model used is not in the compatibility list, please contact NSING Technologies Pte. Ltd.

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2. Version History

Version	Date	Changes
V1.0	2022.05.19	Initial version.
V1.1.0	2022.10.31	The recommended LSE configuration parameter value is modified to 0x1D7.

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