Application Note

Slow Power-up

Introduction

This article takes the N32G45x series MCU as an example to introduce the issues that slow power-up may cause and software solutions.

This document is only applicable to NSING MCU products, currently supported product series are N32G4FR series, N32G45x series and N32WB452 series.

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1. Overview

During the slow power-up process of the chip, when the voltage reaches the operating voltage of the chip core (such as 1.7V), the core of the chip has already started running. However, this voltage cannot guarantee that peripherals can work properly. As the program has already started operating the peripherals, this can lead to abnormal initialization of the peripherals.

2. Solution

In the SystemInit (if there is no SystemInit, search for System_Initializes) function, add code to wait for the PVD to reach a threshold value, which should be determined based on the specific application of the customer. In this example, the threshold value is set to 2.9V.

The code is shown in the following figure, with the added code highlighted in red box:

Figure 2-1 IRQHandler

```
#ifdef POWER_ON_SLOWLY
#define PVDLEVEL_2V2 ((uint32_t)0x00000000)
#define PVDLEVEL_2V3 ((uint32_t)0x00000020)
#define PVDLEVEL_2V4 ((uint32_t)0x00000040)
#define PVDLEVEL_2V5 ((uint32_t)0x00000060)
#define PVDLEVEL_2V6 ((uint32_t)0x00000080)
#define PVDLEVEL_2V7 ((uint32_t)0x000000A0)
#define PVDLEVEL_2V8 ((uint32_t)0x000000C0)
#define PVDLEVEL_2V9 ((uint32_t)0x000000E0)

#define PVD_THRESHOLD PVDLEVEL_2V9


void PVD_IRQHandler(void)
{
    if ((EXTI->PEND & EXTI_LINE16) != (uint32_t)RESET)
    {
        /* Clear the EXTI line pending bit */
        EXTI->PEND = EXTI_LINE16;
        PVD_interrupt_flag = 1;
    }
}
#endif
```


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Figure 2-2 SystemInit

```
void SystemInit(void)
{
    uint32_t tmpregister = 0;

    /* FPU settings
#if (  FPU_PRESENT == 1) && (  FPU_USED == 1)
    /* Reset the RCC clock configuration to the default reset state(for debug purpose) */
    /* Set HSIEN bit */
    RCC->CTRL |= (uint32_t)0x00000001;

    /* Reset SW, HPRE, PPRE1, PPRE2, ADCPRE and MCO bits */
    RCC->CFG &= (uint32_t)0xF8FFC000;

    /* Reset HSEON, CLKSSEN and PLLEN bits */
    RCC->CTRL &= (uint32_t)0xFEF6FFFF;

    /* Reset HSEBYP bit */
    RCC->CTRL &= (uint32_t)0xFFFBFFFF;

    /* Reset PLLSRC, PLLXTPRE, PLLMUL and USBPRES/OTGFSPRE bits */
    RCC->CFG &= (uint32_t)0xF700FFFF;

    /* Reset CFG2 register */
    RCC->CFG2 = 0x00003800;

    /* Reset CFG3 register */
    RCC->CFG3 = 0x00003840;

    /* Disable all interrupts and clear pending bits  */
    RCC->CLKINT = 0x009F0000;

    /* Enable ex mode */
    RCC->APB1PCLKEN |= RCC_APB1PCLKEN_PWREN;
    PWR->CTRL3 |= 0x00000001;
    RCC->APB1PCLKEN &= (uint32_t)(~RCC_APB1PCLKEN_PWREN);

    /* Enable ICACHE and Prefetch Buffer */
     FLASH->AC |= (uint32_t)(FLASH_AC_ICAHEN | FLASH_AC_PRFTBFEN);

#ifdef POWER_ON_SLOWLY
    /* Enable PWR clock */
    RCC->APB1PCLKEN |= (uint32_t)0x10000000;
    /* PVD's EXTI configureation */
    EXTI->IMASK |= EXTI_LINE16;
    EXTI->FT_CFG |= EXTI_LINE16;
    /* NIIC configuration */
    NVIC_SetPriority(PVD_IRQn, 0);
    NVIC_EnableIRQ(PVD_IRQn);
    tmpregister = PWR->CTRL;
    /* Clear PRS[7:5] bits */
    tmpregister &= 0xFFFFFD1F;
    /* Set PRS[7:5] bits according to PWR_PVDLevel value */
    tmpregister |= PVD_THRESHOLD;
    /* Store the new value */
    PWR->CTRL = tmpregister;
    /* Enable PVD */
    PWR->CTRL |= (uint32_t)0x00000010;
    /* Wait for VDD voltage to reach PVD threshold */
    while(PVD_interrupt_flag == 0);
#endif
```


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3. Version History

Version	Date	Changes
V1.0.0	2023.03.28	Initial release

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