N32G4FR Series Errata Sheet

NSING Technologies Pte. Ltd.
Add: NSING, Teletech Park #02-28, 20 Science Park Road,
Singapore 117674
Tel: +65 69268090
Email: sales@nsing.com.sg

CONTENTS

NSING Technologies Pte. Ltd.
Add: NSING, Teletech Park #02-28, 20 Science Park Road,
Singapore 117674
Tel: +65 69268090
Email: sales@nsing.com.sg

NSING Technologies Pte. Ltd.
Add: NSING, Teletech Park #02-28, 20 Science Park Road,
Singapore 117674
Tel: +65 69268090
Email: sales@nsing.com.sg

1 Errata List

Table 1-1 Overview of Errata

Errata link			Chip version
			Version B
Ch 2: Power control (PWR)	2.1: STOP2 mode wake up		●
Ch 3: Reset and clock control (RCC)	3.1: System Timer (SysTick)		●
Ch 4: GPIO and AFIO	4.1: SPI1 slave mode, USART2 sync mode		●
	4.2: SPI1 master mode, USART2 sync mode		●
	4.3: SPI2 slave mode, USART3 sync mode		●
	4.4: SPI2 master mode, USART3 sync mode		●
Ch 5: Analog/Digital conversion (ADC)	5.1: ADC data left alignment		●
	5.2: ADC analog watchdog		●
	5.3: ADC injection channels trigger regular channel conversions		●
	5.4: Slave ADC conversion impacted by master ADC conversion		●
	5.5: Affecting adjacent ADC data registers		●
Ch6: Serial peripheral interface (SPI)	6.1: SPI interface	6.1.1: SPI baud rate setting	●
		6.1.2: Checking slave mode CRC	●
	6.2: I2S interface	6.2.1: PCM long frame mode	●
Ch 7: I2C interface	7.1: Handling software events before current byte transferring		●
	7.2: Notes on single read of one or two bytes		●

NSING Technologies Pte. Ltd.
Add: NSING, Teletech Park #02-28, 20 Science Park Road, Singapore 117674
Tel: +65 69268090
Email: sales@nsing.com.sg

	7.3: Using DMA simultaneously with other peripherals	●
Ch 8: Universal synchronous asynchronous receiver (USART)	8.1: Parity error flag	●
	8.2: RTS hardware flow control	●
Ch 9: Debug interface (DBG)	9.1: The Debug registers	●
Ch 10: Timer (TIM)	10.1: Timer repetitive capture detection	●
Ch 11: Real time clock (RTC)	11.1: RTC prescaler	●
	11.2: RTC calibration	●
	11.3: RTC timing	●
	11.4: RTC Periodic wakeup	●

NSING Technologies Pte. Ltd.
Add: NSING, Teletech Park #02-28, 20 Science Park Road,
Singapore 117674
Tel: +65 69268090
Email: sales@nsing.com.sg

2 Power Control (PWR)

2.1 STOP2 Mode Wake Up

Description

When the MCU is in STOP2 mode, wakeup and NRST reset occurs simultaneously, the NRST reset cannot reset MCU.

Wakeup takes precedence, and the MCU will respond to the wakeup event first.

Workaround

To resolve this issue, it is advised to avoid triggering an NRST reset of the MCU simultaneously with the wakeup event. Alternatively, if an NRST reset is necessary in a specific scenario, perform consecutive NRST reset to ensure the MCU is properly reset.

NSING Technologies Pte. Ltd.
Add: NSING, Teletech Park #02-28, 20 Science Park Road,
Singapore 117674
Tel: +65 69268090
Email: sales@nsing.com.sg

3 Reset and Clock Control (RCC)

3.1 System Timer (SysTick)

Description

The MCU can’t be awakened when external clock source (STCLK) is chosen as clock source.

Workaround

To address this issue, configure the SysTick control register to use the core clock as the clock source instead of the External Reference Clock (STCK).

NSING Technologies Pte. Ltd.
Add: NSING, Teletech Park #02-28, 20 Science Park Road,
Singapore 117674
Tel: +65 69268090
Email: sales@nsing.com.sg

4 GPIO and AFIO

4.1 SPI1 Slave Mode, USART2 Sync Mode

Description

With SPI1 and USART2 clocks already enabled, when pin PA4 is configured as multiplexed output, SPI1 operating in slave mode with NSS software mode (SSMEN=1, SSEL=0), the USART2 clock in synchronous mode cannot be transmitted.

Workaround

No solution is provided for this issue.

4.2 SPI1 Master Mode, USART2 Sync Mode

Description

With SPI1 and USART2 clocks already enabled, when pin PA4 is configured as multiplexed output, SPI1 operating in master mode with NSS software mode (SSMEN=1, SSEL=0), the USART2 clock in synchronous mode cannot be transmitted.

Workaround

Enable the SSOEN bit in SPI1 master mode.

4.3 SPI2 Slave Mode, USART3 Sync Mode

Description

With SPI2 and USART3 clocks already enabled, when pin PB12 is configured as multiplexed output, SPI2 operating in slave mode with NSS software mode (SSMEN=1, SSEL=0), the USART3 clock in synchronous mode cannot be transmitted.

Workaround

No solution is provided for this issue.

NSING Technologies Pte. Ltd.
Add: NSING, Teletech Park #02-28, 20 Science Park Road,
Singapore 117674
Tel: +65 69268090
Email: sales@nsing.com.sg

4.4 SPI2 Master Mode, USART3 Synch Mode

Description

With SP2 and USART3 clocks already enabled, when pin PB12 is configured as a multiplexed output, SPI2 operating in master mode with NSS software mode (SSMEN=1, SSEL=0), the USART3 clock in synchronous mode cannot be transmitted

Workaround

Enable the SSOEN bit in SPI2 master mode.

NSING Technologies Pte. Ltd.
Add: NSING, Teletech Park #02-28, 20 Science Park Road,
Singapore 117674
Tel: +65 69268090
Email: sales@nsing.com.sg

5 Analog/Digital Conversion (ADC)

5.1 ADC Data Left Alignment

Description

In the ADC single conversion mode, when using a non-12bit precision with left alignment, and triggering the conversion of regular channel by software, the most significant bit of the invalid bit in the ADC_DAT register is 1.

Workaround

To address this issue, either retain only the valid data bits or switch to right-aligned mode.

5.2 ADC Analog Watchdog

Description

In ADC independent mode, with single conversion, and non-12bit precision, enabling the analogue watchdog feature, and triggering the conversion of rule regular/injected channels by software, if the high threshold value of the analogue watchdog has valid bits equal to the value in the ADC data register, with all invalid bits set to 0, it may lead to a false triggering of the analogue watchdog.

Workaround

In this situation, ensure that the most significant bit of the invalid bits in the high threshold value of the analogue watchdog is set to 1 to prevent unintended triggering.

5.3 ADC Injection Channels Triggers Regular Channel Conversion

Description

In continuous conversion mode, with external triggering disable for regular channels and only software-triggered injection channel conversions, it is possible that the regular channels may be inadvertently triggered, leading to data being generated in ADC_DAT register, and the corresponding status bit in ADC_STS for regular channel conversion being set.

Workaround

Ignore the flags bits and data generated by regular channel conversions.

NSING Technologies Pte. Ltd.
Add: NSING, Teletech Park #02-28, 20 Science Park Road,
Singapore 117674
Tel: +65 69268090
Email: sales@nsing.com.sg

5.4 Slave ADC Conversion Impacted By Master ADC Conversion

Description:

When the ADC operates in dual ADC mode and synchronous injected mode, and only the software triggers the regular channel conversion of the master ADC, the regular channels of the slave ADC are also triggered. Additionally, the lower 16 bits from the ADC_DAT of the slave ADC are merged into the upper 16 bits of the master ADC_DAT.

Workaround:

No solution is provided for this issue.

5.5 Affecting Adjacent ADC Data Registers

Description:

In independent mode, when software triggers the conversion of the ADC4/2 regular channels, the lower 16 bits of the ADC4/2 DAT register content are merged into the upper 16 bits of the ADC3/1 DAT register.

Workaround:

No solution is provided for this issue.

NSING Technologies Pte. Ltd.
Add: NSING, Teletech Park #02-28, 20 Science Park Road,
Singapore 117674
Tel: +65 69268090
Email: sales@nsing.com.sg

6 Serial Peripheral Interface (SPI)

6.1 SPI Interface

6.1.1 SPI Baud Rate Setting

Description

CRC validation may fail if SPI master mode, when setting the bitrate control bits (BR[2:0]) to fPLCK/2.

Workaround

Avoid setting the bitrate control bits (BR[2:0]) to fPLCK/2 in this scenario.

6.1.2 Checking Slave Mode CRC

Description

The SPI operates in slave mode with CRC verification enabled, even if the NSS pin is at a high level, CRC calculations continues if the SPI receives a clock signal.

Workaround

Before using CRC validation, clear the CRC data register to ensure synchronization between the CRC checks of master and slave devices

The clearing steps are as follows:

1. Reset the SPI enable bit (set to 0)
2. Reset the CRC check bit (set to 0)
3. Set the CRC check bit (set to 1)
4. Set the SPI enable bit (set to 1)

NSING Technologies Pte. Ltd.
Add: NSING, Teletech Park #02-28, 20 Science Park Road,
Singapore 117674
Tel: +65 69268090
Email: sales@nsing.com.sg

6.2 I2S interface

6.2.1 PCM Long Frame Mode

Description

When I2S is operating in master mode, PCM long frame mode, and the data format is directly set to 32-bit or is extended from 16-bit to 32-bit, the WS (word select) signal occurs every 16bits instead of every 32bits.

Workaround

If I2S must operate in master mode and use long frame mode, it is recommended to use only the 16-bit data mode to ensure proper WS signal alignment.

NSING Technologies Pte. Ltd.
Add: NSING, Teletech Park #02-28, 20 Science Park Road,
Singapore 117674
Tel: +65 69268090
Email: sales@nsing.com.sg

7 I2C Interface

7.1 Handling Software Events Before Current Byte Transferring

Description

In the occurrence of events EV7, EV7_1, EV6_1, EV6, EV2, EV8, and EV3, it is essential to handle the events before the current byte transfer to prevent issues such as reading an extra byte, obtaining duplicate data, or losing data. If the software fails to read the N-1 data before the stop signal generation, the data in the shift register for the Nth byte may become corrupted (shifted left by one bit).

Workaround

1. When transferring more than one byte inI2C, consider using DMA if possible.
2. When using I2C interrupts, set the interrupt priority to the highest priority in the application
3. When the read data reaches the N-1 byte:

a) Check that BSF (Byte Shift Flag) is set to 1

b) Configure SCL as a GPIO open-drain output and set it to 0

c) Set STOPGEN to 1

d) Read the N-1 byte

e) Configure SCL back to I2C multiplex open-drain output mode.

f) Read the last byte

7.2 Notes On Single Read of One or Two Bytes

Description

In master read mode, errors in reading data may occur when reading single-byte or double-byte lengths.

Workaround

1. Single byte Read:

a) Upon receiving ADDRF

b) Set ACKEN to 0

c) Clear ADDRF bit (by reading STS1 first and then STS2)

d) Set STOPGEN to 1

e) Read one byte of data.

NSING Technologies Pte. Ltd.
Add: NSING, Teletech Park #02-28, 20 Science Park Road,
Singapore 117674
Tel: +65 69268090
Email: sales@nsing.com.sg

2. Double-byte read:

a) Upon receiving ADDRF

b) Set ACKPOS to 1

c) Clear ADDRF bit (by reading STS1 first and then STS2)

d) Set ACKEN to 0

e) Check that BSF (Byte Shift Flag) is 1

f) Set STOPGEN to 1

g) Read two consecutive bytes of data

7.3 Using DMA Simultaneously with Other Peripherals

Description

During I2C communication using DMA, it may lead to abnormal I2C communication, if there are other peripherals also use the same DMA controller.

Workaround

1. Use different DMA controllers.
2. Disable DMA for other peripherals during I2C DMA communication.

NSING Technologies Pte. Ltd.
Add: NSING, Teletech Park #02-28, 20 Science Park Road,
Singapore 117674
Tel: +65 69268090
Email: sales@nsing.com.sg

8 Universal Synchronous Asynchronous Receiver (USART)

8.1 Parity Error Flag

Description

During the reception of a byte of data, if a parity error is detected before receiving the stop bit, the parity error flag is set. During this period, the parity error flag cannot be cleared through software (by reading the status register and then reading data register again). If the parity error interrupt is enabled, it may repeatedly enter parity error interrupt handing function.

Workaround

1. When the read data buffer flag is set and data is received, clear the parity error flag.
2. Disable the parity error interrupt during the first entry into the parity error interrupt, the re-enable it after receiving the data.

8.2 RTS Hardware Flow Control

Description

When the RTS (Request to Send) hardware flow control is enabled, and a USART receives a frame of data, the RTS signal is automatically asserted (pulled high) upon receiving the first byte of data. If the first byte is not promptly read from the data register, upon receiving the next byte of data, the RTS signal is de-asserted (pulled low) again, and the USART waits for the reception of the next frame of data.

Workaround

Read the data from the data register promptly before receiving the next new data.

NSING Technologies Pte. Ltd.
Add: NSING, Teletech Park #02-28, 20 Science Park Road,
Singapore 117674
Tel: +65 69268090
Email: sales@nsing.com.sg

9 Debug Interface (DBG)

9.1 The Debug Registers

Description

The DBGMCU_IDCODE debugging register can only be accessed in debug mode (not accessible to user programs). When attempting to read it in user mode, the returned value is 0xFF.

Workaround

Avoid using IDCODE in user applications to prevent issues related to its restricted access in non-debug modes.

NSING Technologies Pte. Ltd.
Add: NSING, Teletech Park #02-28, 20 Science Park Road, Singapore 117674
Tel: +65 69268090
Email: sales@nsing.com.sg

10 Timer (TIM)

10.1 Timer Repetitive Capture Detection

Description

When an input capture occurs, if a new input capture is generated during the reading of TIMx_CCDATx (capture/compare register x) –where the read operation automatically clears the capture flag –the CCxOCF(capture/compare x repeat capture flag) might still remain set.

Workaround

No solution is provided for this issue.

NSING Technologies Pte. Ltd.
Add: NSING, Teletech Park #02-28, 20 Science Park Road,
Singapore 117674
Tel: +65 69268090
Email: sales@nsing.com.sg

11 Real Time Clock (RTC)

11.1 RTC Prescaler

Description

The asynchronous prescaler factor and the synchronous prescaler factor in the RTC cannot be set to 0, as it may lead to easily RTC pre-allocation to failure.

Workaround

Avoid setting the asynchronous prescaler register (TRC_PRE) DIVA[6:0] (asynchronous prescaler segment) and DIVS[14:0](synchronous prescaler segment) to 0.

11.2 RTC Calibration

Description

During RTC automatic calibration (when the CP bit in the RTC_CALIB register is set to 1), the automatic calibration may not successful if the asynchronous prescaler factor (DIVA) is not set to 128/64/32/16/8.

Workaround

To ensure successful RTC automatic calibration, choose an asynchronous prescaler (DIVA) factor of 128/64/32/16/8.

11.3 RTC Timing

Description

While the RTC is active, if an NRST (external reset) occurs, the reset period will cause the RTC to stop counting.

Workaround

No solution is provided for this issue.

11.4 RTC Periodic Wake-up

Description

Periodic wake-up from the RTC module does not work to wake up from STANDBY mode.

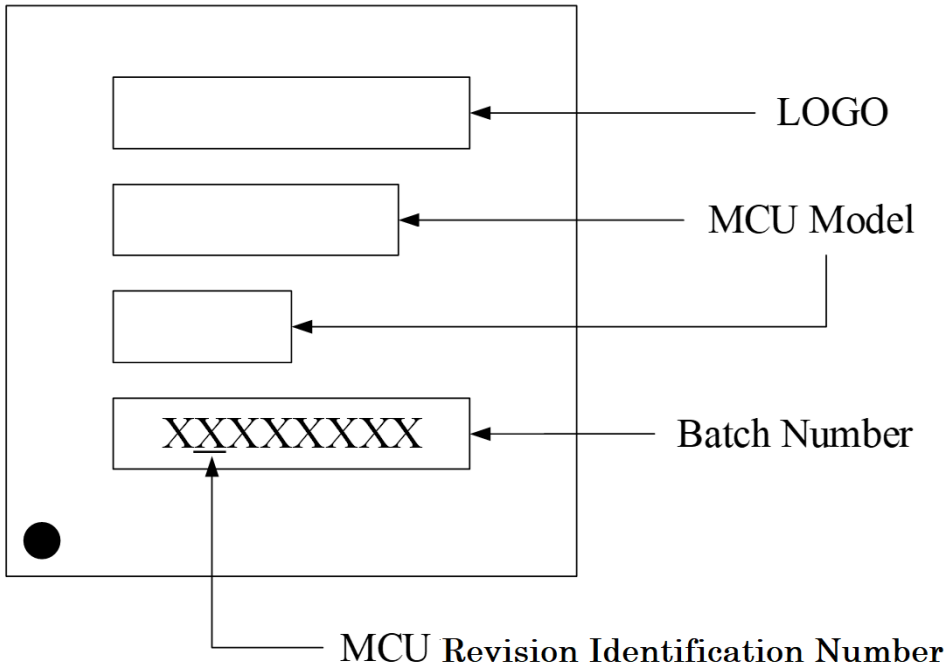
Workaround

NSING Technologies Pte. Ltd.
Add: NSING, Teletech Park #02-28, 20 Science Park Road, Singapore 117674
Tel: +65 69268090
Email: sales@nsing.com.sg

Use the RTC alarm wake-up feature instead of the periodic wake-up.

NSING Technologies Pte. Ltd.
Add: NSING, Teletech Park #02-28, 20 Science Park Road,
Singapore 117674
Tel: +65 69268090
Email: sales@nsing.com.sg

12 Chip Marking and Version Description



NSING Technologies Pte. Ltd.
Add: NSING, Teletech Park #02-28, 20 Science Park Road,
Singapore 117674
Tel: +65 69268090
Email: sales@nsing.com.sg

13 Version History

Version	Date	Changes
V1.0	2021.09.17	Initial release
V1.1.0	2022.09.02	Added the RTC wake-up errata item

NSING Technologies Pte. Ltd.
Add: NSING, Teletech Park #02-28, 20 Science Park Road,
Singapore 117674
Tel: +65 69268090
Email: sales@nsing.com.sg

14 Disclaimer

This document is the exclusive property of NSING TECHNOLOGIES PTE. LTD.(Hereinafter referred to as NSING). This document, and the product of NSING described herein (Hereinafter referred to as the Product) are owned by NSING under the laws and treaties of Republic of Singapore and other applicable jurisdictions worldwide. The intellectual properties of the product belong to Nations Technologies Inc. and Nations Technologies Inc. does not grant any third party any license under its patents, copyrights, trademarks, or other intellectual property rights. Names and brands of third party may be mentioned or referred thereto (if any) for identification purposes only. NSING reserves the right to make changes, corrections. enhancements, modifications, and improvements to this document at any time without notice. Please contact NSING and obtain the latest version of this document before placing orders. Although NATIONS has attempted to provide accurate and reliable information, NATIONS assumes no responsibility for the accuracy and reliability of this document. It is the responsibility of the user of this document to properly design, program, and test the functionality and safety of any application made of this information and any resulting product. In no event shall NATIONS be liable for any direct, indirect, incidental, special, exemplary, or consequential damages arising in any way out of the use of this document or the Product.

NATIONS Products are neither intended nor warranted for usage in systems or equipment, any malfunction or failure of which may cause loss of human life, bodily injury or severe property damage. Such applications are deemed, Insecure Usage’. Insecure usage includes, but is not limited to: equipment for surgical implementation, atomic energy control instruments, airplane or spaceship instruments, all types of safety devices, and other applications intended to supporter sustain life. All Insecure Usage shall be made at user's risk. User shall indemnify NATIONS and hold NATIONS harmless from and against all claims, costs, damages, and other liabilities, arising from or related to any customer's Insecure Usage Any express or implied warranty with regard to this document or the Product, including, but not limited to. The warranties of merchantability, fitness for a particular purpose and non-infringement are disclaimed to the fullest extent permitted by law. Unless otherwise explicitly permitted by NATIONS, anyone may not use, duplicate, modify, transcribe or otherwise distribute this document for any purposes, in whole or in part.

NSING Technologies Pte. Ltd.
Add: NSING, Teletech Park #02-28, 20 Science Park Road, Singapore 117674
Tel: +65 69268090
Email: sales@nsing.com.sg