

User Guide

N32G457QE_EVB Development board hardware User Guide

Introduction

The purpose of this document is to enable users to quickly get familiar with the N32G457QE_EVB development board, understand the function of the development board, use instructions and precautions, so as to conduct MCU debugging and development based on the development board.

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1 Hardware Development Instructions

1.1 Introduction

The N32G457QEL7_EVB development board is used for sample development of high-performance 32-bit N32G45x series chips of Nations Technologies Inc. This document describes in detail the functions, usage instructions, and precautions of the N32G457QE series development board.

1.2 Development board function

The main MCU chip model of the development board is N32G457QEL7, LQFP128 pin package, all function interfaces are connected to facilitate customer development, in addition, there are power supply and GND distributed everywhere in the board to facilitate debugging.

The main functional interfaces are listed as follows:

Table 1-1 Main function ports

No.	Interface	Interface to a number	Instructions
1	USB	J4	The USB connector
2	NSLINK	J183	The USB connector
3	NSLINK_SWD/JTAG/UART	J3	NSLINK signal
4	MCU IO	J24, J26, J27	96 MCU pins

In addition to the above interfaces, the comparator, ADC, DAC, general GPIO and other interfaces of the chip can be defined by referring to the corresponding pins in the user manual.

1.3 Development board layout

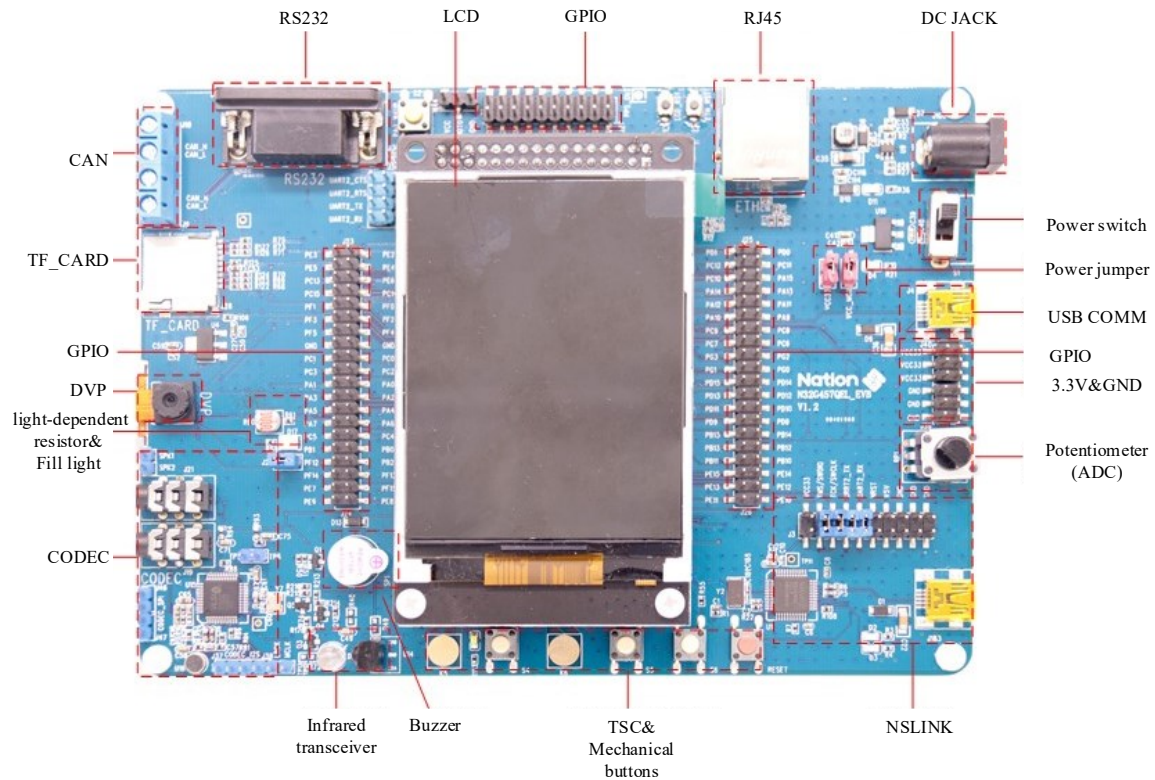


Figure 1-1 Development board layout TOP layer

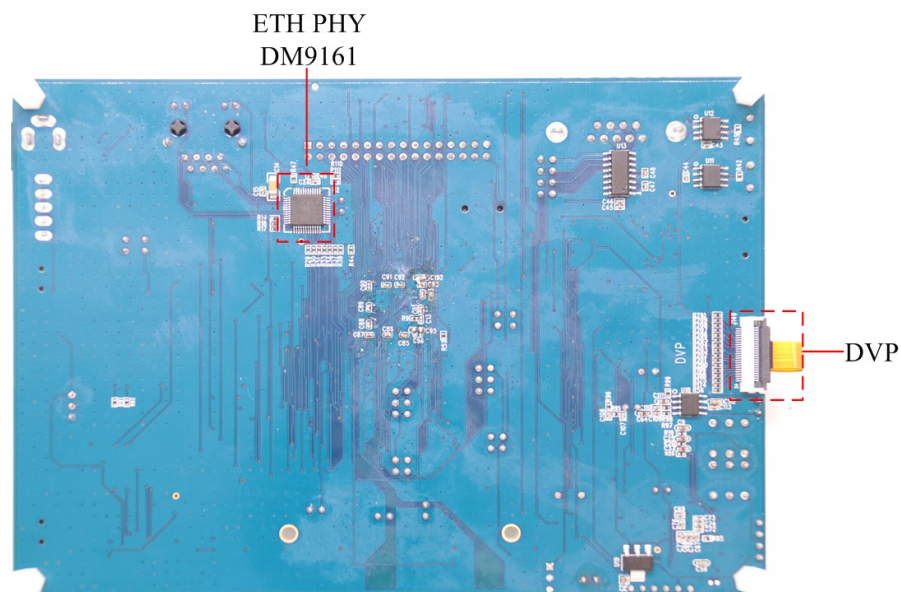


Figure 1-2 Development board layout BOTTOM layer

1) Power supply for development board

The development board has three power supply modes: 1) DCJACK power supply, the input voltage range is 6-12V; 2) USB power supply; 3) NSLINK power supply. DCJACK bit number J100, USB bit number J4, NSLINK bit number J183, the three power supply modes are controlled by switch S1. After switching S1, the power input to LDO is converted to 3.3V voltage, and then the voltage is divided into two channels, one of which supports MCU power supply alone and is selected by jumper J6, and one of which supports other functional modules power supply and is selected by jumper J5.

2) NSLINK Interface (J3)

NSLINK interface can be used for program download debugging, support two download modes: JTAG and SWD, with a virtual serial port, through the jumper J3 selection.

3) DVP Interface (J149)

The development board is equipped with a DVP interface to support camera function, and a photosensitive resistor R60 and a white light-emitting diode D17 to automatically adjust and compensate brightness.

4) RS232 interface

UART1 interface through RS232 interface chip (ADM3202) for level conversion, can support DB9 interface (J11). RS232 interface chip (ADM3202) is located in the BOTTOM layer, bit number U13, DB9 interface is located in the TOP layer. If the RS232 interface is enabled, connect jumpers J33, J34, J35, and J36.

5) CAN interface

CAN1&CAN2 convert two CAN interfaces J9 and J10 through CAN transceiver (TJA1050).

Both CAN interfaces are located at the TOP layer.

6) TF_CARD

Onboard TF card slot, TF card slot is located on the TOP surface of the development board, bit number J28.

7) CODEC

The development board adopts CODEC chip (VS1053B), input LINE_IN interface J19 and electret MIC U16, output a headphone interface J21 through power amplifier chip (TDA1308T), and output an external speaker interface SPK1&SPK2 through power amplifier chip (HT6872).CODEC chip is located in the TOP layer, bit number U15, power amplifier chip (TDA1308T) is located in the BOTTOM layer, bit number U17, power amplifier chip (HT6872) is located in the BOTTOM layer, bit number U18.CODEC supports SPI and I2S. If YOU choose SPI, you need to connect jumper J46 and J46.If I2S communication is selected, jumpers J37 and J38 need to be connected.

8) ETH

The development board uses Ethernet chip (DM9161) to output to RJ45 interface Y3 through RMII.The Ethernet chip is located in the BOTTOM layer, the bit number IS U2, and the RJ45 interface is located in the TOP layer.

9) EEROM&PSRAM

The development board adopts EEROM chip (AT24C02) and PSRAM chip (IS66WV51216EBLL), located at the TOP layer of the development board, with EEROM chip bit number U6 and PSRAM chip bit number U8.

10) SPI_FLASH&QSPI_FLASH

Develop onboard SPI FLASH (W25Q128JVSQTR) and QSPI FLASH (P25Q40ha-SSH-it), SPI FLASH is located at the TOP layer, bit number U7, QSPI FLASH is located at the TOP layer, bit number U5, both through jumper selection, If SPI FLASH is selected, connect jumper J29, J30, J31, J32; If QSPI FLASH is used, connect jumpers J1, J2, J8, J12, J15, and J20.

11) LCD

Develop onboard LCD display, connector is located in the TOP layer, bit number J14.

12) Infrared circuit and buzzer

The onboard infrared transmitting circuit and integrated infrared receiver are developed. The infrared transmitting tube is located at the TOP layer (bit number D12), and the integrated infrared receiver is located at the TOP layer (bit number U14). Development board onboard one buzzer, located in the TOP layer, bit number SP1.

13) TSC&KEY

Development of onboard three-way touch buttons, located in the TOP layer, bit number K5, K6, K7. Development of onboard three mechanical buttons, located in the TOP layer, S4, S5, S6.

14) GPIO port

96 independent GPIO ports, which can be reused with other function pins, refer to DS_N32G45x series data Manual V1.1 for details.

1.4 Development board key jumper instructions

Table 1-2 Development board key jumper description list-

No.	Jump line item No.	Jump line function	Directions for use
1	J5	3.3V power supply option	Power supply for other functional modules except MCU must be connected
2	J6	3.3V power supply option	To supply power to MCU, must connect
3	J16, J17	Ethernet Clock selection	It must be connected when using the Ethernet function.
4	J44	BOOT0 drop-down selection	Then pull up the left side, pull down the right side.
5	J45	BOOT1 Drop-down selection	Then pull down on the left, pull up on the right.
6	J3	NSlink jumper selection	Select the required download mode by silkscreen.
7	J46, J47	CODEC SPI communication options	CODEC connects this item when SPI communication mode is selected
8	J36, J37	CODEC I2S communication option	CODEC connects this item when I2S communication mode is selected
9	J29, J30, J31, J32	SPI flash choice	Connect this item when using SPI Flash
10	J1, J2, J8, J12, J15, J20	QSPI flash choice	Connect this item when using QSPI Flash
11	J33, J34, J35, J36	RS232 choice	Connect this item when RS232 level conversion is used
12	J41, J42, J43	Mechanical button selection	Connect this item when using mechanical buttons

1.5 Schematic diagram of N32G457QE development board

For the schematic diagram of N32G457QE, see the PDF file N32G457QE_EVB_V1.2.

Description of peripheral devices:

- 1) VCC_MCU: pin VDD_3 two capacitors, 4.7uF and 0.1uF respectively, the rest of the power pin nearby 0.1uF capacitor.
- 2) VCC33: Place 0.1uF capacitor near pin to ground.
- 3) DP, DM: 33 Ω series resistance, placed near the chip pin.

2 Version history

Version	Date	Note
V1.0	2020-5-16	Create a document

3 Disclaimer

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