N32G003 series

32-bit ARM® Cortex®-M0 microcontroller

User manual

Contents

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1 Abbreviations

1.1 Describes the List of Abbreviations Used in the Register Table

The following abbreviations are used in register descriptions:

read/write(rw)	Software can read and write these bits.
read-only(r)	Software can only read these bits.
write-only(w)	Software can only write this bit, and reading this bit will return the reset value.
read/clear(rc_w1)	Software can read this bit or clear it by writing' 1', and writing' 0' has no effect on this bit.
read/clear(rc_w0)	Software can read this bit or clear it by writing' 0', and writing' 1' has no effect on this bit.
read/clear by read(rc_r)	Software can read this bit. Reading this bit will automatically clear it to' 0'. Writing' 0' has no effect on this bit.
read/set(rs)	Software can read or set this bit. Writing' 0' has no effect on this bit.
read-only write trigger(rt_w)	Software can read this bit and write' 0' or' 1' to trigger an event, but it has no effect on this bit value.
toggle(t)	Software can only flip this bit by writing' 1', and writing' 0' has no effect on this bit.
Reserved(Res.)	Reserved bit, must be kept at reset value.

1.2 Available Peripherals

For all models of N32G003 microcontroller series, the existence and number of a peripheral, please refer to the data sheet of the corresponding model.

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2 Memory and Bus Architecture

2.1 System Architecture

2.1.1 Bus Architecture

The main system consists of the following parts:

- One master device:
  - Cortex®-M0 core
- Five slave devices:
  - Internal Flash memory
  - Internal SRAM
  - AHB2AHB bridge, which connects AHB modules
  - ADC
  - AHB2APB bridge, which connects APB modules

The system bus architecture is shown as in Figure 2-1:

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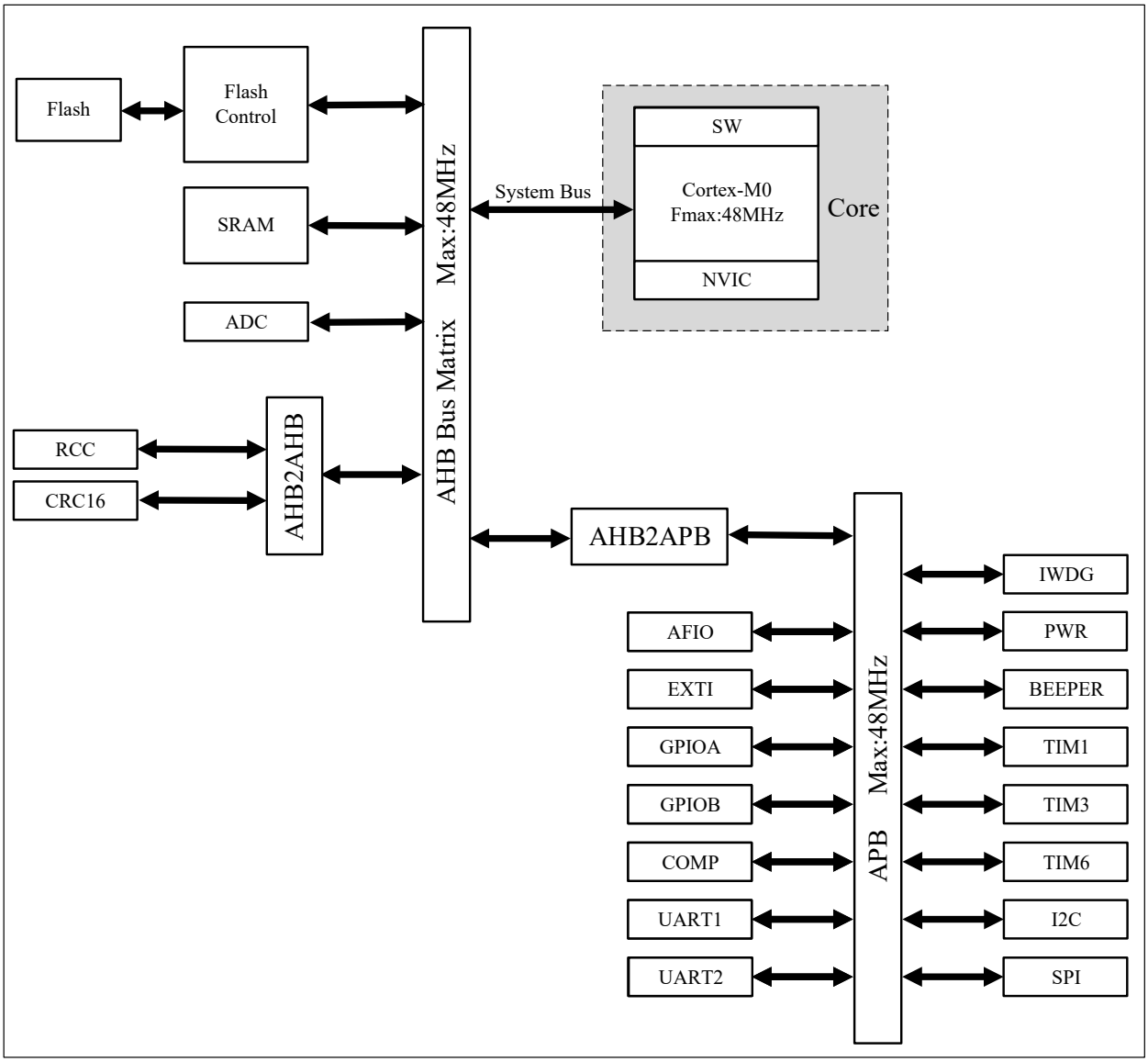
Figure 2-1 Bus Architecture



- CPU System bus: this bus connects the Cortex®-M0 core to bus matrix, utilied for instruction pre-fetch, data load (including constant load and debug access) and accessing AHB/APB peripherals.
- The bus matrix coordinates access arbitration for the core system bus. It comprises a single driver component (CPU system bus) and five slave components (Flash memory interface, SRAM, ADC, AHB and APB system bus). Certain AHB peripherals are connected to system bus via the bus matrix.
- The system comprises one AHB2APB bridge. APB consists of 16 APB peripherals, with a maximum PCLK speed of 48MHz.

2.1.2 Bus Address Mapping

The address mapping includes all AHB peripherals, APB peripherals, Flash, SRAM, System Memory, etc. The specific mapping is as follows:

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Figure 2-2 Bus Address Map

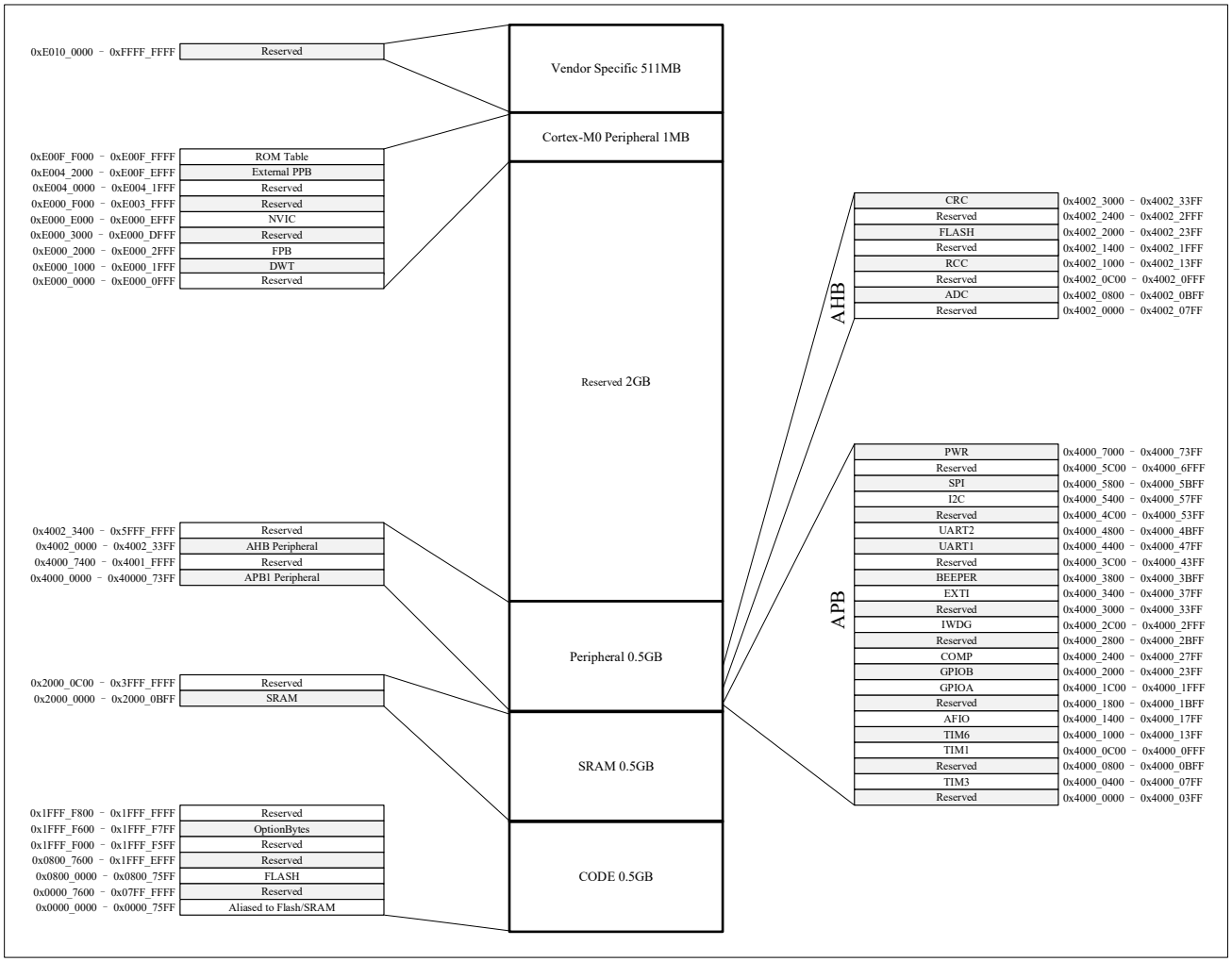

Table 2-1 List of Peripheral Register Addresses

Address Range	Peripherals	Bus
0x4002_3400 – 0x5FFF_FFFF	Reserved	AHB
0x4002_3000 – 0x4002_33FF	CRC	
0x4002_2400 – 0x4002_2FFF	Reserved	
0x4002_2000 – 0x4002_23FF	Flash	
0x4002_1400 – 0x4002_1FFF	Reserved	
0x4002_1000 – 0x4002_13FF	RCC	
0x4002_0C00 – 0x4002_0FFF	Reserved	
0x4002_0800 – 0x4002_0BFF	ADC	
0x4002_0000 – 0x4002_07FF	Reserved	
0x4000_7400 – 0x4001_FFFF	Reserved	APB
0x4000_7000 – 0x4000_73FF	PWR	
0x4000_5C00 – 0x4000_6FFF	Reserved	
0x4000_5800 – 0x4000_5BFF	SPI	
0x4000_5400 – 0x4000_57FF	I2C1	

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Address Range	Peripherals	Bus
0x4000_4C00 – 0x4000_53FF	Reserved	
0x4000_4800 – 0x4000_4BFF	UART2	
0x4000_4400 – 0x4000_47FF	UART1	
0x4000_3C00 – 0x4000_4300	Reserved	
0x4000_3800 – 0x4000_3BFF	BEEPER	
0x4000_3400 – 0x4000_37FF	EXTI	
0x4000_3000 – 0x4000_33FF	Reserved	
0x4000_2C00 – 0x4000_2FFF	IWDG	
0x4000_2800 – 0x4000_2BFF	Reserved	
0x4000_2400 – 0x4000_27FF	COMP	
0x4000_2000 – 0x4000_23FF	GPIOB	
0x4000_1C00 – 0x4000_1FFF	GPIOA	
0x4000_1800 – 0x4000_1BFF	Reserved	
0x4000_1400 – 0x4000_17FF	AFIO	
0x4000_1000 – 0x4000_13FF	TIM6	
0x4000_0C00 – 0x4000_0FFF	TIM1	
0x4000_0800 – 0x4000_0BFF	Reserved	
0x4000_0400 – 0x4000_07FF	TIM3	
0x4000_0000 – 0x4000_03FF	Reserved	

2.1.3 Boot Management

2.1.3.1 Boot address

During system startup, after a startup delay, the CPU fetches the address of the top-of-stack from address 0x0000_0000 and executes the code from the reset vector address indicated by address 0x0000_0004. Because of the Cortex®-M0 always gets the top-of-stack value and reset vector from addresses 0x0000_0000 and 0x0000_0004, so boot is only suitable for booting from the CODE area, and address remapping is designed for boot space.

- Boot from Main Flash memory:
  - Main Flash memory is mapped to the boot space (0x0000_0000);
  - Main Flash memory is accessible in two address areas, 0x0000_0000 or 0x0800_0000.

2.2 Memory System

The program memory, data memory, registers and I/O ports are organized in the same 4GB linear address space. Data bytes are stored in the memory in Little Endian format. The lowest numbered byte in a word is regarded as the least significant byte of the word, while the highest numbered byte is the most significant byte. The specifications of program memory and data memory are as follows.

2.2.1 Flash Specification

The Flash consists of a main memory block and the information block, which are described below:

- The maximum size of the main memory block is 29.5KB, also known as main Flash memory, which contains 59 pages for the storing and running of user programs, as well as data storage.

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- The information block is 2KB, containing 4 pages, which is composed of the system configuration area (1.5KB), and option byte area (0.5KB):
  - The system configuration area is 1.5KB and contains three pages.
  - The option byte area is 0.5KB, including 1 page, also known as option byte, with an effective space of 16B. User programs can read, write and erase this area.

2.2.1.1 Flash memory organization

Both the main memory block and the information block are allocated to bus address space.

Table 2-2 Flash Bus Address List

Memory Area	Page Name	Address Range	Size
Main memory block	Page 0	0x0800_0000 – 0x0800_01FF	0.5 KB
	Page 1	0x0800_0200 – 0x0800_03FF	0.5 KB
	Page 2	0x0800_0400 – 0x0800_05FF	0.5 KB
	⋮	⋮	⋮
	Page 58	0x0800_7400 – 0x0800_75FF	0.5 KB
Information block	System configuration area	0x1FFF_F000 – 0x1FFF_F5FF	1.5 KB
	Option byte area	0x1FFF_F600 – 0x1FFF_F60F	16B
Flash memory interface registers	FLASH_AC	0x4002_2000 – 0x4002_2003	4B
	FLASH_KEY	0x4002_2004 – 0x4002_2007	4B
	FLASH_OPTKEY	0x4002_2008 – 0x4002_200B	4B
	FLASH_STS	0x4002_200C – 0x4002_200F	4B
	FLASH_CTRL	0x4002_2010 – 0x4002_2013	4B
	FLASH_ADD	0x4002_2014 – 0x4002_2017	4B
	Reserved	0x4002_2018 – 0x4002_201B	4B
	FLASH_OB	0x4002_201C – 0x4002_201F	4B
	FLASH_USER2	0x4002_2020 – 0x4002_2023	4B
	FLASH_VTOR	0x4002_2024 – 0x4002_2027	4B

The Flash memory is organized as 32-bit wide memory cells that can store code and data constants.

The information block is divided into two parts:

- System configuration area, which contains basic chip information.
- Option byte area.

Writing to main memory block and information block is managed by embedded Flash programming/erasing controller.

There is two ways to protect Flash memory from illegal access (read, write and erase):

- Permission protection
- Readout protection (RDP)

During the Flash memory write operations, any read operation to the Flash memory will stall the bus, and the read operation can only be performed correctly after the write operation is completed. This means that code or data fetches cannot be

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made while a program/erase operation is ongoing.

When performing Flash programming operations (write or erase), the internal RC oscillator (HSI) must be turned on.

Note: in the low power consumption mode, all Flash memory operations are suspended.

2.2.1.2 Read and write operation

The Flash write operation only supports 32-bit operations. The Flash should be erased before the write operation. The the minimum block size for erasing is one page (0.5KB). The write operation is divided into erasing and programming phases.

When reading Flash, the number of waiting cycles for reading can be configured by the register. When using, it needs to be calculated in combination with the clock frequency of SYSCLK. For example, if SYSCLK <= 24MHz, the minimum number of wait cycles is 0; if 24MHz < SYSCLK <= 48MHz, the minimum number of wait cycles is 1.

Note: whether number of wait cycles is not zero, enabling prefetch buffer can improve overall efficiency.

2.2.1.3 Unlock Flash

After reset, the Flash module is protected and cannot be written into the FLASH_CTRL register to prevent accidental operation of Flash due to electrical disturbances and other reasons. By writing a specific sequence of key values into the FLASH_KEY register, you can unlock the operation authority of the FLASH_CTRL register. The specific sequence is: firstly, writing KEY1 = 0x45670123 to the FLASH_KEY register; secondly, writing KEY2 = 0xCDEF89AB to the FLASH_KEY register.

If there is an error in sequence or key value, a bus error will be returned and the FLASH_CTRL register will be locked until the next reset. Software can check FLASH_CTRL.LOCK bit to confirm whether the Flash is unlocked. If normal lock is required, software can set the FLASH_CTRL.LOCK bit to 1. After that, Flash can be unlocked by writing the correct key value series in FLASH_KEY register.

2.2.1.4 Erase and program

2.2.1.5 Erase of main memory block

The main memory block can be erased page by page or completely (Mass Erase).

- **Page Erase**

  Page Erase process:

  – Check the FLASH_STS.BUSY bit to confirm that there are no other Flash operations in progress;

  – Set the FLASH_CTRL.PER bit to '1';

  – Select the page to be erased with the FLASH_ADD register;

  – Set the FLASH_CTRL.START bit to '1';

  – Wait for the FLASH_STS.BUSY bit to change to '0';

  – Read out the content of the erased page and verify it.

- **Mass Erase**

  Mass Erase process (the first 3KB will not be erased if FLASH_OB.BOOT_LOCK = 1):

  – Check the FLASH_STS.BUSY bit to confirm that there are no other Flash operations in progress;

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- Set the FLASH_CTRL.MER bit to '1';
- Set the FLASH_CTRL.START bit to '1';
- Wait for the FLASH_STS.BUSY bit to change to '0';
- Read out all pages and verify.

2.2.1.6 Program of main memory block

The main memory block can be programmed 32 bits at a time. When the FLASH_CTRL.PG bit is '1', writing a word into a Flash address will start programming once; writing any half word of data will result in a bus error. During the programming process (the FLASH_STS.BUSY bit is '1'), any operation of reading or writing the Flash memory will cause the CPU to pause until the end of the Flash programming.

Main memory block programming process:

- Check the FLASH_STS.BUSY bit to confirm that there are no other Flash operations in progress;
- Set the FLASH_CTRL.PG bit to '1';
- Write the word to be programmed at the specified address;
- Wait for the FLASH_STS.BUSY bit to change to '0';
- Read the written address and verify the data.

Note: when the FLASH_STS.BUSY bit is '1', user cannot write to any register.

2.2.1.6.1 Erase and program of option byte

The option byte area is programmed differently from the main memory block. The number of option bytes is limited to 8 bytes (2 bytes for read protection, 4 byte for configuration options, and 2 bytes for user data memory). After unlocking the Flash, KEY1 and KEY2 must be written respectively (refer to section 2.2.1.3) to the FLASH_OPTKEY register, and then set the FLASH_CTRL.OPTWE bit to '1'. At this time, the option byte area can be programmed: set the FLASH_CTRL.OPTPG bit to '1' and then write a word to the specified address.

When programming the word in the option byte area, use the low byte in the half-word and automatically calculate the high byte (the high byte is the complement of the low byte) before starting the programming operation. This ensures that the option byte and its complement are always correct.

Option byte erase process:

- Check the FLASH_STS.BUSY bit to confirm that there are no other Flash operations in progress;
- Unlock the FLASH_CTRL.OPTWE bit;
- Set the FLASH_CTRL.OPTER bit to '1';
- Set the FLASH_CTRL.START bit to '1';
- Wait for the FLASH_STS.BUSY bit to change to '0';
- Read the erased option byte and verify it.

Option byte area programming process:

- Check the FLASH_STS.BUSY bit to confirm that there are no other Flash operations in progress;

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- Unlock the FLASH_CTRL.OPTWE bit;
- Set the FLASH_CTRL.OPTPG bit to '1';
- Writing the word to be programmed to the specified address;
- Wait for the FLASH_STS.BUSY bit to change to '0';
- Read the written address and verify the data.

2.2.1.7 Instruction prefetching

The Flash module supports instruction prefetch function with the prefetch buffer size of 8B. Through instruction prefetching, the instruction execution efficiency of CPU can be improved. The instruction prefetch function can be enabled or disabled through the register, and it is enabled by default.

2.2.1.8 Option byte

Option byte area is used to configure read protection, software/hardware watchdog, and reset options when the system is in power-off or shutdown mode. They consist of 8 option bytes: 2 bytes for read protection, 4 byte for configuration options, and 2 bytes defined by the user. The option byte area also contains the complement codes corresponding to the 8 option bytes, which are automatically calculated by the hardware when option bytes are written, and used for verification when the option bytes are read.

By default, option byte area is always read-accessible and write-protected. To write to the option byte area (program/erase), first unlock the Flash, and then unlock the option byte: write the correct key value sequence into FLASH_OPTKEY (KEY1 = 0x45670123, KEY2 = 0xCDEF89AB), and then write operation of the option byte area will be allowed. If the order or the key value is incorrect, the bus error will be returned and the option bytes will be locked until the next reset. To lock option byte normally, write ‘0’ to the OPTWE bit in the FLASH_CTRL register by software. The option bytes can be unlocked by writing the correct key value sequence to the FLASH_OPTKEY.

After each system reset, the option byte data is read from the option byte area and stored in the option byte register (FLASH_OB/FLASH_USER) with read-only properties. The complement data of option byte is read together to verify whether the option byte data is correct. If it does not match, an option byte error flag (FLASH_OB.OBERR) will be generated. When an option byte error occurs, the corresponding option byte is forced to 0xFF. If the optional byte and its complement code are both 0xFF (the state after erasing), the above verification steps are skipped and no verification is required.

Table 2-3 Option Byte List

Address	[31:24] Corresponding Complement code	[23:16] Option Byte	[15:8] Corresponding Complement Code	[7:0] Option Byte
0x1FFF_F600	nUSER	USER	nRDP1	RDP1
0x1FFF_F604	nData1	Data1	nData0	Data0
0x1FFF_F608	nUSER3	USER3	nUSER2	USER2
0x1FFF_F60C	nUSER4	USER4	nRDP2	RDP2

- Configuration option: USER
  - USER[7:5]: Reserved

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  - USER[4]: NRST_PA0 configuration option, read through FLASH_OB[6]
    0: PA0 is a normal GPIO pin
    1: PA0 is NRST pin
  - USER[3]: BOOT_LOCK configuration option, read through FLASH_OB[5]
    0: Flash first 3KB is unlocked
    1: Flash first 3KB is locked
  - USER[2]: nRST_PD configuration option, read through FLASH_OB[4]
    0: A reset occurs when entering PD mode
    1: No reset occurs when entering PD mode
  - USER[1]: nRST_STOP configuration option, read through FLASH_OB[3]
    0: A reset occurs when entering STOP mode
    1: No reset occurs when entering the STOP mode
  - USER[0]: WDG_SW configuration option, read through FLASH_OB[2]
    0: Hardware watchdog
    1: Software watchdog
- Two bytes of user data: Datax
  - Data1 (stored in FLASH_OB[25:18])
  - Data0 (stored in FLASH_OB[17:10])
- Configuretion options bytes: USERx
  - USER2[7:0]: LVR filter counter control, read through FLASH_USER[7:0]
  - USER3[3:0]: LVR power on level configure, read through FLASH_USER[11:8]
  - USER3[4]: LVR enable, read through FLASH_USER[12]
  - USER3[5]: LVR filter enable, read through FLASH_USER[13]
  - USER3[6]: LVR reset enable, read through FLASH_USER[14]
  - USER4[7:0]: Power on delay reset control, read through FLASH_USER[23:16]

  Note: when USER and nUSER are both 0xFF, indicating the state after erasing, the function of the corresponding bit is invalid. To activate the function, it needs to be programmed to the complement code state.
- Read protection L1 level option byte: RDP1
  - Protect code stored in Flash memory
  - When the correct value is written, it is not allowed to write Flash memory via SWD
  - The result of whether RDP1 is enabled can be queried through FLASH_OB[1]
- Read protection L2 level option byte: RDP2

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- Add protection function on the basis of L1. For details, refer to Section 2.2.1.7 Read protection
- The result of whether RDP2 is enabled can be queried through FLASH_OB[31]

2.2.1.9 Read protection

The user code in Flash can be protected against unauthorized reading by setting read protection. Read protection is set by configuring RDP bytes in the option byte area. Three different read protection levels can be configured, as shown in the following Table:

Table 2-4 Read Protection Configuration List

Read Protection Status	RDP1	nRDP1	nRDP2	RDP2
L1 level	0xFF	0xFF	RDP2! = 0xCC || nRDP2! = 0x33	
L0 level	0xA5	0x5A	RDP2! = 0xCC || nRDP2! = 0x33	
L2 level	0xXX	0xXX	0x33	0xXX
L1 level	None of the preceding three configurations			

- L0 level:
  - In the unprotected state, (RDP1 == 0xA5 & NRDP1 == 0x5A) && (RDP2 != 0xCC | nRDP2 != 0 x33)
  - Main memory and option byte area can be read arbitrarily
  - Can be rewritten to L1 or L2 level
- L1 level:
  - The corresponding ~(((RDP1 == 0xa5&nrdP1 == 0x5A) && (RDP2 != 0xCC | nRDP2 != 0 x33) | | (RDP2 == 0 XCC & nRDP2 == 0 x33))
  - When read protection of the option bytes are reprogrammed to unprotected L0 level, all the main memory block will automatically be erased. The process is as follows: (Erasing the option byte area will not trigger Mass Erase operation, because the result of erasing is 0xFF, which is equivalent to remaining in protection state of L1 level)
    - Write the correct sequence of key value sequence into the FLASH_OPTKEY to unlock option byte area
    - Initiates the command to erase the entire option byte area (Page erase)
    - Write 0xA5 to read protection option byte
    - Automatically erase of all main memory block by hardware
    - Automatically write 0xA5 to read protection option byte by hardware
    - When the system is reset (such as software reset, etc.), option byte area (including the new RDP value 0xA5) will be reloaded into the system, and read protection will be released
  - All functions of loading and executing code into the built-in SRAM via SWD are still valid, and can also be enabled from the built-in SRAM via SWD. This function can be used to remove read protection.
- L2 level:
  - The L2 level is realized by configuring another option byte RDP2. No matter what the value of RDP1 is, as long as it satisfies (RDP2 = 0xCC & nRDP2 = 0x33), it is the L2 level

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- The protection level cannot be modified (irreversible)
- Except for option byte/page erase and SWD disable, all other features are the same as L1 level

2.2.1.10 Permission protection

- Flash main memory permissions:
  - At the L0 level: all main memory block can be read. When FLASH_OB.BOOT_LOCK = 0, then first 3K byte can write and erase; when FLASH_OB.BOOT_LOCK = 1, then first 3K byte can not write and erase.
  - At the L1/2 level:
    - The first 3K byte is read-only, while access to other content (W/R/PE) is allowed during code execution in FLASH/SRAM
    - SWD is not allowed to access to FLASH/SRAM
    - When transitioning from L1 level to L0, entire Flash main memory block is automatically erased
- Flash options byte area permissions:
  - At the L0/L1 level, access is allowed (W/R/PE).
  - L2 level: Read-only access to Flash option bytes is allowed except for debugging mode.
- Flash system configuration area
  - Read-only after being seal

Table 2-5 Flash Read-write-erase Permission Control Table

Protect level	Boot mode Perform user / Access area	Flash		Changing a Protection Level
		Flash/SRAM	SWD	
L0 Level	First 3KB of Flash main memory block FLASH_OB.BOOT_LOCK = 0	Read-Write-Erase	Read-Write-Erase	Change to L1 or L2 is allowed
	First 3KB of Flash main memory block FLASH_OB.BOOT_LOCK = 1	Only read	Only read	
	Last 3KB Flash main memory block	Read-Write-Erase	Read-Write-Erase	
	Flash main memory block mass erase(1)	Allow	Allow	
	Flash option byte area	Read-Write-Erase	Read-Write-Erase	
	System configuration area	Only read	Only read	
	SRAM (All)	Read-Write	Read-Write	
L1 Level	First 3KB of Flash main memory block FLASH_OB.BOOT_LOCK = 0	Only read	Forbid	Change to L0 or L2 is allowed. When changed to L0, the main memory block is automatically erased
	First 3KB of Flash main memory block FLASH_OB.BOOT_LOCK = 1	Only read		
	Last 3KB of Flash main memory block	Read-Write-Erase		
	Flash main memory block mass erase(1)	Allow	Forbid	
	Flash option byte area	Read-Write-Erase	Read-Write-Erase	
	System configuration area	Only read	Only read	

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	SRAM (All)	Read-Write	Forbid	
L2 Level	First 3KB of Flash main memory block FLASH_OB.BOOT_LOCK = 0	Only read	Forbid	No modification is allowed
	First 3KB of Flash main memory block FLASH_OB.BOOT_LOCK = 1	Only read		
	Last 3KB of Flash main memory area	Read-Write-Erase		
	Flash main memory block mass erase(1)	Allow		
	Flash option byte area	Only read		
	System configuration area	Only read		
	SRAM (All)	Read-Write		

Note:

(1) When FLASH_OB.BOOT_LOCK = 1, the first 3K can not be erased.

2.2.2 SRAM

SRAM is mainly used for code operations to store variables, data or stacks during program execution, with a maximum capacity of 3KB.

SRAM supports byte, half word, word read and write access.

SRAM supports code operations and can run programs at full speed in SRAM. The maximum address range of SRAM is from 0x2000_0000 to 0x2000_0BFF.

SRAM cannot retain data in PD mode; data in STOP mode can be retained.

The main features are as follows:

- The maximum total capacity is 3KB
- Supports byte/half word/word reading and writing
- Supports CPU access
- The CPU bus can be remapped to SRAM to run the programs at full speed

2.2.3 Flash Register Description

All register operations must be performed in words (32 bits).

2.2.3.1 Flash register overview

Table 2-6 Flash Register Overview

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
000h	FLASH_AC	Reserved																										PRFTBFS	PRFTBFE	Reserved	LATENCY		
	Reset Value																											1	1		0	0	0
004h	FLASH_KEY	FKEY																															
	Reset Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
008h	FLASH_OPTKEY	OPTKEY																															
	Reset Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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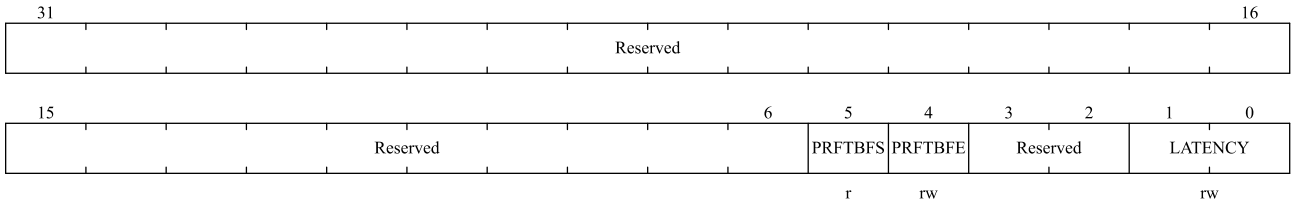
Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
00Ch	FLASH_STS	Reserved																								ECCERR	Reserved	EOP	WRPERR	Reserved	PGERR	Reserved	BUSY
	Reset Value																									0		0	0		0		0
010h	FLASH_CTRL	Reserved																		ECCERRITE	EOPITE	Reserved	ERRITE	OPTWE	Reserved	LOCK	START	OPTER	OPTPG	Reserved	MER	PER	PG
	Reset Value																			0	0		0	0		1	0	0	0		0	0	0
014h	FLASH_ADD	FADD																															
	Reset Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
018h	Reserved																																
01Ch	FLASH_OB	RDPRT2	Reserved							Data1								Data0								Reserved		Reserved	NRST_PA0	BOOT_LOCK	nRST_PD	nRST_STOP	WDG_SW	RDPRT1	OBERR
	Reset Value	0						1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1	0	0
020h	FLASH_WRP	Reserved																WRPT															
	Reset Value																	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
024h	FLASH_ECC	Reserved																										ECC					
	Reset Value																											0	0	0	0	0	0

2.2.3.2 Flash access control register (FLASH_AC)

Address offset: 0x00

Reset value: 0x0000 0030



Bit Field	Name	Description
31:6	Reserved	Reserved, the reset value must be maintained.
5	PRFTBFS	Pre-fetch buffer status This bit indicates the state of the pre-fetch buffer 0: The pre-fetch buffer is disabled. 1: The pre-fetch buffer is enabled.
4	PRFTBFE	Pre-fetch buffer 0: Disables the pre-fetch buffer. 1: Enables the pre-fetch buffer.
3:2	Reserved	Reserved, the reset value must be maintained
1:0	LATENCY	Time delay These bits represent the ratio of the SYSCLK (system clock) cycle to the Flash access time

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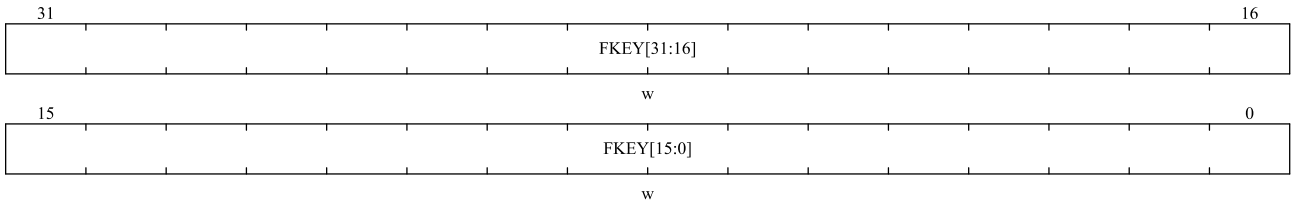
Bit Field	Name	Description
		00: Zero periodic delay, when 0 < SYSCLK ≤ 24MHz 01: A periodic delay, when 24MHz < SYSCLK ≤ 48MHz Others: Reserved

2.2.3.3 Flash key register (FLASH_KEY)

Address offset: 0x04

Reset value: 0xXXXX XXXX

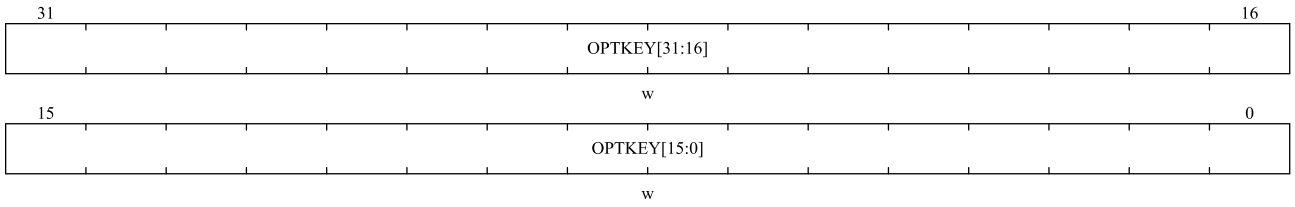


Bit Field	Name	Description
31:0	FKEY	Used to unlock the FLASH_CTRL.LOCK bit.

2.2.3.4 Flash OPTKEY register (FLASH_OPTKEY)

Address offset: 0x08

Reset value: 0xXXXX XXXX

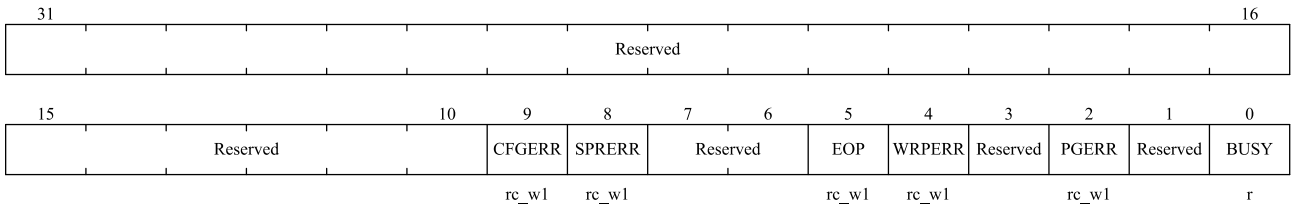


Bit Field	Name	Description
31:0	OPTKEY	Used to unlock the FLASH_CTRL.OPTWE bit.

2.2.3.5 Flash status register (FLASH_STS)

Address offset: 0x0C

Reset value: 0x0000 0000



Bit Field	Name	Description
31:10	Reserved	Reserved,the reset value must be maintained

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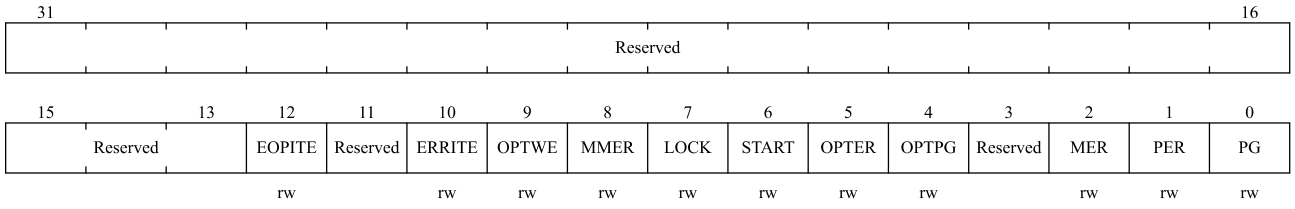
Bit Field	Name	Description
9	CFGERR	Flash iniaial configuration error. Whether the Flash iniaial configuration value read out in the config is consistent with calibration value. 0: Right 1: Error
8	SPRERR	Special Pattern read error Whether the Special Pattern value read out in the config is consistent with calibration value. 0: Right 1: Error
7:6	Reserved	Reserved,the reset value must be maintained
5	EOP	End of the operation When the Flash operation (programming/erasing) is complete, the hardware sets this to '1' and writing '1' clears this state. *Note: EOP status is set for each successful programming or erasure.*
4	WRPERR	Write protection error When attempting to program a write protected Flash address, hardware sets this to '1' and writing '1' clears this state.
3	Reserved	Reserved,the reset value must be maintained
2	PGERR	Programming error When trying to program to an address whose content is not '0xFFFF_FFFF', the hardware sets this to '1'. Writing '1' clears this state. *Note: before programming, the FLASH_CTRL.START bit must be cleared.*
1	Reserved	Reserved,the reset value must be maintained
0	BUSY	Busy This bit indicates that a Flash operation is in progress.This bit is set to '1' at the start of the Flash operation; This bit is cleared to '0' at the end of the operation or when an error occurs.

2.2.3.6 Flash control register (FLASH_CTRL)

Address offset: 0x10

Reset value: 0x0000 0080



Bit Field	Name	Description
31:13	Reserved	Reserved, the reset value must be maintained
12	EOPITE	Allow operation completion interrupt.

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Bit Field	Name	Description
		This bit allows an interrupt to be generated when the FLASH_STS.EOP bit becomes '1'. 0: Forbid interruption. 1: Interrupts are allowed.
11	Reserved	Reserved,the reset value must be maintained
10	ERRITE	Allow error status to be interrupted This bit allows interrupts in the event of Flash errors (when FLASH_STS.PGERR/FLASH_STS.WRPERR is set to '1'). 0: Forbid interruption. 1: Interrupts are allowed.
9	OPTWE	Allows option bytes to be written When the bit is '1', programmatic manipulation of the option byte is allowed. When the correct key sequence is written to the FLASH_OPTKEY register, the bit is set to '1'. Software can clear this bit.
8	MMER	Erase main memory block 0: None 1: Erase main memory block first 48 page
7	LOCK	Lock This bit can only be written as '1'. When the bit is '1', Flash and FLASH_CTRL are locked. Hardware clears this bit to '0' after detecting a correct unlock sequence. After an unsuccessful unlock operation, this bit cannot be changed until the next system reset.
6	START	Start An erase operation is triggered when the bit is '1'.This bit can only be set by software to '1' and cleared to '0' when FLASH_STS.BUSY changes to '1'.
5	OPTER	Erase option bytes 0: Disable option bytes erase mode. 1: Enable option bytes erase mode.
4	OPTPG	Program option bytes 0: Disable option bytes program mode. 1: Enable option bytes program mode.
3	Reserved	Reserved, the reset value must be maintained.
2	MER	Mass erase. Erase main memory block all pages. 0: Disable mass erase mode. 1: Enable mass erase mode.
1	PER	Page erase 0: Disable mass erase mode. 1: Enable mass erase mode.
0	PG	Program 0: Disable Program mode.

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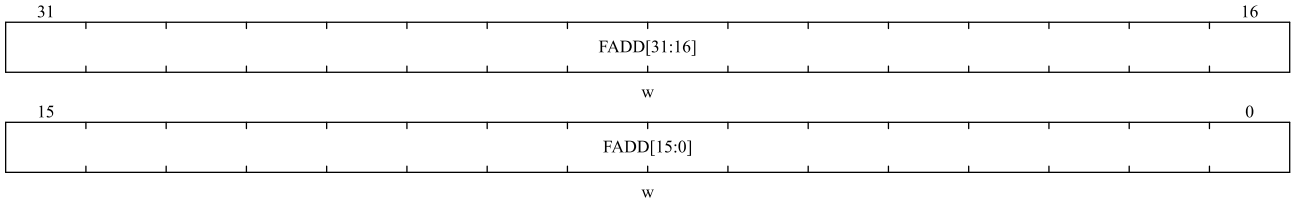
Bit Field	Name	Description
		1: Enable Program mode.

Note: please refer to Section 2.2.1.4 for programming and erasing.

2.2.3.7 Flash address register (FLASH_ADD)

Address offset: 0x14

Reset value: 0x0000 0000

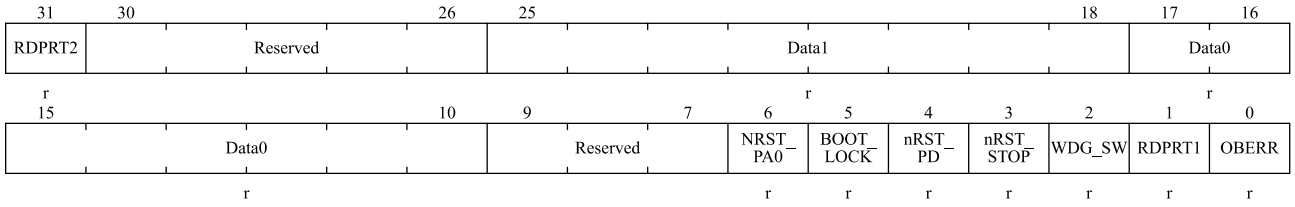


Bit Field	Name	Description
31:0	FADD	Flash memory address Select the address to program when programming and the page to erase when erasing. *Note: when the FLASH_STS.BUSY bit is '1', this register cannot be written.*

2.2.3.8 Flash option byte register (FLASH_OB)

Address offset: 0x1C

Reset value: 0x03FF FFDC



Bit Field	Name	Description
31	RDPRT2	Read protection level L2 0: Read protection L2 is disabled. 1: Read protection L2 is enabled. *Note: this bit is read-only.*
30:26	Reserved	Reserved, the reset value must be maintained
25:18	Data1[7:0]	Data1 *Note: these bits are read-only.*
17:10	Data0[7:0]	Data0 *Note: these bits are read-only.*
9:7	Reserved	Reserved, the reset value must be maintained
6	NRST_PA0	PA0 pin configuration. 0: Common I/O pin 1: NRST pin

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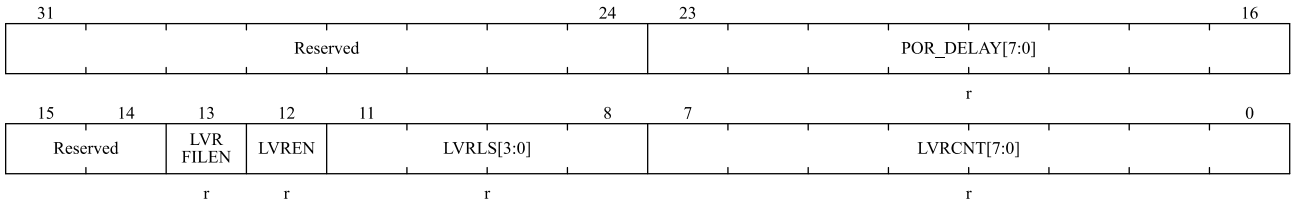
Bit Field	Name	Description
		Note: this bit is read-only.
5	BOOT_LOCK	Lock the first 3K of the main Flash. 0: Not locked 1: Lock *Note : this bit is read-only. the first 3kb Flash is not erasable when locked*
4	nRST_PD	The PD mode is used to reset the configuration 0: A reset occurs immediately after the system enters the PD mode. Even if the system enters the PD mode, the system will be reset instead of entering the PD mode. 1: The system does not reset after entering the PD mode. *Note: this bit is read-only.*
3	nRST_STOP	Enter the STOP mode to reset the configuration 0: A reset occurs immediately after entering the STOP mode. Even if the process of entering the STOP mode is executed, the system will be reset instead of entering the STOP mode. 1: No reset is generated after the STOP mode is entered. *Note: this bit is read-only.*
2	WDG_SW	Watchdog Settings 0: Hardware watchdog. 1: Software watchdog. *Note: this bit is read-only.*
1	RDPRT1	Read protection level L1 0: L1 level of read protection is disabled. 1: L1 read protection is enabled. *Note: this bit is read-only.*
0	OBERR	Option byte error When this bit is '1', the option byte does not match its complement code. *Note: this bit is read-only.*

2.2.3.9 USER register (FLASH_USER)

Address offset: 0x20

Reset value: 0xFFFF FFFF



Bit Field	Name	Description
31:24	Reserved	Reserved, the reset value must be maintained
23:16	POR_DELAY	Delay of CPU reset after POR is triggered. After initial system power-on, the Cortex®-M0's system dereset delay can be

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<table>
<tr><th>Bit Field</th><th>Name</th><th>Description</th></tr>
<tr><td></td><td></td><td>configured via this bit to control the reset delay time of the core.
0x00: Maximum delay
...
0xFF: No delay
Delay time = (1/f_{LSI}) × (0xFF - POR_DELAY).</td></tr>
<tr><td>15</td><td>Reserved</td><td>Reserved, the reset value must be maintained</td></tr>
<tr><td>14</td><td>LVRRSTEN</td><td>LVR reset enable
0: Enables LVR reset
1: Disables LVR reset</td></tr>
<tr><td>13</td><td>LVRFILEN</td><td>LVR filter enable
0: Enables LVR filter
1: Disables LVR filter</td></tr>
<tr><td>12</td><td>LVREN</td><td>LVR enable
0: Enables LVR
1: Disables LVR</td></tr>
<tr><td>11:8</td><td>LVRLS</td><td>LVR level select.
Value = 0x0F - LVRLS
<table>
<tr><th>Value</th><th>Voltage</th></tr>
<tr><td>0000</td><td>1.8v</td></tr>
<tr><td>0001</td><td>2.0v</td></tr>
<tr><td>0010</td><td>2.2v</td></tr>
<tr><td>0011</td><td>2.4v</td></tr>
<tr><td>0100</td><td>2.6v</td></tr>
<tr><td>0101</td><td>2.8v</td></tr>
<tr><td>0110</td><td>3.0v</td></tr>
<tr><td>0111</td><td>3.2v</td></tr>
<tr><td>1000</td><td>3.4v</td></tr>
<tr><td>1001</td><td>3.6v</td></tr>
<tr><td>1010</td><td>3.8v</td></tr>
<tr><td>1011</td><td>4.0v</td></tr>
<tr><td>1100</td><td>4.2v</td></tr>
<tr><td>1101</td><td>4.4v</td></tr>
<tr><td>1110</td><td>4.6v</td></tr>
<tr><td>1111</td><td>4.8v</td></tr>
</table></td></tr>
<tr><td>7:0</td><td>LVRCNT</td><td>LVR filter control count value
0x00: Maximum filtering width
...
0xFF: Not filtered
Filter width = (1/f_{LSI}) × (0xFF - LVRCNT).</td></tr>
</table>

2.2.3.10 VTOR register (FLASH_VTOR)

Address offset: 0x24

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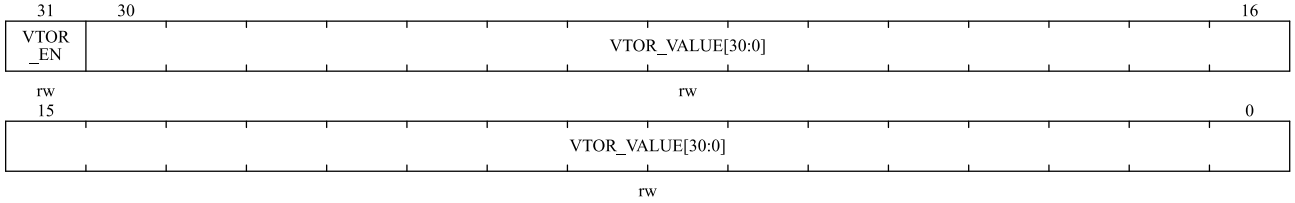
Reset value: 0x0000 0000



Bit Field	Name	Description
31	VTOR_EN	VTOR enable 0: Enables VTOR 1: Disables VTOR
30:0	VTOR_VALUE	Used for interrupt vector remapping to store the first address of the interrupt vector table These bits are valid when VTOR_EN = 1. If the first address of the interrupt vector table needs to be remapped to the 0x08000C00, the VTOR_VALUE is configured to 0x08000C00.

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3 Power Control (PWR)

3.1 General Description

The operating voltage (V_{DD}) of N32G003 is 2V~5.5V. It mainly has two power domains: analog/digital power domains. Please refer to Figure 3-1 Power Block Diagram. As the power control unit, PWR's main function is to control N32G003 to enter/exit different power modes. The N32G003 supports RUN, STOP and PD modes.

3.1.1 Power Supply

The functions of different power domains are described below, and the digital part of the power domain is described in the following sections of this document. Refer to Figure 3-1 for Power Block Diagram.

- V_{DD}: The voltage input range is 2V~5.5V. It mainly provides power for PMU, HSI, etc.
- V_{DDD}: The voltage regulator provides power for CPU, AHB, APB, SRAM, Flash and most digital peripherals.

The embedded voltage regulator is used to power the internal digital module. The voltage regulator has three modes: normal mode, low power mode and power down mode.

- Normal mode (MR)

  MR is mainly used in RUN mode. The output voltage is 1.5V (typical).

- Low-power mode (LPR)

  LPR is mainly used in STOP mode. In STOP mode, low-power mode output voltage (1.5V/1.2V) can be configured for lower current consumption. The default output is 1.5V, and the V_{DDD} PDR trigger voltage is 1.2V. When PWR_CTRL5.STPMRSEL[1:0] = '01', output voltage is 1.5V, and PWR_CTRL.PDRS[1:0] must be configured for '11' (V_{DDD} PDR trigger voltage 1.2V); when PWR_CTRL5.STPMRSEL[1:0] = '11', output voltage is 1.2V, and PWR_CTRL.PDRS[1:0] must be configured as '10' (V_{DDD} PDR trigger voltage 1.0V).

- Power-down mode (PD)

  PD is mainly used in PD mode. Voltage regulator is off.

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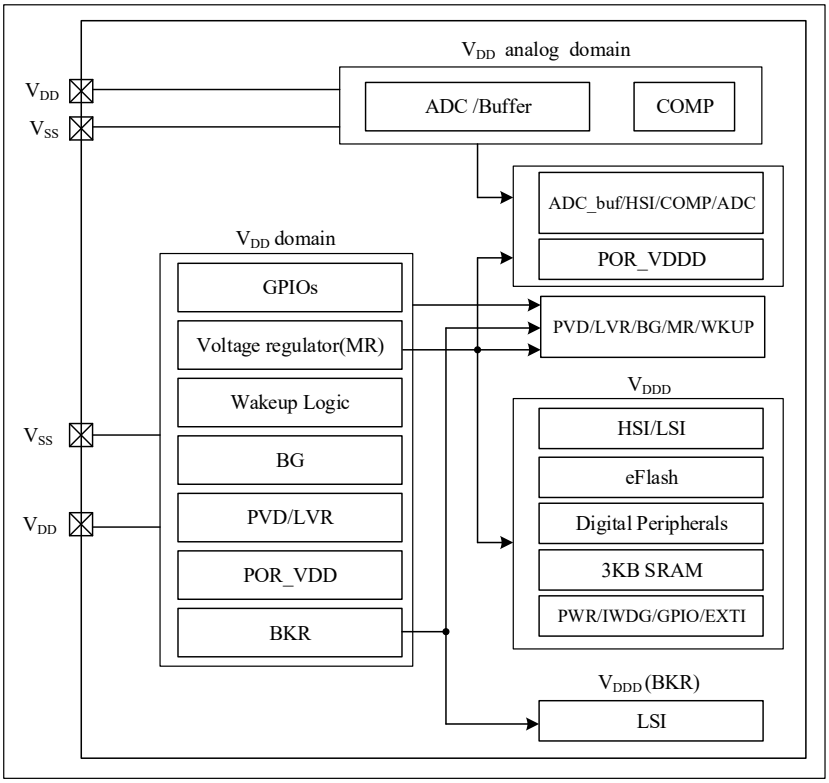
Figure 3-1 Power Supply Diagram



3.1.2 Power Supply Supervisor

3.1.2.1 Power on reset (POR) / power down reset (PDR)

N32G003 has an integrated power-on reset (POR) and power-down reset (PDR) circuits, which can work at a minimum voltage of 2V and requires no external reset circuit. When V_{DD} is lower than the specified threshold ($V_{POR/PDR}$), N32G003 will remain in reset state.

For more information about the reset threshold of the switching power supply, please refer to the electrical characteristics section of the relevant data sheet.

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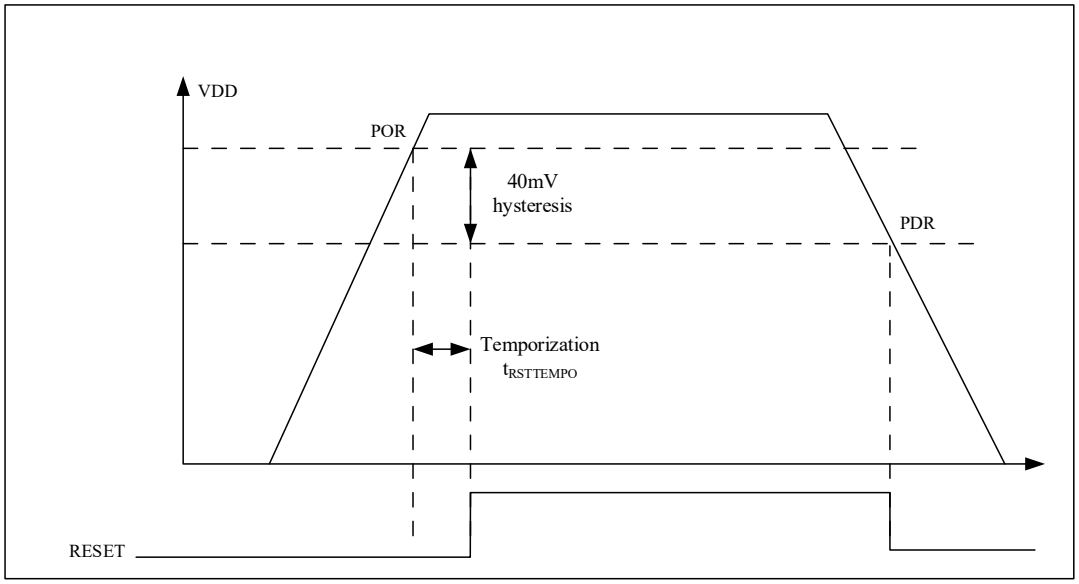
Figure 3-2 Power On Reset (POR) / Power Down Reset (PDR) Waveform

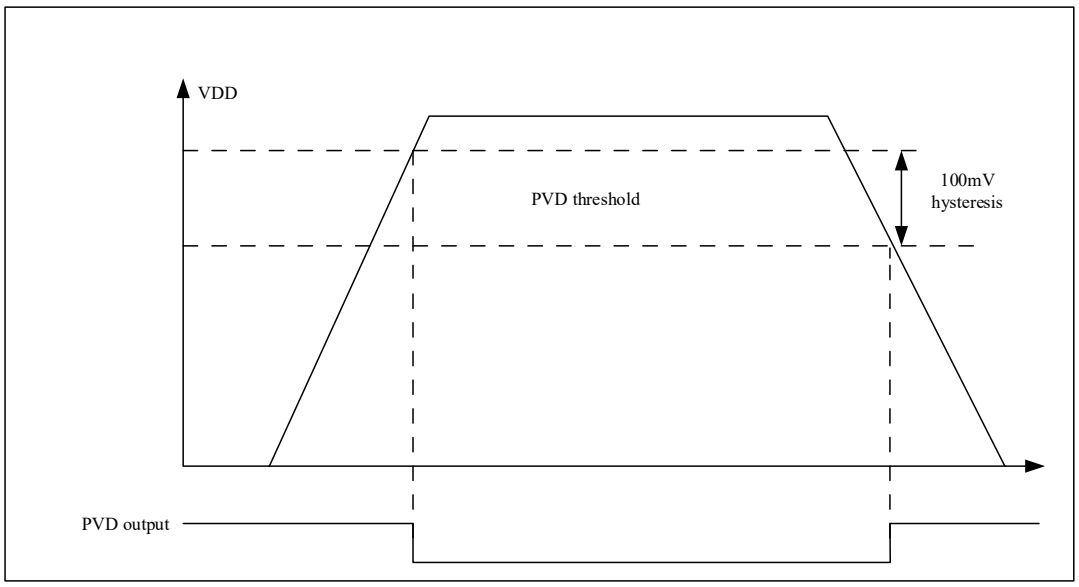


3.1.2.2 Programmable voltage detector (PVD)

The PVD is used to detect V_{DD} voltage level. The threshold of PVD is controlled by PWR_CTRL.PLS [3:0]. PVD can be enabled/disabled by PWR_CTRL.PVDEN bit.

The PWR_CTRLSTS.PVDO flag is used to indicate whether V_{DD} is higher or lower than PVD threshold. This event also is connected internally to EXTI line18. If the EXTI register is enabled, an interrupt can be generated. When V_{DD} drops below PVD threshold and/or when V_{DD} rises above PVD threshold, a PVD interrupt can be generated according to the rising/falling edge trigger configuration of EXTI line18. For example, this feature can be used to perform emergency shutdown tasks.

Figure 3-3 PVD Threshold Diagram



3.1.2.3 Low voltage reset (LVR)

LVR is used to detect V_{DD} voltage level. The threshold of LVR is controlled by PWR_CTRL2.LVRLS [3:0]. LVR can be

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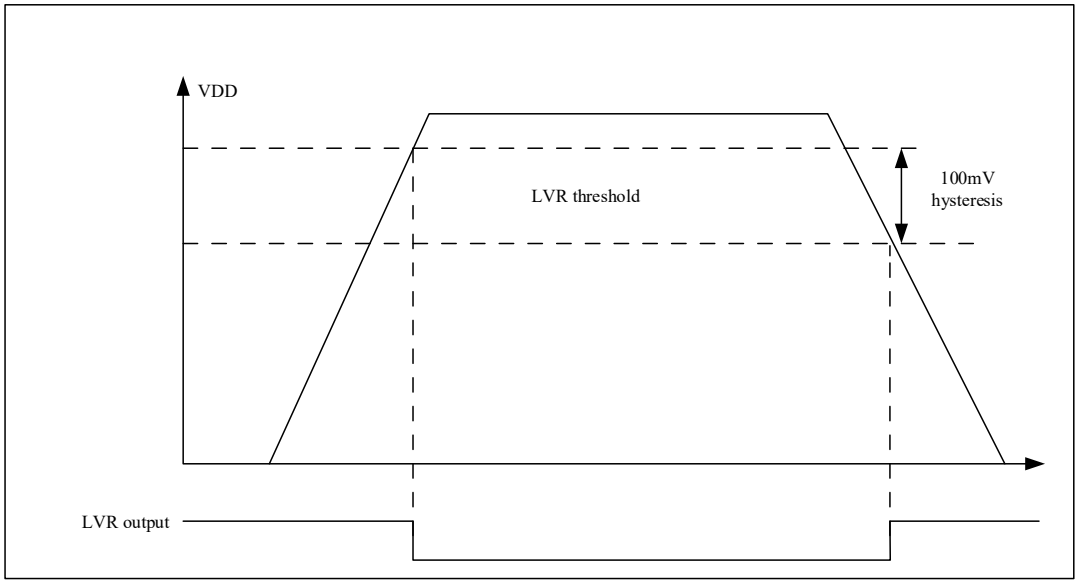
enabled/disabled by PWR_CTRL2.LVREN bit.

The PWR_CTRL2.LVRO flag is used to indicate whether V_{DD} is higher or lower than LVR threshold. This event will trigger a system reset.

Figure 3-4 LVR Threshold Diagram



3.2 Power Modes

N32G003 has 3 power modes: RUN, STOP, and PD mode. Different modes have different performance and power consumption. Please refer to the following table for N32G003 power modes:

Table 3-1 Power Modes

Mode	Condition	Enter	Exit
RUN	CPU running. Peripheral running depending on configuration.	Power-on, system reset, low power wake-up.	Entering STOP or PD modes.
STOP	CPU deep sleep mode. The peripheral clock is turned off, and the voltage regulator is still running in a low-power mode. HSI is turned off. LSI switch can be configured. All GPIO states are kept, and all SRAM and registers keep data. All IO, PVD can be used to wake up the CPU. Or other peripherals (TIM6) can be configured to wake up. After waking up, the HSI is turned on, and the code starts from where it was suspended.	WFI/WFE: 1）SCB_SCR.SLEEPDEEP = 1，No interrupt (for WFI) or event (for WFE) is pending. 2）PWR_CTRL.PDSTP = 0	Any interrupt wake-up event by EXTI, NRST, IWDG.

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Mode	Condition	Enter	Exit
	Flash enters deep sleep mode.		
PD	The main voltage regulator is turned off, and the HSI/LSI is turned off. NRST and PA1_WKUP0/ PA2_WKUP1 two wake-up IOs to the wake-up circuit in the V_{DD} domain are used for PD wake-up. Most of the IO ports are in a high-Z state.	WFI/WFE: 1）SCB_SCR.SLEEPDEEP = 1，No interrupt (for WFI) or event (for WFE) is pending. 2）PWR_CTRL.PDSTP = 1	WKUP0/1 rising or falling edge can be configured, NRST reset.

Note:

(1) After waking up from STOP mode, the code can continue to run from the stop position.

The operating enabled status of different modules in different power consumption modes are shown in the following table:

Table 3-2 Peripheral Running Status

Peripheral	RUN mode	STOP mode		PD mode	
		Status	Wakeup capability	Status	Wakeup capability
Cortex®-M0	Y	-	-	-	-
MR	Y	-	-	-	-
LPR	Y	Y	-	-	-
POR_VDD	Y	Y	Y	-	-
PDR_VDD	Y	Y	Y	-	-
POR_VDDD	Y	Y	-	-	-
PDR_VDDD	Y	O	O	-	-
PVD	O	O	O	-	-
LVR	O	O	O	-	-
Flash	Y	DSTB	-	-	-
SRAM3KB	Y	Y	-	-	-
HSI	Y	-	-	-	-
LSI	Y	O	-	-	-
UART1/2	O	-	-	-	-
I2C	O	-	-	-	-
SPI	O	-	-	-	-
ADC	O	-	-	-	-
TIM1/3	O	-	-	-	-
TIM6	O	O	O	-	-
IWDG	O	O	O	-	-
COMP	O	-	-	-	-
SysTick timer	O	-	-	-	-
CRC	O	-	-	-	-
GPIOs	O	O	O	-	2 pins

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Notes:

(1) Y: Yes (Enable)，O: Optional（Disabled by default and enabled by software configuration），-: Not available，DSTB: deep-standby.

(2) The pins that can wake up from PD are PA1 (WKUP0), PA2 (WKUP1), NRST.

3.2.1 STOP Mode

STOP mode is based on Cortex®-M0 deep sleep mode, combined with peripheral clock gating. Voltage regulator operates in low power mode. The output voltage (1.5V/1.2V) is configurable. In STOP mode, HSI is disabled. But the contents of SRAM and all registers are retained. Flash automatically enter deep sleep mode. In STOP mode, all I/O pins retain the same state as in RUN mode.

3.2.1.1 Entering STOP mode

To enter STOP mode, the register bits should be configured: SCB_SCR.SLEEPDEEP = 1 and PWR_CTRL.PDSTP = 0.

If a Flash operation is in progress, the time to enter STOP mode will be delayed until the memory access is completed.

If the access to the APB bus is in progress, the time to enter the STOP mode will be delayed until the APB access is completed.

In STOP mode, the following peripherals are available:

- Independent Watchdog (IWDG): The independent watchdog will be activated when its related register is written by software or by hardware operation. Once enabled, it will keep counting until a reset is generated.
- IO and TIM6/PVD peripherals can be used for waking up purposes.
- Internal RC oscillator (LSI RC): It can be turned on by the PWR_CTRL3.LSIEN bit.

ADC should be disabled when entering STOP mode to avoid unnecessary power consumption.

3.2.1.2 Exiting STOP mode

When the STOP mode is exited by an interrupt or wake-up event, the HSI RC oscillator is selected as the system clock, and code execution will continue from where it suspended. Since the voltage regulator is in low power mode, it takes extra start-up time to wake up from STOP mode. In addition, shorten the Flash wake up time by setting PWR_CTRL4.FLHWKUP = 1 before entering STOP mode.

3.2.2 PD Mode

PD (Power Down) mode is based on Cortex®-M0 deep sleep mode, enabling lower power consumption. In this mode, the CPU, all peripherals, voltage regulator, HSI/LSI clock sources and all digital power supplies (V_{DDD}) are turned off. All GPIO pins are in a high-impedance state, where NRST/PA1_WKUP0/PA2_WKUP1 can be used to wake up from PD mode.

3.2.2.1 Enter PD mode

To enter the PD mode, user needs to set SCB_SCR.SLEEPDEEP = 1 and PWR_CTRL.PDSTP = 1.

If a Flash operation is in progress, entering PD mode will be delayed until memory access is complete.

If the access to the APB bus is in progress, entering PD mode will be delayed until the APB access is complete.

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3.2.2.2 Exit PD mode

When external reset (NRST pin), WKUP pin rising/falling edge events occur, MCU will exit PD mode. All registers are reset when wake up from PD mode.

After waking up from PD mode, code execution is equivalent to execution after reset (read reset vector, etc.).

3.3 Debug mode

By default, if application puts the MCU in STOP or PD mode while using the debugging feature, the debugging connection will be lost. Because the Cortex®-M0 core loses its clock.

However, by setting some configuration bits in the DBG_CTRL register, the software can be debugged even in the STOP and PD mode. If these register bits are configured, the voltage regulator and HSI will not be disabled or turned off.

3.3.1 Low Power Mode Debug Mode Support

When debugging in low power mode, you need to ensure that the FCLK of the core is enabled to provide the necessary clock for core debugging. The software needs to configure the DBG_CTRL.STOP or DBG_CTRL.PD bit in the debug control register, start the internal RC oscillator and provide the clock for FCLK. For specific features and functions, refer to the description of DBG_CTRL.PD and DBG_CTRL.STOP bit fields in the DBG_CTRL register in Section 3.4.9.

3.3.2 Peripheral Debug Support

In addition to supporting debug in low power mode, it also supports some peripherals to stop working in debug state (TIM1, TIM3, TIM6, IWDG). When the corresponding bit of the peripheral control bit in the DBGCTRL register is set, the corresponding peripheral enters the debugging state after the core stops. For specific operations and features, please refer to the description of the other bit fields of the DBG_CTRL register in Section 3.4.9.

3.4 PWR Registers

3.4.1 PWR Register Overview

Table 3-3 PWR Register Overview

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x00	PWR_CTRL	Reserved					PVDITEN	PVDFILEN	PVDCNT[7:0]								Reserved					NRSTPOL	PDRS[1:0]		PLS[3:0]				PVDEN	CLRDBGPDF	CLRWKUPF	PDSTP	IWDGRSTEN
	Reset value						0	0	0	0	0	0	0	0	0	0						0	1	1	0	0	0	0	0	0	0	0	0	1
0x04	PWR_CTRLSTS	Reserved																					WKUPPOL	WKUP1EN	WKUP0EN	Reserved					PVDO	DBGPDF	WKUPF
	Reset value																						1	0	0						0	0	0
0x08	PWR_CTRL2	LVRKEY[7:0]								Reserved								LVRO	LVRLS[3:0]				LVREN	LVRRSTEN	LVRFILEN	LVRCNT[7:0]								
	Reset value	0	0	0	0	0	0	0	0									0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0

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Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x14	PWR_CTRL3	Reserved																			LSISTPCNT[2:]			PDRSEL	Reserved	LSIEN	HSISEL	HSIPWR	Reserved				
	Reset value																				0	1	1	1		1	0	1					
0x20	PWR_CTRL4	Reserved																													RUNF	STBFLH	FLHWKUP
	Reset value																														0	0	0
0x24	PWR_CTRL5	Reserved																												STPMRSEL[1:0]		Reserved	
	Reset value																													0	1		
0x28	PWR_CTRL6	Reserved																												STPMRE N[1:0]		Reserved	
	Reset value																													0	0		
0x30	DBG_CTRL	Reserved																							TIM6STP	TIM3STP	TIM1STP	IWDGSTP	Reserved		PD	STOP	Reserved
	Reset value																								0	0	0	0			0	0	

3.4.2 Power Control Register (PWR_CTRL)

Address offset: 0x00

Reset value: 0x0000 0601

31	27	26	25	24	17	16
Reserved		PVD ITEN	PVD FILEN	PVDCNT[7:0]		Reserved
		rw	rw			

15	12	11	10	9	8	5	4	3	2	1	0
Reserved		NRST POL	PDRS[1:0]		PLS[3:0]		PVDEN	CLR DBGPDF	CLR WKUPF	PDSTP	IWDG RSTEN
		rw	rw		rw		rw	rc_w1	rc_w1	rw	rw

Bit Field	Name	Description
31:27	Reserved	Reserved, the reset value must be maintained.
26	PVDITEN	PVD interrupt enable. 0: PVD interrupt disabled. 1: PVD interrupt enabled.
25	PVDFILEN	PVD filter enable. 0: PVD filter disabled. 1: PVD filter enabled.
24:17	PVDCNT	PVD filter control counter value. 0x00: Not filtered ... 0xFF: Maximum filtering width Filter width = $(1/f_{LSI}) \times$ PVDCNT.
16:12	Reserved	Reserved, the reset value must be maintained.

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Bit Field	Name	Description
11	NRSTPOL	NRST polarity select. 0: The falling edge of NRST pin. 1: The rising edge of NRST pin.
10:9	PDRS[1:0]	Adjust the V_{DDD} PDR trigger level in STOP mode. 00: Reserved. 01: Reserved. 10: V_{DDD} PDR trigger level is 1.0V. 11: V_{DDD} PDR trigger level is 1.2V. Only V_{DDD} POR/PDR can reset this bit, if $V_{PDRS} < V_{STOP}$ values, the PDR will be triggered.
8:5	PLS[3:0]	PVD level selection. PVD threshold is controlled below: PWR_CTRL.PLS / Voltage 0000 / 1.8v 0001 / 2.0v 0010 / 2.2v 0011 / 2.4v 0100 / 2.6v 0101 / 2.8v 0110 / 3.0v 0111 / 3.2v 1000 / 3.4v 1001 / 3.6v 1010 / 3.8v 1011 / 4.0v 1100 / 4.2v 1101 / 4.4v 1110 / 4.6v 1111 / 4.8v
4	PVDEN	The Power voltage detector (PVD) enable. 0: PVD disabled. 1: PVD enabled.
3	CLRDBGPDF	The software writes a '1' to this bit to clear the DBGPDF status bit. Always read as 0. 0: Invalid. 1: Clear the DBGPDF status bit.
2	CLRWKUPF	Clear the wake-up bit. Always read as 0. 0: Invalid. 1: Clear WKUPF (write) after 2 system clock cycles.

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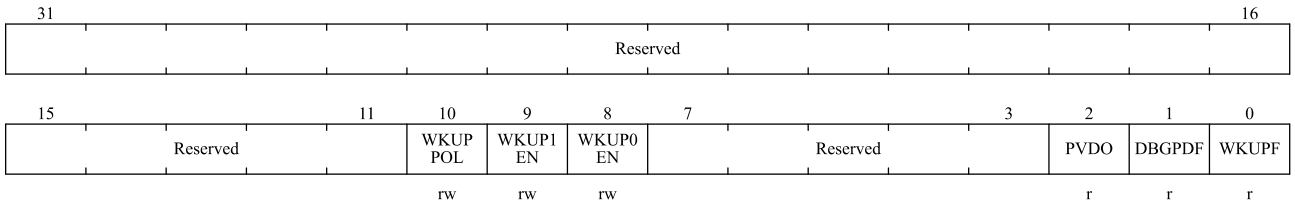
Bit Field	Name	Description
1	PDSTP	Enter STOP/PD mode selection. 0: CPU output DEEPSLEEP is '1', and the chip enters STOP mode. 1: CPU output DEEPSLEEP is '1', and the chip enters PD mode.
0	IWDGRSTEN	IWDG reset enable control. 0: IWDG reset request will not generate a system reset. 1: IWDG reset request will generate a system reset.

3.4.3 Power Control Status Register (PWR_CTRLSTS)

Address offset: 0x04

Reset value: 0x0000 0400



Bit Field	Name	Description
31:11	Reserved	Reserved, the reset value must be maintained.
10	WKUPPOL	Wakeup polarity for PA1/PA2. To wakeup PD mode by using rising edge or falling edge. Make sure disable wakeup enable before changing polarity value. 0: Falling edge. 1: Rising edge.
9	WKUP1EN	WKUP pin PA2 enable control. 0: WKUP pin is used for general purpose I/O. An event on the WKUP pin does not wakeup the device from PD mode. 1: WKUP pin is used for wakeup from PD mode. *Note: this bit is reset by V_{DDD} POR Reset only.*
8	WKUP0EN	WKUP pin PA1 enable control. 0: WKUP pin is used for general purpose I/O. An event on the WKUP pin does not wakeup the device from PD mode. 1: WKUP pin is used for wakeup from PD mode. *Note: this bit is reset by VDDD POR Reset only.*
7:3	Reserved	Reserved, the reset value must be maintained.
2	PVDO	PVD output. It is valid only if PWR_CTRL.PVDEN = 1. 0: V_{DD} is higher than the PVD threshold selected with PWR_CTRL.PLS [3:0]. 1: V_{DD} is lower than the PVD threshold selected with PWR_CTRL.PLS [3:0].
1	DBGPDF	DBGPD mode status bit. When entering DBGPD mode, hardware sets this bit to '1'. Hardware clears this bit when software sets PWR_CTRL.CLRDBGPDF = 1. Only V_{DDD} POR/PDR can reset this bit.

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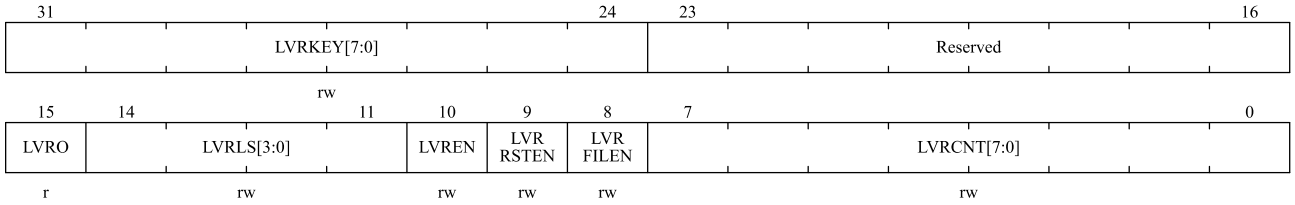
Bit Field	Name	Description
		0: Chip never entered DBGPD mode. 1: Chip has entered DBGPD mode.
0	WKUPF	DBGPD mode wake-up status bit. This bit is set by hardware after WKUP pin wakes up DBGPD mode. Hardware clears this bit when software sets PWR_CTRL.CLRWKUPF = 1. Only V_{DDD} POR/PDR can reset this bit. 0: No wakeup event occurred. 1: A wakeup event was received from the WKUP pin.

3.4.4 Power Control Register 2 (PWR_CTRL2)

Address offset: 0x08

Reset value: 0x0000 0400

This register is write-protected. Each time the software writes to this register, it must first write the key 0xA5000000 (unlocked) to this register.



Bit Field	Name	Description
31:24	LVRKEY	LVR key.
23:16	Reserved	Reserved, the reset value must be maintained.
15	LVRO	LVR output. It is valid only if PWR_CTRL2.LVREN = 1. 0: V_{DD} is higher than the LVR threshold selected by PWR_CTRL2.LVRLS [3:0]. 1: V_{DD} is lower than the LVR threshold selected by PWR_CTRL2.LVRLS [3:0].
14:11	LVRLS[3:0]	LVR level selection. LVR threshold is controlled below:

PWR_CTRL2.LVRLS	Voltage
0000	1.8v
0001	2.0v
0010	2.2v
0011	2.4v
0100	2.6v
0101	2.8v
0110	3.0v
0111	3.2v
1000	3.4v
1001	3.6v

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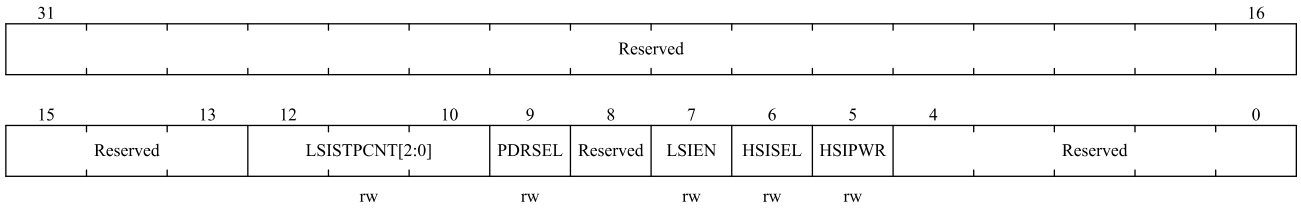
Bit Field	Name	Description
		1010 3.8v 1011 4.0v 1100 4.2v 1101 4.4v 1110 4.6v 1111 4.8v
10	LVREN	LVR enable. 0: LVR disabled. 1: LVR enabled.
9	LVRRSTEN	LVR reset Enable. 0: LVR reset disabled. 1: LVR reset enabled.
8	LVRFILEN	LVR filter Enable. 0: LVR filter disabled. 1: LVR filter enabled.
7:0	LVRCNT	LVR filter control count value. 0x00: Not filtered ... 0xFF: Maximum filtering width Filter width = $(1/f_{LSI}) \times$ LVRCNT.

3.4.5 Power Control Register 3 (PWR_CTRL3)

Address offset: 0x14

Reset value: 0x0000 0EAF



Bit Field	Name	Description
31:13	Reserved	Reserved, the reset value must be maintained.
12:10	LSISTPCNT	After exit STOP mode, user can delay starting the LSI to stabilize the LSI. The delay is determined by the LSISTPCNT configuration. *Note: these bits are used with PWR_CTRL3.LSIEN.*
9	PDRSEL	0: V_{DDD} PDR selection signal is pulled high by default. In this case, PWR_CTRL.PDRS [1:0] == '11'. 1: V_{DDD} PDR selection is controlled by PWR.
8	Reserved	Reserved, the reset value must be maintained.
7	LSIEN	Control PWR to enable LSI. 0: PWR (always included in STOP mode) request to enable LSI.

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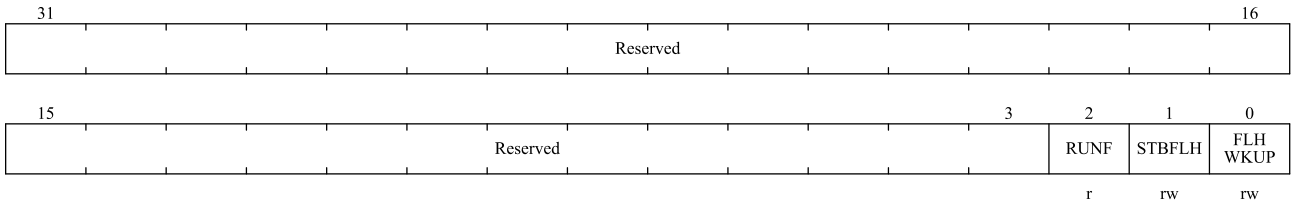
Bit Field	Name	Description
		1: After entering STOP mode, PWR no longer requests to enable LSI.
6	HSISEL	HSI frequency trim select. 0: HSI 48M trim. 1: HSI 40M trim.
5	HSIPWR	HSI controller select 0: HSI is not controlled by PWR. 1: HSI is controlled by PWR. *Note: after this bit is enabled, you can configure PWR_CTRL3.HSISEL*
4:0	Reserved	Reserved, the reset value must be maintained.

3.4.6 Power Control Register 4 (PWR_CTRL4)

Address offset: 0x20

Reset value: 0x0000 0000

This register is write-protected. Each time the software writes to this register, it must first write the key 0x0175_3603 (unlocked) to this register.



Bit Field	Name	Description
31:3	Reserved	Reserved, the reset value must be maintained.
2	RUNF	RUN mode flag. 0: System not in RUN mode. 1: System in RUN mode.
1	STBFLH	Flash deep standby mode enable (configurable in RUN mode) This bit is set and reset by software, or reset by hardware in STOP and PD modes. 0: After the software clears this bit, Flash exit the deep standby mode and return to the normal operating mode. 1: After the software set this bit to '1', the Flash enter deep standby mode.
0	FLHWKUP	Enable Flash fast wake-up. 0: When the chip exits from STOP mode, use Flash to wake up normally. 1: When the chip exits from STOP mode, use Flash to wake up quickly. *Note: please refer to the data sheet for the wake-up time.*

3.4.7 Power Control Register 5 (PWR_CTRL5)

Address offset: 0x24

Reset value: 0x0000 0004

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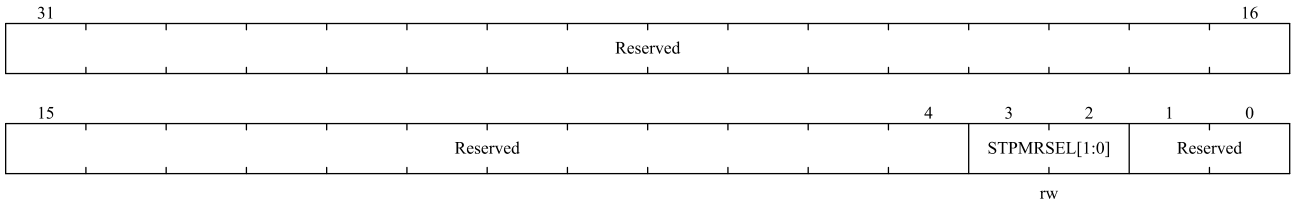
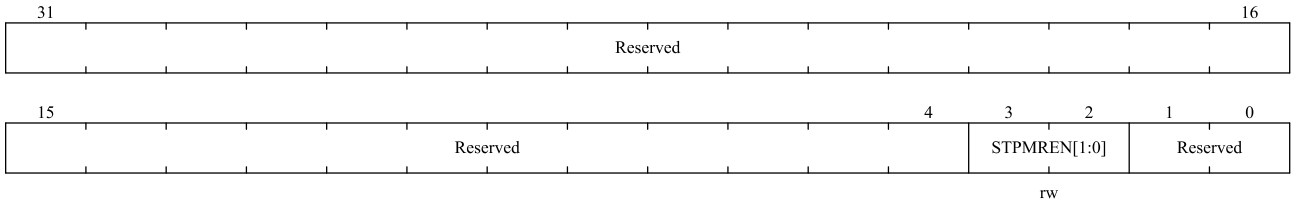


Bit Field	Name	Description
31:4	Reserved	Reserved, the reset value must be maintained.
3:2	STPMRSEL[1:0]	After the chip enters STOP mode, V_{DDD} output voltage is selected. Before configuring this register bit, the software must first configure PWR_CTRL6.STPMREN = '11'. 00: No used. 01: V_{DDD} output voltage 1.5V. 10: Reserved. 11: V_{DDD} output voltage 1.2V. This bit is reset by V_{DDD} POR only.
1:0	Reserved	Reserved, the reset value must be maintained.

3.4.8 Power Control Register 6 (PWR_CTRL6)

Address offset: 0x28

Reset value: 0x0000 0000



Bit Field	Name	Description
31:4	Reserved	Reserved, the reset value must be maintained.
3:2	STPMREN[1:0]	V_{DDD} Output voltage selection enable. 00: Enter STOP mode, V_{DDD} Output voltage 1.5V. 01/10: Reserved. 11: Enter STOP mode, V_{DDD} Output voltage control by PWR_CTRL5.STPMRSEL. This bit is reset by V_{DDD} POR only.
1:0	Reserved	Reserved, the reset value must be maintained.

3.4.9 Debug Control Register (DBG_CTRL)

Address offset: 0x30

Reset value: 0x0000 0000

Only V_{DDD} POR/PDR can reset this register. Only after the Debugger is connected, the software can write access to this register.

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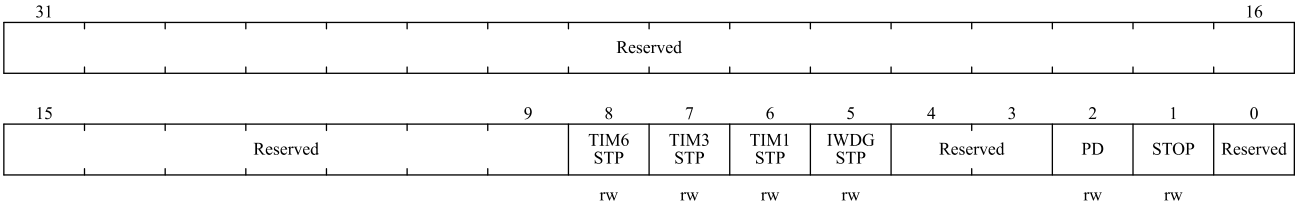

Bit Field	Name	Description
31:9	Reserved	Reserved, the reset value must be maintained.
8	TIM6STP	The counter of TIM6 stops working when the core enters the debug state. Set or cleared by software. 0: The counter of TIM6 still works normally. 1: The counter of TIM6 stops working.
7	TIM3STP	The counter of TIM3 stops working when the core enters the debug state. Set or cleared by software. 0: The counter of TIM3 still works normally. 1: The counter of TIM3 stops working.
6	TIM1STP	The counter of TIM1 stops working when the core enters the debug state. Set or cleared by software. 0: The counter of TIM1 still works normally. 1: The counter of TIM1 stops working.
5	IWDGSTP	The counter of IWDG stops working when the core enters the debug state. Set or cleared by software. 0: The counter of IWDG still works normally. 1: The counter of IWDG stops working.
4:3	Reserved	Reserved, the reset value must be maintained.
2	PD	Debug PD mode control. Set or cleared by software. 0: (FCLK off, HCLK off) system enters PD mode, digital circuit part is unpowered. From a software point of view, exiting PD mode is the same as a power-on reset. 1: (FCLK on, HCLK on) system enters DBGPD mode, digital circuit part is powered, and FCLK clock is provided by the internal RC oscillator. In addition, the microcontroller exits DBGPD mode by generating a system reset, which is the same as a system reset.
1	STOP	Debug STOP mode control. Set or cleared by software. 0: (FCLK off, HCLK off) system enters STOP mode, clock controller disables all clocks (including HCLK and FCLK). When exiting STOP mode, the configuration of the clock is the same as after reset (Microcontroller is clocked by the 48MHz internal RC oscillator (HSI)). 1: (FCLK on, HCLK on) system enters DBGSTOP mode, FCLK clock is provided by the internal RC oscillator.
0	Reserved	Reserved, the reset value must be maintained.

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4 Reset and Clock Control (RCC)

4.1 Reset Control Unit

N32G003 supports the following two types of reset:

- Power Reset
- System Reset

4.1.1 Power Reset

A power reset occurs in the following circumstances:

- Power-on/ Power-down reset (POR/PDR reset).
- When exiting PD mode.

A power reset sets all registers to their reset values.

4.1.2 System Reset

A system reset is generated when one of the following events occurs:

- A low level on the NRST pin (external reset)
- Independent watchdog event (IWDG reset)
- Software reset (SW reset)
- Low power management reset
- EMC reset
- LVR reset

Except for the following registers, a system reset will reset all registers to their reset states:

- RCC_CTRLSTS
- RCC_EMCCTRL
- PWR_CTRL.PDRS[1:0], PWR_CTRL.NRSTPOL
- PWR_CTRLSTS.WKUPF, PWR_CTRLSTS.WKUP0EN, PWR_CTRLSTS.WKUP1EN, PWR_CTRLSTS.WKUPPOL
- PWR_CTRL3.HSISEL
- DBG_CTRL

The reset source can be identified by checking the reset flags in the Control/Status Register (RCC_CTRLSTS).

4.1.2.1 Software reset

A software reset can be generated by setting the SYSRESETREQ bit in Cortex®-M0 Application Interrupt and Reset Control Register. Refer to Cortex®-M0 technical reference manual for further information.

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4.1.2.2 Low-power management reset

Low-power management reset can be generated by using the following methods:

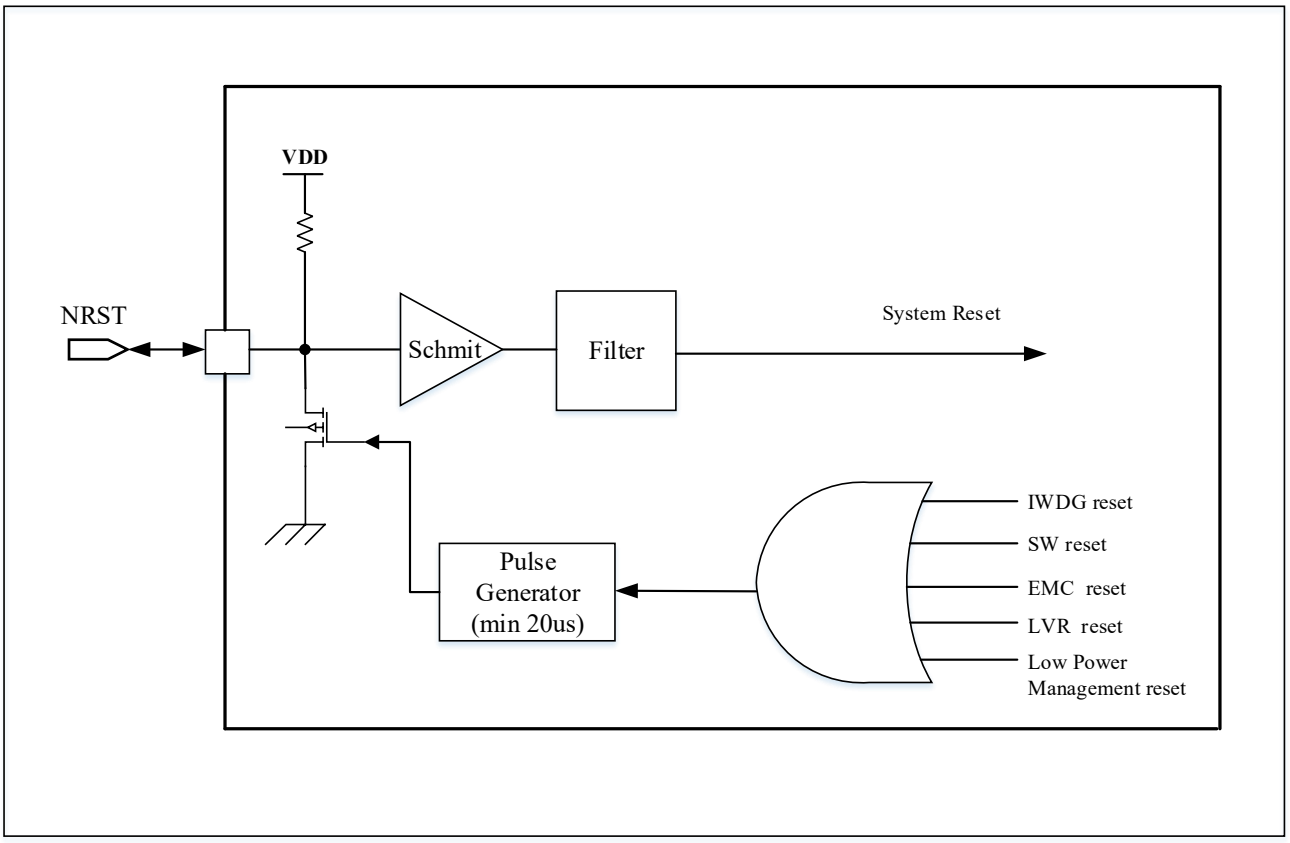
- Low-power management reset is generated when entering PD mode: This reset is enabled by resetting the nRST_PD bit in user option bytes. In this case, whenever a PD mode entry sequence is successfully executed, the system is reset instead of entering PD mode.
- Low-power management reset generated when entering STOP modes: This reset is enabled by resetting the nRST_STOP bit in user option bytes. In this case, whenever a STOP mode entry sequence is successfully executed, the system is reset instead of entering STOP modes.

The reset source will act on the NRST pin and remain low during reset. The reset entry vector is fixed at address 0x0000_0004. For more details, refer to Table 6-1 Vector Table.

The system reset signal provided to the chip is output on the NRST pin. The pulse generator guarantees a minimum reset pulse duration of 20μs for each reset source (external or internal). For external reset, the reset pulse is generated while the NRST pin is asserted low.

The figure below shows the system reset generation circuit.

Figure 4-1 System Reset Generation



4.2 Clock Control Unit

The HSI oscillator clock source is used to drive the system clock (SYSCLK).

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The 32KHz low-speed internal RC is used as a secondary clock source, which can be programmed to drive an independent watchdog (IWDG), TIM6 (for wake-up from STOP mode).

The frequency of the AHB, APB domains can be configured by the user through multiple prescalers. The maximum allowable frequency of the AHB and APB domain is 48MHz.

All peripheral clocks are derived from the system clock (SYSCLK) except in the following cases:

- ADC working clock source and ADC1M clock source are HSI
- By configuring RCC_CFG2.TIM1CLKSEL, you can select one of the following two options as the TIM1 working clock source:
  - APB clock (PCLK)
  - LSI clock
- By configuring RCC_CFG2.TIM6CLKSEL, you can select one of the following two options as the TIM1 working clock source:
  - APB clock (PCLK)
  - SYSCLK

When the clock source of timer is PCLK, timer clock frequency is automatically set by hardware in the following 2 cases:

- If the corresponding APB prescaler is 1, the timer clock frequency is the same as the APB frequency.
- If the corresponding APB prescaler is not 1, the timer clock frequency is twice the APB frequency.

- IWDG clock source is LSI oscillator.
- Flash memory programming interface clock is always the HSI clock
- By configuring the SysTick control and status registers, you can select one of the following two options as the SysTick clock source:
  - AHB clock (HCLK) divided by 8
  - AHB clock (HCLK)

FCLK is the free-running clock of the Cortex®-M0. Refer to ARM's Cortex®-M0 Technical Reference Manual for details.

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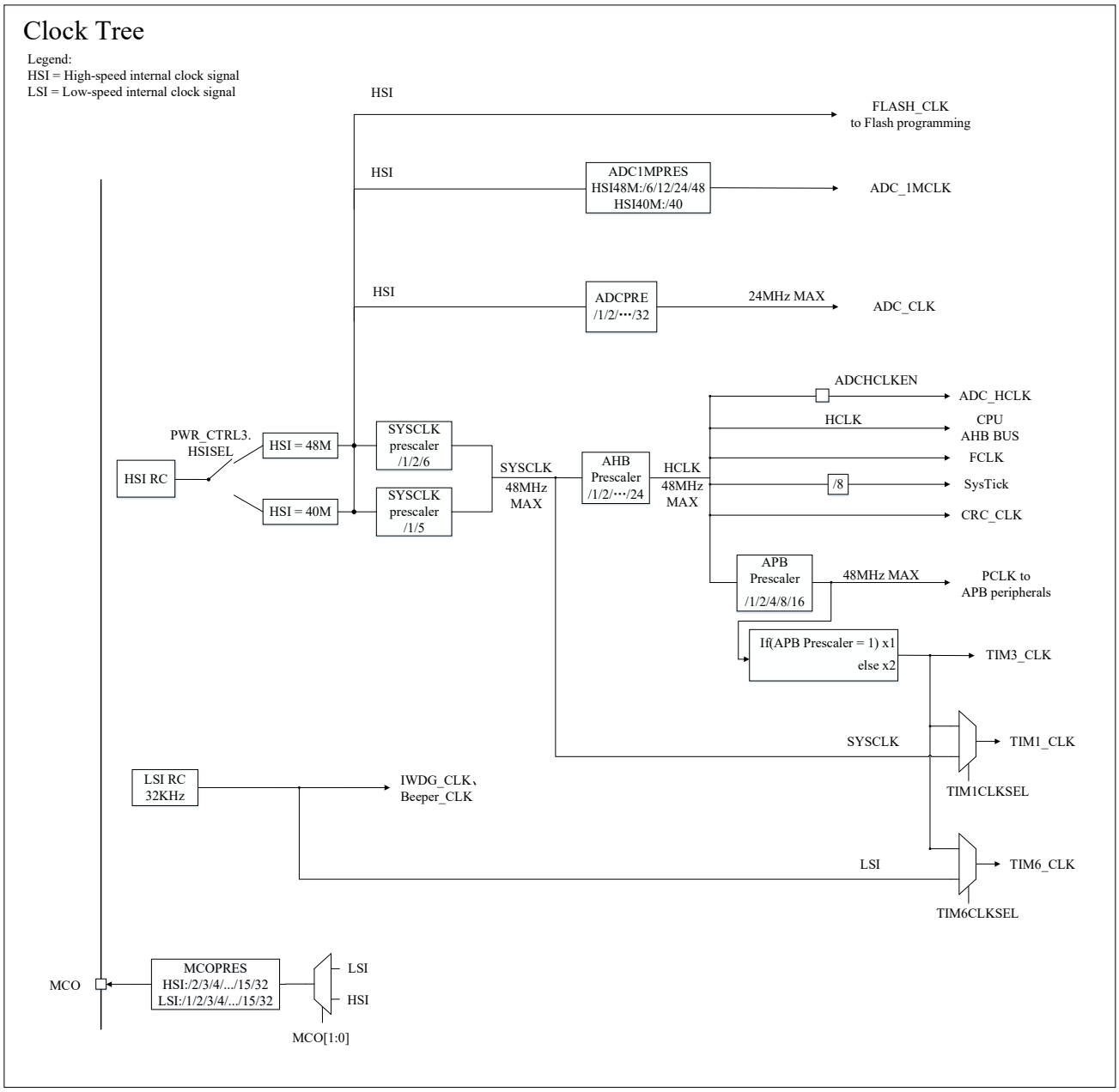
4.2.1 Clock Tree Diagram

Figure 4-2 Clock Tree



1. The maximum frequency available for the system clock is 48MHz.

2. For more details about the internal and external clock source characteristics, please refer to the "Electrical Characteristics" section in the product datasheet.

4.2.2 HSI Clock

By configuring PWR_CTRL5.HSISEL, HSI (High Speed Internal) clock signal is generated by an internal 48MHz or 40MHz RC oscillator, which can be used directly as a system clock or input after division. The HSI RC oscillator provides a clock source without any external devices.

RC oscillator frequencies can vary from one chip to another due to manufacturing process variations. Therefore, the HSI

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clock frequency of the chip has been calibrated to 1% (25°C) before leaving the factory.

If the user application is subject to voltage or temperature variations, this may affect the accuracy of the RC oscillator. The HSI frequency can be trimmed by using the RCC_HSICTRL.HSITRIM[3:0] bits.

The RCC_CTRL.HSI48MRDF or RCC_CTRL.HSI40MRDF bit flag indicates if the HSI RC oscillator is stable. At startup, the HSI RC output clock is not released until this bit is set by hardware.

4.2.3 LSI Clock

The LSI RC can clock the IWDG and PWR in STOP mode. The LSI clock frequency is about 32kHz. Please refer to the Electrical Characteristics section of the data sheet for further information.

The RCC_LSICTRL.LSIRDF bit flag indicates if the LSI clock is stable. At startup, the clock is not released until this bit is set by hardware.

4.2.3.1 LSI Calibration

The low-speed internal oscillator LSI frequency errors can be calibrated to obtain higher accuracy LPTIM, beeper, and IWDG time bases (when these peripherals are clocked from the LSI).

The LSI calibration steps are as follows:

1. Enable RCC_LSICTRL.LSIDETEN, which initiates LSI clock calibration;
2. Check RCC_LSICTRL.LSIDETFF flag bit. A value of 1 indicates the end of calibration, then read RCC_LSICTRL.LSIFREQ[15:0];
3. Take the average of the RCC_LSICTRL as many times as needed, then clear RCC_LSICTRL.LSIDETFF flag, and disable RCC_LSICTRL.LSIDETEN;
4. Calculate actual LSI frequency according to the formula: LSICLK(kHz) = 8*HSICLK/LSIFREQ[15:0] (Frequency of HSICLK is 48000kHz or 40000kHz);
5. Adjust the RCC_LSICTRL.LSITRIM[4:0] (default 16, adjustable step size 1kHz) according to the deviation of the actual LSI frequency from 32kHz

4.2.4 System Clock (SYSCLK) Selection

After the system reset, the HSI oscillator is selected as the system clock.

By configuring the HSI divider factor RCC_CFG.SYSPRES[1:0], when the HSI is 48M, the system clock can be configured to 8M, 24M, or 48M; When the HSI is 40M, the system clock can be configured to 8M or 40M.

4.2.5 Watchdog Clock

If the independent watchdog is started by hardware option or software, the LSI oscillator will be forced on and cannot be turned off. The clock is supplied to the IWDG after the LSI oscillator is stable.TIM6 Clock

In normal mode, the TIM6 clock supports 2 clock sources: PCLK and LSI. Since PCLK will be turned off in low power mode, software should switch the TIM6 clock to LSI before entering low power mode.

When LSI and PCLK are switched between each other, software must ensure that both clocks are turned on to switch without glitches.

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4.2.6 Clock Output(MCO)

The microcontroller clock output (MCO) capability allows the clock signal to be output onto the external MCO pin.

MCO pin is PA13, the corresponding GPIO port register must be configured for the corresponding function.

The following 2 clock signals can be selected as the MCO clock:

- HSI clock division
- LSI clock division

The MCO clock is selected by RCC_CFG.MCO[1:0], and the clock is divided by RCC_CFG.MCOPRES[3:0].

4.3 RCC Registers

4.3.1 RCC Register Overview

Table 4-1 RCC Register Overview

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
000h	RCC_HSICTRL	Reserved																								HSITRIM[3:0]				Reserved		HSI48MRDF	HSI40MRDF
	Reset Value																									1	0	0	0			1	0
004h	RCC_CFG	MCORES[3:0]				Reserved	MCO[1:0]		Reserved											SYSPRES[1:0]		Reserved	APBPRES [2:0]			AHBPRES[3:0]				Reserved				
	Reset Value	0	0	1	0		0	0												1	1		0	0	0	0	0	0	0				
00Ch	RCC_PRST	Reserved																	COMPRST	TIM6RST	TIM3RST	TIM1RST	SPIRST	Reserved	ADCRST	PWRRST	I2CRST	UART2RST	UART1RST	IOPBRST	IOPARST	BEEPERRST	AFIORST
	Reset Value																		0	0	0	0	0		0	0	0	0	0	0	0	0	0
010h	RCC_AHBPCLKEN	Reserved																			ADCEN	Reserved				CRCEN	Reserved						
	Reset Value																				0					0							
014h	RCC_APBPCLKEN	Reserved																	IWDGEN	TIM6EN	TIM3EN	TIM1EN	SPIEN	PWREN	I2CEN	UART2EN	UART1EN	COMPFILTEN	COMPEN	IOPBEN	IOPAEN	BEEPEREN	AFIOEN
	Reset Value																		1	0	0	0	0	1	0	0	0	0	0	0	0	0	0
018h	RCC_LSICTRL	Reserved							LSIDETFF	LSIFREQ[15:0]																LSIDETEN	LSITRIM[4:0]					LSIRDF	Reserved
	Reset Value								0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	1	0
01Ch	RCC_CTRLSTS	Reserved																				EMCRSTF	Reserved		LPWRRSTF	LVRRSTF	IWDGRSTF	SFTRSTF	PORRSTF	PINRSTF	Reserved		RMRSTF
	Reset Value																					0			0	0	0	0	1	1			0

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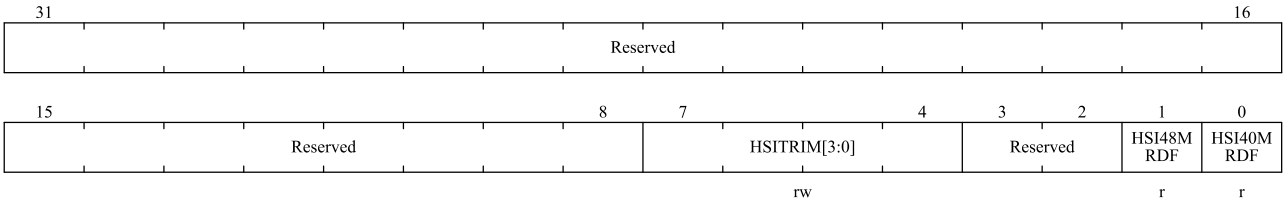
020h	RCC_CFG2	TIM1CLKSEL	TIM6CLKSEL	Reserved						ADC1MPRES[1:0]		Reserved		ADCPRE [3:0]		
	Reset Value	0	0							1	1			0	0	0	1
024h	RCC_EMCCTRL	Reserved							EMCRSTEN	Reserved						EMCDETEN
	Reset Value								0							0

4.3.2 HSI Clock Control Register (RCC_HSICTRL)

Address offset: 0x00

Reset value: 0x0000 0082



Bit Field	Name	Description
31:8	Reserved	Reserved, the reset value must be maintained.
7:4	HSITRIM[3:0]	High-speed internal clock trimming Written by software to calibrate the frequency of the internal HSI RC oscillator for higher accuracy as required by the application. The default value is 8, and the HSITRIM adjustment step is target frequency * 0.33% (the target frequency is 48M or 40M).
3:2	Reserved	Reserved, the reset value must be maintained.
1	HSI48MRDF	48M high-speed internal clock ready flag Set by hardware to indicate that internal 48 MHz RC oscillator is stable. 0: internal 48 MHz RC oscillator not ready 1: internal 48 MHz RC oscillator ready
0	HSI40MRDF	40M high-speed internal clock ready flag Set by hardware to indicate that internal 40 MHz RC oscillator is stable. 0: internal 40 MHz RC oscillator not ready 1: internal 40 MHz RC oscillator ready

4.3.3 Clock Configuration Register (RCC_CFG)

Address offset: 0x04

Reset value: 0x2000 3000

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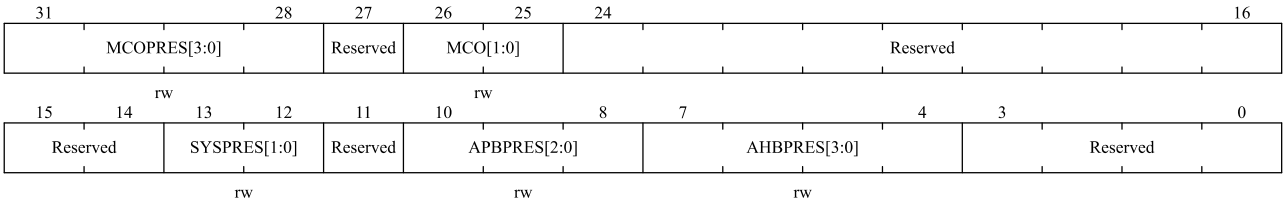

Bit Field	Name	Description
31:28	MCOPRES[3:0]	MCO prescaler Set and cleared by software. 0000: LSI clock is divided by 1 as MCO clock; HSI clock is divided by 2 as MCO clock 0001: LSI/HSI clock is divided by 2 as MCO clock 0010: LSI/HSI clock is divided by 3 as MCO clock 0011: LSI/HSI clock is divided by 4 as MCO clock 0100: LSI/HSI clock is divided by 5 as MCO clock 0101: LSI/HSI clock is divided by 6 as MCO clock 0110: LSI/HSI clock is divided by 7 as MCO clock 0111: LSI/HSI clock is divided by 8 as MCO clock 1000: LSI/HSI clock is divided by 9 as MCO clock 1001: LSI/HSI clock is divided by 10 as MCO clock 1010: LSI/HSI clock is divided by 11 as MCO clock 1011: LSI/HSI clock is divided by 12 as MCO clock 1100: LSI/HSI clock is divided by 13 as MCO clock 1101: LSI/HSI clock is divided by 14 as MCO clock 1110: LSI/HSI clock is divided by 15 as MCO clock 1111: LSI/HSI clock is divided by 32 as MCO clock
27	Reserved	Reserved, the reset value must be maintained.
26:25	MCO[1:0]	Microcontroller clock output selection Set and cleared by software. 00: no clock 01: LSI clock 10: LSE clock Others: Not allowed to set *Note: this clock output may be truncated at startup or during MCO clock source switching.* *When the HSI clock is selected to output to the MCO pin, the output clock frequency must not exceed the maximum I/O speed (For details of the maximum frequency of the I/O port, refer to the data sheet).*
24:14	Reserved	Reserved, the reset value must be maintained.
13:12	SYSPRES[1:0]	SYSCLK prescaler Set and cleared by software to control the division factor of the SYSCLK clock. **When HSI is 48M:** 00: HSI not divided as SYSCLK

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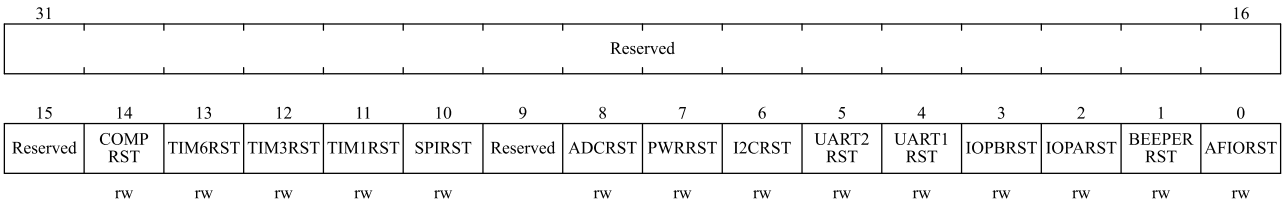
Bit Field	Name	Description
		01: HSI divided by 2 as SYSCLK Others: HSI divided by 6 as sysclk **When HSI is 40M:** 00: HSI not divided as SYSCLK Others: HSI divided by 5 as SYSCLK *Note: After exiting STOP mode, the bit reverts to the reset value.*
11	Reserved	Reserved, the reset value must be maintained.
10:8	APBPRES[2:0]	APB prescaler Set and cleared by software to control the division factor of the APB clock (PCLK). 0xx: HCLK not divided 100: HCLK divided by 2 101: HCLK divided by 4 110: HCLK divided by 8 111: HCLK divided by 16
7:4	AHBPRES[3:0]	AHB prescaler Set and cleared by software to control the division factor of the AHB clock (HCLK). 0xxx: SYSCLK not divided 1000: SYSCLK divided by 2 1001: SYSCLK divided by 4 1010: SYSCLK divided by 8 1011: SYSCLK divided by 12 1100: SYSCLK divided by 16 Others: SYSCLK divided by 24
3:0	Reserved	Reserved, the reset value must be maintained.

4.3.4 Peripheral Reset Register (RCC_PRST)

Address offset: 0x0c

Reset value: 0x0000 0000



Bit Field	Name	Description
31:15	Reserved	Reserved, the reset value must be maintained.
14	COMPRST	COMP reset Set and cleared by software. 0: Clear reset 1: Reset COMP
13	TIM6RST	TIM6 reset

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Bit Field	Name	Description
		Set and cleared by software. 0: Clear reset 1: Reset TIM6
12	TIM3RST	TIM3 reset Set and cleared by software. 0: Clear reset 1: Resets TIM3
11	TIM1RST	TIM1 reset Set and cleared by software. 0: Clear reset 1: Resets TIM1
10	SPIRST	SPI reset Set and cleared by software. 0: Clear reset 1: Reset SPI
9	Reserved	Reserved, the reset value must be maintained.
8	ADCRST	ADC reset Set and cleared by software. 0: Clear reset 1: Reset ADC
7	PWRRST	Power interface reset Set and cleared by software. 0: Clear reset 1: Reset the power interface
6	I2CRST	I2C reset Set and cleared by software. 0: Clear reset 1: Reset I2C
5	UART2RST	UART2 reset Set and cleared by software. 0: Clear reset 1: Reset UART2
4	UART1RST	UART1 reset Set and cleared by software. 0: Clear reset 1: Reset UART1
3	IOPBRST	GPIO port B reset Set and cleared by software. 0: Clear reset 1: Reset GPIO port B
2	IOPARST	GPIO port A reset Set and cleared by software.

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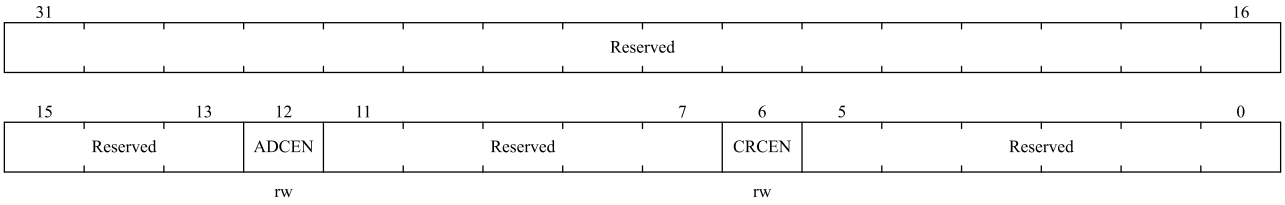
Bit Field	Name	Description
		0: Clear reset 1: Reset GPIO port A
1	BEEPERRST	Beeper reset Set and cleared by software. 0: Clear reset 1: Reset Beeper
0	AFIORST	Alternate function IO reset Set and cleared by software. 0: Clear reset 1: Reset alternate function IO

4.3.5 AHB Peripheral Clock Enable Register (RCC_AHBPCLKEN)

Address offset: 0x10

Reset value: 0x0000 0000



Bit Field	Name	Description
31:13	Reserved	Reserved, the reset value must be maintained.
12	ADCEN	ADC clock enable Set and cleared by software. 0: Disable ADC clock 1: Enable ADC clock
11:7	Reserved	Reserved, the reset value must be maintained.
6	CRCEN	CRC clock enable Set and cleared by software. 0: Disable CRC clock 1: Enable CRC clock
5:0	Reserved	Reserved, the reset value must be maintained.

4.3.6 APB Peripheral Clock Enable Register (RCC_APBPCLKEN)

Address offset: 0x14

Reset value: 0x0000 4200

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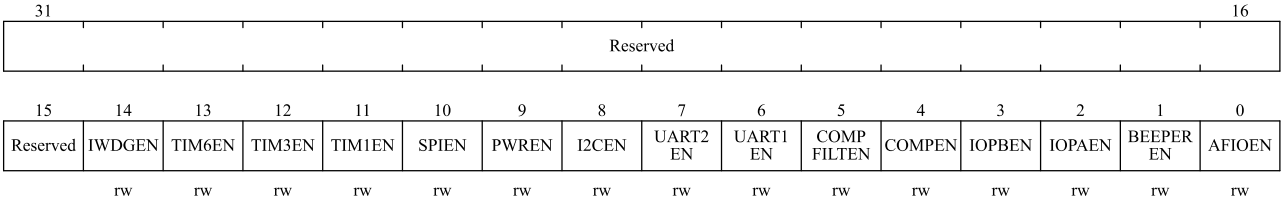

Bit Field	Name	Description
31:15	Reserved	Reserved, the reset value must be maintained.
14	IWDGEN	IWDG clock enable Set and cleared by software. 0: Disable IWDG clock 1: Enable IWDG clock
13	TIM6EN	TIM6 Clock Enable Set and cleared by software. 0: Disable TIM6 clock 1: Enable TIM6 clock
12	TIM3EN	TIM3 clock enable Set and cleared by software. 0: Disable TIM3 clock 1: Enable TIM3 clock
11	TIM1EN	TIM1 clock enable Set and cleared by software. 0: Disable TIM1 clock 1: Enable TIM1 clock
10	SPIEN	SPI clock enable Set and cleared by software. 0: Disable SPI clock 1: Enable SPI clock
9	PWREN	Power interface clock enable Set and cleared by software. 0: Disable the power interface clock 1: Enable the power interface clock
8	I2CEN	I2C clock enable Set and cleared by software. 0: Disable I2C clock 1: Enable I2C clock
7	UART2EN	UART2 clock enable Set and cleared by software. 0: Disable UART2 clock 1: Enable UART2 clock
6	UART1EN	UART1 clock enable Set and cleared by software. 0: Disable UART1 clock

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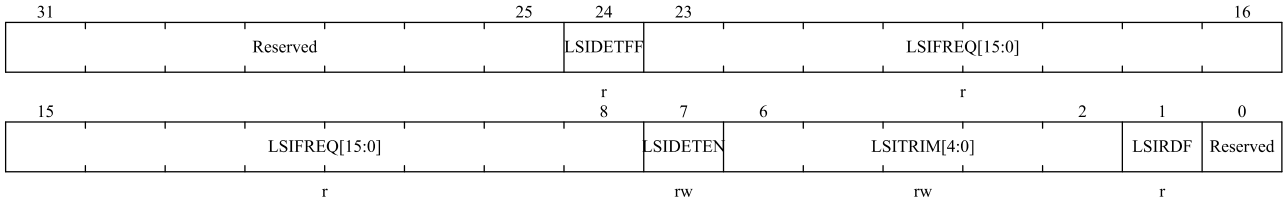
Bit Field	Name	Description
		1: Enable UART1 clock
5	COMPFILTEN	COMP filter clock enable 0: Disable the comparator filter clock 1: Enable the comparator filter clock
4	COMPEN	COMP clock enable 0: Disable the comparator clock 1: Enable the comparator clock
3	IOPBEN	GPIO port B clock enable Set and cleared by software. 0: Disable the clock of GPIO port B 1: Enable the clock of GPIO port B
2	IOPAEN	GPIO port A clock enable Set and cleared by software. 0: Disable the clock of GPIO port A 1: Enable the clock of GPIO port A
1	BEEPEREN	Beeper clock enable 0: Disable the Beeper clock 1: Enable the Beeper clock
0	AFIOEN	Alternate function IO clock enable Set and cleared by software. 0: Disable the alternate function IO clock 1: Enable the alternate function IO clock

4.3.7 Low Speed Clock Control Register (RCC_LSICTRL)

Address offset: 0x18

Reset value: 0x0000 0042



Bit Field	Name	Description
31:25	Reserved	Reserved, the reset value must be maintained
24	LSIDETFF	LSI detect finish flag Set by the hardware, and it is cleared by the disable LSIDETEN bit. 0: LSI detection has not finish 1: LSI detect finish
23:8	LSIFREQ[15:0]	LSI detect count

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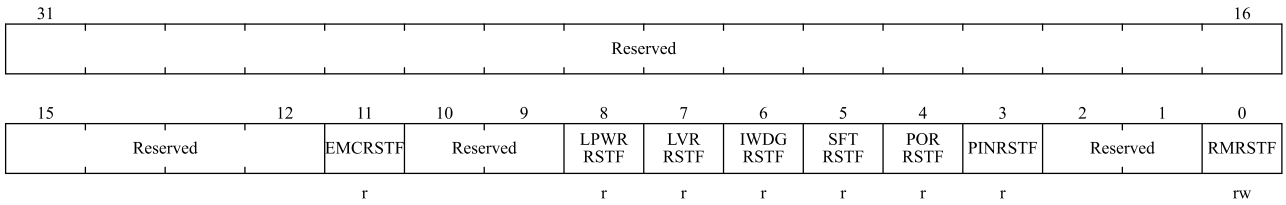
Bit Field	Name	Description
		Read-only, can be used for LSI frequency calibration. Actual LSI frequency LSICLK(kHz)= 8*HSICLK/LSIFREQ[15:0] (HSICLK is 48000kHz or 40000kHz)
7	LSIDETEN	LSI detect enable Set and cleared by software 0: Disable LSI detect 1: Enable LSI detect
6:2	LSITRIM[4:0]	LSI clock trimming Written by software to calibrate the frequency of the internal LSI RC oscillator for higher accuracy as required by the application. The default value is 16, and the LSITRIM adjustment step is 1kHz.
1	LSIRDF	LSI ready Set and cleared by hardware to indicate when the LSI is stable. 0: LSI not ready 1: LSI ready
0	Reserved	Reserved, the reset value must be maintained

4.3.8 Control/Status Register (RCC_CTRLSTS)

Address offset: 0x1c

Reset value: 0x0000 0018



Bit Field	Name	Description
31:12	Reserved	Reserved, the reset value must be maintained
11	EMCRSTF	EMC reset flag Set by hardware when EMC clamp is reset. It is cleared by writing RMRSTF bit. 0: No EMC clamp reset occurred 1: EMC clamp reset occurred
10:9	Reserved	Reserved, the reset value must be maintained
8	LPWRRSTF	Low-power reset flag Set by hardware at Low-power reset. It is cleared by writing RMRSTF bit. 0: No Low-power reset occurred 1: Low-power reset occurred
7	LVRRSTF	LVR reset flag Set by hardware at LVR reset.

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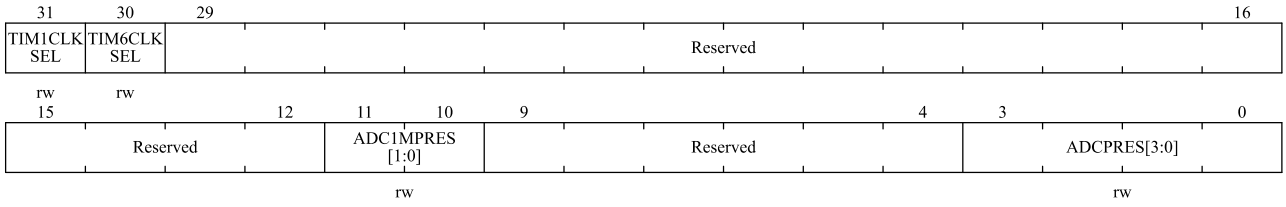
Bit Field	Name	Description
		It is cleared by writing RMRSTF bit. 0: No Low-power reset occurred 1: Low-power reset occurred
6	IWDGRSTF	Independent watchdog reset flag Set by hardware when an independent watchdog reset occurs It is cleared by writing RMRSTF bit. 0: No independent watchdog reset occurred 1: Independent watchdog reset occurred
5	SFTRSTF	Software reset flag Set by hardware when a software reset occurs. It is cleared by writing RMRSTF bit. 0: No software reset occurred 1: Software reset occurred
4	PORRSTF	POR/PDR reset flag Set by hardware when POR/PDR is reset. Cleared by writing to the RMRSTF bit 0: No POR/PDR reset occurred 1: POR/PDR reset occurred
3	PINRSTF	External pin reset flag Set by hardware when a reset from the NRST pin occurs. It is cleared by writing RMRSTF bit. 0: No NRST pin reset occurred 1: NRST pin reset occurred
2:1	Reserved	Reserved, the reset value must be maintained
0	RMRSTF	Remove reset flag Set and clear by software 0: No effect 1: Clear these reset flags

4.3.9 Clock Configuration Register 2 (RCC_CFG2)

Address offset: 0x20

Reset value: 0x0000 0c01



Bit Field	Name	Description
31	TIM1CLKSEL	TIM1 clock source selection Set and cleared by software.

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Bit Field	Name	Description
		0: PCLK is selected as TIM1 clock source if APB prescaler is 1. Otherwise, PCLK × 2 is selected. 1: SYSCLK clock is selected as TIM1 clock source.
30	TIM6CLKSEL	TIM6 clock source selection Set and cleared by software. 0: PCLK is selected as TIM6 clock source if APB prescaler is 1. Otherwise, PCLK × 2 is selected. 1: LSI clock is selected as TIM6 clock source.
29:12	Reserved	Reserved, the reset value must be maintained.
11:10	ADC1MPRES[1:0]	ADC 1M clock prescaler Set and cleared by software to configure the division factor of ADC 1M clock source. To ensure normal work of the ADC module, the HSI divide result must be 1M. **When HSI is 48M:** 00: HSI divided by 6 as ADC 1M clock 01: HSI divided by 12 as ADC 1M clock 10: HSI divided by 24 as ADC 1M clock 11: HSI divided by 48 as ADC 1M clock **When HSI is 40M:** 00~11: HSI divided by 40 as ADC 1M clock
9:4	Reserved	Reserved, the reset value must be maintained.
3:0	ADCPRES[3:0]	ADC work clock prescaler Set and cleared by software to configure the division factor of the ADC working clock source. To ensure normal work of the ADC module, the ADC working clock source cannot exceed 24M. 0000: HSI not divided as ADC work clock 0001: HSI divided by 2 as ADC work clock 0010: HSI divided by 3 as ADC work clock 0011: HSI divided by 4 as ADC work clock 0100: HSI divided by 6 as ADC work clock 0101: HSI divided by 8 as ADC work clock 0110: HSI divided by 10 as ADC work clock 0111: HSI divided by 12 as ADC work clock 1000: HSI divided by 24 as ADC work clock 1001: HSI divided by 32 as ADC work clock Others: HSI divided by 32 as ADC work clock

4.3.10 EMC Control Register (RCC_EMCCTRL)

Address offset: 0x24

Reset value: 0x0000 0000

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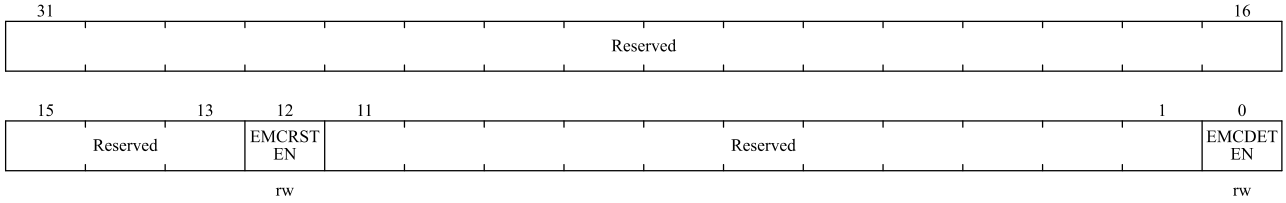

Bit Field	Name	Description
31:24	Reserved	Reserved, the reset value must be maintained.
12	EMCRSTEN	EMC reset enable Set and cleared by software. 0: Disable reset requests 1: Enable reset requests
11:1	Reserved	Reserved, the reset value must be maintained.
0	EMCDETEN	EMC clamp detect enable Set and cleared by software. 0: Disable detect 1: Enable detect

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5 GPIO and AFIO

5.1 Summary

The chip supports up to 18 GPIOs, which are divided into 2 groups (GPIOA/GPIOB). GPIOA has 16 pins, while GPIOB has 2 pins. Each GPIO pin can be configured by software as output (push-pull or open drain), input (with or without pull-up or pull-down) or alternate peripheral function port. (output/input). Most GPIO pins are shared with digital or analog reuse peripherals, and some IO pins are also reused with clock pins. Except for ports with analog input function, all GPIO pins have high current capacity.

GPIO ports have the following features:

- Each GPIO port can be configured with the following modes by software:
  - Input floating
  - Input pull-up
  - Input pull-down
  - Analog function
  - Open drain output and pull-up/pull-down capacity
  - Push-pull output and pull-up/pull-down capacity
  - Push-pull alternate function and pull-up/pull-down capacity
  - Open-drain alternate function and pull-up/pull-down capacity
- Individual bit setting or bit clearing function
- All I/Os support external interrupt function
- All I/Os support low power mode wake up, rising or falling edge configurable
  - 18 EXTI lines can be used to wake up in STOP mode, and all I/Os can be reused as EXTI
  - NRST(PA0)/PA1/PA2 can be used to wake up in PD mode, with a maximum filtering time of 1us
- Support software remapping I/O alternate function
- Support GPIO lock mechanism, reset the lock state to clear

Each I/O port bit can be programmed arbitrarily, but the I/O port register must be accessed as a 32-bit word (16-bit half-word or 8-bit byte are not allowed).The following figure shows the basic structure of an I/O port.

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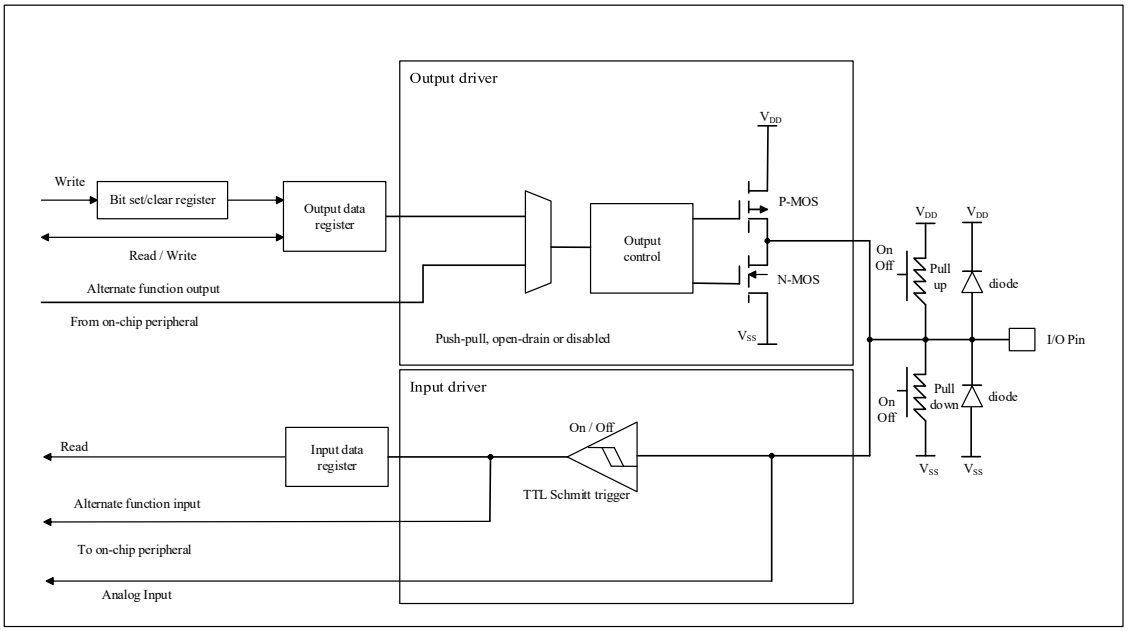
Figure 5-1 Basic Structure of an I/O Port



5.2 IO Function Description

5.2.1 IO Mode Configuration

The I/O port mode can be configured through the registers GPIOx_PMODE (x=A to B), GPIOx_POTYPE (x=A to B) and GPIOx_PUPD (x=A to B). The configuration of different operation modes is shown in the following table:

Table 5-1 Relationship Between I/O Modes and Configurations

PMODE[1:0]	POTYPE	PUPD[1:0]		I/O Configuration
01	0	0	0	General-purpose output push-pull
	0	0	1	General-purpose output push-pull + pull-up
	0	1	0	General-purpose output push-pull + pull-down
	0	1	1	Reserved
	1	0	0	General-purpose output open-drain
	1	0	1	General-purpose output open-drain + pull-up
	1	1	0	General-purpose output open-drain + pull-down
	1	1	1	Reserved
10	0	0	0	Alternate function push-pull
	0	0	1	Alternate function push-pull + pull-up
	0	1	0	Alternate function push-pull + pull-down
	0	1	1	Reserved
	1	0	0	Alternate function open-drain
	1	0	1	Alternate function open-drain + pull-up
	1	1	0	Alternate function open-drain + pull-down
	1	1	1	Reserved

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PMODE[1:0]	POTYPE	PUPD[1:0]		I/O Configuration
00	x	0	0	Input floating
	x	0	1	Input pull-up
	x	1	0	Input pull-down
	x	1	1	Reserved
11	x	0	0	Analog
	x	0	1	Reserved
	x	1	0	
	x	1	1	

In addition, the GPIOx_DS.DSy (x = A to B) bit can be used to configure the high/low drive strength, and the GPIOx_SR.SRy (x = A to B) bit can be used to configure the fast/slow slew rate.

The input and output characteristics of I/O under different configurations are shown in the following table:

Table 5-2 I/O List of Functional Features of the Lipin

Characteristic	GPIO input	GPIO Output	Analog Input	Peripheral Alternate
Output buffer	Disable	Enable	Disable	Configure according to peripheral function
Schmitt trigger	Enable	Enable	Disable The output value is forced to be 0	Enable
Pull-up/pull-down/floating	Configured	Configured	Disable	Configure according to peripheral function
Open-drain mode	Disable	Can be configured, GPIO output 0 when output data is "0", high resistance of GPIO when "1"	Disable	Can be configured, GPIO output 0 when output data is "0", high resistance of GPIO when "1"
Push-pull mode	Disable	Can be configured, GPIO output 0 when output data is "0", GPIO output 1 when output data is "1"	Disable	Can be configured, GPIO output 0 when output data is "0", GPIO output 1 when output data is "1"
Input data register (IO state)	Readable (I/O status)	Readable (I/O status)	Read as 0 (Schmitt OFF)	Readable (I/O status)
Output data register (Output value)	Invalid (last written value)	Readable and written	Invalid (last written value)	Readable

5.2.1.1 Input mode

When I/O port is configured in input mode:

- Output buffer is disabled
- The schmidt trigger input is activated
- Whether the pull-up and pull-down resistors are connected depends on the configuration of the GPIOx_PUPD (x = A

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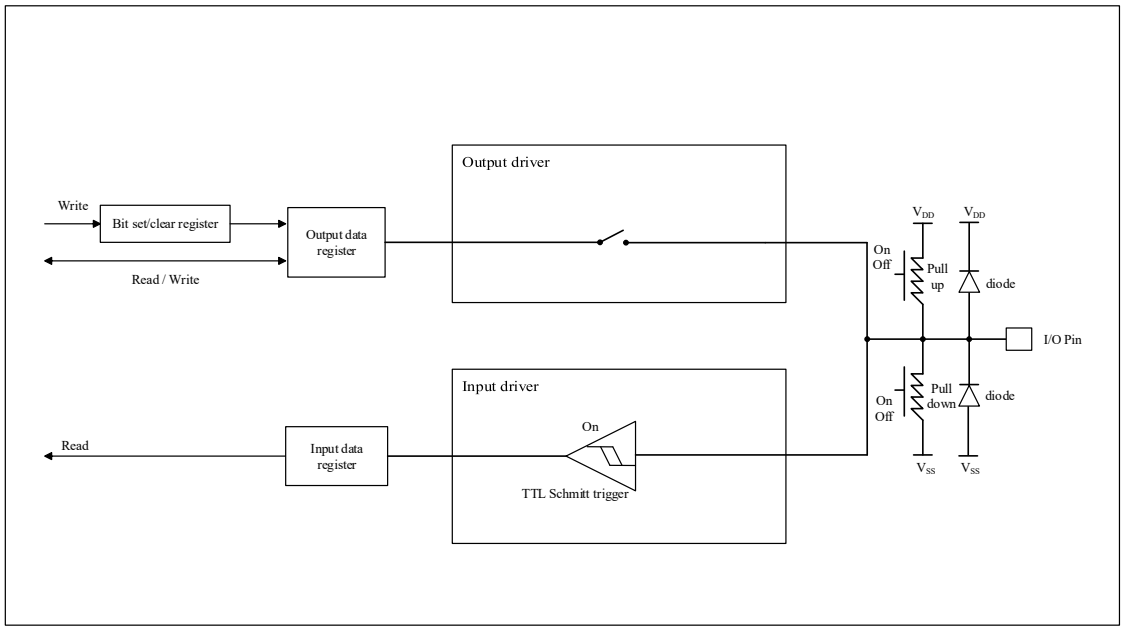
to B) register

- The data that appears on the I/O pin is sampled to the input data register on each APB clock
- Read access to the input data register provides the I/O status

Figure 5-2 Input Mode



5.2.1.2 Output mode

When I/O port is configured as output mode:

- The schmidt trigger input is activated
- Whether the pull-up and pull-down resistors are connected depends on the configuration of the GPIOx_PUPD (x = A to B) register
- The output buffer is activated.
  - Open drain mode: '0' on the output register activates the N-MOS, and the pin outputs a low level. While '1' on the output register places the port in a high resistance state (P-MOS is never activated).
  - Push-pull mode: '0' on the output register activates the N-MOS, and the pin outputs a low level. While '1' on the output register activates the P-MOS, and the pin outputs a high level.
- The data that appears on the I/O pin is sampled to the input data register on each APB clock.
- Read access to input data register to get I/O status.
- Read access to the output data register to get the last written value.

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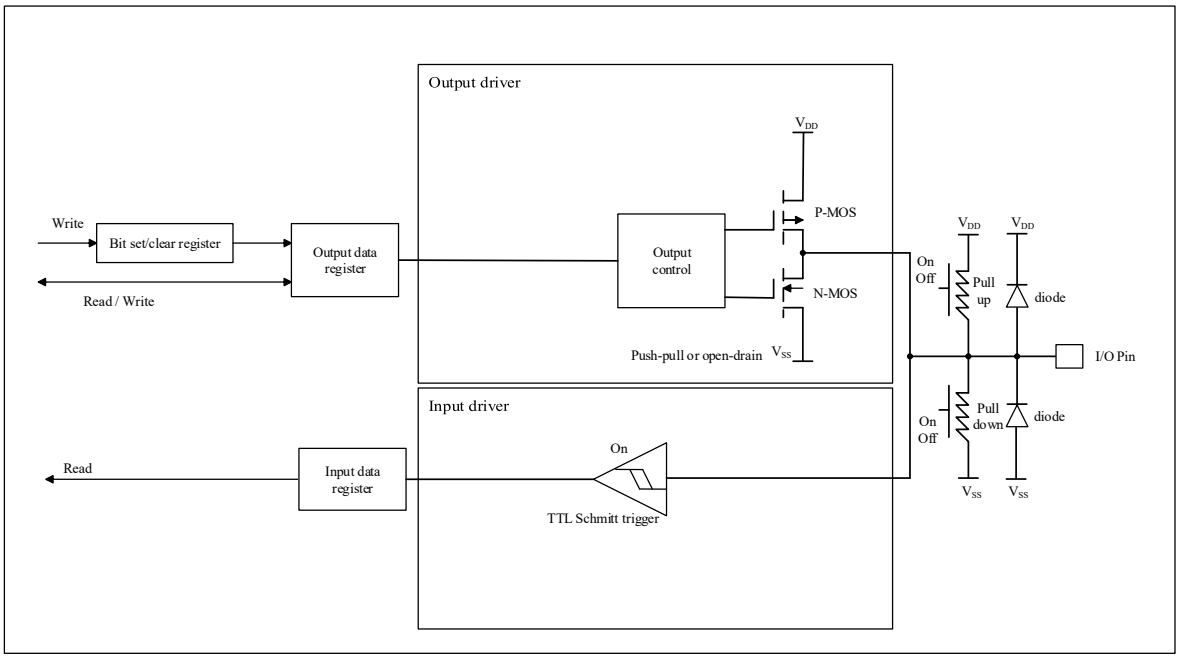
Figure 5-3 Output Mode



5.2.1.3 Alternate functional mode

When the I/O port is configured as alternate function mode:

- The schmidt trigger input is activated.
- Whether the pull-up and pull-down resistors are connected depends on the configuration of the GPIOx_PUPD (x = A to B) register
- In the open-drain or push-pull configuration, the output buffer is controlled by the peripheral.
- Signal-driven output buffers for built-in peripherals.
- At each APB clock cycle, the data appearing on the I/O pin is sampled into the input data register.
- Read access to input data register to get I/O status.
- Read access to the output data register to get the last written value.

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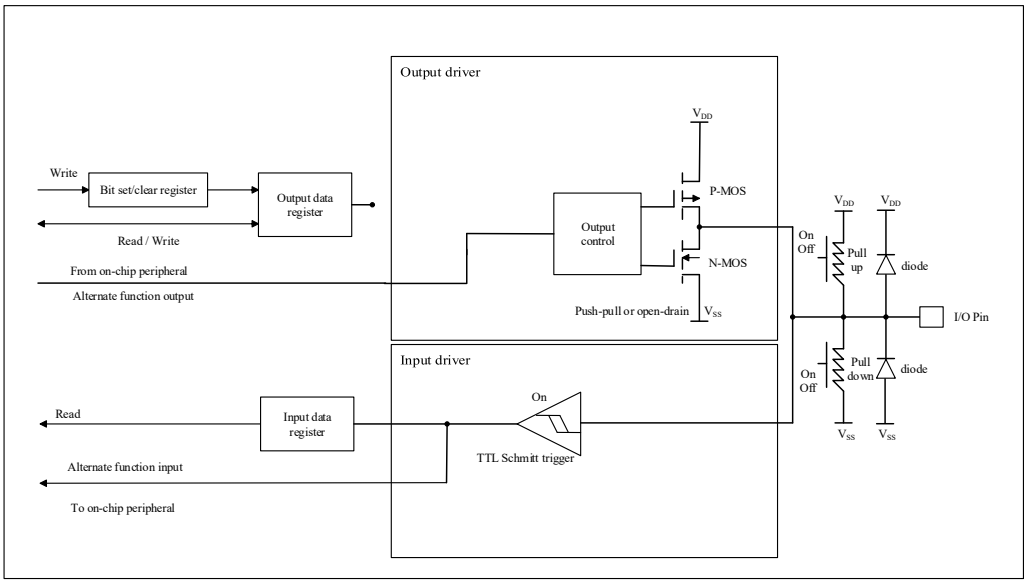
Figure 5-4 Alternate Function Mode

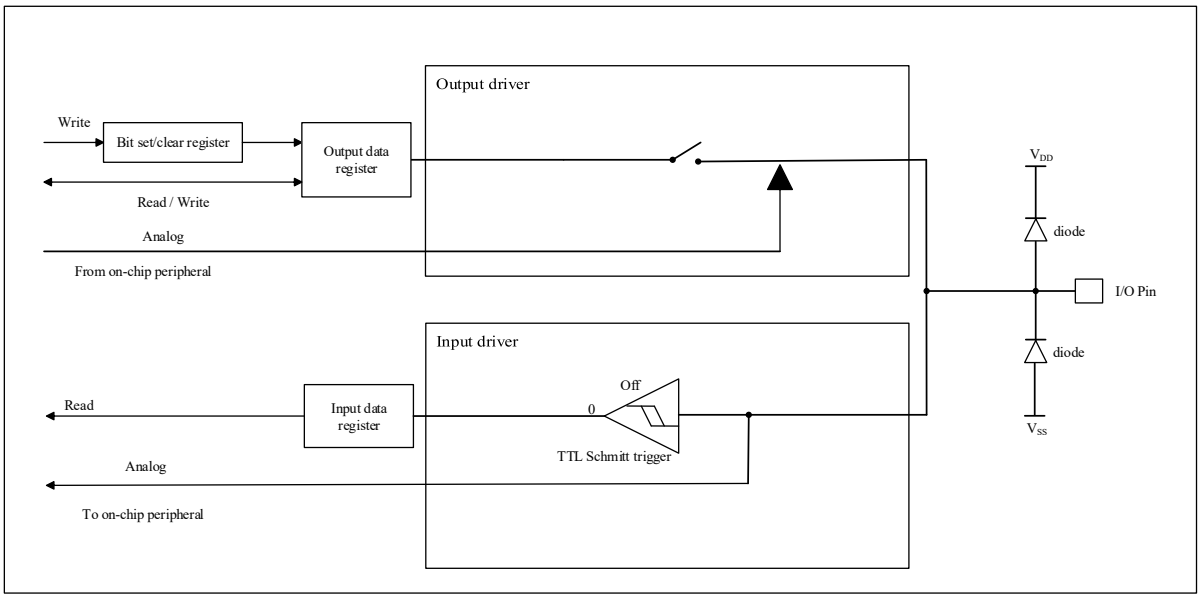


5.2.1.4 Analog mode

When the I/O port is configured as analog mode :

- The pull-up and pull-down resistors are disabled.
- Read access to the input data register gets the value “0”.
- The output buffer is disabled.
- Schmitt trigger input is disabled and output value is forced to '0' (achieves zero consumption on each analog I/O pin).

Figure 5-5 Analog Mode Configuration With High Impedance



5.2.2 Status after Reset

During and just after reset, the alternate functions are not active, and the I/O ports are configured as analog mode

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(GPIOx_PMODE.PMODEy[1:0] = 11). However, with the exception of the I/O ports below.

- NRST（PA0）:
  - FLASH_OB.NRST_PA0=1 (default): NRST in input pull-up mode
  - FLASH_OB.NRST_PA0=0: NRST is a normal GPIO. It cannot be driven low during power-on when used as an input (otherwise the chip will always be in reset state)
- After reset, the SWD_JTAG pins related to the debugging system are enabled by default:
  - PA9: SWCLK in input pull-down mode
  - PA8: SWDIO in input pull-up mode

5.2.3 Individual Bit Setting and Bit Clearing

By writing '1' to the bit in the bit set/clear register (GPIOx_PBSC) (x = A to B) and bit clear register (GPIOx_PBC) (x = A to B), the individual bit operation of the data register (GPIOx_POD) (x = A to B) can be realized, and one or more bits can be set/clear. The bit written with '1' is set or cleared accordingly, and the bit not written with '1' will not be changed. The software does not need to disable interrupts, and is completed in a single APB write operation.

5.2.4 External Interrupt/Wake-up Line

All ports have external interrupt capability, which can be configured in the EXTI module:

- In order to use an external interrupt line, the port must be configured in input mode
- All ports can be configured for STOP mode wake-up, supporting configurable rising or falling edge.
- NRST(PA0)/PA1_WKUP0/PA2_WKUP1 can be used for PD mode wake up, with independent wake-up enable. They support configurable rising/falling edge, which need to configure before entering PD mode.
- General purpose I/O ports are connected to 18 external interrupt/event lines, configured by registers AFIO_CFG.EXTI_SEL[4:0].

Table 5-3 Correspondence Between EXTI Line and Pin

EXTI Line Selection	Pin
EXTI Line0	PA0
EXTI Line1	PA1
EXTI Line2	PA2
EXTI Line3	PA3
EXTI Line4	PA4
EXTI Line5	PA5
EXTI Line6	PA6
EXTI Line7	PA7
EXTI Line8	PA8
EXTI Line9	PA9
EXTI Line10	PA10
EXTI Line11	PA11
EXTI Line12	PA12
EXTI Line13	PA13

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EXTI Line14	PA14
EXTI Line15	PA15
EXTI Line16	PB0
EXTI Line17	PB1

5.2.5 Alternate Function

When I/O ports are configured in alternate function mode, the port bit configuration register (GPIOx_AFL, GPIOx_AFH, GPIOx_PMODE, GPIOx_POTYPE and GPIOx_PUPD) must be programmed before using. The alternate input or output is determined by the peripheral.

5.2.5.1 Software remapping I/O alternate function

To expand the flexibility of alternate peripheral functions under different device packages, some peripheral alternate functions can be remapped to other pins. Each I/O has up to 16 alternate functions (AF0~AF15). After reset, except for PA8 and PA9, other pins' alternate function is AF15(AFSELy = AF15). The I/O alternate function can be remapped by configuring the corresponding registers (GPIOx_AFL/ GPIOx_AFH).

At this time, the alternate functions are no longer mapped to their original pins. For the I/O alternate function of the peripheral, if it is remapped to a different pin, the input can choose one of multiple remapped IO, and the output will be connected to the remapped position while the original position will be disconnected.

5.2.5.2 SWD alternate function I/O remapping

Table 5-4 I/O List of Functional Features of the Pin

Alternate Function	Pin	Remap
SWDIO	PA8	AF0
SWCLK	PA9	AF0

5.2.5.3 TIMx alternate function I/O remapping

5.2.5.3.1 TIM1 alternate function I/O remapping

Table 5-5 TIM1 Alternate Function I/O Remapping

Alternate Function	Pin	Remap
TIM1_ETR	PA14	AF5
	PA15	AF5
TIM1_BKIN	PA1	AF4
	PA5	AF4
	PA9	AF4
TIM1_CH1	PA6	AF4
	PA11	AF0
	PB0	AF4
TIM1_CH2	PA7	AF4
	PA12	AF3
	PA14	AF3
	PA15	AF4
TIM1_CH3	PA1	AF3

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Alternate Function	Pin	Remap
	PA7	AF5
	PA10	AF2
	PA11	AF4
TIM1_CH4	PA3	AF3
	PA6	AF3
	PA7	AF3
	PA8	AF2
	PA10	AF3
	PA11	AF3
	PA12	AF4
	PA13	AF3
	PA14	AF4
	PA15	AF3
	PB1	AF4
TIM1_CH1N	PA5	AF2
	PA11	AF5
	PA13	AF5
TIM1_CH2N	PA6	AF5
	PA12	AF5
	PA13	AF4
TIM1_CH3N	PA2	AF4
	PA3	AF4
	PA4	AF4
	PA10	AF4

5.2.5.4 TIM3 alternate function I/O remapping

Table 5-6 TIM3 Alternate Function I/O Remapping

Alternate Function	Pin	Remap
TIM3_ETR	PA9	AF2
	PB1	AF1
TIM3_CH1	PA1	AF2
	PA3	AF1
	PA6	AF1
	PA7	AF1
	PA10	AF0
	PA11	AF1
	PA12	AF0
	PA13	AF1
	PA14	AF0
	PA15	AF1
TIM3_CH2	PA2	AF2

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Alternate Function	Pin	Remap
	PA3	AF2
	PA6	AF2
	PA7	AF2
	PA10	AF1
	PA11	AF2
	PA12	AF1
	PA13	AF2
	PA14	AF1
	PA15	AF2

5.2.5.5 UARTx alternate function I/O remapping

5.2.5.5.1 UART1 alternate function I/O remapping

Table 5-7 UART1 Alternate Function I/O Remapping

Alternate Function	Pin	Remap
UART1_TX	PA2	AF5
	PA14	AF2
	PB0	AF2
UART1_RX	PA3	AF5
	PA12	AF2
	PB1	AF2

5.2.5.5.2 UART2 alternate function I/O remapping

Table 5-8 UART2 Alternate Function I/O Remapping

Alternate Function	Pin	Remap
UART2_TX	PA2	AF1
	PA8	AF1
	PA9	AF1
UART2_RX	PA1	AF1
	PA7	AF6
	PA9	AF8

5.2.5.6 I2C alternate function I/O remapping

Table 5-9 I2C Alternate Function I/O Remapping

Alternate Function	Pin	Remap
I2C_SCL	PA2	AF6
	PA4	AF6
	PA9	AF6
I2C_SDA	PA1	AF6
	PA3	AF6
	PA5	AF6

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Alternate Function	Pin	Remap
	PA8	AF6

5.2.5.7 SPI alternate function I/O remapping

Table 5-10 SPI Alternate Function I/O Remapping

Alternate Function	Pin	Remap
SPI_NSS	PA3	AF0
	PA8	AF5
SPI_SCK	PA14	AF6
	PA15	AF0
SPI_MISO	PA7	AF0
	PB0	AF6
SPI_MOSI	PA6	AF0
	PB1	AF6

5.2.5.8 COMP alternate function I/O remapping

Table 5-11 COMP Alternate function I/O remapping

Alternate Function	Pin	Remap
COMP1_OUT	PA8	AF3

5.2.5.9 BEEPER alternate function I/O remapping

Table 5-12 BEEPER Alternate Function I/O Remapping

Alternate Function	Pin	Remap
BEEPER1_OUT	PA14	AF7
BEEPER1_N_OUT	PB0	AF7

5.2.5.10 EVENTOUT alternate function I/O remapping

Table 5-13 EVENTOUT Alternate Function I/O Remapping

Alternate Function	Pin	Remap
EVENTOUT	PA4	AF3
	PB0	AF3
	PB1	AF3

5.2.5.11 MCO alternate function I/O remapping

Table 5-14 MCO Alternate Function I/O Remapping

Alternate Function	Pin	Remap
MCO	PA13	AF6

5.2.5.12 ADC external I/O triggers alternate function

The external trigger source for ADC conversion supports PA0~PA15 and PB0~PB1.

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5.2.6 I/O Configuration of Peripherals

Table 5-15 ADC

ADC	PAD Configuration
ADC	Analog function mode

Table 5-16 TIM1

TIM1 Pin	Configuration	PAD Configuration Mode
TIM1_CHx	Input capture channel x	Input floating
	Output compare channel x	Push-pull alternate function
TIM1_CHxN	Complementary output channel x	Push-pull alternate function
TIM1_BKIN	Brake input	Input floating
TIM1_ETR	External trigger timer input	Input floating

Table 5-17 TIM3

TIM3 Pin	Configuration	PAD Configuration Mode
TIM3_CHx	Input capture channel x	Input floating
	Output compare channel x	Push-pull alternate function
TIM3_ETR	External trigger timer input	Input floating

Table 5-18 UART

UART1/2 Pin	Configuration	PAD Configuration
UARTx_TX	Full duplex mode	Push-pull alternate function
	Half duplex mode	Push-pull alternate function
UARTx_RX	Full duplex mode	Input floating or input + pull-up
	Half duplex mode	It is not used. It can be used as general I/O

Table 5-19 I2C

I2C Pin	Configuration	PAD Configuration
I2C_SCL	I2C clock	Open drain alternate function
I2C_SDA	I2C data	Open drain alternate function

Table 5-20 SPI

SPI Pin	Configuration	PAD Configuration
SPI_SCK	Master mode	Push-pull alternate function
	Slave mode	Input floating
SPI_MOSI	Full duplex mode/master mode	Push-pull alternate function
	Full duplex mode/slave mode	Input floating or input + pull-up
	Simplex bidirectional data wire / master mode	Push-pull alternate function
	Simplex bidirectional data wire /slave mode	It is not used. It can be used as general I/O
SPI_MISO	Full duplex mode/ master mode	Input floating or input + pull-up
	Full duplex mode/slave mode	Push-pull alternate function

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SPI Pin	Configuration	PAD Configuration
	Simplex bidirectional data wire /master mode	It is not used. It can be used as general I/O
	Simplex bidirectional data wire /slave mode	Push-pull alternate function
SPI_NSS	Hardware master/slave mode	Input floating or input + pull-up or input + pull-down
	Hardware master mode /NSS output is enabled	Push-pull alternate function (NSS can choose IDLE high impedance or IDLE is 1 when used as host)
	Software mode	It is not used. It can be used as general I/O

Table 5-21 COMP

COMP Pin	PAD Configuration
COMP_OUT	Push-pull alternate function
COMP_IN	Analog input

Table 5-22 BEEPER

BEEPER Pin	PAD Configuration
BEEPER_OUT	Push-pull alternate function
BEEPER_N_OUT	Push-pull alternate function

Table 5-23 Other

Pin	Alternate Function	GPIO Configuration
EVENTOUT	Event output	Push-pull alternate function
MCO	Clock output	Push-pull alternate function
EXTI line input	External interrupt input	Input floating or input + pull-up or input + pull-down

5.2.7 GPIO Locking Mechanism

The locking mechanism allows to freeze contents of I/O configuration (GPIOx_PMODE, GPIOx_POTYPE, GPIOx_PUPD, GPIOx_DS, and GPIOx_SR) and alternate function registers (GPIOx_AFL and GPIOx_AFH). When the lock procedure is executed on one port bit, the configuration of that port bit will no longer be changed until the next reset, referring to the port configuration lock register GPIOx_PLOCK.

- PLOCKK, that is, GPIOx_PLOCK [16], becomes 1 only after the correct sequence w1 -> w0 -> w1 -> r0 (r0 here is also a must). After that, it becomes 0 only if the system reset is performed. GPIOx_PLOCK.PLOCK[15:0] can only be modified at GPIOx_PLOCK.PLOCKK = 0.
- The lock sequence to set GPIOx_PLOCK.PLOCKK bit, w1 -> w0 -> w1 -> r0 will be valid only if the value (1 or 0) in GPIOx_PLOCK.PLOCK [15:0] does not change during this sequence.The GPIOx_PLOCK.PLOCKK bit will not be set if the value in GPIOx_PLOCK.PLOCK [15:0] changes during this sequence.
- As long as GPIOx_PLOCK.PLOCKK = 0 and GPIOx_PLOCK.PLOCKy = 0 or 1, all configuration and alternate function bits can be modified. When GPIOx_PLOCK.PLOCKK = 1 but GPIOx_PLOCK.PLOCKy = 0, the corresponding configuration and alternate function bits corresponding to GPIOx_PLOCK.PLOCKy = 0 can be modified.
- Only when GPIOx_PLOCK.PLOCKK = 1 and GPIOx_PLOCK.PLOCKy = 1, the configurations corresponding to

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GPIOx_PLOCK.PLOCKy = 1 are locked and can not be modified.

- If the lock sequence operation is wrong, then it must be redone (w1 -> w0 -> w1 -> r0) to initiate the lock operation again.

5.3 GPIO Registers

These peripheral registers must be operated in 32-bit word mode.

GPIOA base address: 0x4000 1C00.

GPIOB base address: 0x4000 2000.

5.3.1 GPIOA Register Overview

Table 5-24 GPIOA Register Overview

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x00	GPIOA_PMODE	PMODE15[1:0]		PMODE14[1:0]		PMODE13[1:0]		PMODE12[1:0]		PMODE11[1:0]		PMODE10[1:0]		PMODE9[1:0]		PMODE8[1:0]		PMODE7[1:0]		PMODE6[1:0]		PMODE5[1:0]		PMODE4[1:0]		PMODE3[1:0]		PMODE2[1:0]		PMODE1[1:0]		PMODE0[1:0]	
	Reset value	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
0x04	GPIOA_POTYPE	Reserved																POT15	POT14	POT13	POT12	POT11	POT10	POT9	POT8	POT7	POT6	POT5	POT4	POT3	POT2	POT1	POT0
	Reset value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x08	GPIOA_SR	Reserved																SR15	SR14	SR13	SR12	SR11	SR10	SR9	SR8	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0
	Reset value																	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
0x0C	GPIOA_PUPD	PUPD15[1:0]		PUPD14[1:0]		PUPD13[1:0]		PUPD12[1:0]		PUPD11[1:0]		PUPD10[1:0]		PUPD9[1:0]		PUPD8[1:0]		PUPD7[1:0]		PUPD6[1:0]		PUPD5[1:0]		PUPD4[1:0]		PUPD3[1:0]		PUPD2[1:0]		PUPD1[1:0]		PUPD0[1:0]	
	Reset value	0	1	1	0	0	1	0	0	0	0	0	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x10	GPIOA_PID	Reserved																PID15	PID14	PID13	PID12	PID11	PID10	PID9	PID8	PID7	PID6	PID5	PID4	PID3	PID2	PID1	PID0
	Reset value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x14	GPIOA_POD	Reserved																POD15	POD14	POD13	POD12	POD11	POD10	POD9	POD8	POD7	POD6	POD5	POD4	POD3	POD2	POD1	POD0
	Reset value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x18	GPIOA_PBSC	PBC15	PBC14	PBC13	PBC12	PBC11	PBC10	PBC9	PBC8	PBC7	PBC6	PBC5	PBC4	PBC3	PBC2	PBC1	PBC0	PBS15	PBS14	PBS13	PBS12	PBS11	PBS10	PBS9	PBS8	PBS7	PBS6	PBS5	PBS4	PBS3	PBS2	PBS1	PBS0
	Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x28	GPIOA_PBC	Reserved																PBC15	PBC14	PBC13	PBC12	PBC11	PBC10	PBC9	PBC8	PBC7	PBC6	PBC5	PBC4	PBC3	PBC2	PBC1	PBC0
	Reset value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x1C	GPIOA_PLOCK	Reserved															PLOCKK	PLOCK15	PLOCK14	PLOCK13	PLOCK12	PLOCK11	PLOCK10	PLOCK9	PLOCK8	PLOCK7	PLOCK6	PLOCK5	PLOCK4	PLOCK3	PLOCK2	PLOCK1	PLOCK0
	Reset value																0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x20	GPIOA_AFL	AFSEL7[3:0]				AFSEL6[3:0]				AFSEL5[3:0]				AFSEL4[3:0]				AFSEL3[3:0]				AFSEL2[3:0]				AFSEL1[3:0]				AFSEL0[3:0]			
	Reset value	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
0x24	GPIOA_AFH	AFSEL15[3:0]				AFSEL14[3:0]				AFSEL13[3:0]				AFSEL12[3:0]				AFSEL11[3:0]				AFSEL10[3:0]				AFSEL9[3:0]				AFSEL8[3:0]			
	Reset value	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
0x2C	GPIOA_DS	Reserved																DS15	DS14	DS13	DS12	DS11	DS10	DS9	DS8	DS7	DS6	DS5	DS4	DS3	DS2	DS1	DS0
	Reset value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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5.3.2 GPIOB Register Overview

Table 5-25 GPIOB Register Overview

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x00	GPIOA_PMODE	Reserved																												PMODE1[1:0]		PMODE0[1:0]	
	Reset value																													1	1	1	1
0x04	GPIOA_POTYPE	Reserved																														POT1	POT0
	Reset value																															0	0
0x08	GPIOA_SR	Reserved																														SR1	SR0
	Reset value																															1	1
0x0C	GPIOA_PUPD	Reserved																												PUPD1[1:0]		PUPD0[1:0]	
	Reset value																													0	0	0	0
0x10	GPIOA_PID	Reserved																														PID1	PID0
	Reset value																															0	0
0x14	GPIOA_POD	Reserved																														POD1	POD0
	Reset value																															0	0
0x18	GPIOA_PBSC	Reserved														PBC1	PBC0	Reserved														PBS1	PBS0
	Reset value															0	0															0	0

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Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x28	GPIOA_PBC	Reserved																														PBC1	PBC0
	Reset value																															0	0
0x1C	GPIOA_PLOCK	Reserved															PLOCKK	Reserved														PLOCK1	PLOCK0
	Reset value																0															0	0
0x20	GPIOA_AFL	Reserved																								AFSEL1[3:0]				AFSEL0[3:0]			
	Reset value																									1	1	1	1	1	1	1	1
0x2C	GPIOA_DS	Reserved																														DS1	DS0
	Reset value																															0	0

5.3.3 GPIO Port Mode Register (GPIOx_PMODE)

Address offset: 0x00

Reset value(Port A) : 0xFFFA FFFF

Reset value(Port B) : 0x0000 000F

31 30	29 28	27 26	25 24	23 22	21 20	19 18	17 16
PMODE15[1:0]	PMODE14[1:0]	PMODE13[1:0]	PMODE12[1:0]	PMODE11[1:0]	PMODE10[1:0]	PMODE9[1:0]	PMODE8[1:0]
rw	rw	rw	rw	rw	rw	rw	rw
15 14	**13 12**	**11 10**	**9 8**	**7 6**	**5 4**	**3 2**	**1 0**
PMODE7[1:0]	PMODE6[1:0]	PMODE5[1:0]	PMODE4[1:0]	PMODE3[1:0]	PMODE2[1:0]	PMODE1[1:0]	PMODE0[1:0]
rw	rw	rw	rw	rw	rw	rw	rw

Bit Field	Name	Description
31:30	PMODEy [1:0]	Mode bits y for port GPIOx (x = A,B)
29:28		00: Input mode
27:26		01: General purpose output mode
25:24		10: Alternate function mode
23:22		11: Analog function mode
21:20		*Note: x = A, y = 0...15.*
19:18		*x = B, y =0, 1.*
17:16		
15:14		

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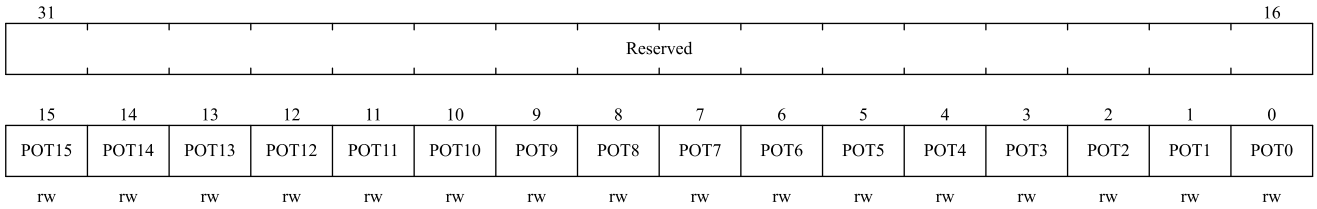
Bit Field	Name	Description
13:12		
11:10		
9:8		
7:6		
5:4		
3:2		
1:0		

5.3.4 GPIO Port Type Register (GPIOx_POTYPE)

Address offset: 0x04

Reset value (Port A) : 0x0000 0000

Reset value (Port B) : 0x0000 0000



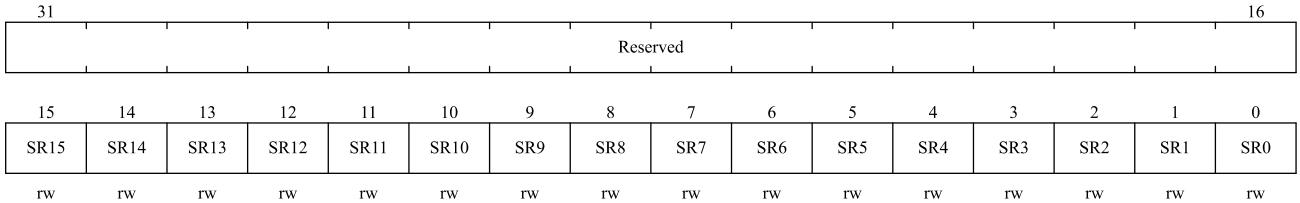
Bit Field	Name	Description
31:16	Reserved	The reset value must be maintained.
15:0	POTy	Output mode bits y for port GPIOx (x = A,B) 0: Output push-pull mode 1: Output open-drain mode *Note: x = A, y = 0...15.* *x = B, y =0, 1.*

5.3.5 GPIO Slew Rate Register (GPIOx_SR)

Address offset: 0x08

Reset value (Port A) : 0x0000 FFFF

Reset value (Port B) : 0x0000 0003



Bit Field	Name	Description
Caused the	Reserved	The reset value must be maintained.
15:0	SRy	Slew rate configuration bits y for port GPIOx (x = A,B):

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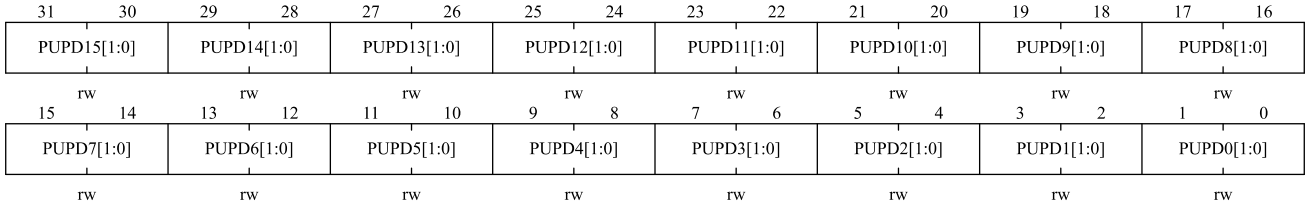
Bit Field	Name	Description
		0: Fast slew rate 1: Slow slew rate *Note: x = A, y = 0...15.* *x = B, y =0, 1 .*

5.3.6 GPIO Port Pull-up/Pull-down Register (GPIOx_PUPD)

Address offset: 0x0C

Reset value (Port A) : 0x0009 0000

Reset value (Port B) : 0x0000 0000



Bit Field	Name	Description
31:30	PUPDy[1:0]	Pull-up/pull-down mode bits y for port GPIOx (x = A,B):
29:28		00: No pull-up, pull-down
27:26		01: Pull-up
25:24		10: Pull-down
23:22		11: Reserved
21:20		*Note: x = A, y = 0...15.*
19:18		*x = B, y =0, 1.*
17:16		
15:14		
13:12		
11:10		
9:8		
7:6		
5:4		
3:2		
1:0		

5.3.7 GPIO Port Input Data Register (GPIOx_PID)

Address offset: 0x10

Reset value (Port A) : 0x0000 0000

Reset value (Port B) : 0x0000 0000

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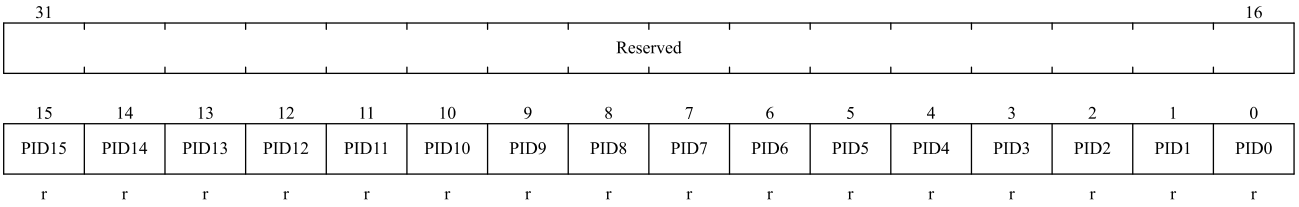


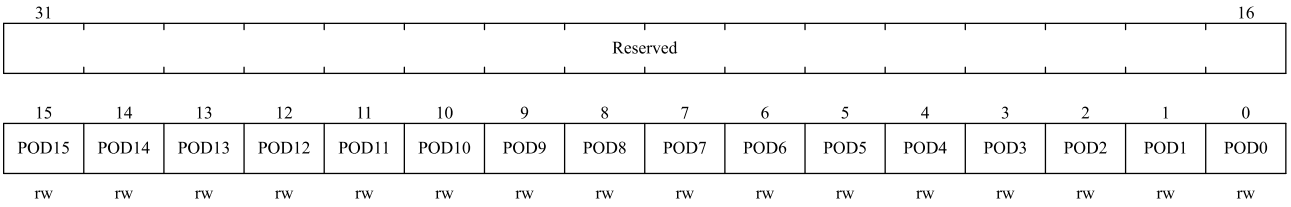
Bit Field	Name	Description
31:16	Reserved	The reset value must be maintained.
15:0	PIDy	Port GPIOx input data (x = A,B): These bits are read-only. They contain the input value of the corresponding I/O port. *Note: x = A, y = 0...15.* *x = B, y =0, 1.*

5.3.8 GPIO Port Output Data Register (GPIOx_POD)

Address offset: 0x14

Reset value (Port A) : 0x0000 0000

Reset value (Port B) : 0x0000 0000



Bit Field	Name	Description
31:16	Reserved	The reset value must be maintained.
15:0	PODy	Port output data These bits can be read and written by software. Port output data, the corresponding POD bits can be independently set/cleared by GPIOx_PBSC (x = A,B) register. *Note: x = A, y = 0...15.* *x = B, y =0, 1.*

5.3.9 GPIO Port Bit Set/Clear Register (GPIOx_PBSC)

Address offset: 0x18

Reset value (Port A) : 0x0000 0000

Reset value (Port B) : 0x0000 0000

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PBC15	PBC14	PBC13	PBC12	PBC11	PBC10	PBC9	PBC8	PBC7	PBC6	PBC5	PBC4	PBC3	PBC2	PBC1	PBC0
w	w	w	w	w	w	w	w	w	w	w	w	w	w	w	w
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PBS15	PBS14	PBS13	PBS12	PBS11	PBS10	PBS9	PBS8	PBS7	PBS6	PBS5	PBS4	PBS3	PBS2	PBS1	PBS0
w	w	w	w	w	w	w	w	w	w	w	w	w	w	w	w

Bit Field	Name	Description
31:16	PBCy	Clear bit y of port GPIOx (x = A,B) These bits can only be written. 0: The corresponding GPIOx_POD.PODy bit is not affected 1: Clears the corresponding GPIOx_POD.PODy bit to 0 *Note: if the corresponding bits of PBSy and PBCy are set at the same time, the PBSy bit takes effect.* *Note: x = A, y = 0...15.* *x = B, y =0, 1.*
15:0	PBSy	Set bit y of port GPIOx (x = A,B) These bits can only be written. 0: The corresponding GPIOx_POD.PODy bit is not affected 1: Sets the corresponding GPIOx_POD.PODy bit to 1 *Note: x = A,B, y = 0...15.* *x = B, y =0, 1.*

5.3.10 GPIO Port Bit Clear Register (GPIOx_PBC)

Address offset: 0x28

Reset value (Port A) : 0x0000 0000

Reset value (Port B) : 0x0000 0000

31															16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PBC15	PBC14	PBC13	PBC12	PBC11	PBC10	PBC9	PBC8	PBC7	PBC6	PBC5	PBC4	PBC3	PBC2	PBC1	PBC0
w	w	w	w	w	w	w	w	w	w	w	w	w	w	w	w

Bit Field	Name	Description
31:16	Reserved	The reset value must be maintained.
15:0	PBCy	Clear bit y of port GPIOx (x = A,B) These bits can only be written. 0: The corresponding GPIOx_POD.PODy bit is not affected 1: Clears the corresponding GPIOx_POD.PODy bit to 0 *Note: x = A, y = 0...15.* *x = B, y =0, 1.*

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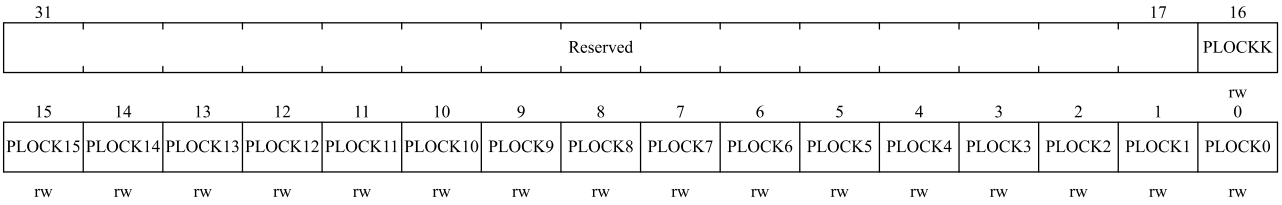
5.3.11 GPIO Port Lock Register (GPIOx_PLOCK)

Address offset: 0x1C

Reset value (Port A) : 0x0000 0000

Reset value (Port B) : 0x0000 0000



Bit Field	Name	Description
31:17	Reserved	The reset value must be maintained.
16	PLOCKK	Lock key This bit can be read anytime. It can only be modified using the lock key writing sequence. 0: Port configuration lock key not active 1: Port configuration lock key active. GPIOx_PLOCK register is locked until an MCU reset occurs. Lock key writing sequence: Write 1 -> write 0 -> write 1 -> read 0 -> read 1 The last reading can be omitted, but it can be used to confirm that the lock key has been activated. *Note: during the lock key writing sequence,the value of PLOCK[15:0] must not change. Any error in the lock sequence will abort the lock.*
15:0	PLOCKy	Configuration lock bit y of port GPIOx (x = A,B) These bits are readable and writable but can only be written when the PLOCKK bit is 0. 0: Do not lock the configuration of the port 1: Locks the configuration of the port *Note: x = A, y = 0...15.* *x = B, y =0, 1.*

5.3.12 GPIO Alternate Function Low Register (GPIOx_AFL)

Address offset: 0x20

Reset value (Port A) : 0xFFFF FFFF

Reset value (Port B) : 0x0000 00FF

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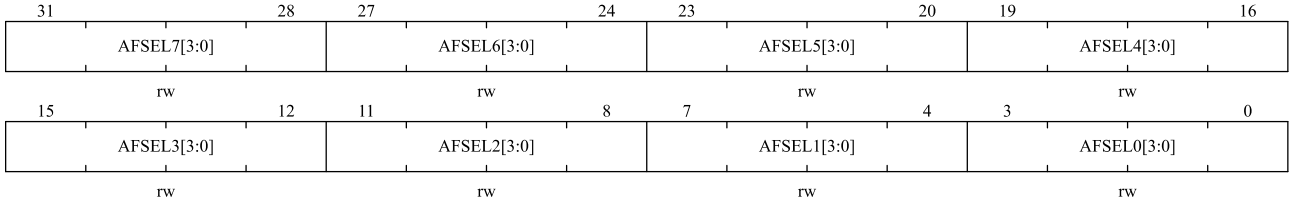
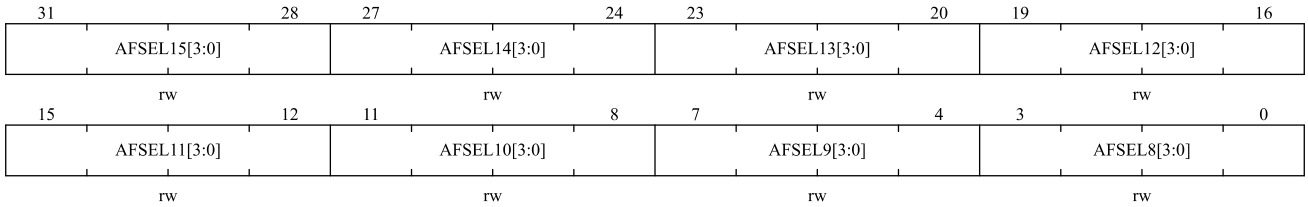


Bit Field	Name	Description
31:28	AFSELy[3:0]	Alternate function configuration bits y for port GPIOx (x = A,B)
27:24		0000: AF0
23:20		0001: AF1
19:16		0010: AF2
15:12		0011: AF3
11:8		0100: AF4
7:4		0101: AF5
3:0		0110: AF6
		0111: AF7
		1000: AF8
		1001: AF9
		1010: AF10
		1011: AF11
		1100: AF12
		1101: AF13
		1110: AF14
		1111: AF15
		Note: x = A, y = 0...7.
		x = B, y =0, 1.

5.3.13 GPIO Alternate Function High Register (GPIOx_AFH)

Address offset: 0x24

Reset value (Port A) : 0xFFFF FF00



Bit Field	Name	Description
31:28	AFSELy[3:0]	Alternate function configuration bits y for port GPIOA (y = 8…15)
27:24		0000: AF0
23:20		0001: AF1
19:16		0010: AF2
15:12		0011: AF3

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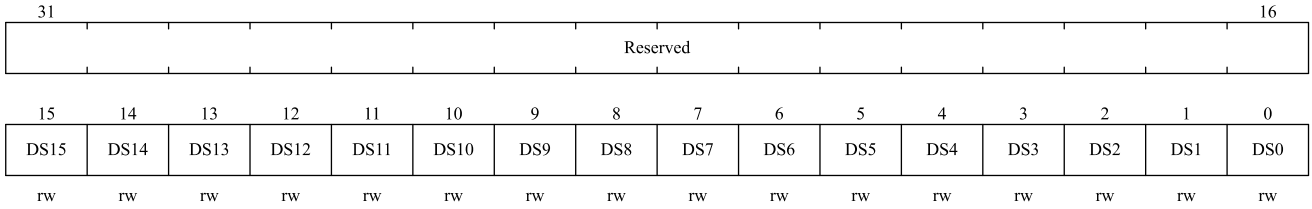
Bit Field	Name	Description
11:8 7:4 3:0		0100: AF4 0101: AF5 0110: AF6 0111: AF7 1000: AF8 1001: AF9 1010: AF10 1011: AF11 1100: AF12 1101: AF13 1110: AF14 1111: AF15

5.3.14 GPIO Driver Strength Register (GPIOx_DS)

Address offset: 0x2C

Reset value (Port A) : 0x0000 0000

Reset value (Port B) : 0x0000 0000



Bit Field	Name	Description
31:16	Reserved	The reset value must be maintained.
15:0	DSy	Port GPIOx drive capability configuration bits y (x = A,B): 0: High drive capacity (16mA(5V)/8mA(3.3V)/4mA(2V)) 1: Low drive capacity (8mA(5V)/4mA(3.3V)/2mA(2V) *Note: x = A, y = 0...15.* *x = B, y =0, 1.*

5.4 AFIO Registers

5.4.1 AFIO Register Overview

AFIO base address: 0x4000 1400

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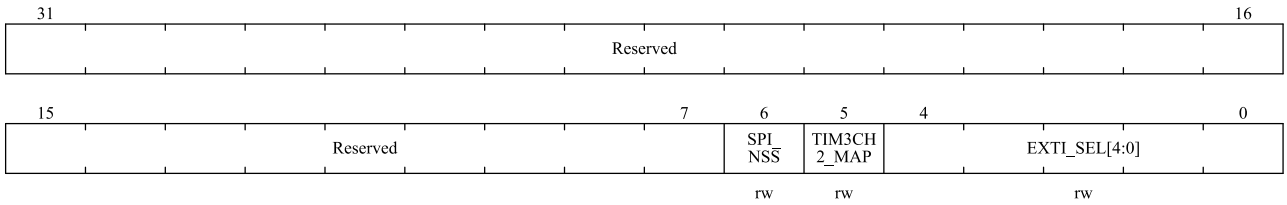
Table 5-26 AFIO register overview

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x00	AFIO_CFG	Reserved																									SPI_NSS	TIM3CH2_MAP	EXTI_SEL[4:0]					
	Reset Value																										0	0	0	0	0	0	0

5.4.2 AFIO Configuration Register (AFIO_CFG)

Address offset: 0x00

Reset value: 0x0000 0000



Bit Field	Name	Description
31:7	Reserved	The reset value must be maintained.
6	SPI_NSS	NSS mode of SPI (when NSS is configured as AFIO push-pull mode). 0: NSS will be high-z when idle 1: NSS will be high level when idle
5	TIM3CH2_MAP	TIM3 channel2 internal remap Set and cleared by software. This bit controls the TIM3_CH2 internal mapping. 0: The TIM3_CH2 is connected to PA2/PA3/PA6/PA7/PA10~PA15. 1: The LSI clock is connected to TIM3_CH2 input for calibration purpose. *Note: This bit is available only in high density value line devices.*
4:0	EXTI_ETRR[4:0]	Select an external pin to trigger the ADC regular conversion. 00000: Select PA0 to trigger the conversion 00001: Select PA1 to trigger the conversion 00010: Select PA2 to trigger the conversion 00011: Select PA3 to trigger the conversion 00100: Select PA4 to trigger the conversion 00101: Select PA5 to trigger the conversion 00110: Select PA6 to trigger the conversion 00111: Select PA7 to trigger the conversion 01000: Select PA8 to trigger the conversion 01001: Select PA9 to trigger the conversion 01010: Select PA10 to trigger the conversion

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Bit Field	Name	Description
		01011: Select PA11 to trigger the conversion 01100: Select PA12 to trigger the conversion 01101: Select PA13 to trigger the conversion 01110: Select PA14 to trigger the conversion 01111: Select PA15 to trigger the conversion 10000: Select PB0 to trigger the conversion 10001: Select PB1 to trigger the conversion

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6 Interrupts And Events

6.1 Nested Vectored Interrupt Controller

Features

- 16 maskable interrupt channels (excluding 16 Cortex®-M0 interrupt line);
- 4 programmable priorities (using 2 bit interrupt priorities);
- Low latency exception and interrupt handling;
- Power management control;
- The realization of system control registers;

The Nested Vectored Interrupt Controller (NVIC) is closely linked to the processor core, enabling low latency interrupt processing and efficient processing of late interrupts. The nested vectored interrupt controller manages interrupts including core exceptions.

6.1.1 SysTick Calibration Value Register

The system tick calibration value is fixed at 6000. When the system tick clock is set to 6MHz (when clock source is HCLK/8), 1 ms time base is generated.

6.1.2 Interrupt and Exception Vectors

Table 6-1 Vector Table

Position	Priority	Priority type	Name	Description	Address
-	-	-	-	Reserved	0x0000 0000
-	-3	Fixed	Reset	Reset	0x0000 0004
-	-2	Fixed	NMI	Non-maskable interrupt.RCC clock security system (CSS) is connected to the NMI vector.	0x0000 0008
-	-1	Fixed	HardFault	All types of errors (fault)	0x0000 000C
-	3	Settable	SVCall	System services invoked by SWI directives	0x0000 002C
-	5	Settable	PendSV	System service requests that can be pending	0x0000 0038
-	6	Settable	SysTick	System tick timer	0x0000 003C
0	7	Settable	PVD	PVD interrupt (connected to EXTI line 18)	0x0000 0040
1	8	Settable	Flash	Flash global interrupt	0x0000 0044
2	9	Settable	EXTI0_1	EXTI line [1:0] is interrupted	0x0000 0048
3	10	Settable	EXTI2_3	EXTI line [3:2] is interrupted	0x0000 004C
4	11	Settable	EXTI4_17	EXTI line [17:4] interrupt	0x0000 0050

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Position	Priority	Priority type	Name	Description	Address
5	12	Settable	TIM1_BRK_UP_TRG_COM	TIM1 break, updates, trigger and communication interrupt	0x0000 0054
6	13	Settable	TIM1_CC	TIM1 capture compare interrupt	0x0000 0058
7	14	Settable	TIM3	TIM3 global interrupt	0x0000 005C
8	15	Settable	TIM6	TIM6 global interrupt (connected to EXTI line 19)	0x0000 0060
9	16	Settable	ADC	ADC global interrupt	0x0000 0064
10	17	Settable	I2C_EV	I2C event interrupt	0x0000 0068
11	18	Settable	I2C_ER	I2C error interrupt	0x0000 006C
12	19	Settable	SPI	SPI global interrupt	0x0000 0070
13	20	Settable	UART1	UART1 global interrupt	0x0000 0074
14	21	Settable	UART2	UART2 global interrupt	0x0000 0078
15	22	Settable	COMP	COMP global interrupt	0x0000 007C

6.2 Extended Interrupt/Event Controller (EXTI)

6.2.1 Introduction

The extended interrupt/event controller contains 20 edge detection circuits that generate interrupt/event triggers. Each input line can be independently configured with pulse or pending input types, and three trigger event types including rising edge, falling edge or double edges, which can also be independently shielded. Interrupt requests that hold the state line in the pending register can be cleared by writing '1' in the corresponding bit of the pending register.

6.2.2 Main Features

The main features of EXTI controller are as follows:

- Support 20 software interrupt/event requests
- Interrupts/events corresponding to each input line can be configured to trigger or mask independently
- Each interrupt line has an independent state bit
- Support for pulse or pending input types
- 3 trigger events are supported: rising edge, falling edge, and double edges
- Can wake up MCU to exit low power mode

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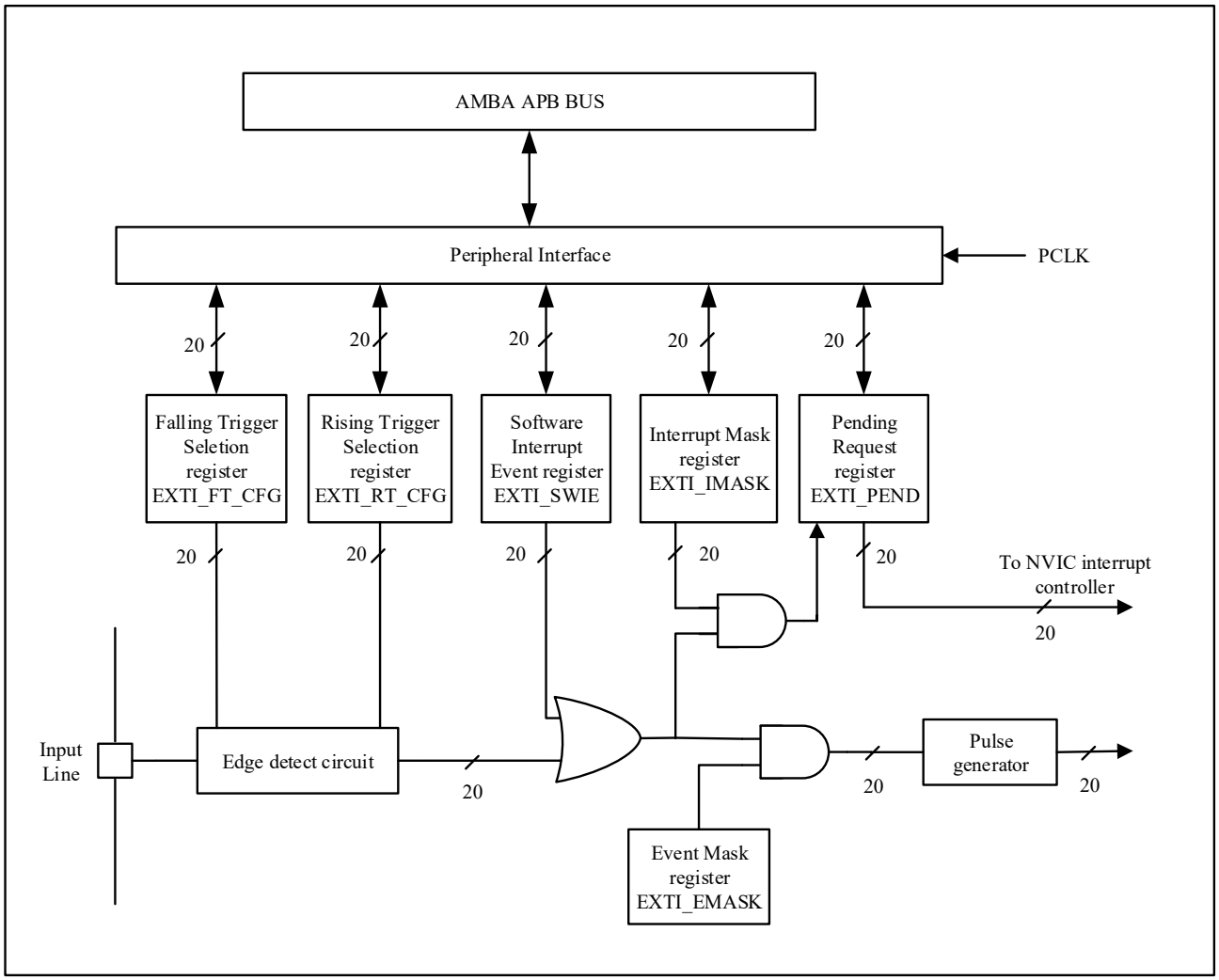
Figure 6-1 Extenal Interrupt/Event Controller Block Diagram



6.2.3 Functional Description

The EXTI contains 20 interrupt lines, 18 lines from I/O pins and 2 lines from internal modules. To generate interrupts, the NVIC interrupt channel of the extendedinterrupt controller must be configured to enable the corresponding interrupt lines. Select rising edge, falling edge, or double edges trigger event types by edge trigger configuration registers EXTI_RT_CFG and EXTI_FT_CFG, and write '1' to the corresponding bit of interrupt masking register EXTI_IMASK to allow interrupt requests. When a preset edge trigger polarity is detected on the external interrupt line, an interrupt request is generated and the corresponding pending bit is set to '1'. Writing '1' to the corresponding bit of the pending register clears the interrupt request.

To generate events, the corresponding event line must be configured and enabled. According to the desired edge detection polarity, set up the rising/falling edge trigger configuration register, while writing '1' in the corresponding bit of the event masking register to allow interrupt requests. When a preset edge occurs on an event line, an event request pulse is generated and the corresponding pending bit is not set to '1'.

In addition, interrupt/event requests can also be generated by software by writing a '1' in the software interrupt/event register.

- Hardware interrupt configuration, select and configure 20 lines as interrupt sources as required:

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  - Configure the mask bit (EXTI_IMASK) for 20 interrupt lines.
  - Configure the Trigger Selection bits of the selected interrupt line(EXTI_RT_CFG and EXTI_FT_CFG);
  - Configure the enable and mask bits of the NVIC interrupt channel corresponding to the external interrupt controller so that the requests in the 20 interrupt lines can be correctly responded.
- Hardware event configuration: Select 20 lines as event sources as required:
  - Configure the mask bit (EXTI_EMASK) for 20 event lines.
  - Configure the Trigger Selection bits for the selected event line (EXTI_RT_CFG and EXTI_FT_CFG).
- Software interrupt/event configuration, select 20 lines as software interrupt/event lines as required:
  - Configure 20 interrupt/event line mask bits (EXTI_IMASK and EXTI_EMASK).
  - Configure the request bit of the software interrupt event register (EXTI_SWIE).

6.2.4 EXTI Line Mapping

To configure external interrupts/events on the GPIO line by AFIO_CFG.EXTI_ETRR[4:0], the AFIO clock must be enabled first. The general-purpose I/O ports and internal modules are connected as follows:

- EXTI line 0 is connected to PA0
- EXTI line 1 is connected to PA1
- EXTI line 2 is connected to PA2
- EXTI line 3 is connected to PA3
- EXTI line 4 is connected to PA4
- EXTI line 5 is connected to PA5
- EXTI line 6 is connected to PA6
- EXTI line 7 is connected to PA7
- EXTI line 8 is connected to PA8
- EXTI line 9 is connected to PA9
- EXTI line 10 is connected to PA10
- EXTI line 11 is connected to PA11
- EXTI line 12 is connected to PA12
- EXTI line 13 is connected to PA13
- EXTI line 14 is connected to PA14
- EXTI line 15 is connected to PA15
- EXTI line 16 is connected to PB0
- EXTI line 17 is connected to PB1
- EXTI line 18 is connected to PVD

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- EXTI line 19 is connected to TIM6 wake up event

6.3 EXTI Registers

EXTI base address: 0x40003400

6.3.1 EXTI Register Overview

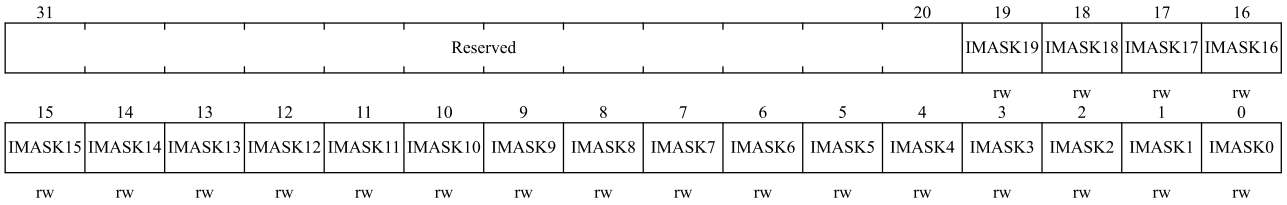
Table 6-2 EXTI Register Overview

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
000h	EXTI_IMASK	Reserved												IMASK19	IMASK18	IMASK17	IMASK16	IMASK15	IMASK14	IMASK13	IMASK12	IMASK11	IMASK10	IMASK9	IMASK8	IMASK7	IMASK6	IMASK5	IMASK4	IMASK3	IMASK2	IMASK1	IMASK0
	Reset Value													0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
004h	EXTI_EMASK	Reserved												EMASK19	EMASK18	EMASK17	EMASK16	EMASK15	EMASK14	EMASK13	EMASK12	EMASK11	EMASK10	EMASK9	EMASK8	EMASK7	EMASK6	EMASK5	EMASK4	EMASK3	EMASK2	EMASK1	EMASK0
	Reset Value													0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
008h	EXTI_RT_CFG	Reserved												RT_CFG19	RT_CFG18	RT_CFG17	RT_CFG16	RT_CFG15	RT_CFG14	RT_CFG13	RT_CFG12	RT_CFG11	RT_CFG10	RT_CFG9	RT_CFG8	RT_CFG7	RT_CFG6	RT_CFG5	RT_CFG4	RT_CFG3	RT_CFG2	RT_CFG1	RT_CFG0
	Reset Value													0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
00Ch	EXTI_FT_CFG	Reserved												FT_CFG19	FT_CFG18	FT_CFG17	FT_CFG16	FT_CFG15	FT_CFG14	FT_CFG13	FT_CFG12	FT_CFG11	FT_CFG10	FT_CFG9	FT_CFG8	FT_CFG7	FT_CFG6	FT_CFG5	FT_CFG4	FT_CFG3	FT_CFG2	FT_CFG1	FT_CFG0
	Reset Value													0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
010h	EXTI_SWIE	Reserved												SWIE19	SWIE18	SWIE17	SWIE16	SWIE15	SWIE14	SWIE13	SWIE12	SWIE11	SWIE10	SWIE9	SWIE8	SWIE7	SWIE6	SWIE5	SWIE4	SWIE3	SWIE2	SWIE1	SWIE0
	Reset Value													0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
014h	EXTI_PEND	Reserved												PEND19	PEND18	PEND17	PEND16	PEND15	PEND14	PEND13	PEND12	PEND11	PEND10	PEND9	PEND8	PEND7	PEND6	PEND5	PEND4	PEND3	PEND2	PEND1	PEND0
	Reset Value													0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

6.3.2 Interrupt Mask Register(EXTI_IMASK)

Address offset : 0x00

Reset value : 0x00000000



Bit Field	Name	Description
31:20	Reserved	Reserved,the reset value must be maintained.
19:0	IMASKx	Interrupt mask on line x. (x is 0,1,2…19) 0: Masking the interrupt request from line x; 1: Not masking the interrupt request from line x

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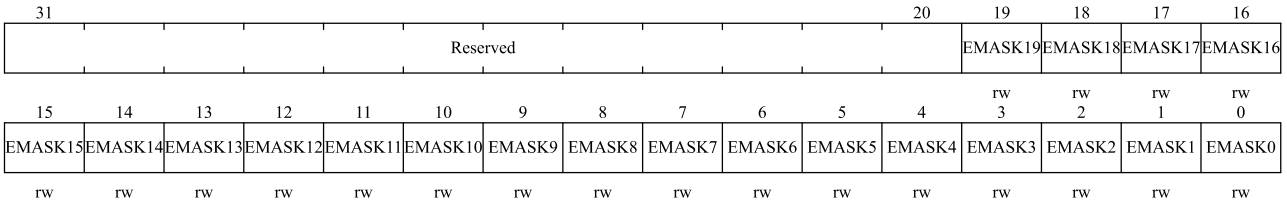
6.3.3 Event Mask Register(EXTI_EMASK)

Address offset : 0x04

Reset value : 0x00000000

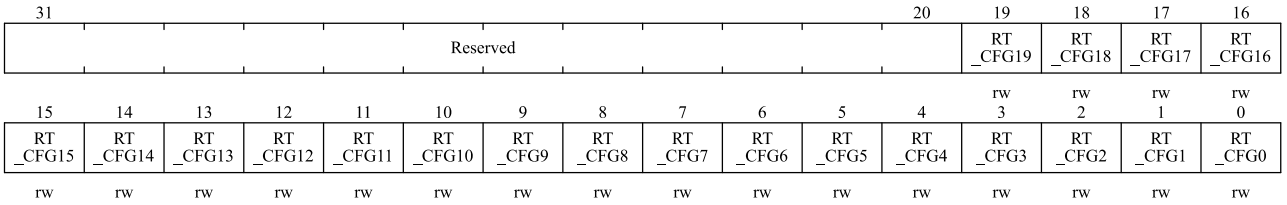


Bit Field	Name	Description
31:20	Reserved	Reserved,the reset value must be maintained.
19:0	EMASKx	Event masking on line x. (x is 0,1,2…19) 0: Masking the event request from line x; 1: Not masking the event request from line x

6.3.4 Rising Edge Trigger Selection Register(EXTI_RT_CFG)

Address offset : 0x08

Reset value : 0x00000000



Bit Field	Name	Description
31:20	Reserved	Reserved,the reset value must be maintained.
19:0	RT_CFGx	The rising edge on line x triggers the configuration bit. (x is 0,1,2…19) 0: Disables rising edge trigger (interrupts and events) on input line x. 1: Enable rising edge trigger (interrupts and events) on input line x.

6.3.5 Falling Edge Trigger Selection Register(EXTI_FT_CFG)

Address offset : 0x0C

Reset value : 0x00000000

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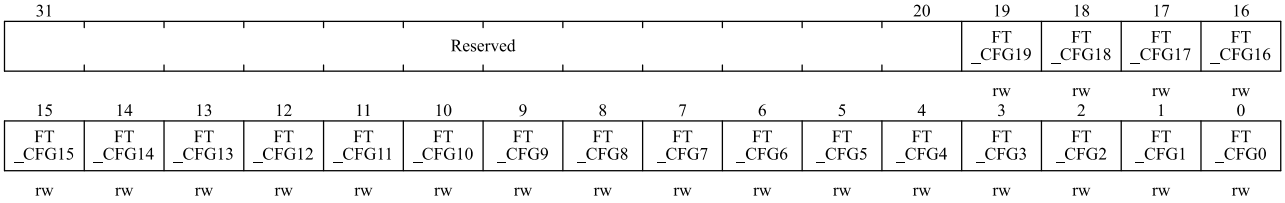
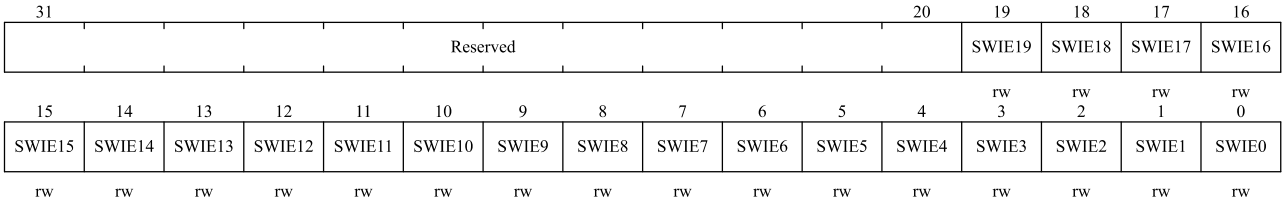


Bit Field	Name	Description
31:20	Reserved	Reserved,the reset value must be maintained.
19:0	FT_CFGx	The falling edge on line x triggers the configuration bit. (x is 0,1,2…19) 0: Disables falling edge trigger (interrupts and events) on input line x. 1: Enable falling edge trigger (interrupts and events) on input line x.

6.3.6 Software Interrupt Enable Register(EXTI_SWIE)

Address offset : 0x10

Reset value : 0x00000000



Bit Field	Name	Description
31:20	Reserved	Reserved,the reset value must be maintained.
19:0	SWIEx	Software interrupt on line x. (x is 0,1,2…19) When the bit is' 0 ', writing '1' sets the corresponding pending bit in EXTI_PEND. If this interrupt is allowed in EXTI_IMASK and EXTI_EMASK, an interrupt will be generated. *Note: this bit can be cleared to '0' by writing '1' to clear the corresponding bit of EXTI_PEND.*

6.3.7 Interrupt Request Pending Register(EXTI_PEND)

Address offset : 0x14

Reset value : 0x00000000

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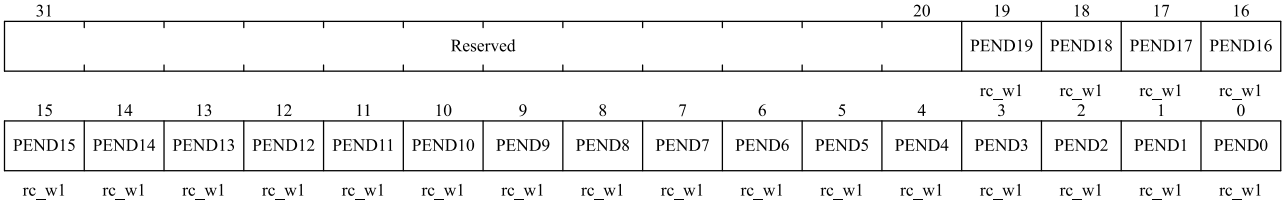

Bit Field	Name	Description
31:20	Reserved	Reserved,the reset value must be maintained.
19:0	PENDx	Pending bit on line x. (x is 0,1,2…19) 0: No pending request occurred. 1: A pending trigger request has occurred. This bit is set to '1' when a selected edge trigger event occurs on the external interrupt line. It can be cleared by writing '1' to the bit.

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7 CRC Calculation Unit

7.1 CRC Introduction

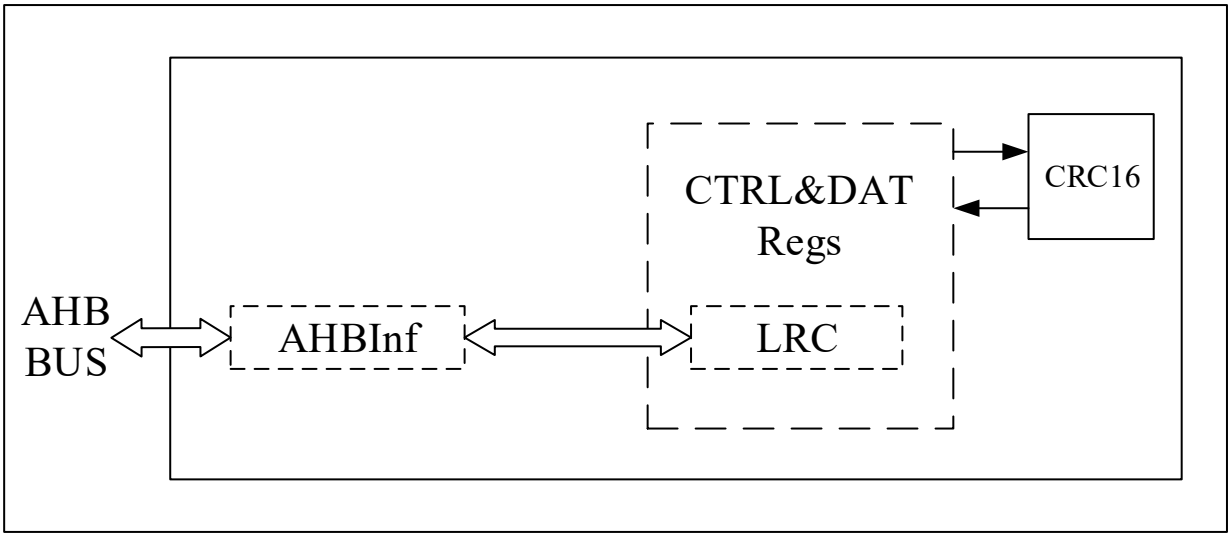
This module integrates the functions of CRC16, and the cyclic redundancy check (CRC) calculation unit obtains any CRC calculation result according to a fixed generator polynomial. In other applications, CRC technology is mainly used to verify the correctness and integrity of data transmission or data storage. CRC calculation unit can calculate the signature of the software during runtime, then compare it with the reference signature generated during linktime, and then store it in the specified memory space.

7.2 CRC Main Features

- CRC16($X^{16}+X^{15}+X^2+1$)
- There are 8 bits of data to be checked and 16 bits of output check code.
- CRC calculation time: 1 AHB clock cycle (HCLK)
- The verification initial value can be configured, and endianness of the data to be verified can be configured.
- Support 8bit LRC check value generation

The following figure is the block diagram of CRC unit.

Figure 7-1 CRC Calculation Unit Block Diagram



7.3 CRC Function Description

CRC_CRC16CTRL.ENDHL controls Little Endian format or Big Endian format.

To clear the result of the last CRC operation, set CRC_CRC16CTRL.CLR to 1 or CRC_CRC16D to 0.

The initial value of CRC calculation can be configured by writing the CRC_CRC16D register. By default, the initial value is the result of the last calculation.

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LRC calculation is the same as CRC calculation. Both are carried out at the same time. CRC or LRC can be read out depending on needs. If the initial value needs to be set, the LRC register should be configured first.

7.4 CRC Software Calculation Method

In practical applications, if software calculation CRC16 is needed to match the hardware calculation result, the following content needs to be correctly configured:

- WIDTH: 16
- POLY: 0x8005
- INIT: 0x0000
- XOROUT: 0x0000
- REFIN: No
- REFOUT: No

7.5 CRC Registers

7.5.1 CRC Register Overview

The following table lists the registers and reset values of CRC.

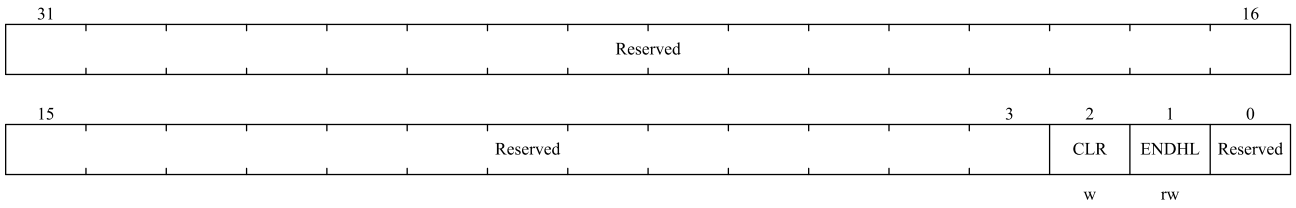
Table 7-1 CRC Register Overview

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
00Ch	CRC16CTRL	Reserved																													CLR	ENDHL	Reserved
	Reset Value																														0	0	
010h	CRC16DAT	Reserved																								CRC16DAT[7:0]							
	Reset Value																									0	0	0	0	0	0	0	0
014h	CRC16D	Reserved																CRC16D[15:0]															
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
018h	LRC	Reserved																								LRCDAT[7:0]							
	Reset Value																									0	0	0	0	0	0	0	0

7.5.2 CRC16 Control Register (CRC_CRC16CTRL)

Address offset: 0x0C

Reset value: 0x0000 0000



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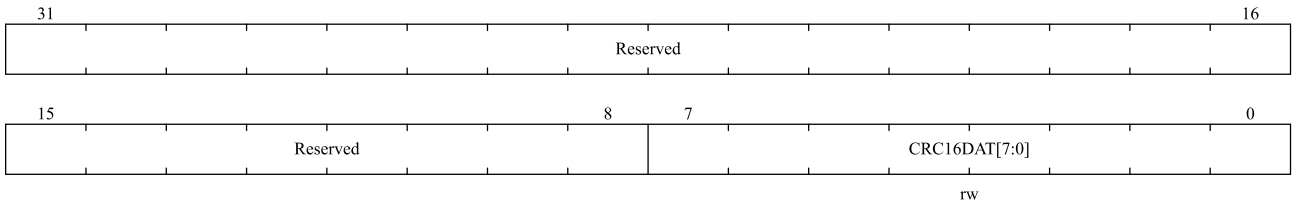
Bit Field	Name	Description
31:3	Reserved	Reserved,the reset value must be maintained
2	CLR	Clear CRC16 results. 0: Not clear. 1: Clear to default value 0x0000. Set this bit to 1 will only maintain 1 clock cycle, hardware will clear automatically. (Software read always 0).
1	ENDHL	Data to be verified start to calculate from MSB or LSB. 0: From MSB to LSB 1: From LSB to MSB This bit is only for data to be verified.
0	Reserved	Reserved,the reset value must be maintained

Note: 8-bits, 16-bits and 32-bits operations are supported.

7.5.3 CRC16 Input Data Register (CRC_CRC16DAT)

Address offset: 0x10

Reset value: 0x0000 0000



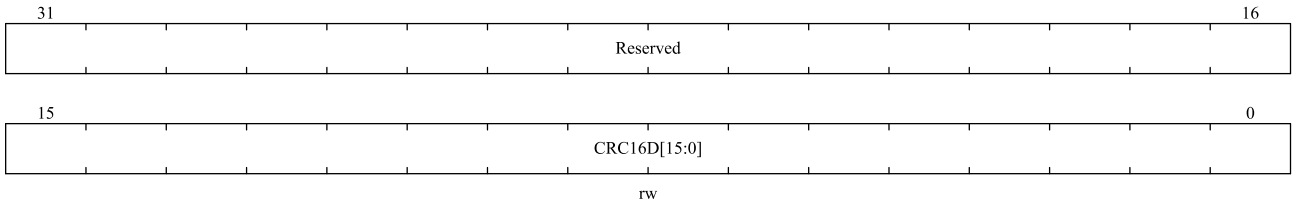
Bit Field	Name	Description
31:8	Reserved	Reserved,the reset value must be maintained
7:0	CRC16DAT[7:0]	Data to be verified.

Note: 8-bits, 16-bits and 32-bits operations are supported.

7.5.4 CRC Cyclic Redundancy Check Code Register (CRC_CRC16D)

Address offset: 0x14

Reset value: 0x0000 0000



Bit Field	Name	Description
31:16	Reserved	Reserved,the reset value must be maintained
15:0	CRC16D[15:0]	16-bit value of cyclic redundancy result data. Every time the software writes the CRC16DAT register, the 16-bit calculated data from

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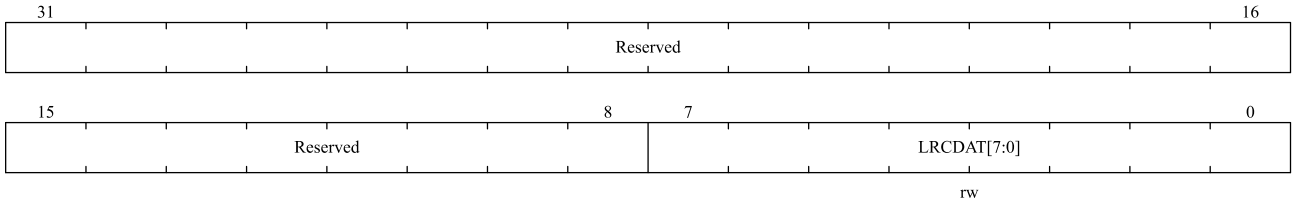
Bit Field	Name	Description
		CRC16 is updated in this register.

Note: 8-bits, 16-bits and 32-bits operations are supported (8-bit operations must be performed twice in a row to ensure that 16-bit initial values are configured properly)

7.5.5 LRC Result Register (CRC_LRC)

Address offset: 0x18

Reset value: 0x0000 0000



Bit Field	Name	Description
31:8	Reserved	Reserved,the reset value must be maintained
7:0	LRCDAT[7:0]	LRC check value register. Software needs to write initial value before usage. Each time data is written to CRC_CRC16DAT, it is "XOR" with the value of the CRC_LCR register. The result will be stored in CRC_LCR. Software reads the result. It should be cleared before next usage.

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8 Advanced-control Timer (TIM1)

8.1 TIM1 Introduction

The advanced-control timer (TIM1) is mainly used in the following scenarios: counting the input signal, measuring the pulse width of the input signals and generating the output waveforms, etc.

The advanced-control timer has complementary output functions with dead-time insertion and break function, which are suitable for motor control.

8.2 Main Features of TIM1

- 16-bit auto-reload counter. (It can realize up-counting, down-counting, up/down counting)
- 16-bit programmable prescaler. (The prescaler factor can be configured with any value between 1 and 65536)
- Programmable repetition counter
- Up to 5 channels.
- 4 capture/compare channels, the working modes are PWM output, ouput compare, one-pulse mode output, input capture.
- The events that generate the interrupt are as follows:
  - Update event
  - Trigger event
  - Input capture
  - Output compare
  - Break input
- Complementary outputs with programable dead-time
  - For TIM1, channel 1, 2, 3 support this feature
- Can be controlled by external signal
- Can be linked internally for timer synchronization or chaining
- TIM1_CC5 can be used for COMP blanking

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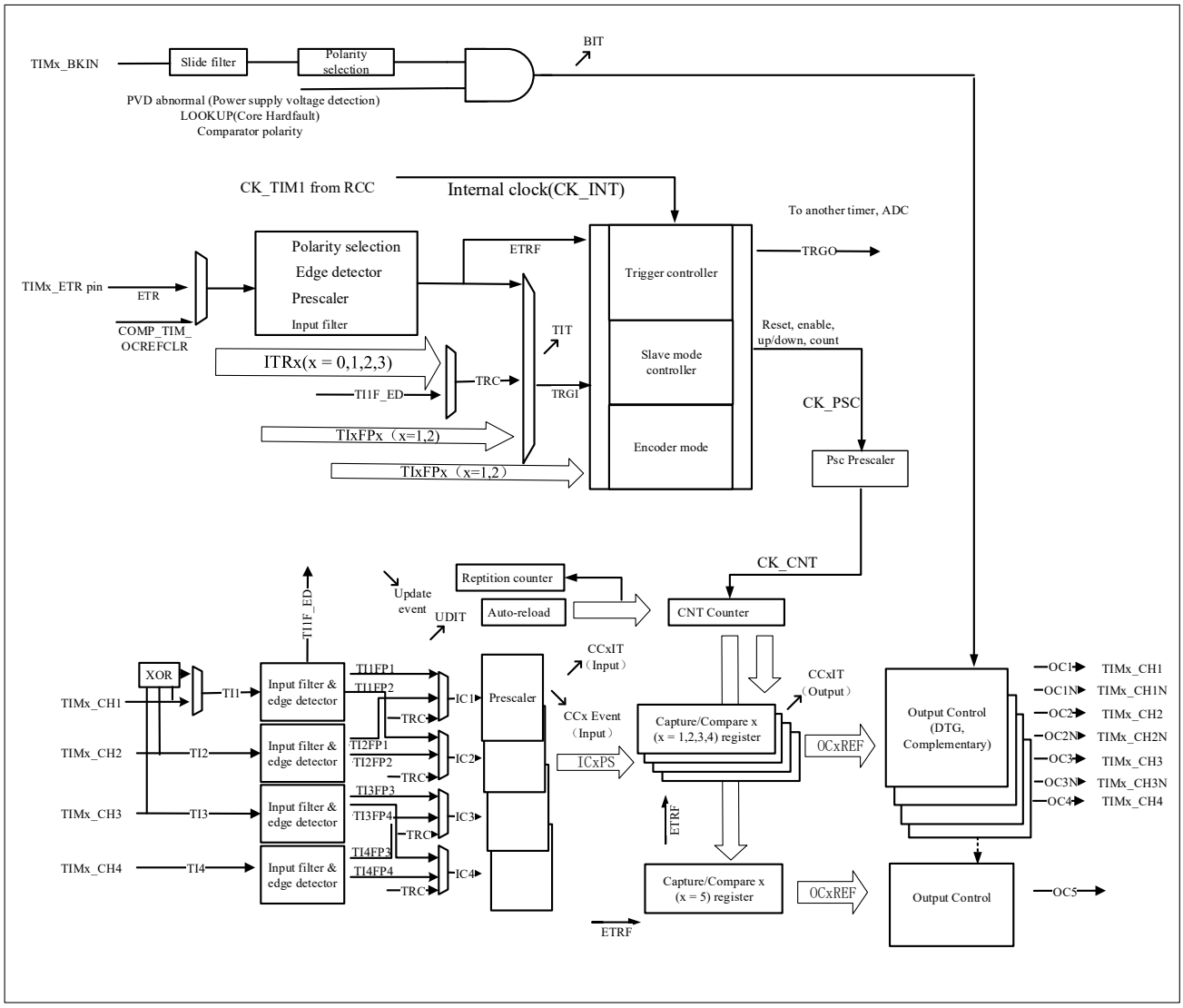
Figure 8-1 Block Diagram of TIM1



The capture channel 1 input can come from IOM or comparator output

8.3 TIM1 Function Description

8.3.1 Time-base Unit

The time-base unit of advanced-control timer mainly includes: prescaler, counter, auto-reload and repetition counter. When the time-base unit is operating, the software can read and write the corresponding registers (TIMx_PSC, TIMx_CNT, TIMx_AR and TIMx_REPCNT) at any time.

Depending on the setting of the auto-reload preload enable bit (TIMx_CTRL1.ARPEN), the value of the preload register is transferred to the shadow register immediately or at each update event UEV. An update event is generated when the counter reaches the overflow/underflow condition and it can be generated by software when TIMx_CTRL1.UPDIS = 0. The counter CK_CNT is valid only when the TIMx_CTRL1.CNTEN bit is set. The

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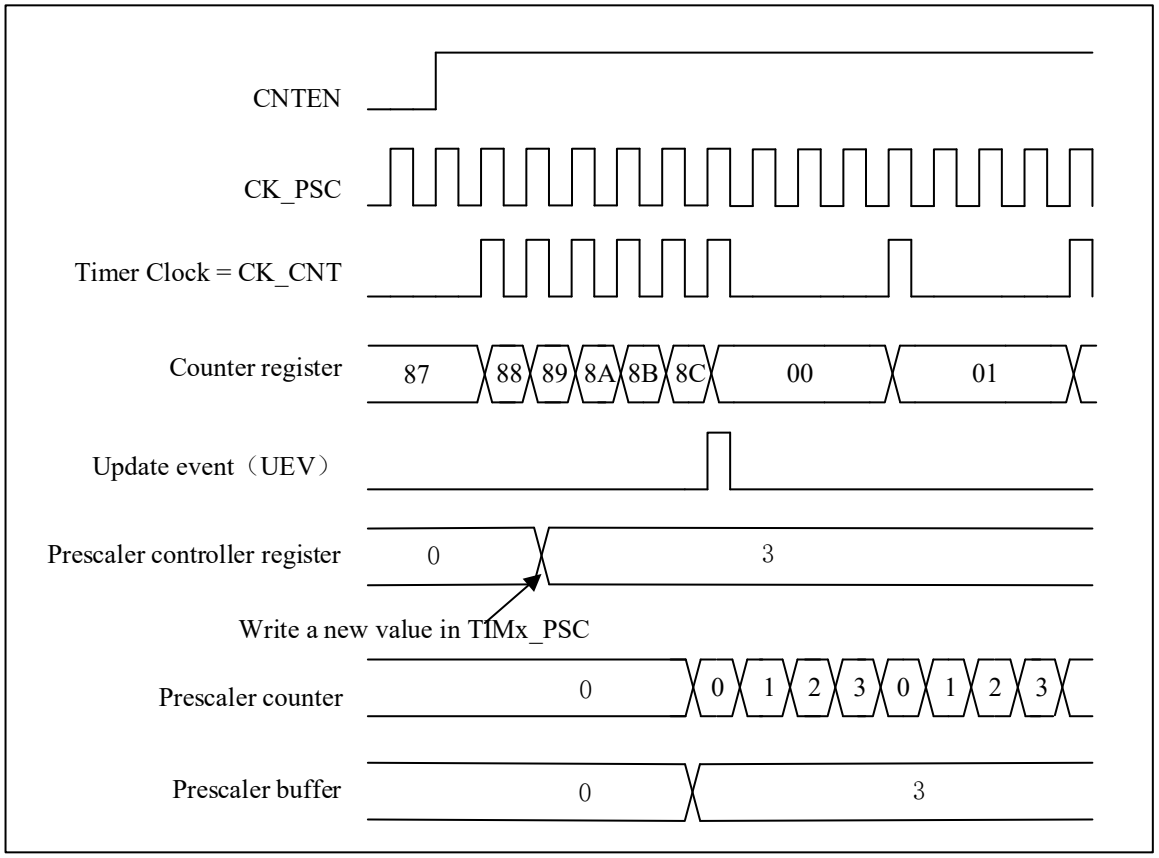
counter starts counting one clock cycle after the TIMx_CTRL1.CNTEN bit is set.

8.3.1.1 Prescaler description

The TIMx_PSC register consists of a 16-bit counter that can be used to divide the counter clock frequency by any factor between 1 and 65536. It can be changed on the fly as this buffer is buffered. The new prescaler value is only taken into account at the next update event.

Figure 8-2 Counter Timing Diagram with Prescaler Division Change from 1 to 4



8.3.2 Counter Mode

8.3.2.1 Up-counting mode

In up-counting mode, the counter will count from 0 to the value of the register TIMx_AR, then it resets to 0 and generate a counter overflow event.

If the TIMx_CTRL1.UPRS bit (select update request) and the TIMx_EVTGEN.UDGN bit are set, an update event (UEV) will be generated but without setting TIMx_STS.UDITF by hardware, thus no update interrupts or DMA requests will be generated. This is to avoid generating both update and capture interrupts when clearing the counter on the capture event.

Depending on the update request source configured in the TIMx_CTRL1.UPRS, when an update event occurs, all registers are updated and the TIMx_STS.UDITF is set:

- The repetition counter reloads the content of the TIMx_REPCNT
- Update auto-reload shadow register with preload value(TIMx_AR), when TIMx_CTRL1.ARPEN = 1.

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- The prescaler shadow register is reloaded with the preload value(TIMx_PSC).

To avoid updating the shadow registers when new values are written to the preload registers, the UEV event can be disabled by setting TIMx_CTRL1.UPDIS=1.

When an update event occurs, the counter will still be cleared and the prescaler counter will also be set to 0 (but the prescaler value will remain unchanged).

The figure below shows some examples of the counter behavior and the update flags for different division factors in the up-counting mode.

Figure 8-3 Timing Diagram Of Up-counting. The Internal Clock Divider Factor = 2/N

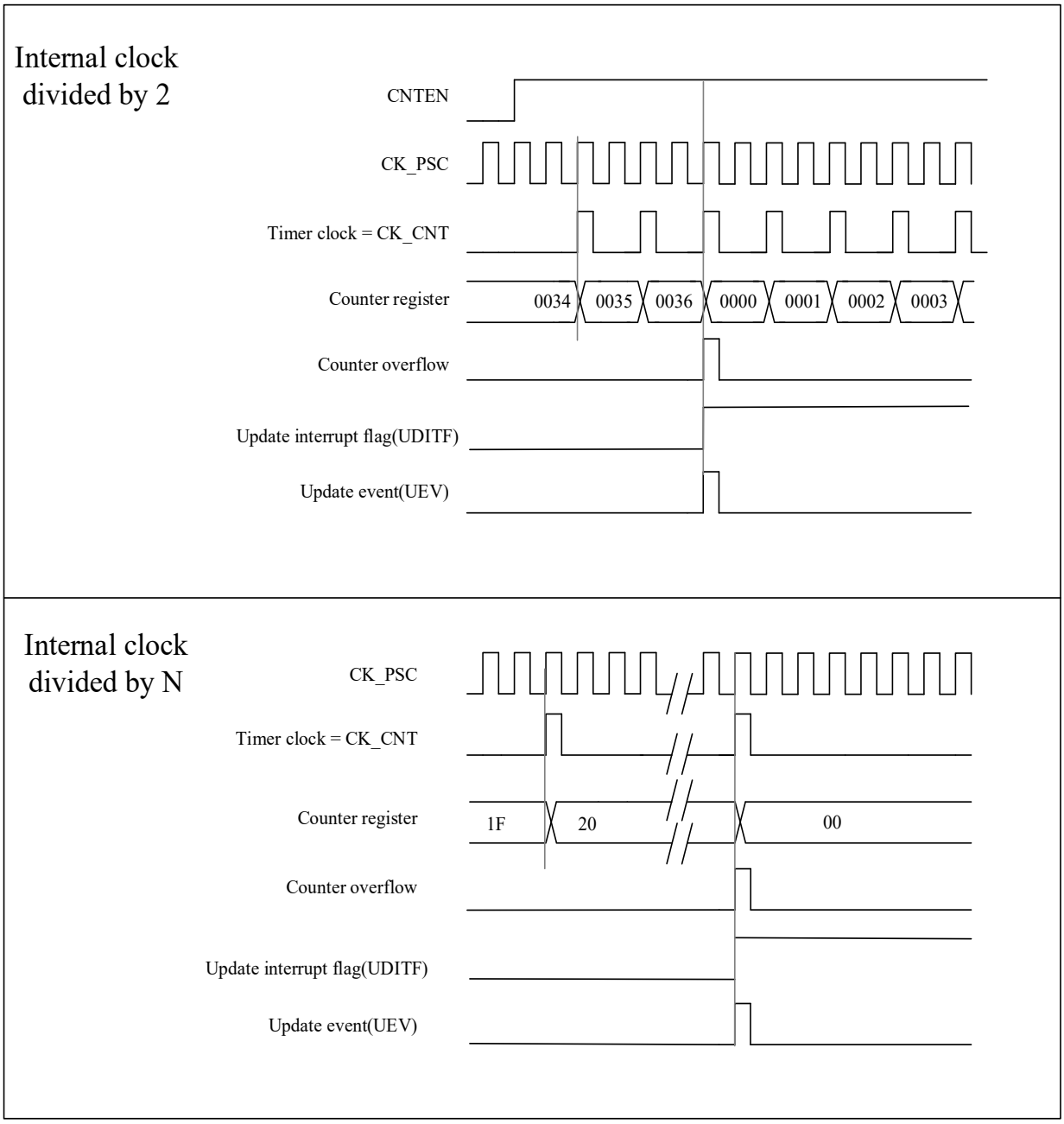

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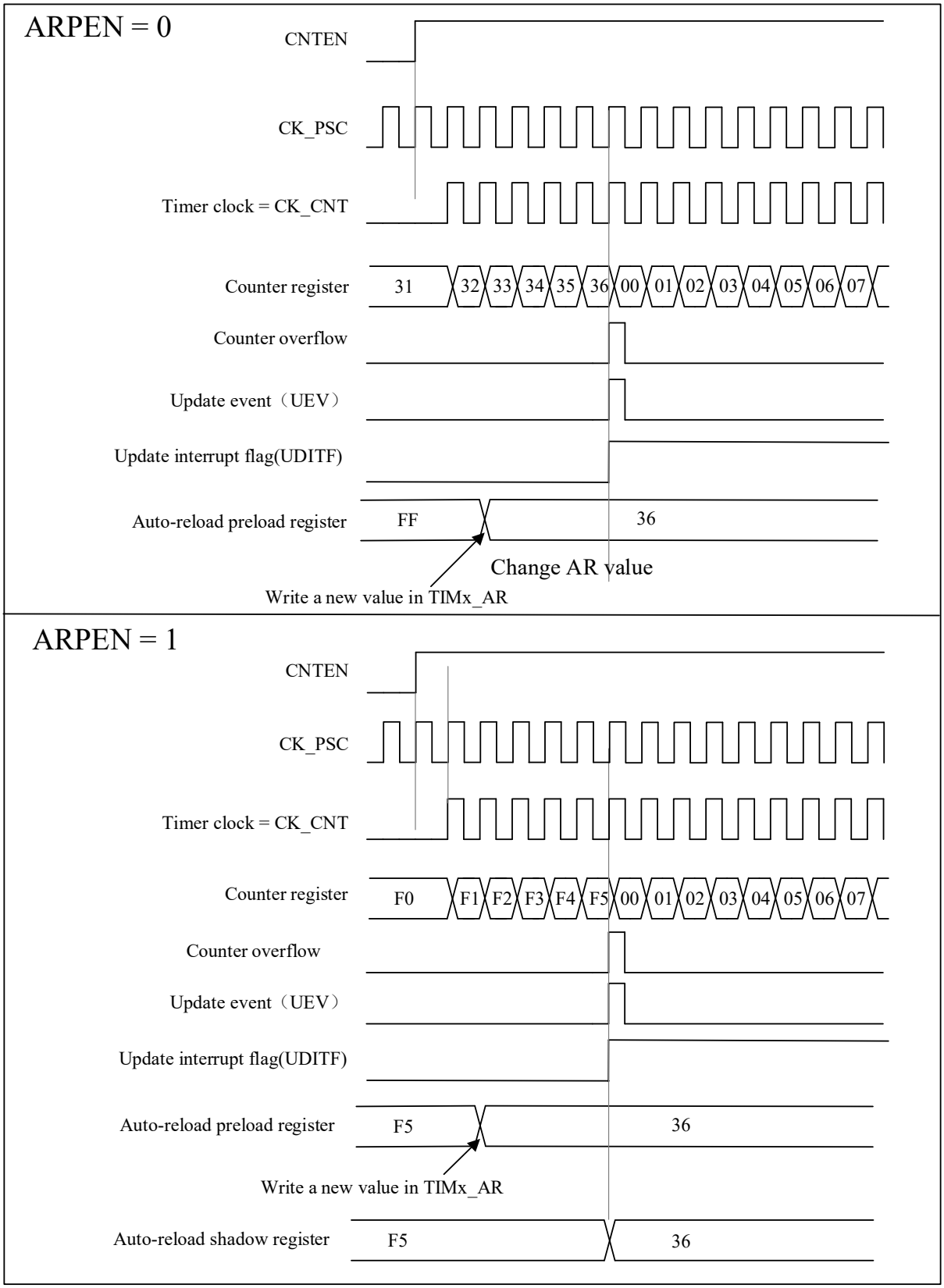
Figure 8-4 Timing Diagram of the Up-counting, Update Event when ARPEN=0/1



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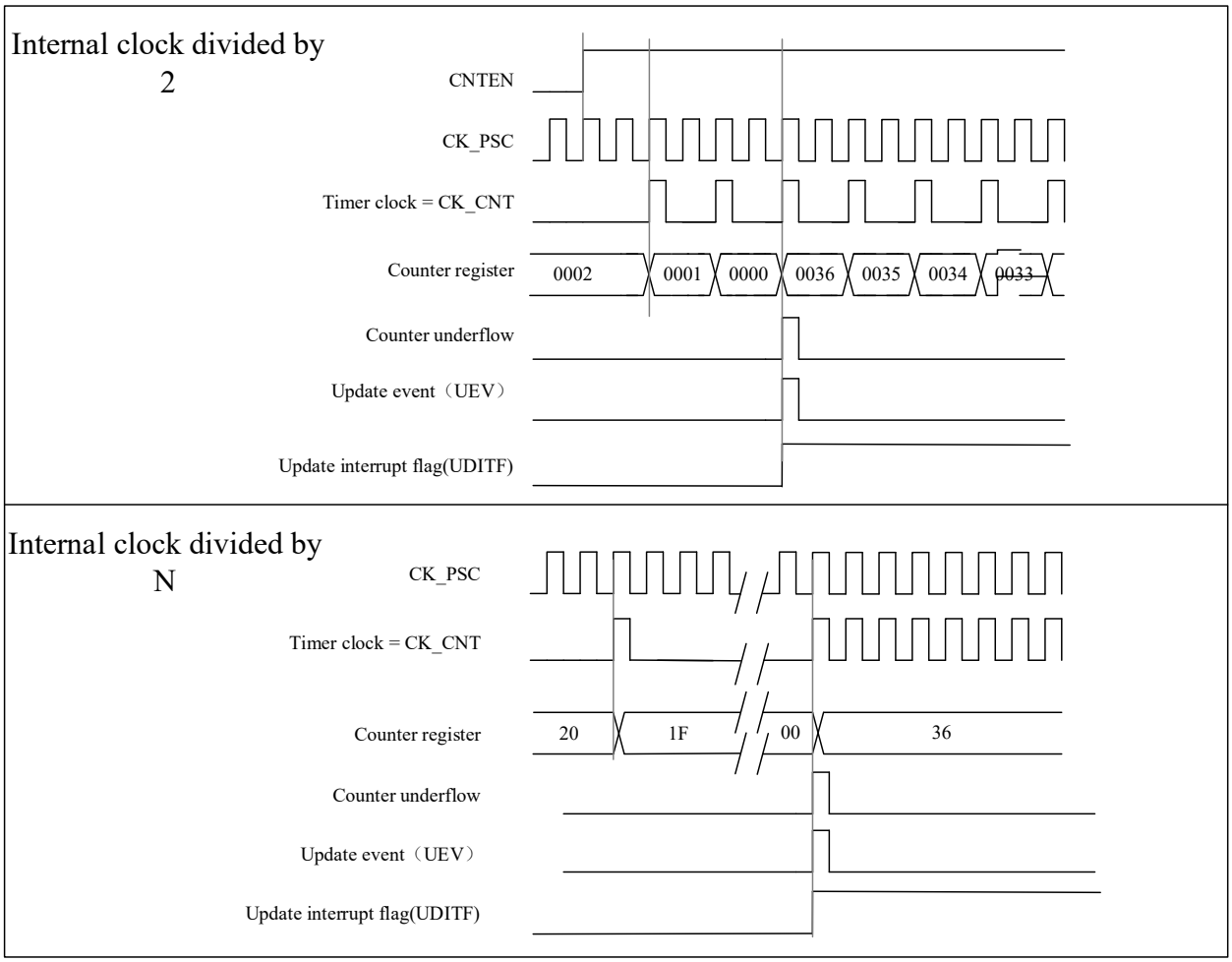
8.3.2.2 Down-counting mode

In down-counting mode, the counter decrements from the value of the register TIMx_AR to 0, then restarts from the auto-reload value and generates a counter underflow event.

The process of configuring update events and updating registers in down-counting mode is the same as in up-counting mode, refer to Section 8.3.2.1.

The figure below shows some examples of the counter behavior and the update flags for different division factors in the down-counting mode.

Figure 8-5 Timing Diagram of the Down-counting, Internal Clock Divided Factor = 2/N



8.3.2.3 Center-aligned mode

In center-aligned mode, the counter increments from 0 to the value (TIMx_AR) – 1 and generates a counter overflow event, then counts down from the auto-reload value (TIMx_AR) to 1 and generates a counter underflow event. Then the counter resets to 0 and starts counting up again.

In this mode, the TIMx_CTRL1.DIR direction bits have no effect and the count direction is updated and specified by hardware. Center-aligned mode is active when the TIMx_CTRL1. CAMSEL bit is not equal to "00".

An update event can be generated each time the counter overflows and underflows. Alternatively, an update event can also be generated by setting the TIMx_EVTGEN. UDGN bit (either by software or using a slave mode controller).

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In this case, the counter restarts from 0, and the prescaler counter also restarts from 0.

Note that if the update source is a counter overflow, the auto-reload is updated before reloading the counter.

Figure 8-6 Timing Diagram of the Center-aligned, Internal Clock Divided Factor =2/N

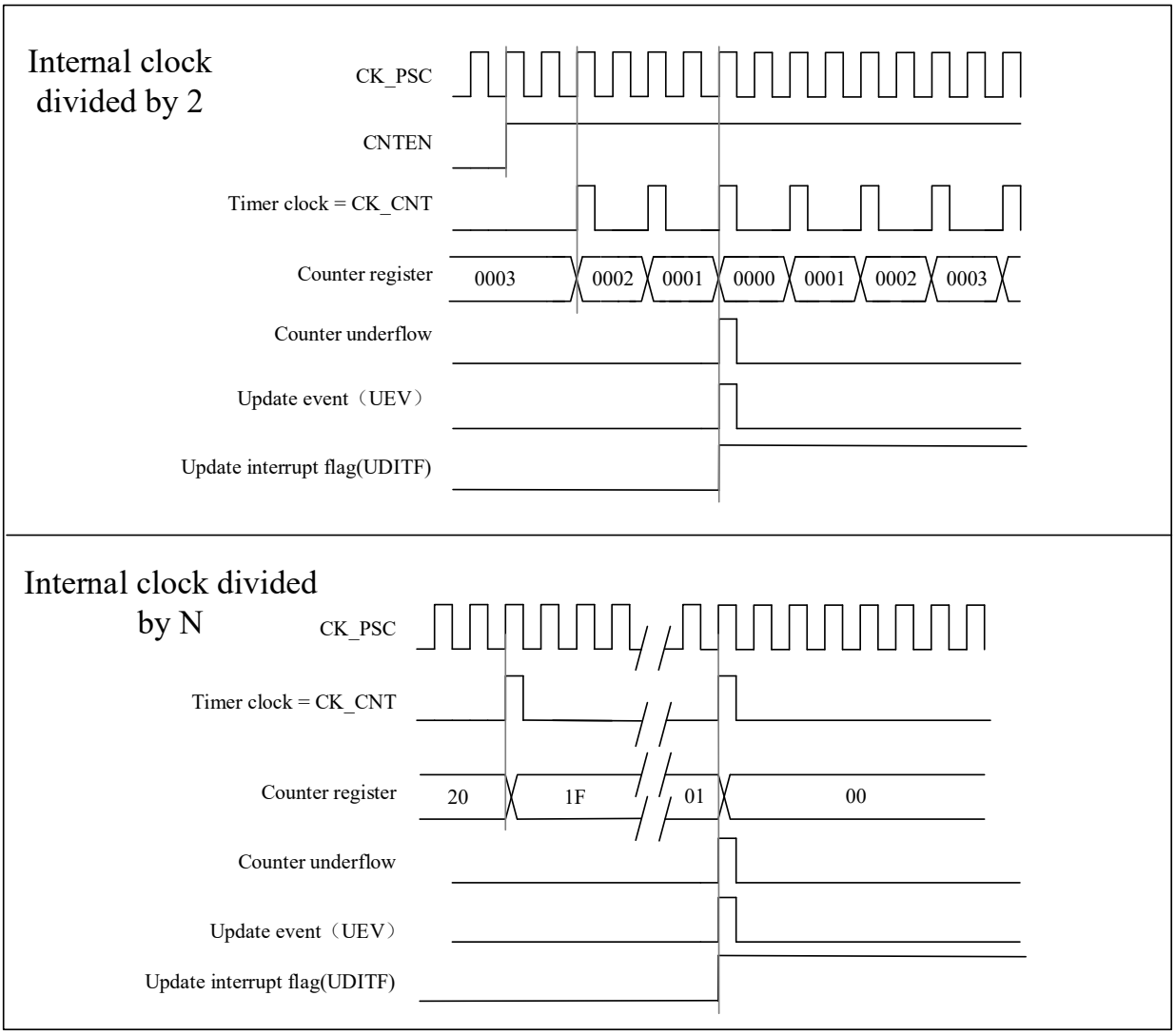

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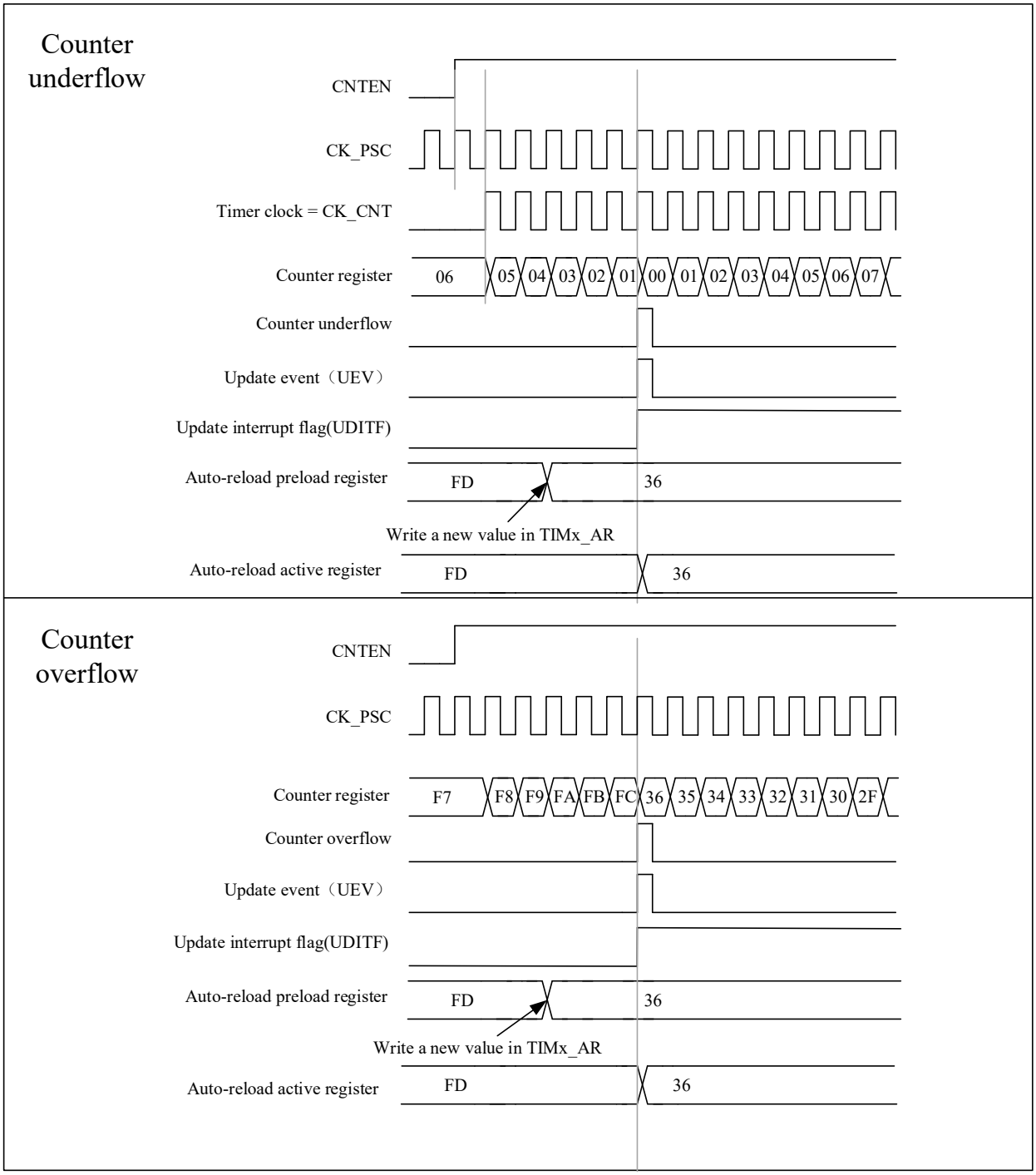
Figure 8-7 Center-Aligned Sequence Diagram Including Counter Overflows and Underflows (ARPEN = 1)



8.3.2.4 Repetition Counter

The time-base unit of Section 8.3.1 describes the conditions for generating an update event (UEV). An update event (UEV) is actually generated only when the repetition counter reaches zero, which is usefull for generating PWM signals.

This means that data is transferred from the preload registers to the shadow registers every N+1 counter overflows or underflows, where N is the value in the TIMx_REPCNT.

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The repetition counter is decremented:

- In the up-counting mode, each time the counter reaches the maximum value, an overflow occurs.
- In down-counting mode, each time the counter decrements to the minimum value, an underflow occurs.
- In center-aligned mode, each time the counter overflows or underflows.

Its repetition rate is defined by the value of the TIMx_REPCNT register.

Repetition counter features automatic reloading. The update event (generated by setting TIMx_EVTGEN.UDGN or hardware through slave mode controller) occurs immediately, regardless of the value of the repetition counter.

Figure 8-8 Repeat Count Sequence Diagram in Down-counting Mode

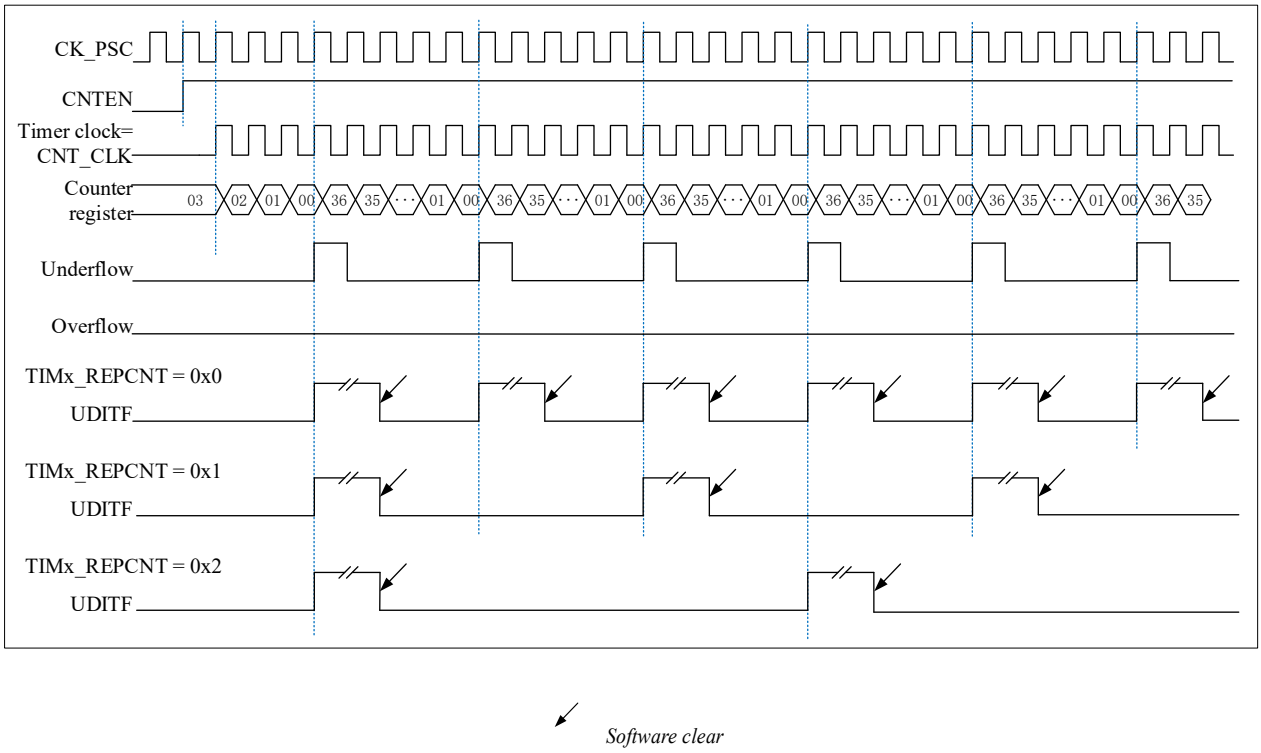

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Figure 8-9 Repeat Count Sequence Diagram in Up-counting Mode

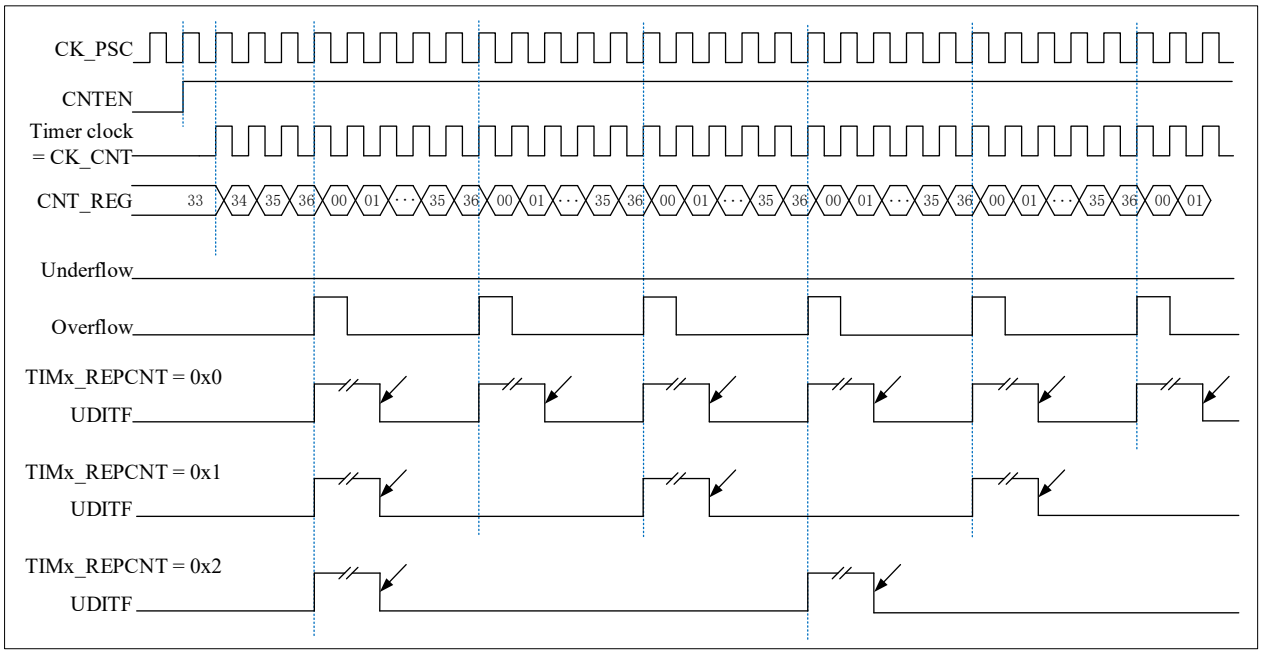
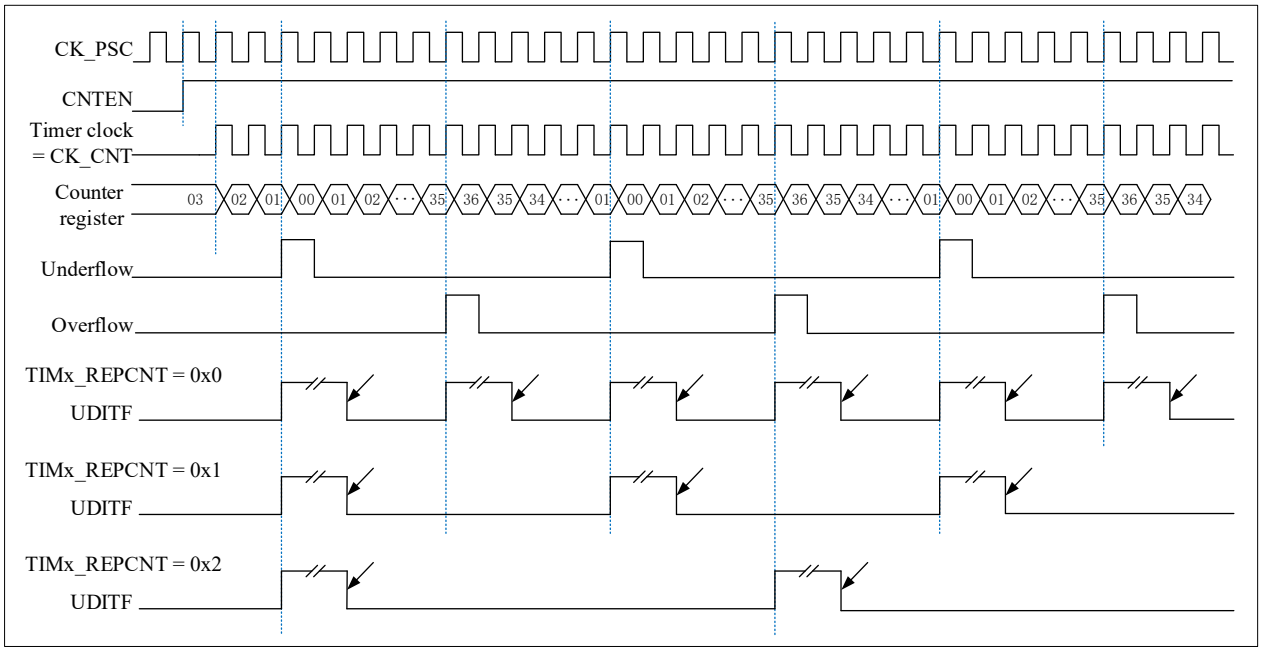


Figure 8-10 Repeat Count Sequence Diagram in Center-aligned Mode



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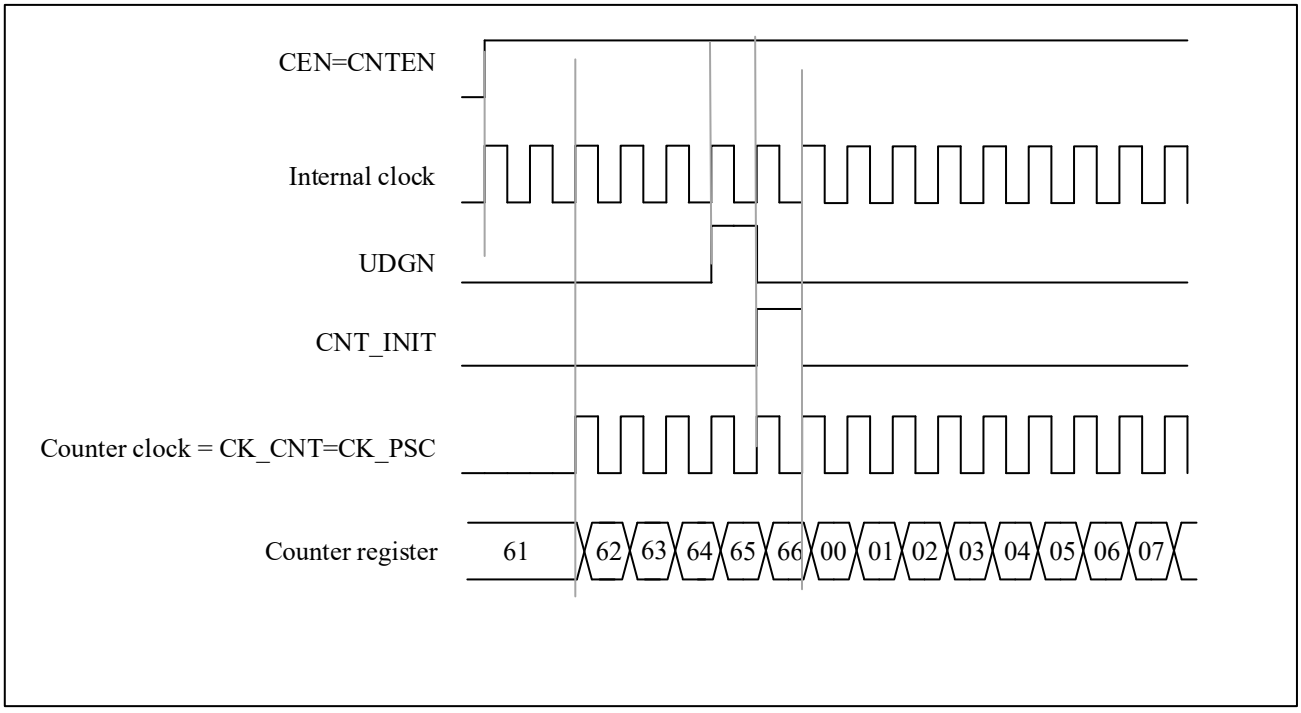
8.3.3 Clock Selection

- The internal clock of advanced-control timer: CK_INT
- Two kinds of external clock mode:
  - external input pin
  - external trigger input ETR
- Internal trigger input (ITRx): one timer is used as a prescaler for another timer.

8.3.3.1 Internal clock source (CK_INT)

When the TIMx_SMCTRL.SMSEL is equal to “000”, the slave mode controller is disabled. The three control bits (TIMx_CTRL1.CNTEN, TIMx_CTRL1.DIR, TIMx_EVTGEN.UDGN) can only be changed by software (except TIMx_EVTGEN.UDGN, which remains cleared automatically). As soon as the TIMx_CTRL1.CNTEN bit is written as '1' by software, the prescaler is clocked by the internal clock CK_INT.

Figure 8-11 Control Circuit in Normal Mode, Internal Clock Divided by 1



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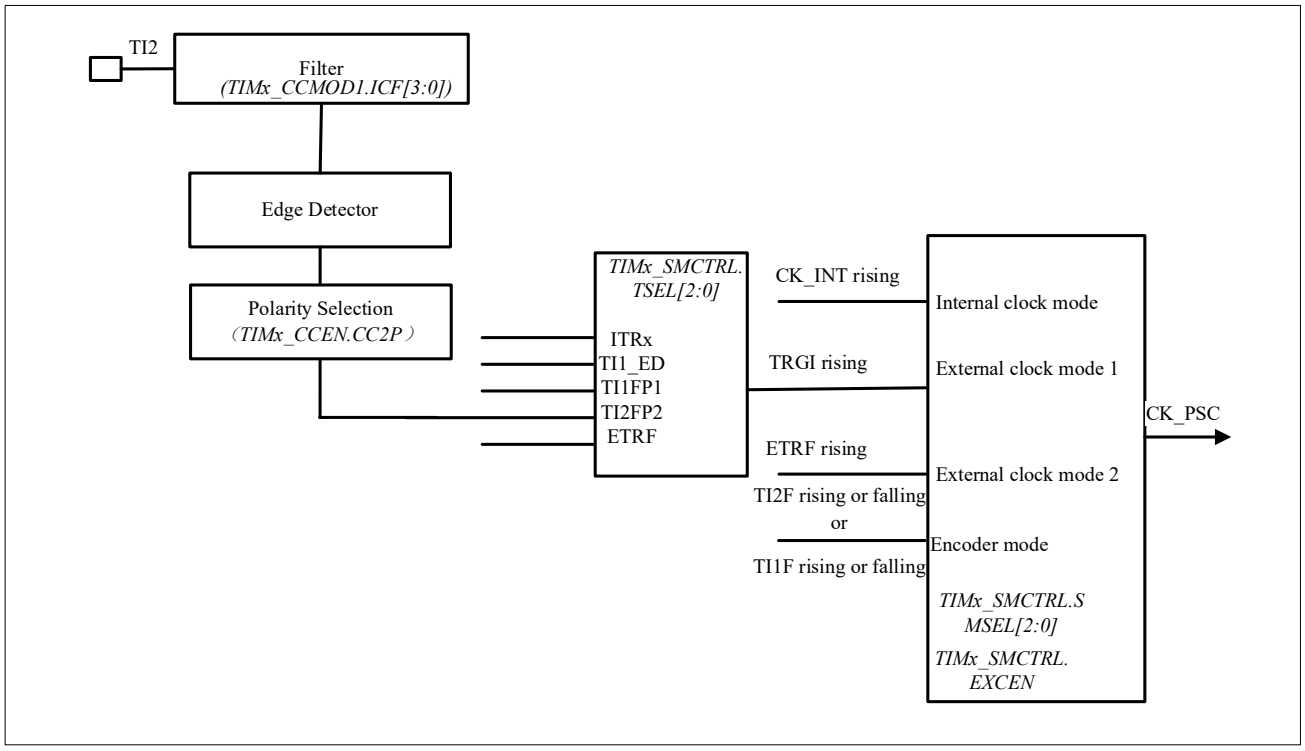
8.3.3.2 External clock source mode 1

Figure 8-12 TI2 External Clock Connection Example



This mode is selected by configuring TIMx_SMCTRL.SMSEL = 111. The counter can be configured to count on the rising or falling edge of the clock at the selected input.

For example, to configure up-counting mode to count on the rising edge of the clock at the TI2 input, the configuration steps are as follows:

- Configure TIMx_CCMOD1.CC2SEL to '01' to configure CC2 channel as input, and mapping IC2 to TI2
- Configure TIMx_CCEN.CC2P to '0' to select clock rising edge polarity
- Configure TIMx_CCMOD1.IC2F[3:0] (if filter is not needed, keep IC2F bit at '0000') to select input filter bandwidth
- Configure TIMx_SMCTRL.SMSEL to '111' to select timer external clock mode 1
- Configure TIMx_SMCTRL.TSEL to '110' to select TI2 as the trigger input source
- Configure TIMx_CTRL1.CNTEN to '1' to start the counter

Note: the capture prescaler is not used for triggering, so it does not need to be configured

When the rising edge of the timer clock occurs at TI2 = 1, the counter counts once and the TIMx_STS .TITF flag isset.

The delay between the rising edge of TI2 and the actual clock of the counter depends on the resynchronization circuit at the input of TI2.

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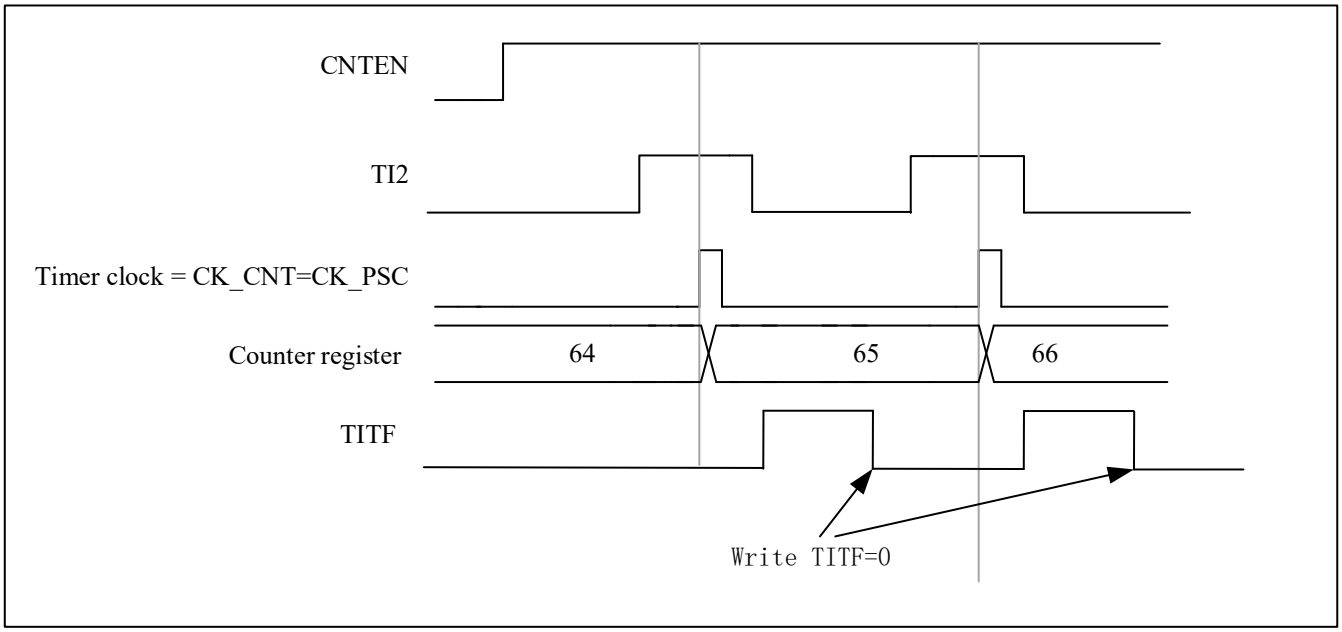
Figure 8-13 Control Circuit in External Clock Mode 1

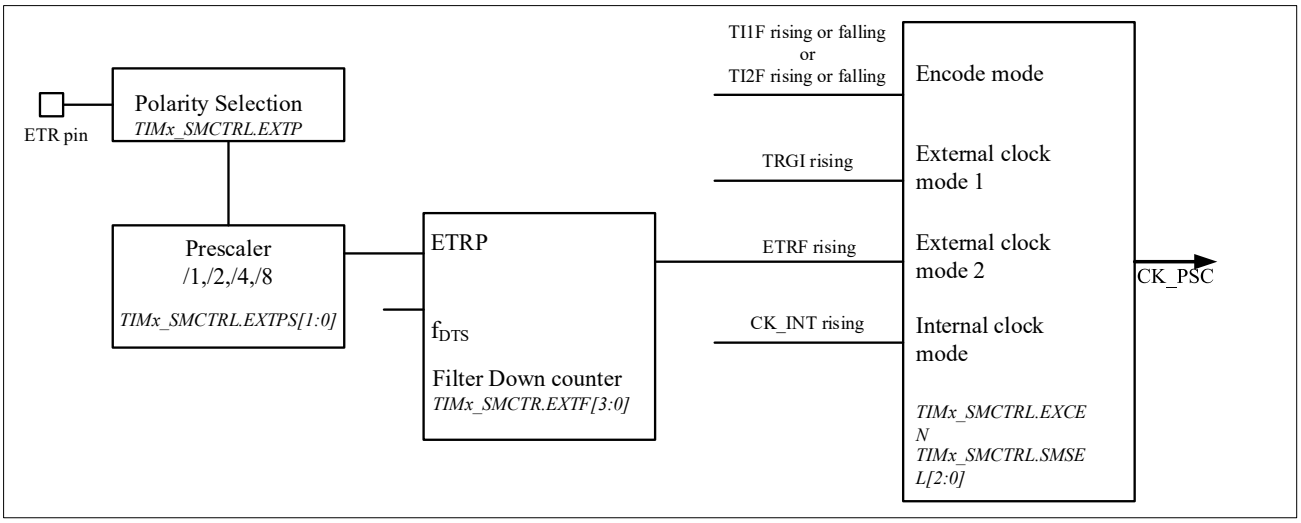


8.3.3.3 External clock source mode 2

This mode is selected by TIMx_SMCTRL .EXCEN equal to 1. The counter can count on every rising or falling edge of the external trigger input ETR.

The following figure is a schematic diagram of the external trigger input module in external clock source mode 2

Figure 8-14 External Trigger Input Block Diagram



For example, to configure the up counter to count every 2 rising edges on ETR, use the following procedure:

- Since no filter is needed in this case, write TIMx_SMCTRL.EXTF[3:0] to '0000'
- Configure the prescaler by writing TIMx_SMCTRL.EXTPS[1:0] to '01'
- Select the polarity of rising edge on ETR pin by setting TIMx_SMCTRL.EXTP to '0'

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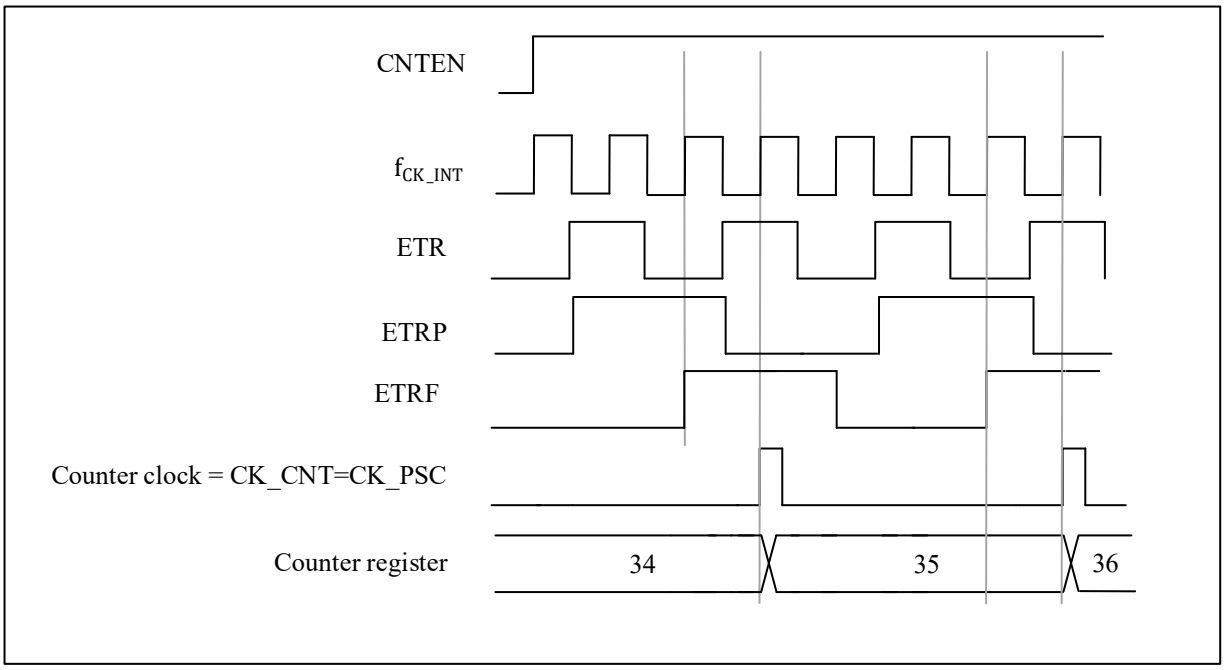
- External clock mode 2 is selected by setting TIMx_SMCTRL .EXCEN to '1'
- Turn on the counter by setting TIMx_CTRL1. CNTEN to '1'

The counter counts every 2 rising edges of ETR. The delay between the rising edge of ETR and the actual clock of the counter is due to a resynchronization circuit on the ETRP signal.

Figure 8-15 Control Circuit in External Clock Mode 2



8.3.4 Capture/Compare Channels

The capture/compare channels include a capture/compare register and a shadow register. The input stage consists of digital filter, multiplexer and prescaler. The output stage includes comparator and output control.

The input signal TIx is sampled and filtered to generate the signal TIxF. A signal (TIxF_rising or TIxF_falling) is then generated by the edge detector with the polarity select function, the polarity of which is selected by the TIMx_CCEN.CCxP bit. This signal can be used as a trigger input for the slave mode controller. At the same time, the signal ICx is sent to the capture register after frequency division. The following figure shows a block diagram of a capture/compare channel.

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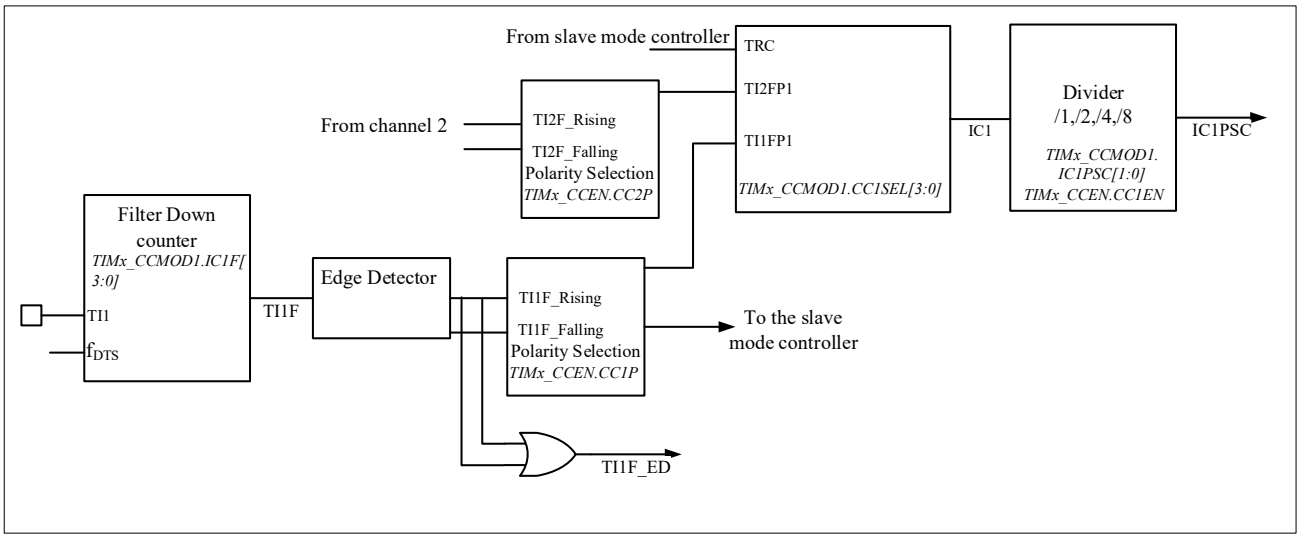
Figure 8-16 Capture/Compare Channel (Example: Channel 1 Input Stage)



The output stage generates an intermediate waveform OCxRef (active high) as reference. The polarity acts at the end of the chain.

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Figure 8-17 Capture/Compare Channel 1 Main Circuit

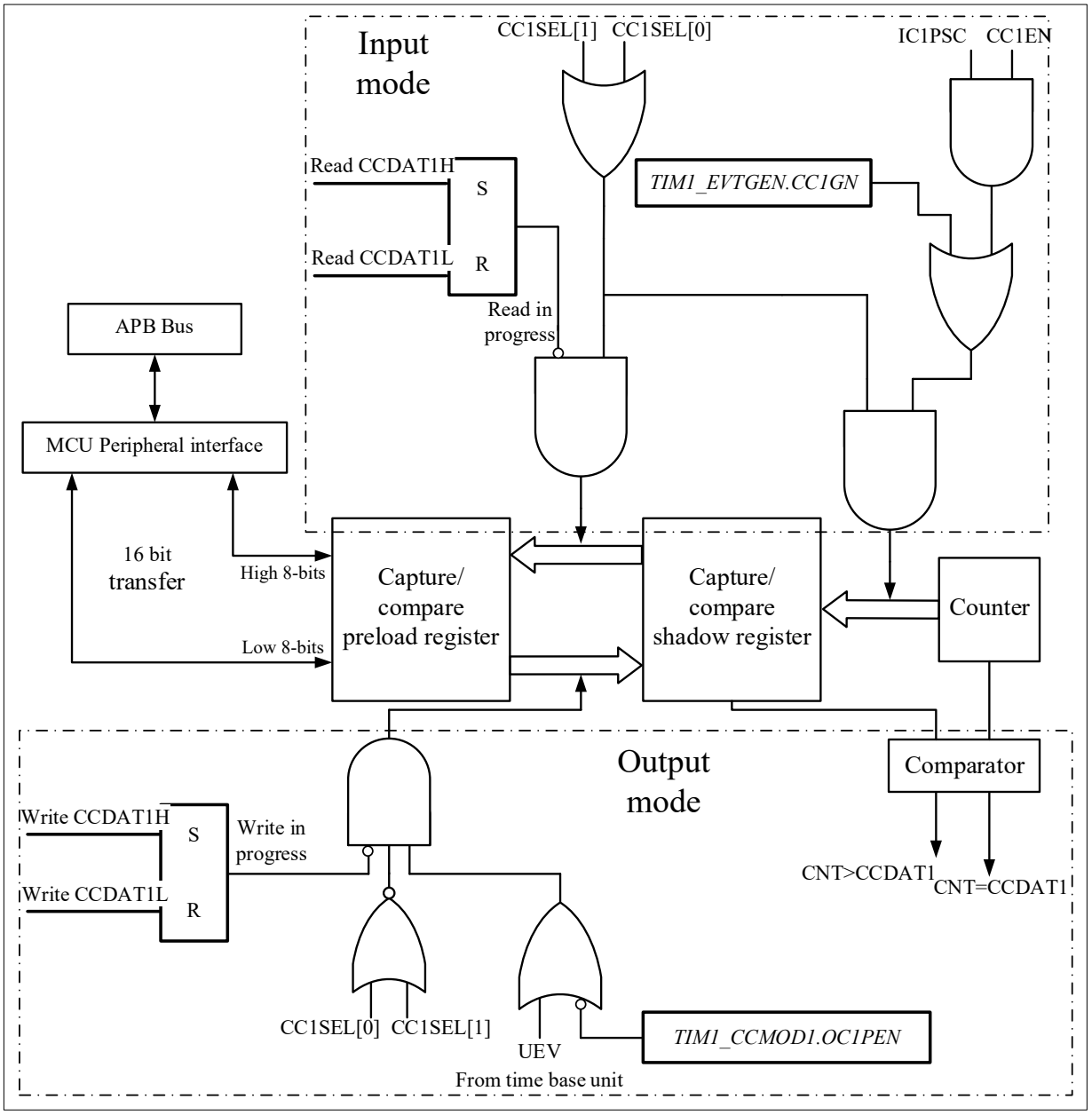

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Figure 8-18 Output Part of Channelx (x= 1,2,3, Take Channel 1 as Example)

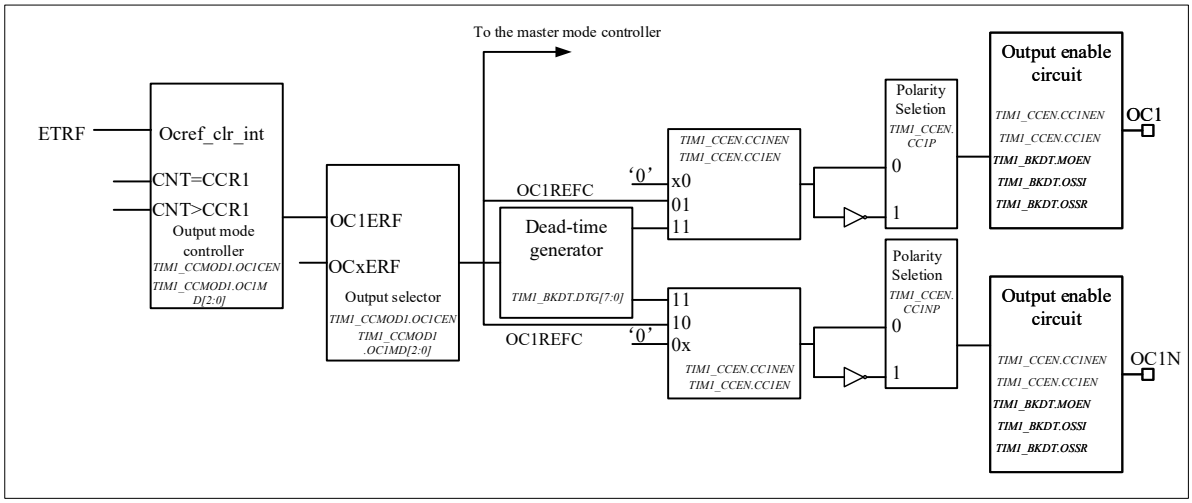
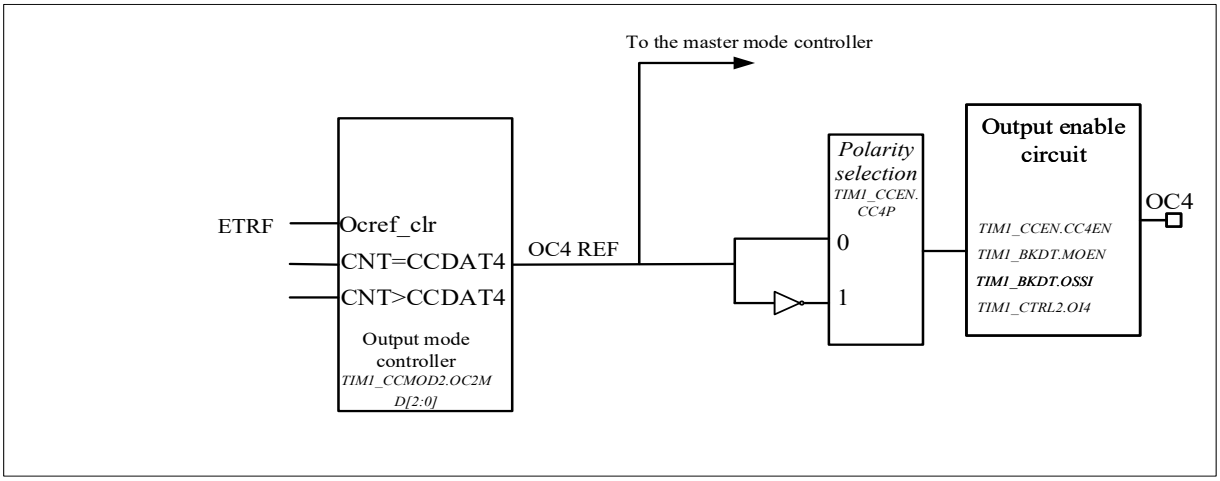


Figure 8-19 Output Part of Channelx (x= 4)



Read and write always access the preload registers when capturing/comparing. The two specific working processes are as follows:

In capture mode, the capture is actually done in the shadow register, and then the value in the shadow register is copied into the preload register.

In compare mode, as opposed to capture mode, the value of the preload register is copied into the shadow register, which is compared with the counter.

8.3.5 Input Capture Mode

In input capture mode, the TIMx_CCDATx registers are used to latch the counter value after the ICx signal is detected.

There is a capture interrupt flag TIMx_STS.CCxITF, which can trigger an interrupt if the corresponding interrupt enable is pulled high.

The TIMx_STS. CCxITF bit is set by hardware when a capture event occurs and is cleared by software or by reading the TIMx_CCDATx register.

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The over-capture flag TIMx_STS.CCxOCF is set when the counter value is captured in the TIMx_CCDATx register and TIMx_STS.CC1ITF is already pulled high. Unlike the former, TIMx_STS.CCxOCF is cleared by writing 0 to it.

To achieve a rising edge of the TI1 input to capture the counter value into the TIMx_CCDAT1 register, the configuration flow is as follows:

- Select a valid input:

  Configure TIMx_CCMOD1.CC1SEL to '01'. At this time, the input is the CC1 channel, and IC1 is mapped to TI1.

- Define the input filter duration required for programming:

  Define the sampling frequency of the TI1 input and the length of the digital filter by configuring the TIMx_CCMODx.ICxF bits. Example: If the input signal jitters up to 5 internal clock cycles, we must choose a filter duration longer than these 5 clock cycles. When 8 consecutive samples (sampled at f_{DTS} frequency) with the new level are detected, we can validate the transition on TI1. Then configure TIMx_CCMOD1.IC1F to '0011'.

- By configuring TIMx_CCEN.CC1P = 0, select the rising edge as the valid transition polarity on the TI1 channel.
- Configure the input prescaler. In this example, configure TIMx_CCMOD1.IC1PSC= '00' to disable the prescaler because we want to capture every valid transition.
- Enable capture by configuring TIMx_CCEN.CC1EN = '1'.

If needed, enable the related interrupt request by setting the TIMx_DINTEN.CC1IEN.

8.3.6 PWM Input Mode

There are some differences between PWM input mode and normal input capture mode, including:

- Two ICx signals are mapped to the same TIx input.
- The two ICx signals are active on edges of opposite polarity.
- Select one of two TIxFP signals as trigger input.
- The slave mode controller is configured in reset mode.

For example, the following configuration flow can be used to know the period and duty cycle of the PWM signal on TI1 (It depends on the frequency of CK_INT and the value of the prescaler).

- Configure TIMx_CCMOD1.CC1SEL to '01' to select TI1 as valid input for TIMx_CCDAT1.
- Configure TIMx_CCEN.CC1P to '0' to select the active polarity of filtered timer input 1(TI1FP1) (active on the rising edge).
- Configure TIMx_CCMOD1.CC2SEL to '10' to select TI1 as valid input for TIMx_CCDAT2.
- Configure TIMx_CCEN.CC2P to '1' to select the valid polarity of filtered timer input 2(TI1FP2) (active on the falling edge).
- Configure TIMx_SMCTRL.TSEL = 101 to select filtered timer input 1 (TI1FP1) as valid trigger input.
- Configure TIMx_SMCTRL.SMSEL = 100 to configure the slave mode controller to reset mode.
- Configure TIMx_CCEN.CC1EN = 1 and TIMx_CCEN.CC2EN=1 to enable capture.

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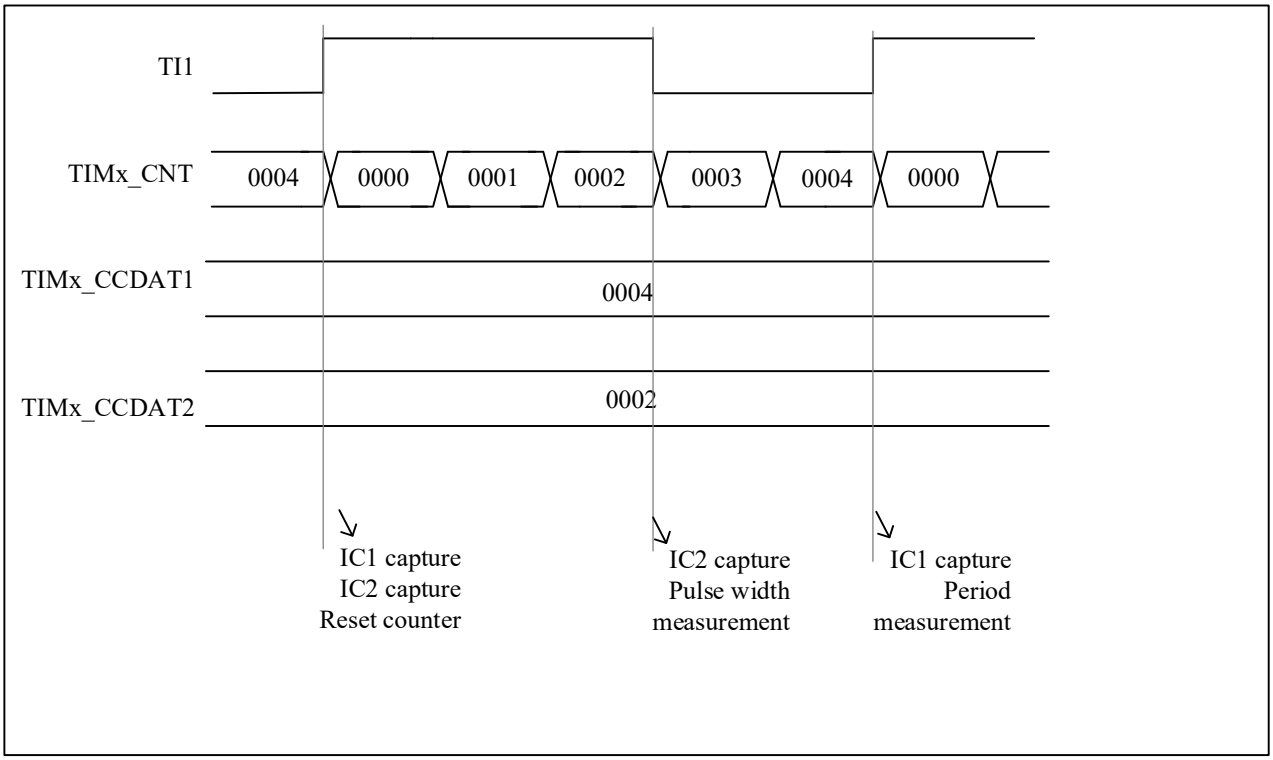
Figure 8-20 PWM Input Mode Timing



Because only filter timer input 1 (TI1FP1) and filter timer input 2 (TI2FP2) are connected to the slave mode controller, the PWM input mode can only be used with the TIMx_CH1/TIMx_CH2 signals.

8.3.7 Forced Output Mode

In output mode (TIMx_CCMODx.CCxSEL = 00), software can force output compare signals to active or inactive level directly.

User can set TIMx_CCMODx.OCxMD = 101 to force the output compare signal to active level. And the OCxREF will be forced high, OCx get opposite value to CCxP polarity bit. On the other hand, user can set TIMx_CCMODx.OCxMD=100 to force the output compare signal to low level.

The values of the TIMx_CCDATx shadow register and the counter still comparing with each other in this mode.

The comparison between the output compare register TIMx_CCDATx and the counter TIMx_CNT has no effect on OCxREF. And the flag still can be set. Therefore, the interrupt still can be sent.

8.3.8 Output Compare Mode

User can use this mode to control the output waveform, or to indicate that a period of time has elapsed.

When the capture/compare register and the counter have the same value, the output compare function's operations are as follow:

- TIMx_CCMODx.OCxMD is for output compare mode, and TIMx_CCEN.CCxP is for output polarity. When the compare matches, if TIMx_CCMODx.OCxMD = 000, the output pin will keep its level; if TIMx_CCMODx.OCxMD = 001, the output pin will be set active; if set TIMx_CCMODx.OCxMD = 010, the output pin will be set inactive; if set TIMx_CCMODx.OCxMD = 011, the output pin will be set to toggle.

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- Set a flag in interrupt status register TIMx_STS.CCxITF.
- If user set TIMx_DINTEN.CCxIEN, a corresponding interrupt will be generated.

User can set TIMx_CCMODx.OCxPEN to choose capture/compare shawdow register using capture/compare preload registers(TIMx_CCDATx).

The time resolution is one count of the counter.

In one-pulse mode, the output compare mode can also be used to output a single pulse.

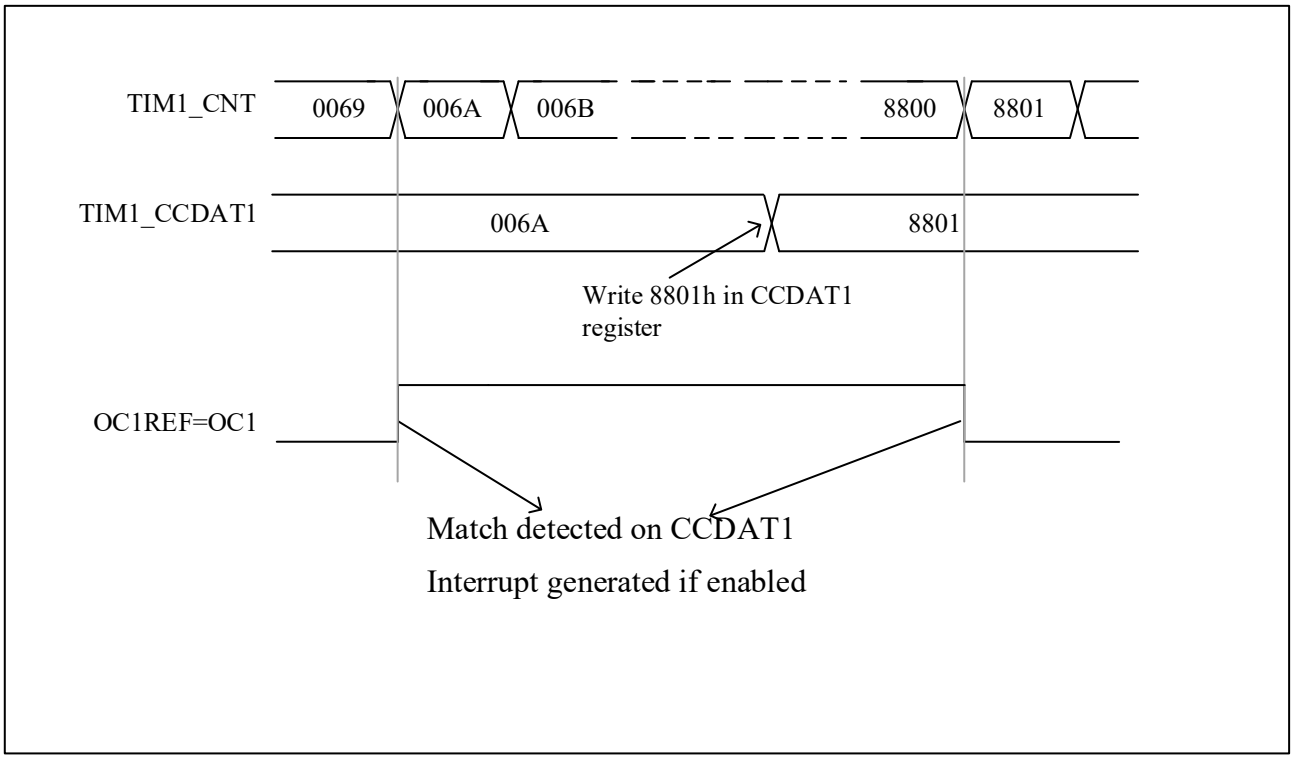
Here are the configuration steps for output compare mode:

- First of all, user should select the counter clock.
- Secondly, set TIMx_AR and TIMx_CCDATx with desired data.
- If user need to generate an interrupt, set TIMx_DINTEN.CCxIEN.
- Then select the output mode by set TIMx_CCEN.CCxP, TIMx_CCMODx.OCxMD, TIMx_CCEN.CCxEN, etc.
- At last, set TIMx_CTRL1.CNTEN to enable the counter.

User can update the output waveform by setting TIMx_CCDATx at any time, as long as the preload register is not enabled. Otherwise the TIMx_CCDATx shadow register will be updated at the next update event.

Here is an example.

Figure 8-21 Output Compare Mode, Toggle on OC1



8.3.9 PWM Mode

PWM mode is used to generate a signal with a duty cycle determined by the value of the TIMx_CCDATx register

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and a frequency determined by the value of the TIMx_AR register. Depending on the value of TIMx_CTRL1.CAMSEL, the TIM can generate PWM signal in edge-aligned mode or center-aligned mode.

User can select PWM mode 1 or PWM mode 2 by setting TIMx_CCMODx. OCxMD = 110 or setting TIMx_CCMODx. OCxMD = 111. To enable preload register, user must set corresponding TIMx_CCMODx.OCxPEN, and then set TIMx_CTRL1.ARPEN to auto-reload preload register eventually.

User can set polarity of OCx by setting TIMx_CCEN.CCxP. On the other hand, to enable the output of OCx, user needs to set the combination of the value of CCxEN, CCxNEN, MOEN, OSSI, and OSSR in TIMx_CCEN and TIMx_BKDT.

The values of TIMx_CNT and TIMx_CCDATx are always compared with each other when the TIM is under PWM mode.

Only when an update event occurs, the preload register will be transferred to the shadow register. Therefore user must reset all the registers by setting TIMx_EVTGEN.UDGN before the counter starts counting.

8.3.9.1 PWM center-aligned mode

If user sets TIMx_CTRL1.CAMSEL to 01, 10 or 11, the PWM center-aligned mode will be active. The setting of the compare flag depends on the value of TIMx_CTRL1.CAMSEL. There are three kinds of situation that the compare flag is set: only when the counter counts up, only when the counter counts down, or both when the counter counts up and counts down. User should not modify TIMx_CTRL1.DIR by software, as it is updated by hardware.

Examples of center-aligned PWM waveforms is as follows, and the settings of the waveform are: TIMx_AR = 8, PWM mode 1, the compare flag is set when the counter counts down corresponding to TIMx_CTRL1.CAMSEL = 01.

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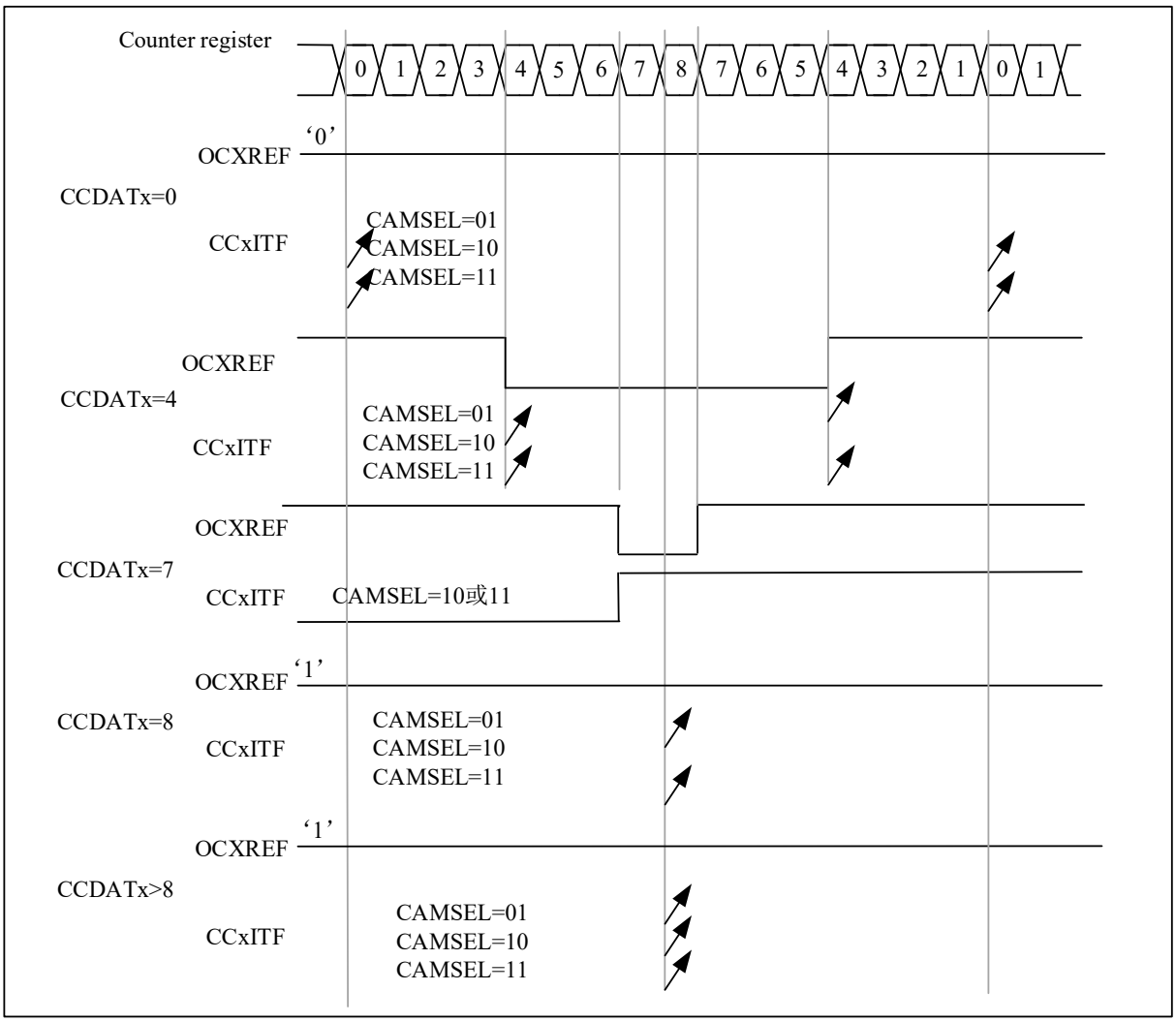
Figure 8-22 Center-aligned PWM Waveform (AR=8)



When using center-aligned mode, users should pay attention to the following considerations:

- It depends on the value of TIMx_CTRL1.DIR that the counter counts up or down. Cautions that the DIR and CAMSEL bits should not be changed at the same time.
- User should not write the counter while running in center-aligned mode, otherwise it will cause unexpected results. Here are some example:
  - If the value written into the counter is 0 or is the value of TIMx_AR, the direction will be updated but the update event will not be generated.
  - If the value written into the counter is greater than the value of auto-reload, the direction will not be updated.
- For safety reasons, It is recommended that users set TIMx_EVTGEN.UDGN to generate an update by software before starting the counter, and do not write the counter while it is running.

8.3.9.2 PWM edge-aligned mode

There are two kinds of configuration in edge-aligned mode, up-counting and down-counting.

- **Up-counting**

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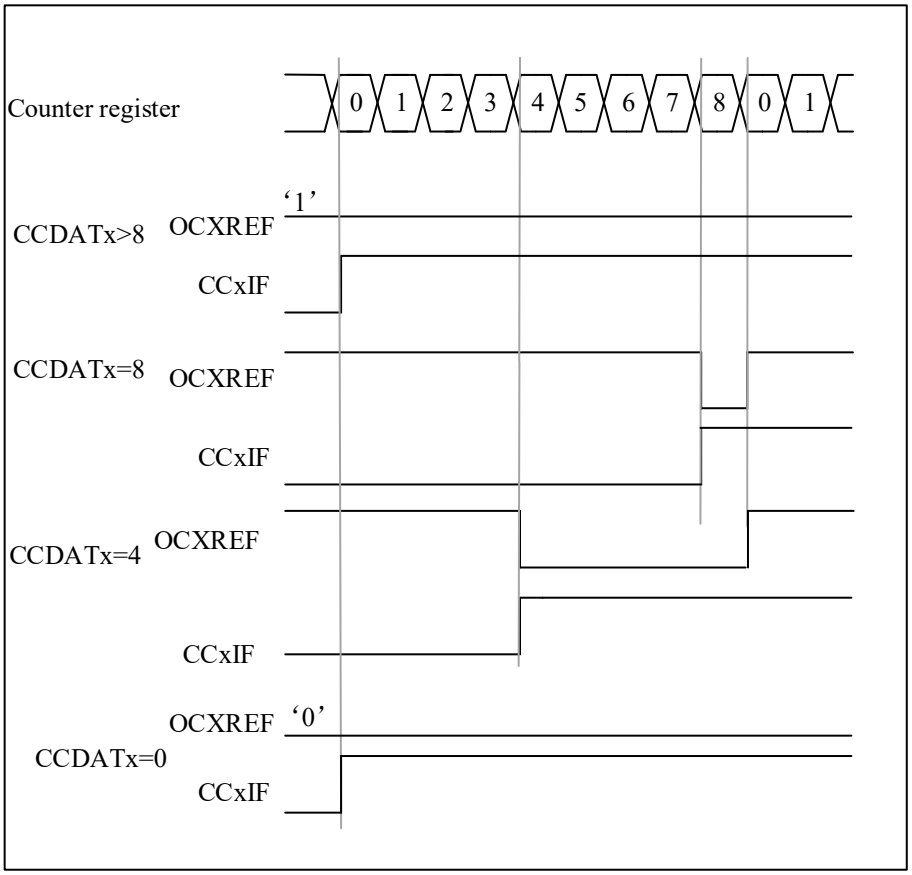
User can set TIMx_CTRL1.DIR = 0 to make counter counts up.

Example for PWM mode1:

When TIMx_CNT < TIMx_CCDATx, the reference PWM signal OCxREF is high. Otherwise it will be low. If the compare value in TIMx_CCDATx is greater than the auto-reload value, the OCxREF will remains 1. Conversely, if the compare value is 0, the OCxREF will remain 0.

When TIMx_A R= 8, the PWM waveforms are as follows.

Figure 8-23 Edge-aligned PWM Waveform (APR = 8)



- **Down-counting**

User can set TIMx_CTRL1.DIR = 1 to make counter counts down.

Example for PWM mode1:

When TIMx_CNT > TIMx_CCDATx, the reference PWM signal OCxREF is low. Otherwise it will be high. If the compare value in TIMx_CCDATx is greater than the auto-reload value, the OCxREF will remain 1.

Note: If the nth PWM cycle CCDATx shadow register >= AR value, the shadow register value of CCDATx in the (n+1)th PWM cycle is 0. At the moment when the counter is 0 in the (n+1)th PWM cycle, although the value of the counter = CCDATx shadow register = 0 and OCxREF = '0', no compare event will be generated.

8.3.10 One-pulse Mode

In the one-pulse mode (ONEPM), a trigger signal is received, and a pulse t_{PULSE} with a programmable pulse width is generated after a programmable delay t_{DELAY}. The output mode needs to be configured as output compare mode or

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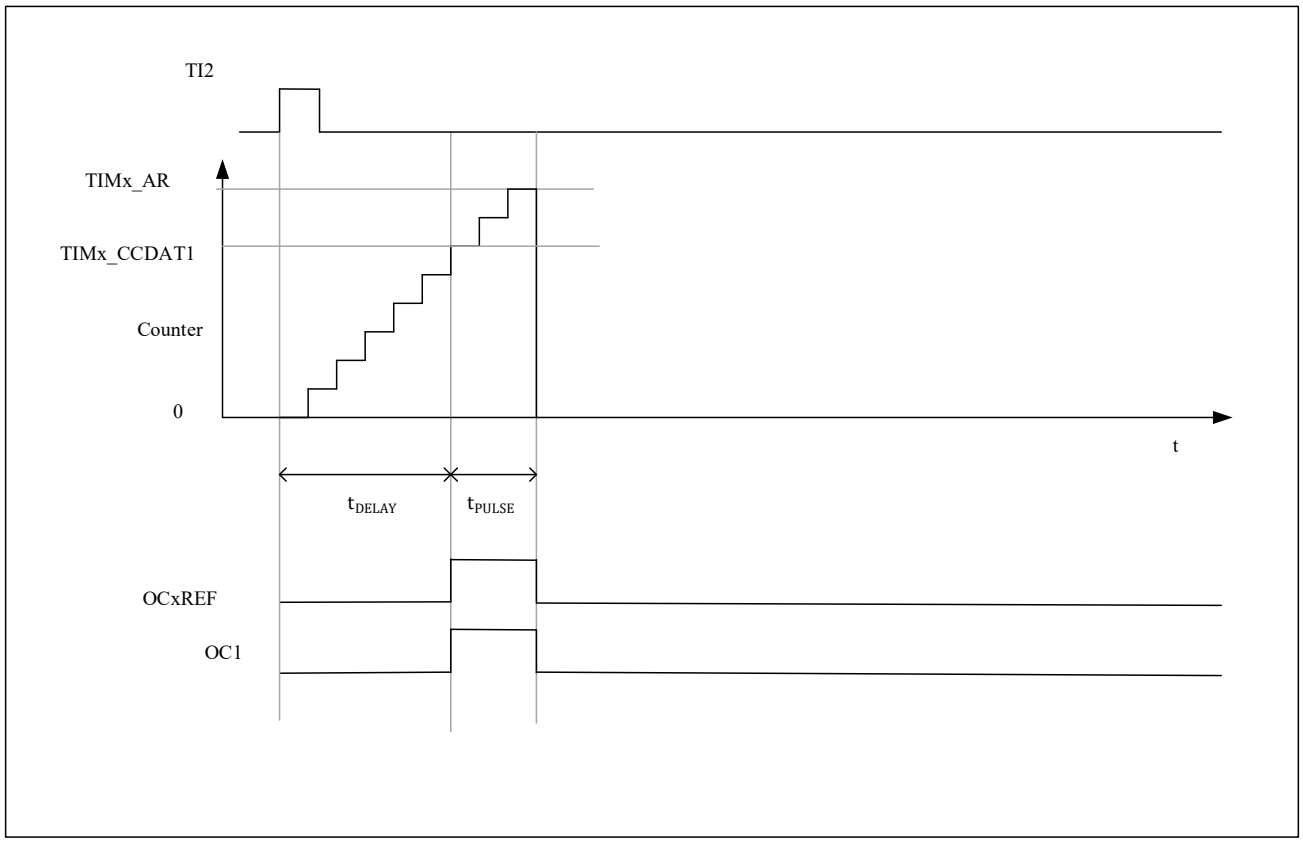
PWM mode. After selecting one-pulse mode, the counter will stop counting after the update event UEV is generated.

Figure 8-24 Example of One-pulse Mode



The following is an example of the one-pulse mode:

A rising edge trigger is detected from the TI2 input, and a pulse with a width of t_{PULSE} is generated on OC1 after a delay of t_{DELAY}.

1. Counter is configurated as up-counting and TIMx_CNT < TIMx_CCDAT1 ≤ TIMx_AR;

2. TI2FP2 is mapped to TI2 by writing TIMx_CCMOD1.CC2SEL = '01'; TI2FP2 is configured for rising edge detection by writing TIMx_CCEN.CC2P = '0';

3. TI2FP2 is configured as the trigger (TRGI) of the slave mode controller by writing TIMx_SMCTRL.TSEL= '110'; TI2FP2 is used to start the counter by writing TIMx_SMCTRL.SMSEL= '110' (trigger mode);

4. The count value to be delayed (t_{DELAY}) is configured in TIMx_CCDAT1; TIMx_AR - TIMx_CCDAT1 is the count value of the pulse width t_{PULSE};

5. Configure TIMx_CTRL1.ONEPM = 1 to enable single pulse mode; Configure TIMx_CCMOD1.OC1MD = '111' to select PWM2 mode;

6. Wait for an external trigger event on TI2, and a one pulse waveform will be output on OC1;

8.3.10.1 Special case: OCx fast enable

In one-pulse mode, an edge is detected through the TIx input, and triggers the counter to count to the comparison value and then output a pulse. These operations limit the minimum delay t_{DELAY} that can be achieved.

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User can set TIMx_CCMODx.OCxFEN = 1 to turn on OCx fast enable. After triggering the rising edge, the OCxREF signal will be forced to be converted to the same level as the comparison match occurs immediately, regardless of the comparison result. OCxFEN fast enable only takes effect when the channel mode is configured for PWM1 and PWM2 modes.

8.3.11 Clearing the OCxREF Signal on an External Event

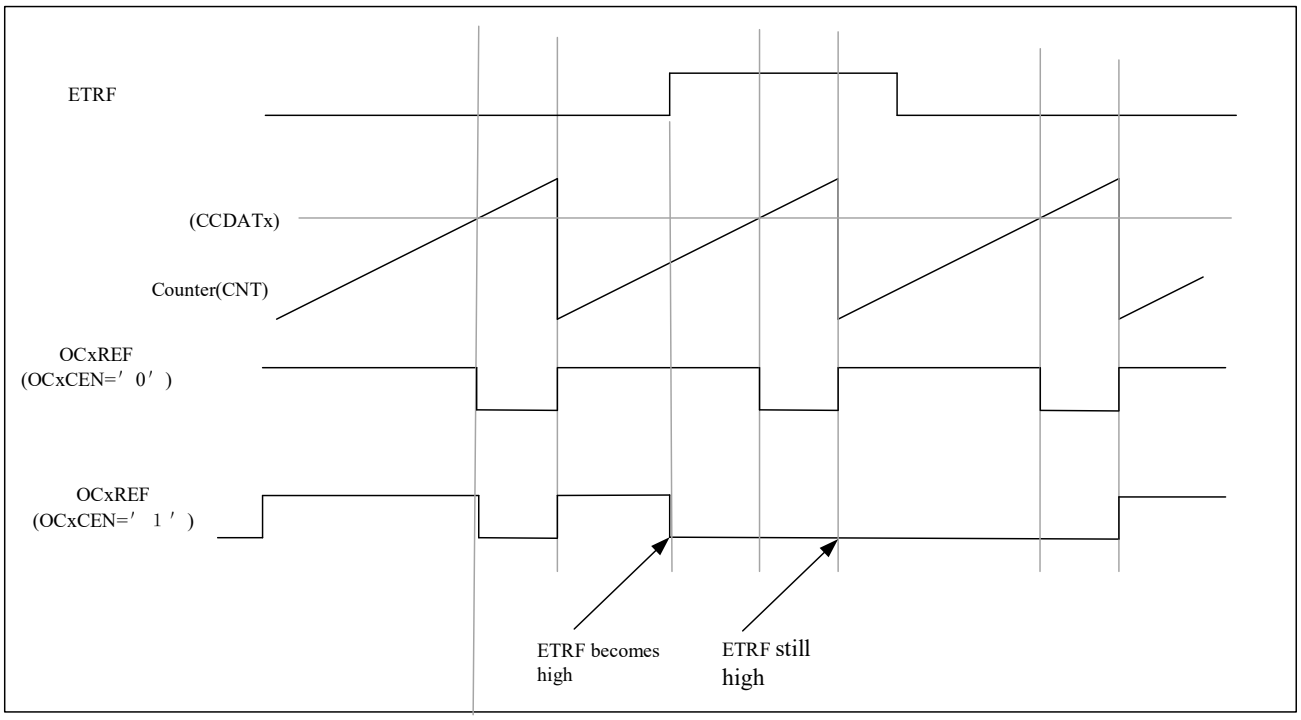
If TIMx_CCMODx.OCxCEN=1, high level of ETRF input can be used to driven the OCxREF signal to low, and the OCxREF signal will remain low until the next UEV happens. Only output compare and PWM modes can use this function. This cannot be used when it is in forced mode.

For example: to control the current, user can connect the ETR signal to the output of a comparator, and the operation for ETR should be as follow:

- Set TIMx_SMCTRL.EXTPS = 00 to disable the external trigger prescaler.
- Set TIMx_SMCTRL.EXCEN = 0 to disable the external clock mode 2.
- Set TIMx_SMCTRL.EXTP and TIMx_SMCTRL.EXTF to configure the external trigger polarity and external trigger filter according to the need.

Here is an example for the case that when ETRF input becomes high, the behavior of OCxREF signal for different value of OCxCEN. Timer is set to be in PWM mode in this case.

Figure 8-25 Clearing the OCxREF of TIMx



8.3.12 Complementary Outputs with Dead-time Insertion

Advanced-control timer can output two complementary signals with dead time. User should adjust dead-time depending on the devices connected to the outputs and their characteristics.

User can select the polarity of outputs by setting TIMx_CCEN.CCxP and TIMx_CCEN.CCxNP. And this selection

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is independently for each output.

User can control the complementary signals OCx and OCxN by setting the combination of several control bits, which are TIMx_CCEN.CCxEN, TIMx_CCEN.CCxNEN, TIMx_BKDT.MOEN, TIMx_CTRL2.OIx, TIMx_CTRL2.OIxN, TIMx_BKDT.OSSI, and TIMx_BKDT.OSSR. When switching to the IDLE state, the dead-time will be activated.

If user set TIMx_CCEN.CCxEN and TIMx_CCEN.CCxNEN at the same time, a dead-time will be insert. If there is a break circuit, the TIMx_BKDT.MOEN should be set too. There are 10-bit dead-time generators for each channel.

Reference waveform OCxREF can generates 2 outputs OCx and OCxN. And if OCx and OCxN are active high, the OCx output signal is the same as the reference signal and the OCxN output signal is the opposite of the reference signal. However, OCx output signal will be delayed relative to the reference rising edge and the OCxN output signal will be delayed relative to the reference falling edge. If the delay is greater than the width of the active OCx or OCxN output, the corresponding pulse will not generated.

The relationships between the output signals of the dead-time generator and the reference signal OCxREF are as follows.

Assume that TIMx_CCEN.CCxP = 0, TIMx_CCEN.CCxNP = 0, TIMx_BKDT.MOEN = 1, TIMx_CCEN.CCxEN = 1, TIMx_CCEN.CCxNEN = 1.

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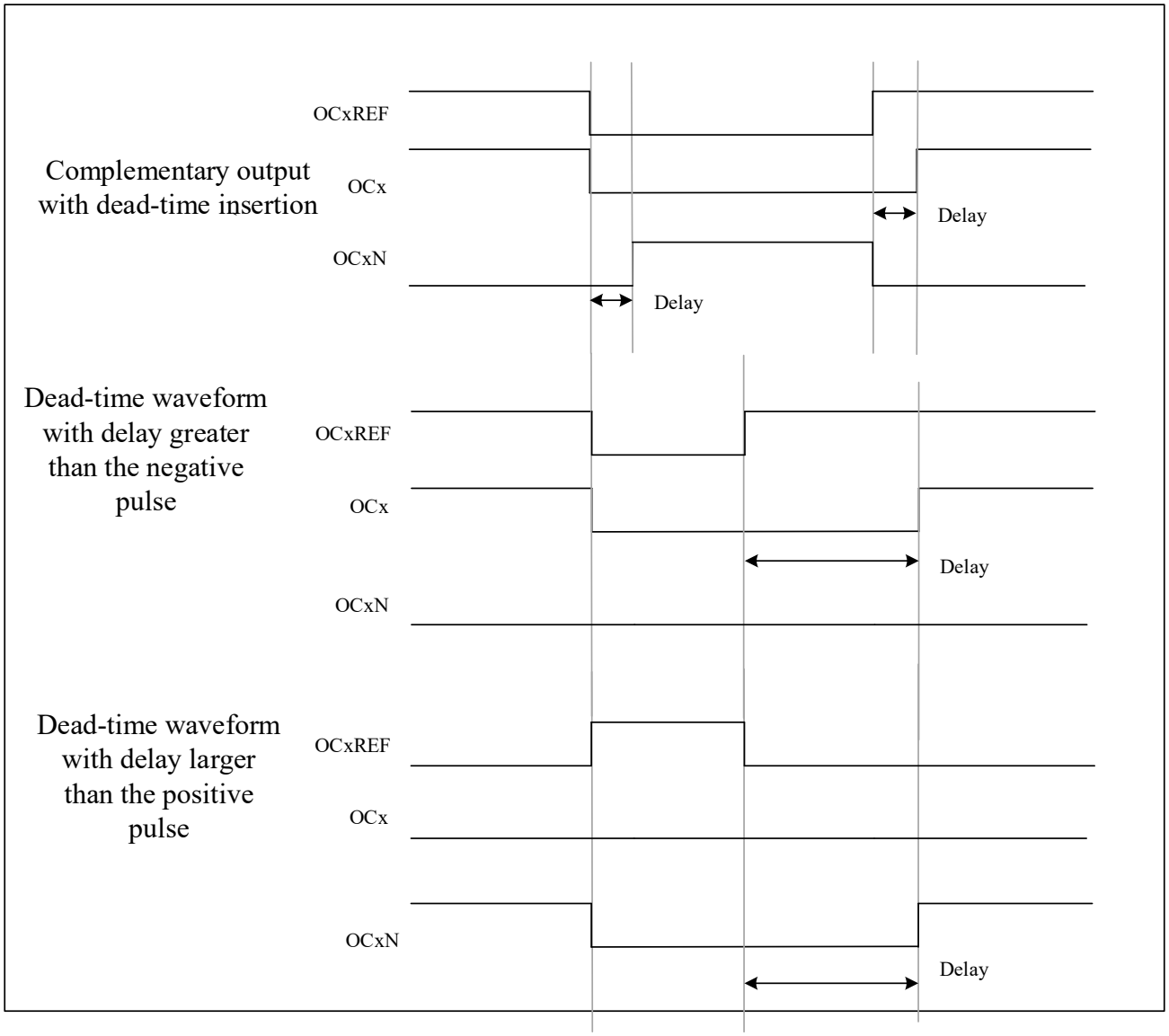
Figure 8-26 Complementary Output with Dead-time Insertion



User can set TIMx_BKDT.DTGN to program the dead-time delay for each of the channels.

8.3.12.1 Redirecting OCxREF To OCx Or OCxN

In output mode, user can set TIMx_CCEN.CCxEN and TIMx_CCEN.CCxNEN to re-directed OCxREF to the OCx output or to OCxN output.

Here are two ways to use this function. When the complementary remains at its inactive level, user can use this function to send a specific waveform, such as PWM or static active level. User can also use this function to set both outputs in their inactive level or both outputs active and complementary with dead-time.

If user set TIMx_CCEN.CCxEN = 0 and TIMx_CCEN.CCxNEN = 1, it will be not complemented, and OCxN will become active when OCxREF is high. On the other hand, if user set TIMx_CCEN.CCxEN = 1 and TIMx_CCEN.CCxNEN = 1, OCx will become active when OCxREF is high. On the contrary, OCxN will become active when OCxREF is low.

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8.3.13 Break Function

The output enable signals and inactive levels will be modified by setting the corresponding control bits when using the break function. However, in any case, the output of OCx and OCxN cannot at the active level at the same time, that is, (CCxP^OIx) ^(CCxNP^OIxN) != 0.

When multiple break signals are enabled, each break signal constitutes an OR logic. Here are some signal which can be the source of breaking.

- The break input pin
- A PVD failure event
- Core Hardfault event
- The output signal of the comparator (configured in the comparator module, high level break)
- By software through the TIMx_EVTGEN.BGN

After reset, the break circuit will be disable and the MOEN bit will be low. User can set TIMx_BKDT.BKEN to enable the break function. The polarity of break input signal can be selected by setting TIMx_BKDT.BKP. User can modify the TIMx_BKDT.BKEN and TIMx_BKDT.BKP at the same time. After user set the TIMx_BKDT.BKEN and TIMx_BKDT.BKP, there is 1 APB clock cycle delay before the configuration take effect. Therefore, user need to wait 1 APB clock cycle to read back the written bit.

The falling edge of MOEN can be asynchronous, so there is a resynchronization circuit between the actual signal and the synchronous control bit. This circuit will cause a delay between the asynchronous and the synchronous signal. When user set TIMx_BKDT.MOEN while it is low, user need to insert a delay before reading the value. Because an asynchronous signal was written but user read the synchronous signal.

The behaviors that after a break occurs are as follows:

- TIMx_BKDT.MOEN will be cleared asynchronously, and then the outputs will be put in inactive state, idle state or reset state. The state of output is selected by setting TIMx_BKDT.OSSI. This will take effect even if the MCU oscillator is off.
- Once TIMx_BKDT.MOEN = 0, each output channel will be driven with the level programmed in TIMx_CTRL2.OIx. Timer will release the enable outputs (taken over by GPIO controller) if TIMx_BKDT.OSSI = 0, otherwise it will remain high.
- If user choose to use complementary outputs, the behaviors of TIM are as follows:
  - Depending on the polarity, the outputs will be set in reset state first. It is an asynchronous option so it still works even if there is no clock provided to the timer.
  - The dead-time generator will be reactivated if the timer clock is still provided, and drive the outputs according to the value of TIMx_CTRL2.OIx and TIMx_CTRL2.OIxN after the dead-time when (CCxP ^ OIx) ^ (CCxNP^OIxN) != 0, that is, the OCx and OCxN still cannot be driven to active level at the same time. Note that the dead-time will be longer than usual because of the resynchronization on MOEN (almost 2 cycles of ck_tim).
  - Timer will release the output control if TIMx_BKDT.OSSI = 0. Otherwise, if the enable output is high, it will remain high. If it is low, it will become high when TIMx_CCEN.CCxEN or TIMx_CCEN.CCxNEN is

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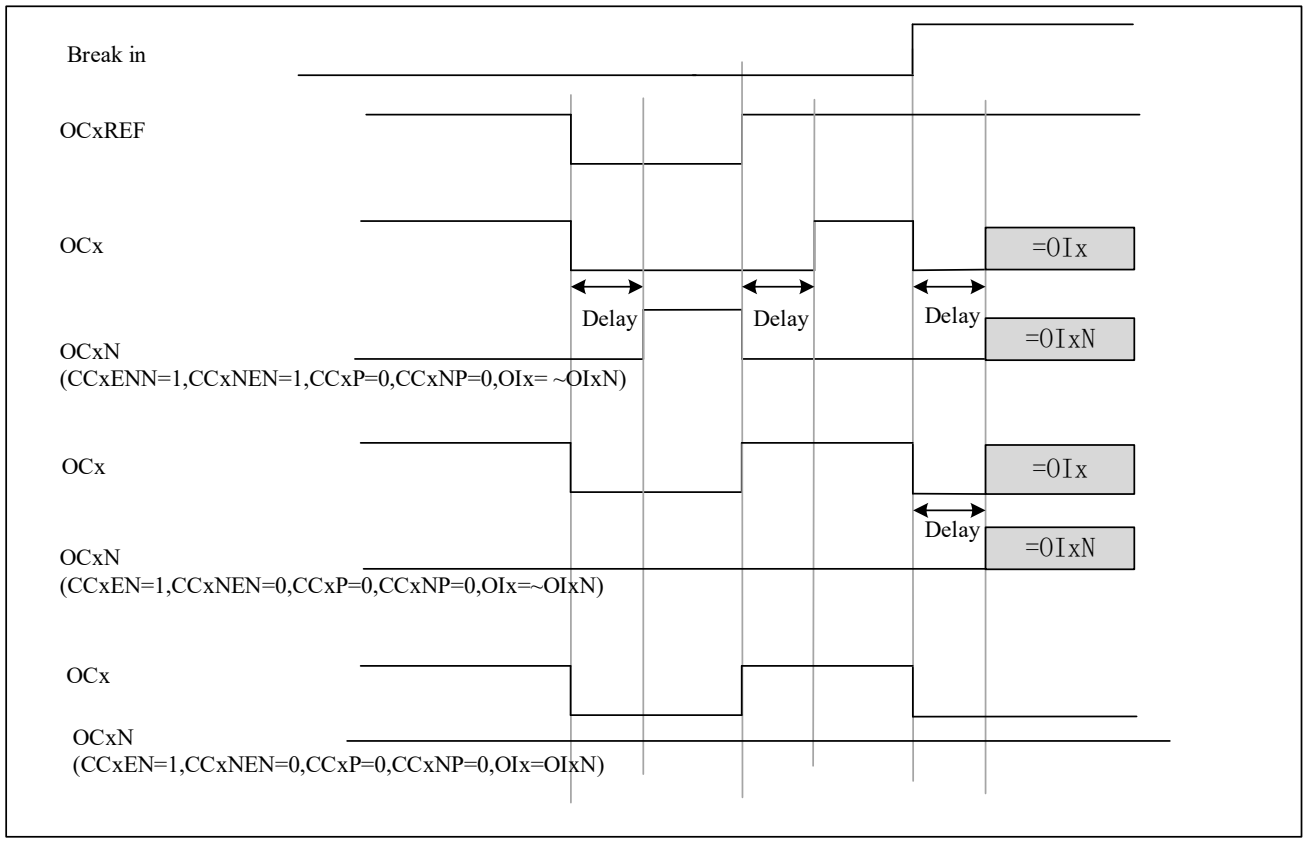
high.

- If TIMx_DINTEN.BIEN = 1, when TIMx_STS.BITF = 1, an interrupt will be generated.
- If user set TIMx_BKDT.AOEN, the TIMx_BKDT.MOEN will be set automatically when the next UEV happened. User can use this to regulate. If user does not set TIMx_BKDT.AOEN, the TIMx_BKDT.MOEN will remain low until it is set to 1 again. At this situation, user can use this for security. User can connect the break input to thermal sensors, alarm for power drivers, or other security components.
- When the break input is active, TIMx_BKDT.MOEN cannot be set automatically or by software at the same time, and the TIMx_STS.BITF cannot be cleared. Because the break inputs are active on level.

To ensure the security of application, the break circuit has the write protection function, as well as break input and output management. It allow user to freeze some parameters, such as dead-time duration, OCx/OCxN polarities and state when disabled, OCxMD configurations, break enable and polarity. User can choose one of the 3 levels of protection to use by setting TIMx_BKDT.LCKCFG. However, the TIMx_BKDT.LCKCFG can only be written once after an MCU reset.

An example for output behavior in response to a break is as follows

Figure 8-27 Output Behavior in Response to a Break



8.3.14 Debug Mode

When the microcontroller is in debug mode (the Cortex®-M0 core halted), depending on the DBG_CTRL.TIMx_STOP configuration in the PWR module, the TIMx counter can either continue to work normally or stop. For more details, refer to Section 3.4.9.

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8.3.15 Timx and External Trigger Synchronization

TIMx timers can be synchronized by a trigger in slave mode (reset, trigger and gated).

8.3.15.1 Slave mode: reset mode

In reset mode, the trigger event can reset the counter and the prescaler updates the preload registers TIMx_AR, TIMx_CCDATx, and generates the update event UEV (TIMx_CTRL1.UPRS=0).

The following is an example of the reset mode:

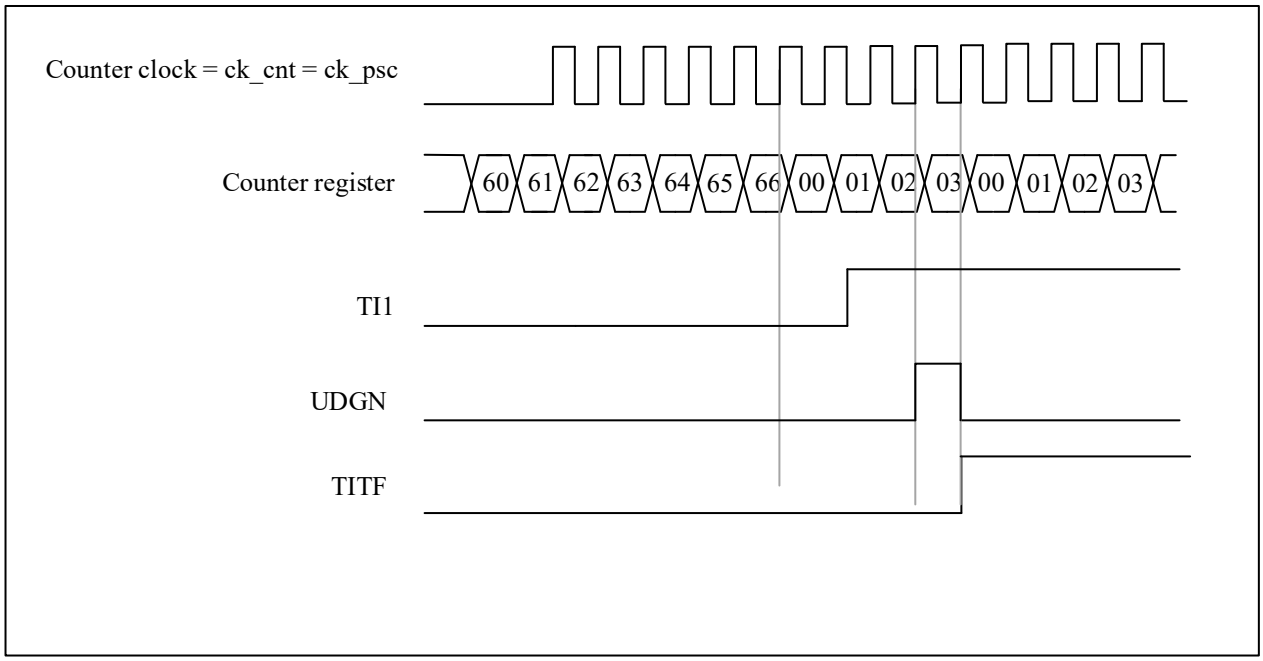
1. Channel 1 is configured as input to detect the rising edge of TI1 (TIMx_CCMOD1.CC1SEL=01, TIMx_CCEN.CC1P=0);

2. The slave mode is selected as reset mode (TIMx_SMCTRL.SMSEL=100), and the trigger input is selected as TI1 (TIMx_SMCTRL.TSEL=101);

3. Start counter (TIMx_CTRL1.CNTEN = 1).

After starting the timer, when TI1 detects a rising edge, the counter resets and restarts counting, and the trigger flag is set (TIMx_STS.TITF=1); The delay between the rising edge on TI1 and the actual reset of the counter is due to the resynchronization circuit on TI1 input.

Figure 8-28 Control Circuit in Reset Mode



8.3.15.2 Slave mode: trigger mode

In trigger mode, the trigger event (rising edge/falling edge) of the input port can trigger the counter to start counting.

The following is an example of a trigger pattern:

1. Channel 2 is configured as input to detect the rising edge of TI2 (TIMx_CCMOD1.CC2SEL=01, TIMx_CCEN.CC2P=0);

2. Select slave mode as trigger mode (TIMx_SMCTRL.SMSEL=110), and select TI2 as trigger input

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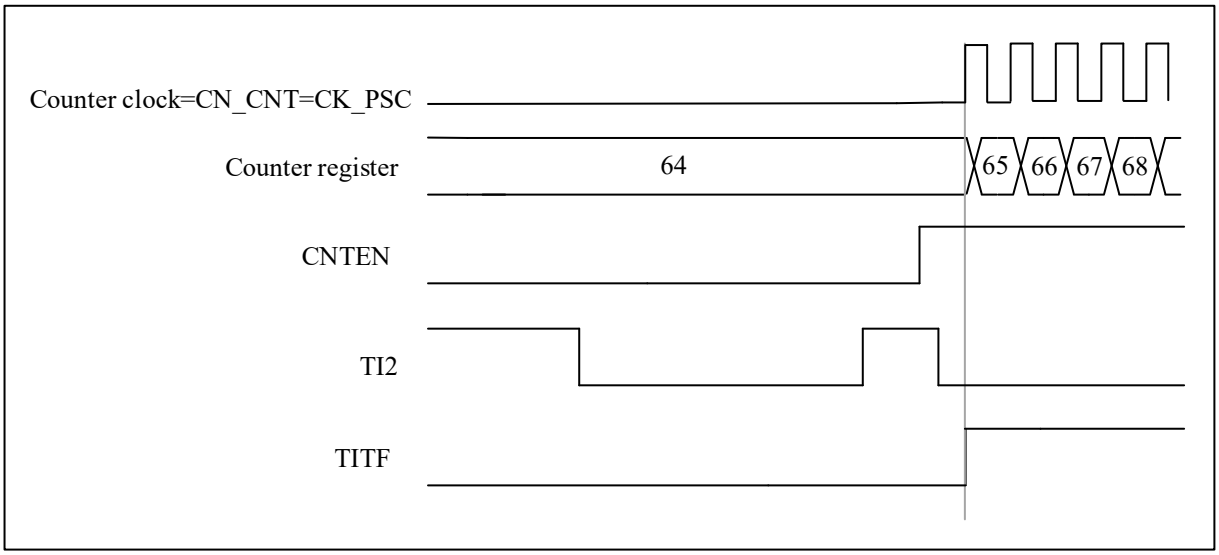
(TIMx_SMCTRL.TSEL=110);

When a rising edge is detected on TI2, the counter starts counting, and the trigger flag is set (TIMx_STS.TITF=1);

The delay between the rising edge on TI2 and the actual start of the counter is due to the resynchronization circuit on TI2 input.

Figure 8-29 Control Circuit in Trigger Mode



8.3.15.3 Slave mode: gated mode

In gated mode, the level polarity of the input port can enable the counter.

The following is an example of the gated mode:

1. Channel 1 is configured to low levelon TI1 (TIMx_CCMOD1.CC1SEL = 01, TIMx_CCEN.CC1P = 1);

2. Select the slave mode as the gated mode (TIMx_SMCTRL.SMSEL = 101), and select TI1 as the trigger input (TIMx_SMCTRL.TSEL = 101);

3. Start counter(TIMx_CTRL1.CNTEN = 1).

When TI1 detects that the level changes from low to high, the counter stops counting, and when TI1 detects that the level changes from high to low, the counter starts counting, and the trigger flag will be set (TIMx_STS.TITF = 1) when it starts or stops counting;

The delay between the rising edge on TI1 and the actual stop of the counter is due to the resynchronization circuit on TI1 input.

Figure 8-30 Control Circuit in Gated Mode

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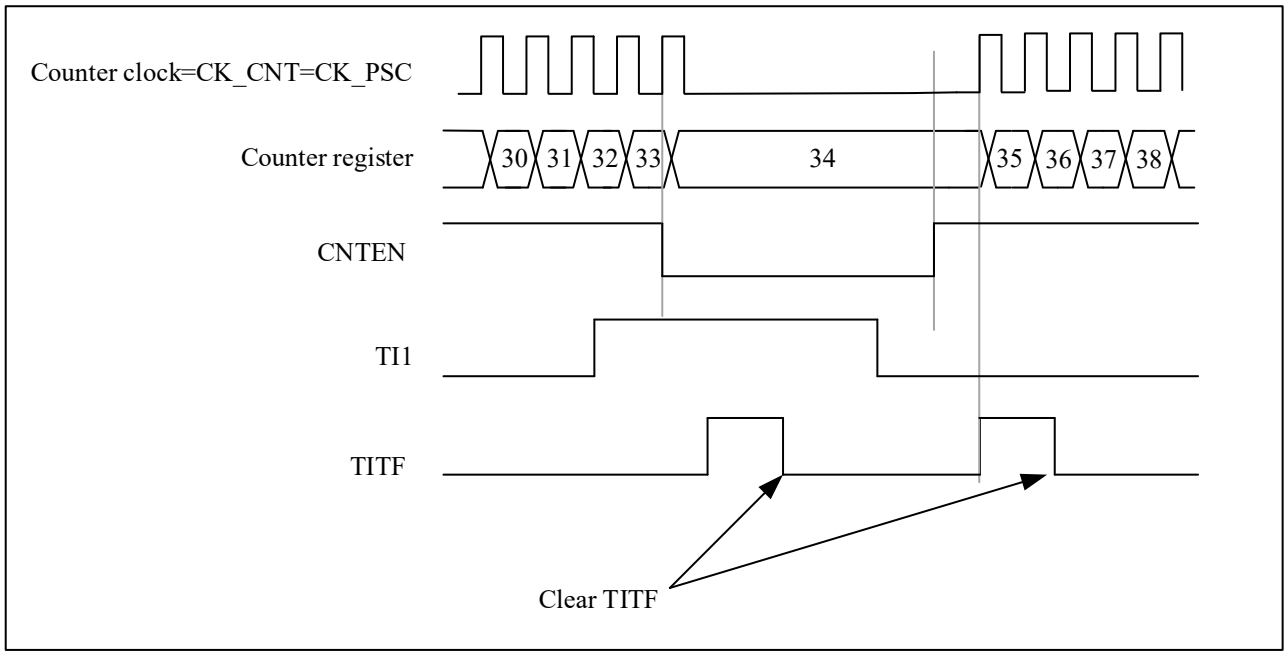

8.3.15.4 Slave mode: trigger mode + external clock mode 2

In reset mode, trigger mode and gate control mode, the counter clock can be selected as external clock mode 2, and the ETR signal is used as the external clock source input. At this time, the trigger selection needs to select non-ETRF (TIMx_SMCTRL.TSEL=111).

Here is an example:

1. Channel 1 is configured as input to detect the rising edge of TI1 (TIMx_CCMOD1.CC1SEL=01, TIMx_CCEN.CC1P=0);

2. Enable external clock mode 2 (TIMx_SMCTRL.EXCEN=1), and select rising edge for external trigger polarity (TIMx_SMCTRL.EXTP=0), and select slave mode as trigger mode (TIMx_SMCTRL.SMSEL=110), and select TI1 for trigger input (TIMx_SMCTRL.TSEL=101);

When TI1 detects a rising edge, the counter starts counting on the rising edge of ETR, and the trigger flag is set (TIMx_STS.TITF=1);

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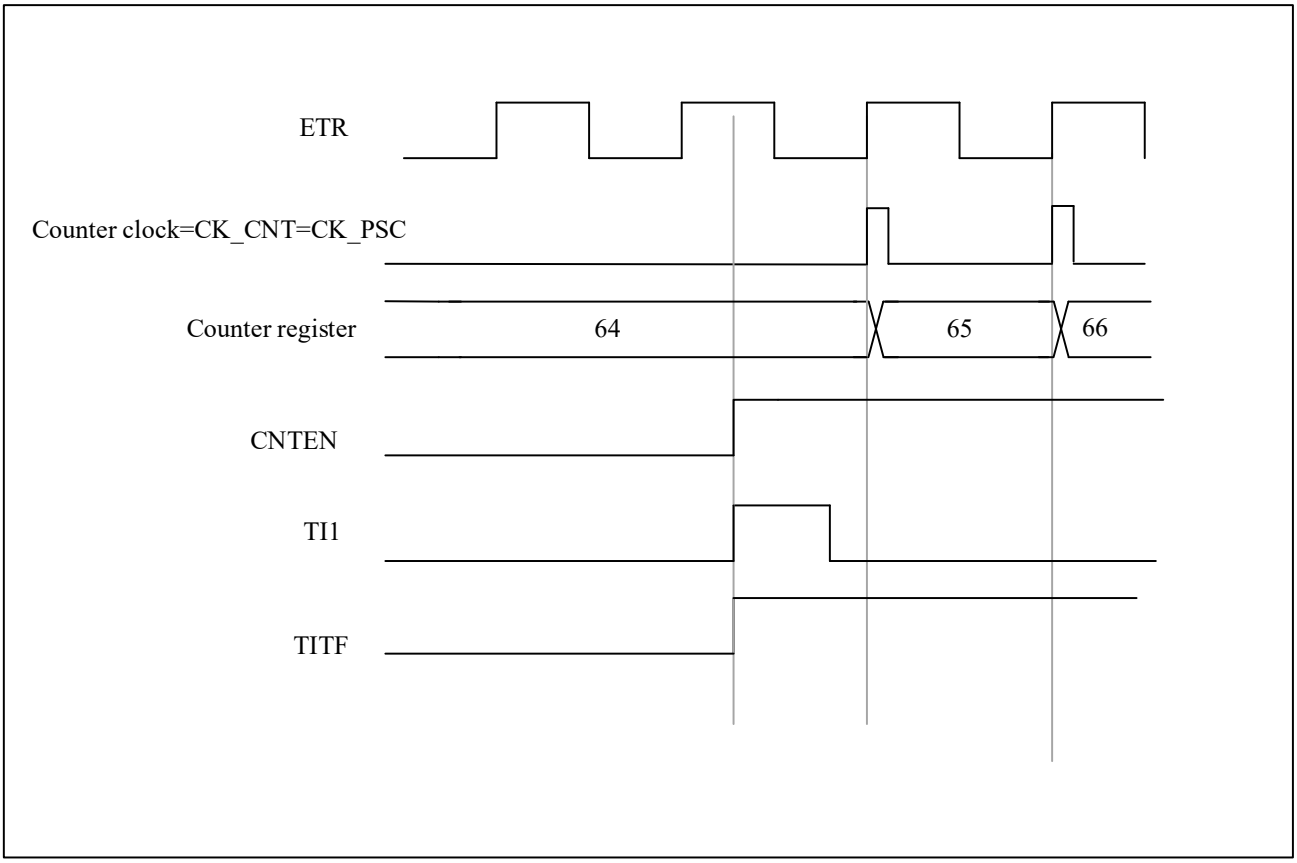
Figure 8-31 Control Circuit in Trigger Mode + External Clock Mode 2



8.3.16 Timer Synchronization

All TIM timers are internally connected for timer synchronization or chaining. For more details, refer to Section 9.3.14.

8.3.17 6-step PWM Generation

In order to modify the configuration of all channels at the same time, the configuration of the next step can be set in advance (the preloaded bits are OCxMD, CCxEN and CCxNEN). When a COM commutation event occurs, the OCxMD, CCxEN, and CCxNEN preload bits are transferred to the shadow register bits.

COM can be generated by software by setting the COM bit in the TIMx_EGR register or by hardware (on TRGI rising edge).

When a COM commutation event occurs, the TIMx_STS.COMITF flag will be set, which will generate interrupts (if TIMx_DINTEN.COMIEN is set).

The following figure shows the output timing diagram of OCx and OCxN when a COM commutation event occurs in three different configurations:

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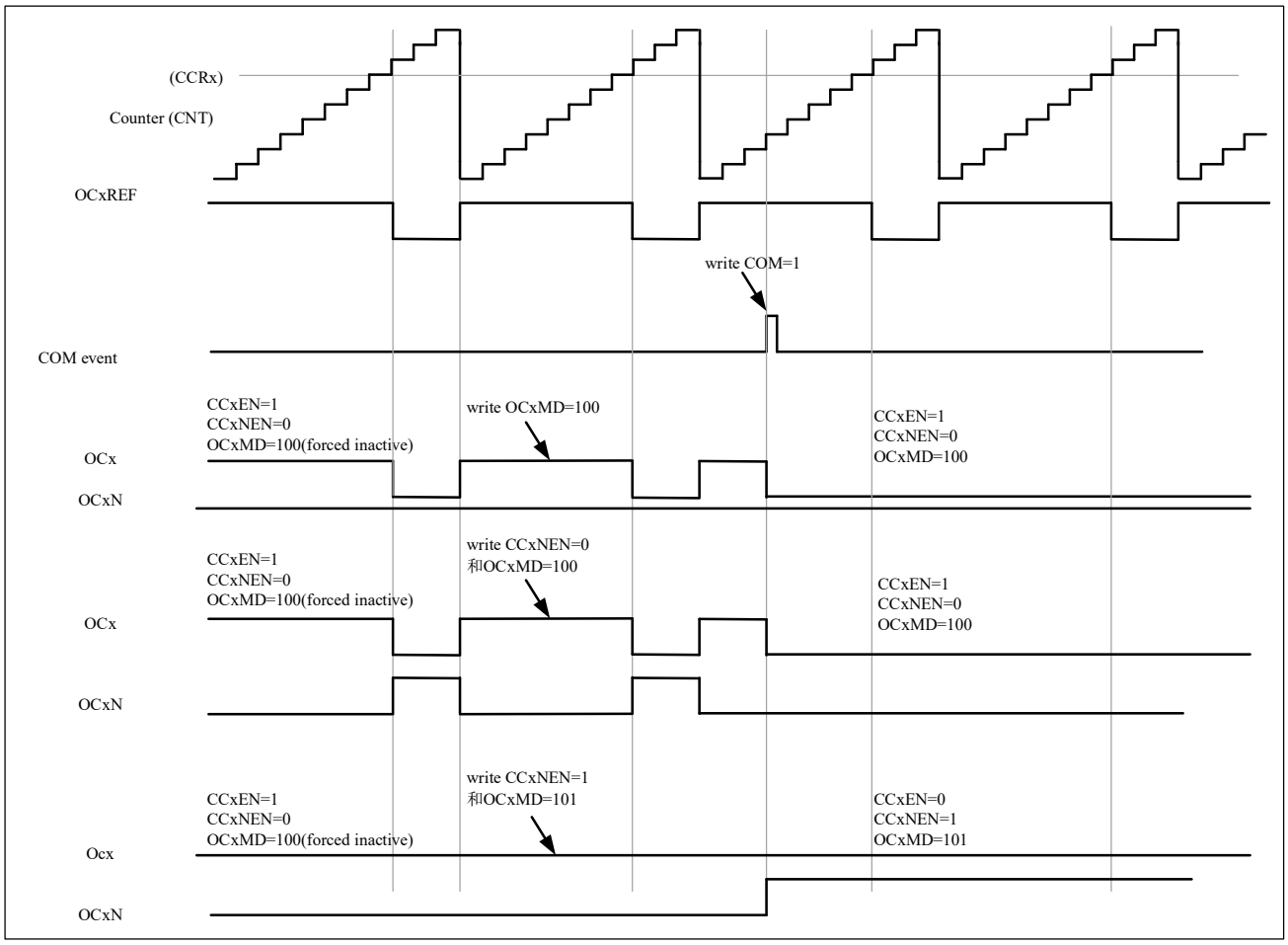
Figure 8-32 6-Step PWM Generation, COM Example (OSSR=1)



8.4 TIMx Register Description(x=1)

8.4.1 Register Overview

Table 8-1 Register Overview

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
000h	TIMx_CTRL1	Reserved														PBKPEN	LBKPEN	CLRSEL	Reserved	Reserved	Reserved	C1SEL	IOMBKPEN	CLKD[1:0]		ARPEN	CAMSEL[1:0]		DIR	ONEPM	UPRS	UPDIS	CNTEN
	Reset Value															0	0	0				0	0	0	0	0	0	0	0	0	0	0	0
004h	TIMx_CTRL2	Reserved															OI5	Reserved	OI4	OI3N	OI3	OI2N	OI2	OI1N	OI1	TI1SEL	MMSEL[2:0]			Reserved	CCUSEL	Reserved	CCPCTL
	Reset Value																0		0	0	0	0	0	0	0	0	0	0	0		0		0
008h	TIMx_SMCTRL	Reserved																EXTP	EXCEN	EXTPS[1:0]		EXTF[3:0]				MSMD	TSEL[2:0]			Reserved	SMSEL[2:0]		
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0		0	0	0
00Ch	TIMx_DINTEN	Reserved																								BIEN	TIEN	COMIEN	CC4IEN	CC3IEN	CC2IEN	CC1IEN	UIEN

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	Reset Value												0	0	0	0	0	0	0	0
010h	TIMx_STS	Reserved		CC5ITF	Reserved			CC4OCF	CC3OCF	CC2OCF	CC1OCF	Reserved	BITF	TITF	COMITF	CC4ITF	CC3ITF	CC2ITF	CC1ITF	UDITF
	Reset Value			0				0	0	0	0		0	0	0	0	0	0	0	0
014h	TIMx_EVTGEN	Reserved											BGN	TGN	CCUDGN	CC4GN	CC3GN	CC2GN	CC1GN	UDGN
	Reset Value												0	0	0	0	0	0	0	0
018h	TIMx_CCMOD1	Reserved			OC2CEN	OC2M[2:0]			OC2PEN	OC2FEN	CC2SEL[1:0]		OC1CEN	OC1M[2:0]			OC1PEN	OC1FEN	CC1SEL[1:0]	
	Reset Value				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	TIMx_CCMOD1	Reserved			IC2F[3:0]				IC2PSC[1:0]		CC2SEL[1:0]		IC1F[3:0]				IC1PSC[1:0]		CC1SEL[1:0]	
	Reset Value				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
01Ch	TIMx_CCMOD2	Reserved			OC4CEN	OC4M[2:0]			OC4PEN	OC4FEN	CC4SEL[1:0]		OC3CEN	OC3M[2:0]			OC3PEN	OC3FEN	CC3SEL[1:0]	
	Reset Value				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	TIMx_CCMOD2	Reserved			IC4F[3:0]				IC4PSC[1:0]		CC4SEL[1:0]		IC3F[3:0]				IC3PSC[1:0]		CC3SEL[1:0]	
	Reset Value				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
020h	TIMx_CCEN	Reserved	CC5P	CC5EN	Reserved		CC4P	CC4EN	CC3NP	CC3NEN	CC3P	CC3EN	CC2NP	CC2NEN	CC2P	CC2EN	CC1NP	CC1NEN	CC1P	CC1EN
	Reset Value		0	0			0	0	0	0	0	0	0	0	0	0	0	0	0	0
024h	TIMx_CNT	Reserved			CNT[15:0]															
	Reset Value				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
028h	TIMx_PSC	Reserved			PSC[15:0]															
	Reset Value				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
02Ch	TIMx_AR	Reserved			AR[15:0]															
	Reset Value				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
030h	TIMx_REPCNT	Reserved											REPCNT[7:0]							
	Reset Value												0	0	0	0	0	0	0	0
034h	TIMx_CCDAT1	Reserved			CCDAT1[15:0]															
	Reset Value				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
038h	TIMx_CCDAT2	Reserved			CCDAT2[15:0]															
	Reset Value				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
03Ch	TIMx_CCDAT3	Reserved			CCDAT3[15:0]															
	Reset Value				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
040h	TIMx_CCDAT4	Reserved			CCDAT4[15:0]															
	Reset Value				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
044h	TIMx_BKDT	Reserved			MOEN	AOEN	BKP	BKEN	OSSR	OSSI	LCKCFG[1:0]		DTGN[7:0]							
	Reset Value				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
054h	TIMx_CCMOD3	Reserved											OC5CEN	OC5MD[2:0]			OC5PEN	OC5FEN	Reserved	
	Reset Value												0	0	0	0	0	0		
058h	TIMx_CCDAT5	Reserved			CCDAT5[15:0]															
	Reset Value				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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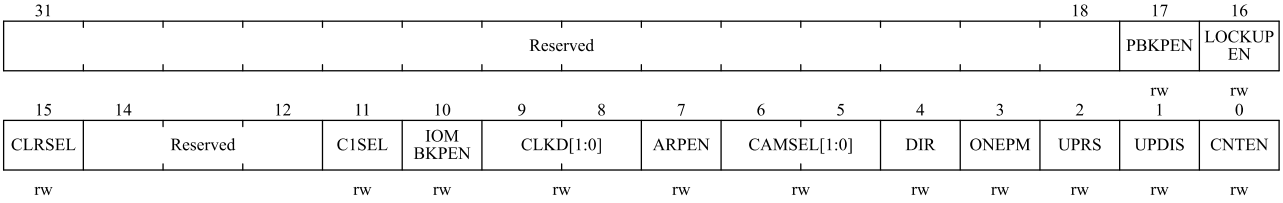
8.4.2 Control Register 1 (Timx_CTRL1)

Offset address: 0x00

Reset value: 0x0000 0000



Bit Field	Name	Description
31:18	Reserved	Reserved, the reset value must be maintained
17	PBKPEN	PVD as BKP enable 0: Disable 1: Enable
16	LBKPEN	LockUp as BKP enable 0: Disable 1: Enable
15	CLRSEL	OCxREF clear selection 0: Select the external OCxREF clear from ETR 1: Select the internal OCxREF clear from comparator
14:12	Reserved	Reserved, the reset value must be maintained
11	C1SEL	Channel 1 selection 0: Select external CH1 signal from IOM 1: Select internal CH1 signal from COMP
10	IOMBKPEN	Enabling IOM as BKP 0: Enable 1: Disable
9:8	CLKD[1:0]	Clock division CLKD[1:0] indicates the division ratio between CK_INT (timer clock) and DTS (clock used for dead-time generator and digital filters (ETR, TIx)) 00: $t_{DTS} = t_{CK\_INT}$ 01: $t_{DTS} = 2 \times t_{CK\_INT}$ 10: $t_{DTS} = 4 \times t_{CK\_INT}$ 11: Reserved, do not use this configuration
7	ARPEN	ARPEN: Auto-reload preload enable 0: Shadow register disable for TIMx_AR register 1: Shadow register enable for TIMx_AR register
6:5	CAMSEL[1:0]	Center-aligned mode selection 00: Edge-aligned mode. TIMx_CTRL1.DIR specifies up-counting or down-counting. 01: Center-aligned mode 1. The counter counts in center-aligned mode, and the output compare interrupt flag bit is set to 1 when down-counting.

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Bit Field	Name	Description
		10: Center-aligned mode 2. The counter counts in center-aligned mode, and the output compare interrupt flag bit is set to 1 when up-counting. 11: Center-aligned mode 3. The counter counts in center-aligned mode, and the output compare interrupt flag bit is set to 1 when up-counting or down-counting. *Note: Switching from edge-aligned mode to center-aligned mode is not allowed when the counter is still enabled (TIMx_CTRL1.CNTEN = 1).*
4	DIR	Direction 0: Up-counting 1: Down-counting *Note: This bit is read-only when the counter is configured in center-aligned mode.*
3	ONEPM	One-pulse mode 0: Disable one-pulse mode. The counter counts are not affected when an update event occurs. 1: Enable one-pulse mode. The counter stops counting when the next update event occurs (clearing TIMx_CTRL1.CNTEN bit)
2	UPRS	Update request source This bit is used to select the UEV event sources by software. 0: If update interrupt is enabled, any of the following events will generate an update interrupt : – Counter overflow/underflow – The TIMx_EVTGEN.UDGN bit is set – Update generation from the slave mode controller 1: If update interrupt is enabled, only counter overflow/underflow will generate update interrupt
1	UPDIS	Update disable This bit is used to enable/disable the update event (UEV) events generation by software. 0: Enable UEV. UEV will be generated if one of following condition been fulfilled: – Counter overflow/underflow – The TIMx_EVTGEN.UDGN bit is set – Update generation from the slave mode controller Shadow registers will update with preload value. 1: UEV disabled. No update event is generated, and the shadow registers (AR, PSC, and CCDATx) keep their values. If the TIMx_EVTGEN.UDGN bit is set or a hardware reset is issued by the slave mode controller, the counter and prescaler are reinitialized.
0	CNTEN	Counter Enable 0: Disable counter 1: Enable counter *Note: external clock, gating mode can only work after TIMx_CTRL1.CNTEN bit is set in the software. Trigger mode can automatically set TIMx_CTRL1.CNTEN bit by hardware*.

8.4.3 Control Register 2 (TIMx_CTRL2)

Offset address: 0x04

Reset value: 0x0000 0000

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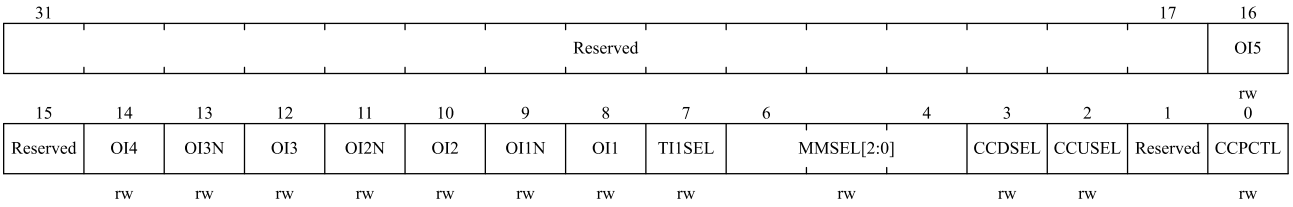

Bit Field	Name	Description
31:17	Reserved	Reserved, the reset value must be maintained
16	OI5	Output idle state 5 (OC5 output). Refer ro TIMx_CTRL2.OI1 bit.
15	Reserved	Reserved, the reset value must be maintained
14	OI4	Output idle state 4 (OC4 output). Refer to TIMx_CTRL2.OI1 bit.
13	OI3N	Output idle state 3 (OC3N output). Refer to TIMx_CTRL2.OI1N bit.
12	OI3	Output idle state 3 (OC3 output). Refer to TIMx_CTRL2.OI1 bit.
11	OI2N	Output idle state 2 (OC2N output). Refer to TIMx_CTRL2.OI1N bit.
10	OI2	Output idle state 2 (OC2 output). Refer to TIMx_CTRL2.OI1 bit.
9	OI1N	Output Idle state 1 (OC1N Output) 0: OC1N = 0 after dead-time when TIMx_BKDT.MOEN = 0 1: OC1N = 1 after dead-time when TIMx_BKDT.MOEN = 0
8	OI1	Output Idle state 1 0: OC1 = 0 (after dead-time if OC1N is implemented) when TIMx_BKDT.MOEN = 0 1: OC1 = 1 (after dead-time if OC1N is implemented) when TIMx_BKDT.MOEN = 0
7	TI1SEL	TI1 selection 0: TIMx_CH1 pin connected to TI1 input. 1: TIMx_CH1, TIMx_CH2, and TIMx_CH3 pins are XOR connected to the TI1 input.
6:4	MMSEL[2:0]	Master Mode Selection These 3 bits (TIMx_CTRL2. MMSEL [2:0]) are used to select the synchronization information (TRGO) sent to the slave timer in the master mode. Possible combinations are as follows: 000: Reset –When the TIMx_EVTGEN.UDGN is set or a reset is generated by the slave mode controller, a TRGO pulse occurs. And in the latter case, the signal on TRGO is delayed compared to the actual reset. 001: Enable - The TIMx_CTRL1.CNTEN bit is used as the trigger output (TRGO). Sometimes you need to start multiple timers at the same time or enable slave timer for a period of time. The counter enable signal is set when TIMx_CTRL1.CNTEN bit is set or the trigger input in gated mode is high. When the counter enable signal is controlled by the trigger input, there is a delay on TRGO except if the master/slave mode is selected (refer to the description of the TIMx_SMCTRL.MSMD bit). 010: Update - The update event is selected as the trigger output (TRGO). For example, a master timer clock can be used as a slave timer prescaler. 011: Compare pulse - Triggers the output to send a positive pulse (TRGO) when the TIMx_STS.CC1ITF is to be set (even if it is already high), when a capture or a comparison succeeds.

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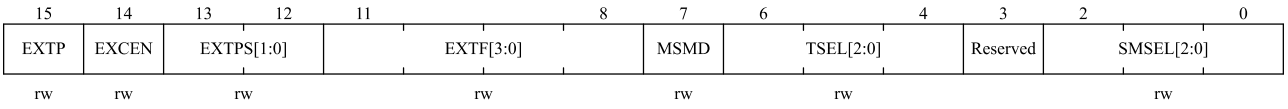
Bit Field	Name	Description
		100: Compare - OC1REF signal is used as the trigger output (TRGO). 101: Compare - OC2REF signal is used as the trigger output (TRGO). 110: Compare - OC3REF signal is used as the trigger output (TRGO). 111: Compare - OC4REF signal is used as the trigger output (TRGO).
3	Reserved	Reserved, the reset value must be maintained
2	CCUSEL	Capture/compare control update selection 0: If TIMx_CTRL2.CCPCTL = 1, they can only be updated by setting CCUDGN bit 1: If TIMx_CTRL2.CCPCTL = 1, they can be updated by setting CCUDGN bit or a rising edge on TRGI. *Note: This bit only applied to channels with complementary outputs.*
1	Reserved	Reserved, the reset value must be maintained
0	CCPCTL	Capture/compare preloaded control 0: No preloading of CCxEN, CCxNEN and OCxMD bits occurs. 1: Preloading of CCxEN, CCxNEN and OCxMD bits occurs. they are updated only when a commutation event COM occurs (TIMx_EVTGEN.CCUDGN bit set or rising edge on TRGI depending on CCUSEL bit) *Note: This bit only applied to channels with complementary outputs.*

8.4.4 Slave Mode Control Register (TIMx_SMCTRL)

Offset address: 0x08

Reset value: 0x0000



Bit Field	Name	Description
15	EXTP	External trigger polarity This bit is used to select whether the trigger operation is to use ETR or the inversion of ETR. 0: ETR active at high level or rising edge. 1: ETR active at low level or falling edge.
14	EXCEN	External clock enable This bit is used to enable external clock mode 2, and the counter is driven by any active edge on the ETRF signal in this mode. 0: External clock mode 2 disable. 1: External clock mode 2 enable. *Note 1: When external clock mode 1 and external clock mode 2 are enabled at the same time, the input of the external clock is ETRF.* *Note 2: The following slave modes can be used simultaneously with external clock mode 2: reset mode, gated mode and trigger mode; however, TRGI cannot connect to ETRF (TIMx_SMCTRL.TSEL ≠ '111').*

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Bit Field	Name	Description
		Note 3: Setting the TIMx_SMCTRL.EXCEN bit has the same effect as selecting external clock mode 1 and connecting TRGI to ETRF (TIMx_SMCTRL.SMSEL = 111 and TIMx_SMCTRL.TSEL = 111).
13:12	EXTPS[1:0]	External trigger prescaler The frequency of the external trigger signal ETRP must be at most 1/4 of TIMxCLK frequency. When a faster external clock is input, a prescaler can be used to reduce the frequency of ETRP. 00: Prescaler disable 01: ETRP frequency divided by 2 10: ETRP frequency divided by 4 11: ETRP frequency divided by 8
11:8	EXTF[3:0]	External trigger filter These bits are used to define the frequency at which the ETRP signal is sampled and the bandwidth of the ETRP digital filtering. In effect, the digital filter is an event counter that generates a validate output after consecutive N events are recorded. 0000: No filter, sampling at f_{DTS} 0001: $f_{SAMPLING} = f_{CK\_INT}$, N = 2 0010: $f_{SAMPLING} = f_{CK\_INT}$, N = 4 0011: $f_{SAMPLING} = f_{CK\_INT}$, N = 8 0100: $f_{SAMPLING} = f_{DTS}/2$, N = 6 0101: $f_{SAMPLING} = f_{DTS}/2$, N = 8 0110: $f_{SAMPLING} = f_{DTS}/4$, N = 6 0111: $f_{SAMPLING} = f_{DTS}/4$, N = 8 1000: $f_{SAMPLING} = f_{DTS}/8$, N = 6 1001: $f_{SAMPLING} = f_{DTS}/8$, N = 8 1010: $f_{SAMPLING} = f_{DTS}/16$, N = 5 1011: $f_{SAMPLING} = f_{DTS}/16$, N = 6 1100: $f_{SAMPLING} = f_{DTS}/16$, N = 8 1101: $f_{SAMPLING} = f_{DTS}/32$, N = 5 1110: $f_{SAMPLING} = f_{DTS}/32$, N = 6 1111: $f_{SAMPLING} = f_{DTS}/32$, N = 8
7	MSMD	Master/ Slave mode 0: No action 1: Events on the trigger input (TRGI) are delayed to allow a perfect synchronization between the current timer (via TRGO) and its slaves. This is useful when several timers are required to be synchronized to a single external event.

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Bit Field	Name	Description
6:4	TSEL[2:0]	Trigger selection These 3 bits are used to select the trigger input of the synchronous counter. 000: Internal trigger 0 (ITR0) 100: TI1 edge detector (TI1F_ED) 001: Internal trigger 1 (ITR1) 101: Filtered timer input 1 (TI1FP1) 010: Internal trigger 2 (ITR2) 110: Filtered timer input 2 (TI2FP2) 011: Internal trigger 3 (ITR3) 111: External triggered Input (ETRF) For more details on ITRx, refer to Table 8-2 below. *Note: These bits must be changed only when not in use (e. g. TIMx_SMCTRL.SMSEL=000) to avoid false edge detection at the transition.*
3	Reserved	Reserved, the reset value must be maintained
2:0	SMSEL[2:0]	Slave mode selection When an external signal is selected, the active edge of the trigger signal (TRGI) is linked to the selected external input polarity (refer to input control register and control register description) 000: Disable slave mode. If TIMx_CTRL1.CNTEN = 1, the prescaler is driven directly by the internal clock. 001: reserved. 010: reserved. 011: reserved. 100: Reset mode. On the rising edge of the selected trigger input (TRGI), the counter is reinitialized and the shadow register is updated. 101: Gated mode. When the trigger input (TRGI) is high, the clock of the counter is enabled. Once the trigger input becomes low, the counter stops counting, but is not reset. In this mode, the start and stop of the counter are controlled. 110: Trigger mode. When a rising edge occurs on the trigger input (TRGI), the counter is started but not reset. In this mode, only the start of the counter is controlled. 111: External clock mode 1. The counter is clocked by the rising edge of the selected trigger input (TRGI). *Note: Do not use gated mode if TI1F_ED is selected as the trigger input (TIMx_SMCTRL.TSEL=100). This is because TI1F_ED outputs a pulse for each TI1F transition, whereas gated mode checks the level of the triggered input.*

Table 8-2 TIMx Internal Trigger Connection

Slave timer	ITR0 (TSEL = 000)	ITR1 (TSEL = 001)	ITR2 (TSEL = 010)	ITR3 (TSEL = 011)
TIM1	NA	NA	TIM3	NA

8.4.5 Interrupt Enable Register (TIMx_DINTEN)

Offset address: 0x0C

Reset value: 0x0000

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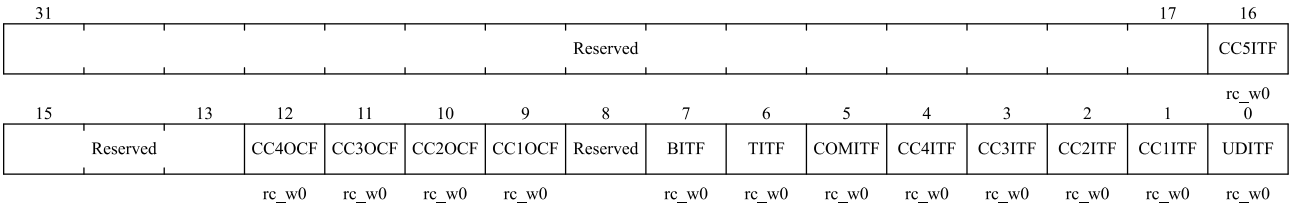
Bit Field	Name	Description
15:8	Reserved	Reserved, the reset value must be maintained
7	BIEN	Break interrupt enable 0: Disable break interrupt 1: Enable break interrupt
6	TIEN	Trigger interrupt enable 0: Disable trigger interrupt 1: Enable trigger interrupt
5	COMIEN	COM interrupt enable 0: Disable COM interrupt 1: Enable COM interrupt
4	CC4IEN	Capture/Compare 4 interrupt enable 0: Disable capture/compare 4 interrupt 1: Enable capture/compare 4 interrupt
3	CC3IEN	Capture/Compare 3 interrupt enable 0: Disable capture/compare 3 interrupt 1: Enable capture/compare 3 interrupt
2	CC2IEN	Capture/Compare 2 interrupt enable 0: Disable capture/compare 2 interrupt 1: Enables capture/compare 2 interrupt
1	CC1IEN	Capture/Compare 1 interrupt enable 0: Disable capture/compare 1 interrupt 1: Enables capture/comparing 1 interrupt
0	UIEN	Update interrupt enable 0: Disable update interrupt 1: Enables update interrupt

8.4.6 Status Register (TIMx_STS)

Offset address: 0x10

Reset value: 0x0000 0000



Bit Field	Name	Description
31:17	Reserved	Reserved, the reset value must be maintained

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Bit Field	Name	Description
16	CC5ITF	Capture/Compare 5 interrupt flag Refer to TIMx_STS.CC1ITF description.
15:13	Reserved	Reserved, the reset value must be maintained
12	CC4OCF	Capture/Compare 4 overcapture flag Refer to TIMx_STS.CC1OCF description.
11	CC3OCF	Capture/Compare 3 overcapture flag Refer to TIMx_STS.CC1OCF description.
10	CC2OCF	Capture/Compare 2 overcapture flag Refer to TIMx_STS.CC1OCF description.
9	CC1OCF	Capture/Compare 1 overcapture flag This bit is set by hardware only when the corresponding channel is configured in input capture mode. This bit cleared by software writing 0. 0: No overcapture occurred 1: TIMx_STS.CC1ITF was already set when the value of the counter has been captured in the TIMx_CCDAT1 register.
8	Reserved	Reserved, the reset value must be maintained
7	BITF	Break interrupt flag This bit is set by hardware once the brake input is active. This bit is cleared by software when the brake input becomes inactive. 0: No break event occurred 1: An active level has been detected
6	TITF	Trigger interrupt flag This bit is set by hardware when an active edge is detected on the TRGI input when the slave mode controller is in a mode other than gated. This bit is set by hardware when any edge in gated mode is detected. This bit is cleared by software. 0: No trigger event occurred 1: Trigger interrupt occurred
5	COMITF	COM interrupt flag This bit is set by hardware once a COM event is generated (when TIMx_CCEN.CCxEN, TIMx_CCEN.CCxNEN, TIMx_CCMOD1.OCxMD have been updated). This bit is cleared by software. 0: No COM event occurred 1: COM interrupt pending
4	CC4ITF	Capture/Compare 4 interrupt flag Refer to TIMx_STS.CC1ITF description.
3	CC3ITF	Capture/Compare 3 interrupt flag Refer to TIMx_STS.CC1ITF description.
2	CC2ITF	Capture/Compare 2 interrupt flag Refer to TIMx_STS.CC1ITF description.
1	CC1ITF	Capture/Compare 1 interrupt flag **When the corresponding channel of CC1 is in output mode:**

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Bit Field	Name	Description
		Except in center-aligned mode, this bit is set by hardware when the counter value is the same as the compare value (refer to TIMx_CTRL1.CAMSEL bit description). This bit is cleared by software. 0: No match occurred. 1: The value of TIMx_CNT is the same as the value of TIMx_CCDAT1. When the value of TIMx_CCDAT1 is greater than the value of TIMx_AR, the TIMx_STS.CC1ITF bit will go high if the counter overflows (in up-counting and up/down-counting modes) and underflows in down-counting mode. **When the corresponding channel of CC1 is in input mode:** This bit is set by hardware when the capture event occurs. This bit is cleared by software or by reading TIMx_CCDAT1. 0: No input capture occurred. 1: Input capture occurred. Counter value has captured in the TIMx_CCDAT1. An edge with the same polarity as selected has been detected on IC1.
0	UDITF	Update interrupt flag This bit is set by hardware when an update event occurs under the following conditions: – When TIMx_CTRL1.UPDIS = 0, and repeat counter value overflow or underflow (An update event is generated when the repeat counter equals 0). – When TIMx_CTRL1.UPRS = 0, TIMx_CTRL1.UPDIS = 0, and the TIMx_EVTGEN.UDGN bit is set by software to reinitialize the CNT. – When TIMx_CTRL1.UPRS = 0, TIMx_CTRL1.UPDIS = 0, and the counter CNT is reinitialized by the trigger event. (Refer to TIMx_SMCTRL Register description) This bit is cleared by software. 0: No update event occurred 1: Update interrupt occurred

8.4.7 Event Generation Register (TIMx_EVTGEN)

Offset address: 0x14

Reset values: 0x0000

15	8	7	6	5	4	3	2	1	0
Reserved		BGN	TGN	CCUDGN	CC4GN	CC3GN	CC2GN	CC1GN	UDGN
		w	w	w	w	w	w	w	w

Bit Field	Name	Description
15:8	Reserved	Reserved, the reset value must be maintained
7	BGN	Break generation This bit can generate a break event when set by software. And at this time TIMx_BKDT.MOEN = 0, TIMx_STS.BITF = 1, if the corresponding interrupt is enabled, the corresponding interrupt will be generated. This bit is automatically cleared by hardware. 0: No action 1: Generated a break event

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Bit Field	Name	Description
6	TGN	Trigger generation This bit can generate a trigger event when set by software. And at this time TIMx_STS.TITF = 1, if the corresponding interrupt is enabled, the corresponding interrupt will be generated. This bit is automatically cleared by hardware. 0: No action 1: Generated a trigger event
5	CCUDGN	Capture/Compare control update generation This bit is set by software. And if TIMx_CTRL2.CCPCTL = 1 at this time, the CCxEN, CCxNEN and OCxMD bits are allowed to be updated. This bit is automatically cleared by hardware. 0: No action 1: Generated a COM event *Note: This bit is only valid for channels with complementary outputs.*
4	CC4GN	Capture/Compare 4 generation Refer to TIMx_EVTGEN.CC1GN description.
3	CC3GN	Capture/Compare 3 generation Refer to TIMx_EVTGEN.CC1GN description.
2	CC2GN	Capture/Compare 2 generation Refer to TIMx_EVTGEN.CC1GN description.
1	CC1GN	Capture/Compare 1 generation This bit can generate a capture/compare event when set by software. This bit is automatically cleared by hardware. When the corresponding channel of CC1 is in output mode: The TIMx_STS.CC1ITF flag will be pulled high, if the corresponding interrupt is enabled, and the corresponding interrupt will be generated. When the corresponding channel of CC1 is in input mode: TIMx_CCDAT1 will capture the current counter value, and the TIMx_STS.CC1ITF flag will be pulled high, if the corresponding interrupt is enabled. If The TIMx_STS.CC1ITF is already pulled high, pull TIMx_STS.CC1OCF high. 0: No action 1: Generated a CC1 capture/compare event
0	UDGN	Update generation This bit can generate an update event when set by software. At this time the counter will be reinitialized, and the prescaler counter will be cleared, and the counter will be cleared in center-aligned or up-counting mode, but take the value of the TIMx_AR register in down-counting mode. This bit is automatically cleared by hardware. 0: No action 1: Generated an update event

8.4.8 Capture/Compare Mode Register 1 (TIMx_CCMOD1)

Offset address: 0x18

Reset value: 0x0000

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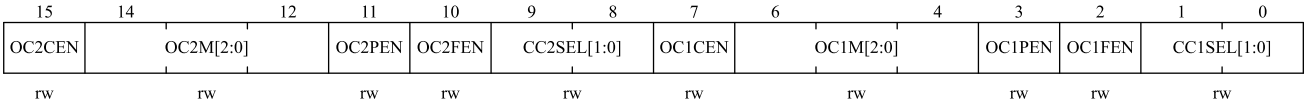
Channels can be used for input (capture mode) or output (compare mode), and the direction of the channel is defined by the corresponding CCxSEL bit. The other bits of the register act differently in input and output modes. OCx describes the function of a channel in output mode, ICx describes the function of a channel in input mode. Hence, please note that the same bit can have different meanings for output mode and for input mode.

Output compare mode:



Bit Field	Name	Description
15	OC2CEN	Output compare 2 clear enable
14:12	OC2MD[2:0]	Output compare 2 mode
11	OC2PEN	Output compare 2 preload enable
10	OC2FEN	Output compare 2 fast enable
9:8	CC2SEL[1:0]	Capture/compare 2 selection These bits are used to select the input/output and input mapping of the channel 00: CC2 channel is configured as output 01: CC2 channel is configured as input, IC2 is mapped on TI2 10: CC2 channel is configured as input, IC2 is mapped on TI1 11: CC2 channel is configured as input, IC2 is mapped on TRC. This mode is only active when the internal trigger input is selected by TIMx_SMCTRL.TSEL. *Note: CC2SEL is writable only when the channel is off (TIMx_CCEN.CC2EN = 0).*
7	OC1CEN	Output compare 1 clear enable 0: OC1REF is not affected by ETRF input level 1: OC1REF is cleared immediately when the ETRF input level is detected as high
6:4	OC1MD[2:0]	Output compare 1 mode These bits are used to manage the output reference signal OC1REF, which determines the values of OC1 and OC1N, and is valid at high levels, while the active levels of OC1 and OC1N depend on the TIMx_CCEN.CC1P and TIMx_CCEN.CC1NP bits. 000: Frozen. Comparison between TIMx_CCDAT1 register and counter TIMx_CNT has no effect on OC1REF signal. 001: Set channel 1 to the active level on match. When TIMx_CCDAT1 = TIMx_CNT, OC1REF signal will be forced high. 010: Set channel 1 as inactive level on match. When TIMx_CCDAT1 = TIMx_CNT, OC1REF signal will be forced low. 011: Toggle. When TIMx_CCDAT1 = TIMx_CNT, OC1REF signal will be toggled. 100: Force to inactive level. OC1REF signal is forced low. 101: Force to active level. OC1REF signal is forced high. 110: PWM mode 1 - In up-counting mode, if TIMx_CNT < TIMx_CCDAT1, OC1REF signal of channel 1 is high, otherwise it is low. In down-counting mode, if TIMx_CNT > TIMx_CCDAT1, OC1REF signal of channel 1 is low, otherwise it is high. 111: PWM mode 2 - In up-counting mode, if TIMx_CNT < TIMx_CCDAT1, OC1REF signal of channel 1 is low, otherwise it is high. In down-counting mode, if TIMx_CNT >

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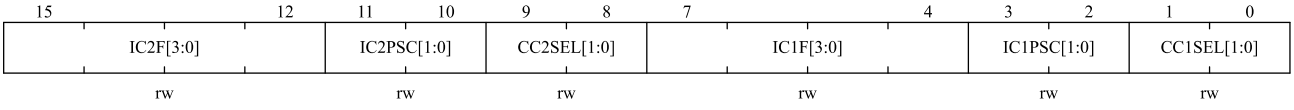
Bit Field	Name	Description
		TIMx_CCDAT1, OC1REF signal of channel 1 is high, otherwise it is low. *Note: in PWM mode 1 or PWM mode 2, the OC1REF level changes only when the comparison result changes or when the output compare mode is switched from frozen mode to PWM mode.*
3	OC1PEN	Output compare 1 preload enable 0: Disable preload function of TIMx_CCDAT1 register. Supports write operations to TIMx_CCDAT1 register at any time, and the written value is effective immediately. 1: Enable preload function of TIMx_CCDAT1 register. Only read and write access to preload registers. When an update event occurs, the value of TIMx_CCDAT1 is loaded into the active register. *Note: only when TIMx_CTRL1.ONEPM = 1(In one-pulse mode), PWM mode can be used without verifying the preload register, otherwise no other behavior can be predicted.*
2	OC1FEN	Output compare 1 fast enable This bit is used to speed up the response of the CC output to the trigger input event. 0: CC1 behaves normally depending on the counter and CCDAT1 values, even if the trigger is ON. The minimum delay for activating CC1 output when an edge occurs on the trigger input is 5 clock cycles. 1: An active edge of the trigger input acts like a comparison match on CC1 output. Therefore, OC is set to the comparison level regardless of the comparison result. The delay time for sampling the trigger input and activating the CC1 output is reduced to 3 clock cycles. OCxFEN only works if the channel is configured in PWM1 or PWM2 mode.
1:0	CC1SEL[1:0]	Capture/compare 1 selection These bits are used to select the input/output and input mapping of the channel 00: CC1 channel is configured as output 01: CC1 channel is configured as input, IC1 is mapped on TI1 10: CC1 channel is configured as input, IC1 is mapped on TI2 11: CC1 channels are configured as inputs and IC1 is mapped to TRC. This mode is only active when the internal trigger input is selected by TIMx_SMCTRL.TSEL. *Note: CC1SEL is writable only when the channel is off (TIMx_CCEN.CC1EN = 0).*

Input capture mode:



Bit field	Name	Description
15:12	IC2F[3:0]	Input capture 2 filter
11:10	IC2PSC[1:0]	Input capture 2 prescaler

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Bit field	Name	Description
9:8	CC2SEL[1:0]	Capture/Compare 2 selection These bits are used to select the input/output and input mapping of the channel 00: CC2 channel is configured as output 01: CC2 channel is configured as input, IC2 is mapped on TI2 10: CC2 channel is configured as input, IC2 is mapped on TI1 11: CC2 channel is configured as input, IC2 is mapped on TRC. This mode is only active when the internal trigger input is selected by TIMx_SMCTRL.TSEL. *Note: CC2SEL is writable only when the channel is off (TIMx_CCEN.CC2EN = 0).*
7:4	IC1F[3:0]	Input capture 1 filter These bits are used to define sampling frequency of TI1 input and the length of digital filter. The digital filter is an event counter that generates an output transition after N events are recorded. 0000: No filter, sampling at f_{DTS} frequency 0001: $f_{SAMPLING} = f_{CK\_INT}$, N = 2 0010: $f_{SAMPLING} = f_{CK\_INT}$, N = 4 0011: $f_{SAMPLING} = f_{CK\_INT}$, N = 8 0100: $f_{SAMPLING} = f_{DTS}/2$, N = 6 0101: $f_{SAMPLING} = f_{DTS}/2$, N = 8 0110: $f_{SAMPLING} = f_{DTS}/4$, N = 6 0111: $f_{SAMPLING} = f_{DTS}/4$, N = 8 1000: $f_{SAMPLING} = f_{DTS}/8$, N = 6 1001: $f_{SAMPLING} = f_{DTS}/8$, N = 8 1010: $f_{SAMPLING} = f_{DTS}/16$, N = 5 1011: $f_{SAMPLING} = f_{DTS}/16$, N = 6 1100: $f_{SAMPLING} = f_{DTS}/16$, N = 8 1101: $f_{SAMPLING} = f_{DTS}/32$, N = 5 1110: $f_{SAMPLING} = f_{DTS}/32$, N = 6 1111: $f_{SAMPLING} = f_{DTS}/32$, N = 8
3:2	IC1PSC[1:0]	Input capture 1 prescaler These bits are used to select the ratio of the prescaler for IC1 (CC1 input). When TIMx_CCEN.CC1EN = 0, the prescaler will be reset. 00: No prescaler, capture is done each time an edge is detected on the capture input 01: Capture is done once every 2 events 10: Capture is done once every 4 events 11: Capture is done once every 8 events
1:0	CC1SEL[1:0]	Capture/Compare 1 selection These bits are used to select the input/output and input mapping of the channel 00: CC1 channel is configured as output 01: CC1 channel is configured as input, IC1 is mapped on TI1 10: CC1 channel is configured as input, IC1 is mapped on TI2 11: CC1 channel is configured as input, IC1 is mapped to TRC. This mode is only active when the internal trigger input is selected by TIMx_SMCTRL.TSEL. *Note: CC1SEL is writable only when the channel is off (TIMx_CCEN.CC1EN = 0).*

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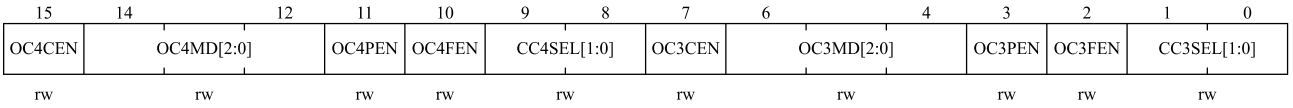
8.4.9 Capture/Compare Mode Register 2 (TIMx_CCMOD2)

Offset address: 0x1C

Reset value: 0x0000

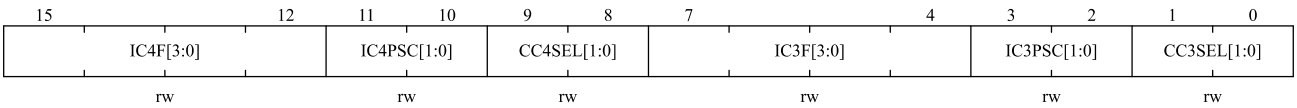
Refer to the description of the CCMOD1 register above

Output comparison mode:



Bit Field	Name	Description
15	OC4CEN	Output compare 4 clear enable
14:12	OC4MD[2:0]	Output compare 4 mode
11	OC4PEN	Output compare 4 preload enable
10	OC4FEN	Output compare 4 fast enable
9:8	CC4SEL[1:0]	Capture/Compare 4 selection These bits are used to select the input/output and input mapping of the channel 00: CC4 channel is configured as output 01: CC4 channel is configured as input, IC4 is mapped on TI4 10: CC4 channel is configured as input, IC4 is mapped on TI3 11: CC4 channel is configured as input, IC4 is mapped on TRC. This mode is only active when the internal trigger input is selected by TIMx_SMCTRL.TSEL. *Note: CC4SEL is writable only when the channel is off (TIMx_CCEN.CC4EN = 0).*
7	OC3CEN	Output compare 3 clear enable
6:4	OC3MD[2:0]	Output compare 3 mode
3	OC3PEN	Output compare 3 preload enable
2	OC3FEN	Output compare 3 fast enable
1:0	CC3SEL[1:0]	Capture/Compare 3 selection These bits are used to select the input/output and input mapping of the channel 00: CC3 channel is configured as output 01: CC3 channel is configured as input, IC3 is mapped to TI3 10: CC3 channel is configured as input, IC3 is mapped on TI4 11: CC3 channel is configured as input, IC3 is mapped to TRC. This mode is only active when the internal trigger input is selected by TIMx_SMCTRL.TSEL. *Note: CC3SEL is writable only when the channel is off (TIMx_CCEN.CC3EN = 0).*

Input capture mode:



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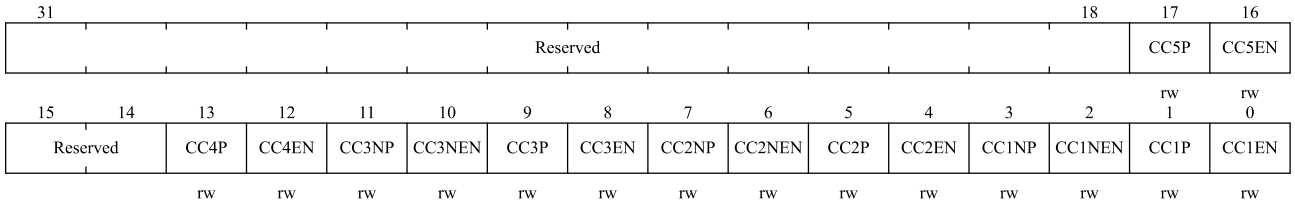
Bit field	Name	Description
15:12	IC4F[3:0]	Input capture 4 filter
11:10	IC4PSC[1:0]	Input capture 4 Prescaler
9:8	CC4SEL[1:0]	Capture/Compare 4 selection These bits are used to select the input/output and input mapping of the channel 00: CC4 channel is configured as output 01: CC4 channel is configured as input, IC4 is mapped on TI4 10: CC4 channel is configured as input, IC4 is mapped on TI3 11: CC4 channel is configured as input, IC4 is mapped on TRC. This mode is only active when the internal trigger input is selected by TIMx_SMCTRL.TSEL. *Note: CC4SEL is writable only when the channel is off (TIMx_CCEN.CC4EN = 0).*
7:4	IC3F[3:0]	Input capture 3 filter
3:2	IC3PSC[1:0]	Input capture 3 Prescaler
1:0	CC3SEL[1:0]	Capture/compare 3 selection These bits are used to select the input/output and input mapping of the channel 00: CC3 channel is configured as output 01: CC3 channel is configured as input, IC3 is mapped to TI3 10: CC3 channel is configured as input, IC3 is mapped on TI4 11: CC3 channel is configured as input, IC3 is mapped to TRC. This mode is only active when the internal trigger input is selected by TIMx_SMCTRL.TSEL. *Note: CC3SEL is writable only when the channel is off (TIMx_CCEN.CC3EN = 0).*

8.4.10 Capture/Compare Enable Register (TIMx_CCEN)

Offset address: 0x20

Reset value: 0x0000 0000



Bit Field	Name	Description
31:18	Reserved	Reserved, the reset value must be maintained
17	CC5P	Capture/Compare 5 output polarity Refer to TIMx_CCEN.CC1P description.
16	CC5EN	Capture/Compare 5 output enable Refer to TIMx_CCEN.CC1EN description.
15:14	Reserved	Reserved, the reset value must be maintained
13	CC4P	Capture/Compare 4 output polarity Refer to TIMx_CCEN.CC1P description.

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Bit Field	Name	Description
12	CC4EN	Capture/Compare 4 output enable Refer to TIMx_CCEN.CC1EN description.
11	CC3NP	Capture/Compare 3 Complementary output polarity Refer to TIMx_CCEN.CC1NP description.
10	CC3NEN	Capture/Compare 3 complementary output enable Refer to TIMx_CCEN.CC1NEN description.
9	CC3P	Capture/Compare 3 output polarity Refer to TIMx_CCEN.CC1P description.
8	CC3EN	Capture/Compare 3 output enable Refer to TIMx_CCEN.CC1EN description.
7	CC2NP	Capture/Compare 2 complementary output polarity Refer to TIMx_CCEN.CC1NP description.
6	CC2NEN	Capture/Compare 2 complementary output enable Refer to TIMx_CCEN.CC1NEN description.
5	CC2P	Capture/Compare 2 output polarity Refer to TIMx_CCEN.CC1P description.
4	CC2EN	Capture/Compare 2 output enable Refer to TIMx_CCEN.CC1EN description.
3	CC1NP	Capture/Compare 1 complementary output polarity 0: OC1N active high 1: OC1N active low
2	CC1NEN	Capture/Compare 1 complementary output enable 0: Disable - Disable output OC1N signal. The level of OC1N depends on the value of these bits TIMx_BKDT.MOEN, TIMx_BKDT.OSSI, TIMx_BKDT.OSSR, TIMx_CTRL2.OI1, TIMx_CTRL2.OI1N and TIMx_CCEN.CC1EN. 1: Enable - Enable output OC1N signal. The level of OC1N depends on the value of these bits TIMx_BKDT.MOEN, TIMx_BKDT.OSSI, TIMx_BKDT.OSSR, TIMx_CTRL2.OI1, TIMx_CTRL2.OI1N and TIMx_CCEN.CC1EN.
1	CC1P	Capture/Compare 1 output polarity When the corresponding channel of CC1 is in output mode: 0: OC1 active high 1: OC1 active low When the corresponding channel of CC1 is in input mode: At this time, this bit is used to select whether IC1 or the inverse signal of IC1 is used as the trigger or capture signal. 0: non-inverted: Capture action occurs when IC1 generates a rising edge. When used as external trigger, IC1 is non-inverted. 1: inverted: Capture action occurs when IC1 generates a falling edge. When used as external trigger, IC1 is inverted. *Note: If TIMx_BKDT.LCKCFG = 3 or 2, these bits cannot be modified.*

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Bit Field	Name	Description
0	CC1EN	Capture/Compare 1 output enable When the corresponding channel of CC1 is in output mode: 0: Disable - Disable output OC1 signal. The level of OC1 depends on the value of these bits TIMx_BKDT.MOEN, TIMx_BKDT.OSSI, TIMx_BKDT.OSSR, TIMx_CTRL2.OI1, TIMx_CTRL2.OI1N and TIMx_CCEN.CC1NEN. 1: Enable - Enable output OC1 signal. The level of OC1N depends on the value of these bits TIMx_BKDT.MOEN, TIMx_BKDT.OSSI, TIMx_BKDT.OSSR, TIMx_CTRL2.OI1, TIMx_CTRL2.OI1N and TIMx_CCEN.CC1NEN. When the corresponding channel of CC1 is in input mode: At this time, this bit is used to disable/enable the capture function. 0: Disable capture 1: Enable capture

Table 8-3 Output Control Bits Of Complementary OCx and OCxN Channels with Break Function

Control Bits					Output State[1)]	
MOEN	OSSI	OSSR	CCxEN	CCxNEN	OCx Output state	OCxN Output state
1	X	0	0	0	Output disabled（not driven by timer） OCx=0,OCx_EN=0	Output disabled（not driven by timer） OCxN=0,OCxN_EN=0
		0	0	1	Output disabled（not driven by timer） OCx=0,OCx_EN=0	OCxREF + polarity, OCxN= OCxREF xor CCxNP,OCxN_EN=1
		0	1	0	OCxREF + polarity, OCx= OCxREF xor CCxP,OCx_EN=1	Output disabled（not driven by timer） OCxN=0,OCxN_EN=0
		0	1	1	OCxREF + polarity + dead-time,OCx_EN=1	Complementary to OCxREF + polarity + dead-time,OCxN_EN=1
		1	0	0	Output disabled（not driven by timer） OCx=CCxP,OCx_EN=0	Output disabled（not driven by timer） OCxN=CCxNP,OCxN_EN=0
		1	0	1	Off-state (Output enabled with inactive state) OCx=CCxP,OCx_EN=1	OCxREF + polarity, OCxN= OCxREF xor CCxNP,OCxN_EN=1
		1	1	0	OCxREF + polarity, OCx= OCxREF xor CCxP, OCx_EN=1	Off-state (Output enabled with inactive state) OCxN=CCxNP,OCxN_EN=1
		1	1	1	OCxREF + polarity + dead-time, OCx_EN=1	Complementary to OCxREF + polarity + dead-time, OCxN_EN=1
0	0	X	0	0	Output disabled（not driven by timer）	
	0		0	1	Asynchronously: OCx=CCxP, OCx_EN=0, OCxN=CCxNP,OCxN_EN=0;	

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Control Bits					Output State[1)]	
MOEN	OSSI	OSSR	CCxEN	CCxNEN	OCx Output state	OCxN Output state
	0		1	0	Then if the clock is present: OCx=OIx and OCxN=OIxN after a dead-time, when	
	0		1	1	(CCxP ^ OIx) ^ (CCxNP^OIxN) != 0.	
	1		0	0	Off-state (Output enabled with inactive state)	
	1		0	1	Asynchronously: OCx=CCxP, OCx_EN=1, OCxN=CCxNP,OCxN_EN=1;	
	1		1	0	Then if the clock is present: OCx=OIx and OCxN=OIxN after a dead-time, when	
	1		1	1	(CCxP ^ OIx) ^ (CCxNP^OIxN) != 0.	

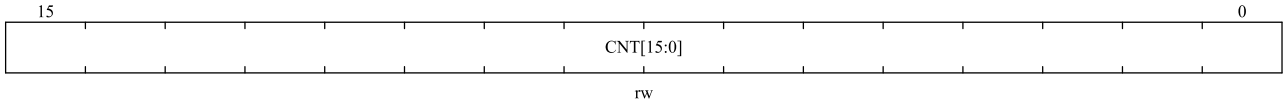
1. If both outputs of a channel are not used (CCxEN = CCxNEN = 0), OIx, OIxN, CCxP and CCxNP must all be cleared.

Note: The status of external I/O pins connected to complementary OCx and OCxN channels depend on the OCx and OCxN channel states and GPIO and AFIO registers.

8.4.11 Counter (TIMx_CNT)

Offset address: 0x24

Reset value: 0x0000

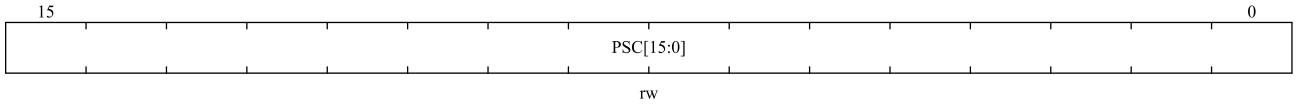


Bit Field	Name	Description
15:0	CNT[15:0]	Counter value

8.4.12 Prescaler (TIMx_PSC)

Offset address: 0x28

Reset value: 0x0000



Bit Field	Name	Description
15:0	PSC[15:0]	Prescaler value Counter clock $f_{CK\_CNT} = f_{CK\_PSC}/$ (PSC [15:0] +1). Each time an update event occurs, the PSC value is loaded into the active prescaler register.

8.4.13 Auto-reload Register (TIMx_AR)

Offset address: 0x2C

Reset values: 0xFFFF

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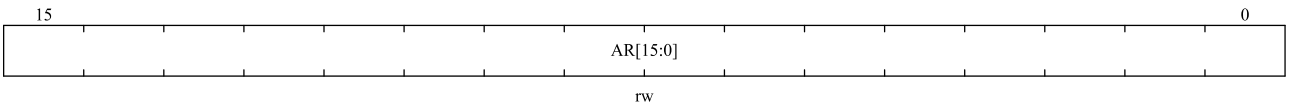
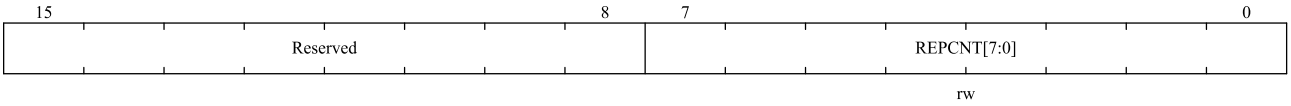


Bit Field	Name	Description
15:0	AR[15:0]	Auto-reload value These bits define the value that will be loaded into the actual auto-reload register. Refer to Section 8.3.1 for more details. When the TIMx_AR.AR [15:0] value is null, the counter does not work.

8.4.14 Repetition Counter Register (TIMx_REPCNT)

Offset address: 0x30

Reset value: 0x0000

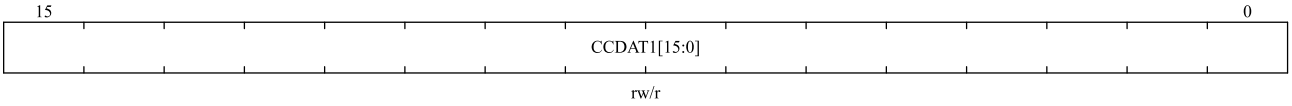


Bit Field	Name	Description
15:8	Reserved	Reserved, the reset value must be maintained
7:0	REPCNT[7:0]	Repetition counter value Repetition counter is used to generate the update event or update the timer registers only after a given number (N+1) cycles of the counter, where N is the value of TIMx_REPCNT.REPCNT. The repetition counter is decremented at each counter overflow in up-counting mode, at each counter underflow in down-counting mode or at each counter overflow and at each counter underflow in center-aligned mode. Setting the TIMx_EVTGEN.UDGN bit will reload the content of TIMx_REPCNT.REPCNT and generate an update event.

8.4.15 Capture/Compare Register 1 (TIMx_CCDAT1)

Offset address: 0x34

Reset value: 0x0000



Bit Field	Name	Description
15:0	CCDAT1[15:0]	Capture/Compare 1 value • CC1 channel is configured as output: CCDAT1 contains the value to be compared to the counter TIMx_CNT, signaling on the OC1 output.

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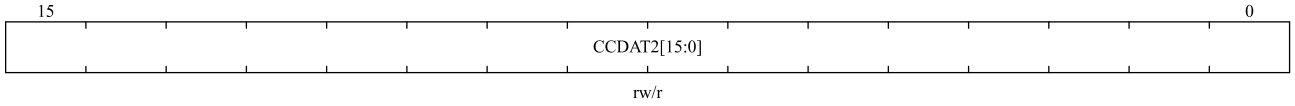
Bit Field	Name	Description
		If the preload feature is not selected in TIMx_CCMOD1.OC1PEN bit, the written value is immediately transferred to the active register. Otherwise, this preloaded value is transferred to the active register only when an update event occurs. • CC1 channel is configured as input: CCDAT1 contains the counter value transferred by the last input capture 1 event (IC1). When configured as input mode, register CCDAT1 and CCDDAT1 are only readable. When configured as output mode, register CCDAT1 and CCDDAT1 are readable and writable.

8.4.16 Capture/Compare Register 2 (TIMx_CCDAT2)

Offset address: 0x38

Reset value: 0x0000

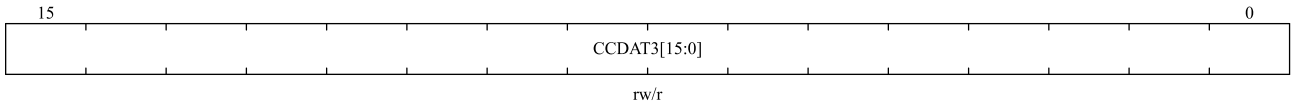


Bit Field	Name	Description
15:0	CCDAT2[15:0]	Capture/Compare 2 values • CC2 channel is configured as output: CCDAT2 contains the value to be compared to the counter TIMx_CNT, signaling on the OC2 output. If the preload feature is not selected in TIMx_CCMOD1.OC2PEN bit, the written value is immediately transferred to the active register. Otherwise, this preloaded value is transferred to the active register only when an update event occurs. • CC2 channel is configured as input: CCDAT2 contains the counter value transferred by the last input capture 2 event (IC2). When configured as input mode, register CCDAT2 and CCDDAT2 are only readable. When configured as output mode, register CCDAT2 and CCDDAT2 are readable and writable.

8.4.17 Capture/Compare Register 3 (TIMx_CCDAT3)

Offset address: 0x3C

Reset value: 0x0000



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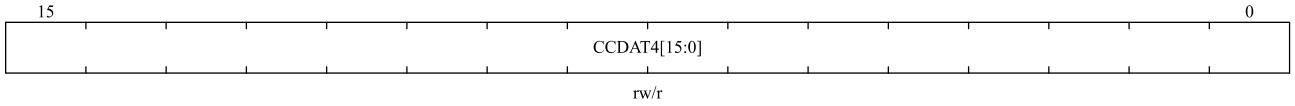
Bit Field	Name	Description
15:0	CCDAT3[15:0]	Capture/Compare 3 value • CC3 channel is configured as output: CCDAT3 contains the value to be compared to the counter TIMx_CNT, signaling on the OC3 output. If the preload feature is not selected in TIMx_CCMOD2.OC3PEN bit, the written value is immediately transferred to the active register. Otherwise, this preloaded value is transferred to the active register only when an update event occurs. • CC3 channel is configured as input: CCDAT3 contains the counter value transferred by the last input capture 3 event (IC3). When configured as input mode, register CCDAT3 and CCDDAT3 are only readable. When configured as output mode, register CCDAT3 and CCDDAT3 are readable and writable.

8.4.18 Capture/Compare Register 4 (TIMx_CCDAT4)

Offset address: 0x40

Reset value: 0x0000

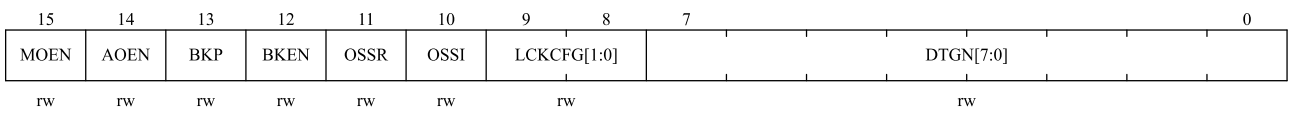


Bit Field	Name	Description
15:0	CCDAT4[15:0]	Capture/Compare 4 value • CC4 channel is configured as output: CCDAT4 contains the value to be compared to the counter TIMx_CNT, signaling on the OC4 output. If the preload feature is not selected in TIMx_CCMOD2.OC4PEN bit, the written value is immediately transferred to the active register. Otherwise, this preloaded value is transferred to the active register only when an update event occurs. • CC4 channel is configured as input: CCDAT4 contains the counter value transferred by the last input capture 4 event (IC4). When configured as input mode, register CCDAT4 and CCDDAT4 are only readable. When configured as output mode, register CCDAT4 and CCDDAT4 are readable and writable.

8.4.19 Break and Dead-time Register (TIMx_BKDT)

Offset address: 0x44

Reset value: 0x0000



Note: AOEN, BKP, BKEN, OSSI, OSSR, and DTGN [7:0] bits can all be write protected depending on the LOCK

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configuration, and it is necessary to configure all of them on the first write to the TIMx_BKDT register.

Bit Field	Name	Description
15	MOEN	Main Output enable This bit can be set by software or hardware depending on the TIMx_BKDT.AOEN bit, and is asynchronously cleared to '0' by hardware once the break input is active. It is only valid for channels configured as outputs. 0: OC and OCN outputs are disabled or forced to idle state. 1: OC and OCN outputs are enabled if TIMx_CCEN.CCxEN or TIMx_CCEN.CCxNEN bits are set. For more details, refer to Section 8.4.10 Capture/Compare enable registers (TIMx_CCEN).
14	AOEN	Automatic output enable 0: Only software can set TIMx_BKDT.MOEN; 1: Software sets TIMx_BKDT.MOEN; or if the break input is not active, when the next update event occurs, hardware automatically sets TIMx_BKDT.MOEN.
13	BKP	Break input polarity 0: Low level of the break input is valid 1: High level of the break input is valid *Note: Any write to this bit requires an APB clock delay to take effect.*
12	BKEN	Break enable 0: Disable break input (BRK and CCS clock failure events) 1: Enable break input (BRK and CCS clock failure events) *Note: Any write to this bit requires an APB clock delay to take effect.*
11	OSSR	Off-state selection for RUN mode This bit is used when TIMx_BKDT.MOEN=1 and the channel is a complementary output. The OSSR bit does not exist in timer without complementary outputs. 0: When inactive, OCx/OCxN outputs are disabled (OCx/OCxN enable output signal = 0) 1: When inactive, OCx/OCxN outputs are enabled with their inactive level as soon as CCxEN = 1 or CCxNEN = 1. Then, OCx/OCxN enable output signal = 1 For more details, Refer to Section 8.4.10, capture/compare enablement registers (TIMx_CCEN).
10	OSSI	Off-state selection for Idle mode This bit is used when TIMx_BKDT.MOEN=0 and the channels configured as outputs. 0: When inactive, OCx/OCxN outputs are disabled (OCx/OCxN enable output signal = 0) 1: When inactive, OCx/OCxN outputs are enabled with their idle level as soon as CCxEN = 1 or CCxNEN = 1. Then, OCx/OCxN enable output signal = 1 For more details, Refer to Section 8.4.10, capture/compare enablement registers (TIMx_CCEN).
9:8	LCKCFG[1:0]	Lock configuration These bits offer a write protection against software errors. 00: No write protected. 01: LOCK Level 1 TIMx_BKDT.DTGN, TIMx_BKDT.BKEN, TIMx_BKDT.BKP, TIMx_BKDT.AOEN, TIMx_CTRL2.OIx, TIMx_CTRL2.OIxN bits enable write protection. 10: LOCK Level 2

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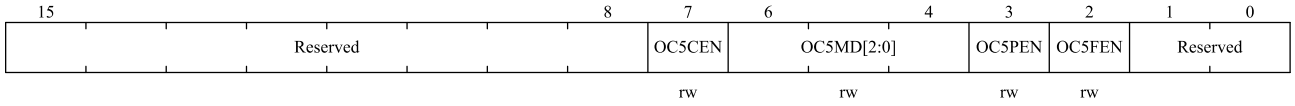
Bit Field	Name	Description
		Except for register write protection in LOCK Level 1 mode, TIMx_CCEN.CCxP and TIMx_CCEN.CCxNP (If the corresponding channel is configured in output mode), TIMx_BKDT.OSSR and TIMx_BKDT.OSSI bits also enable write protection. 11: LOCK Level 3 Except for register write protection in LOCK Level 2, TIMx_CCMODx.OCxMD and TIMx_CCMODx.OCxPEN bits (If the corresponding channel is configured in output mode) also enable write protection. *Note: after the system reset, the LCKCFG bit can only be written once. Once written to the TIMx_BKDT register, LCKCFG will be protected until the next reset.*
7:0	DTGN [7:0]	Dead-time generator These bits define the dead-time duration between inserted complementary outputs. The relationship between the DTGN value and the dead time is as follows: DTGN[7:5] = 0xx: dead time = DTGN[7:0] × (t_{DTS}) DTGN[7:5] = 10x: dead time =(64+DTGN[5:0]) × (2 × t_{DTS}) DTGN[7:5]=110: dead time =(32+DTGN[4:0]) × (8 × t_{DTS}) DTGN [then] = 111: dead time = (32 + DTGN [4:0]) × (16 × t_{DTS}) t_{DTS} value refer to TIMx_CTRL1.CLKD [1:0].

8.4.20 Capture/Compare Mode Register 3(TIMx_CCMOD3)

Offset address: 0x54

Reset value: 0x0000



Bit Field	Name	Description
15:8	Reserved	Reserved, the reset value must be maintained
7	OC5CEN	Output compare 5 clear enable
6:4	OC5MD[2:0]	Output compare 5 mode
3	OC5PEN	Output compare 5 preload enable
2	OC5FEN	Output compare 5 fast enable
1:0	Reserved	Reserved, the reset value must be maintained

8.4.21 Capture/Compare Register 5 (TIMx_CCDAT5)

Offset address: 0x58

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Reset value: 0x0000

Bit Field	Name	Description
15:0	CCDAT5[15:0]	Capture/Compare 5 value • CC5 channel can only configured as output: CCDAT5 contains the value to be compared to the counter TIMx_CNT, signaling on the OC5 output. If the preload feature is not selected in TIMx_CCMOD3.OC5PEN bit, the written value is immediately transferred to the active register. Otherwise, this preloaded value is transferred to the active register only when an update event occurs. TIM1_CC5 and TIM8_CC5 is used for comparator blanking.

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9 General-purpose Timer (TIM3)

9.1 General-purpose Timers Introduction

The general-purpose timer (TIM3) is mainly used in the following scenarios: counting the input signal, measuring the pulse width of the input signal and generating the output waveform, etc.

9.2 Main Features of General-purpose Timer

- 16-bit auto-reload counter. (It can realize up-counting, down-counting, up/down counting)
- 16-bit programmable prescaler. (The prescaler factor can be configured with any value between 1 and 65536)
- Up to 2 channels
- Channel's working modes: PWM output, ouput compare, one-pulse mode output, input capture
- The events that generate the interrupt are as follows:
  - Update event
  - Trigger event
  - Input capture
  - Output compare
- Can be controlled by external signal
- Can be linked internally for timer synchronization or chaining
- Supports capturing internal comparator output signals

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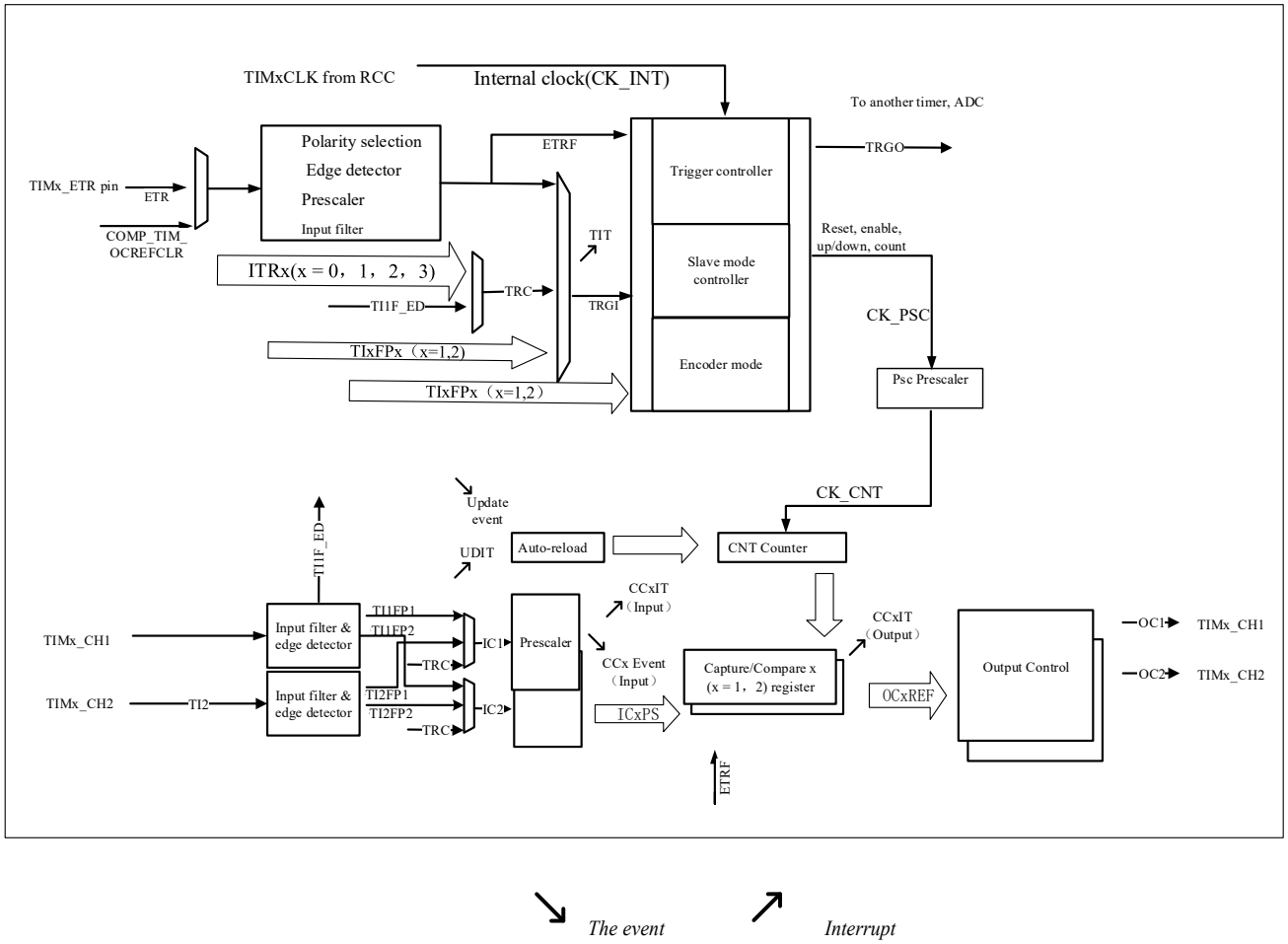
Figure 9-1 Block Diagram of TIMx（x=3）



The capture channel 1 input can come from IOM or comparator output

9.3 General-purpose Timer Description

9.3.1 Time-base Unit

The time-base unit mainly includes: prescaler, counter and auto-reload. When the time base unit is operating, the software can read and write the corresponding registers (TIMx_PSC, TIMx_CNT and TIMx_AR) at any time.

Depending on the setting of the auto-reload preload enable bit (TIMx_CTRL1.ARPEN), the value of the preload register is transferred to the shadow register immediately or at each update event UEV. An update event is generated when the counter reaches the overflow/underflow condition and it can be generated by software when TIMx_CTRL1.UPDIS=0. The counter CK_CNT is valid only when the TIMx_CTRL1.CNTEN bit is set. The counter starts counting one clock cycle after the TIMx_CTRL1.CNTEN bit is set.

9.3.1.1 Prescaler description

The TIMx_PSC register consists of a 16-bit counter that can be used to divide the counter clock frequency by any factor between 1 and 65536. It can be changed on the fly as this register is buffered. The new prescaler value is only taken into account at the next update event.

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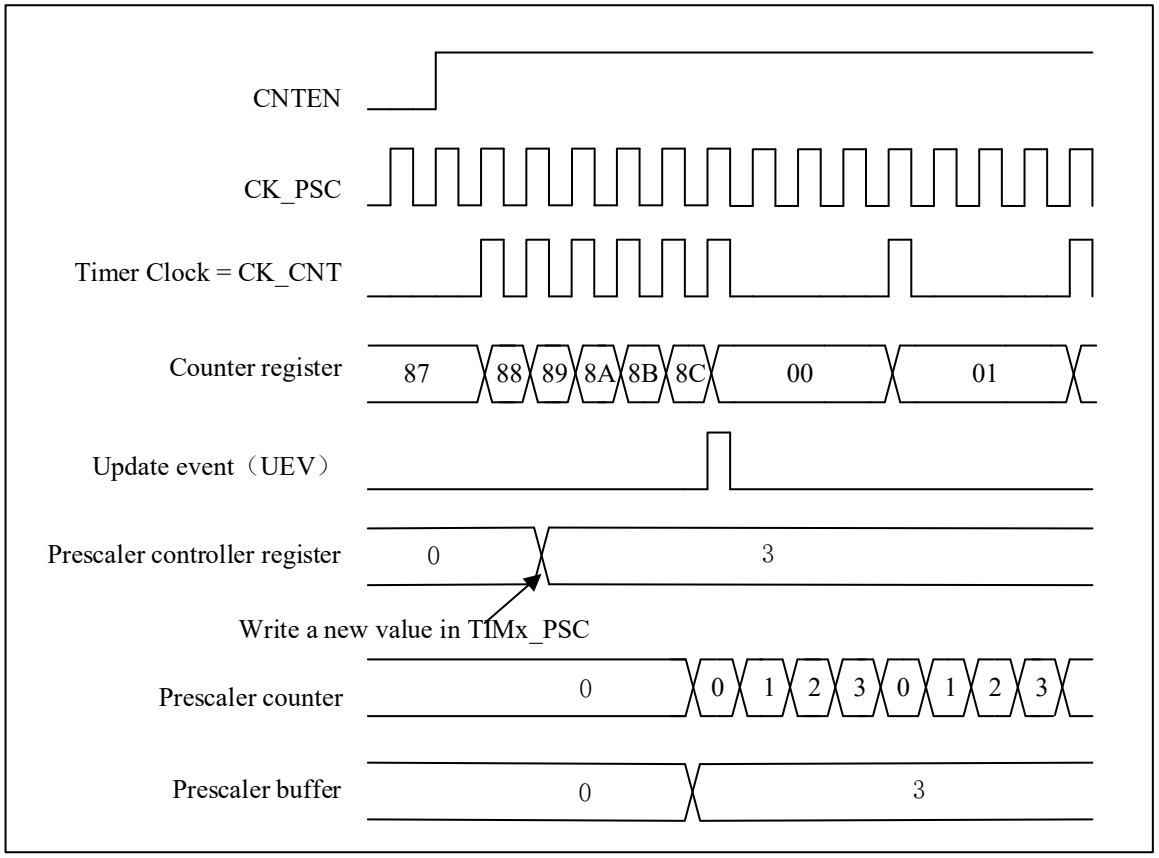
Figure 9-2 Counter Timing Diagram with Prescaler Division Change from 1 to 4



9.3.2 Counter Mode

9.3.2.1 Up-counting mode

In up-counting mode, the counter will count from 0 to the value of the register TIMx_AR, then it resets to 0 and generate a counter overflow event.

If the TIMx_CTRL1.UPRS bit (select update request) and the TIMx_EVTGEN.UDGN bit are set, an update event (UEV) will be generated but without TIMx_STS.UDITF by hardware, thus no update interrupts are generated. This is to avoid generating both update and capture interrupts when clearing the counter on the capture event.

Depending on the update request source configured in TIMx_CTRL1.UPRS, when an update event occurs, all registers are updated and the TIMx_STS.UDITF is set:

- Update auto-reload shadow register with preload value(TIMx_AR), when TIMx_CTRL1.ARPEN = 1.
- The prescaler shadow register is reloaded with the preload value(TIMx_PSC).

To avoid updating the shadow registers when new values are written to the preload registers, the UEV event can be disabled by setting TIMx_CTRL1.UPDIS=1.

When an update event occurs, the counter will still be cleared and the prescaler counter will also be set to 0 (but the prescaler value will remain unchanged).

The figure below shows some examples of the counter behavior and the update flags for different prescaler factors in the up-counting mode.

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Figure 9-3 Timing Diagram of Up-counting with Internal Clock Divider Factor 2/N

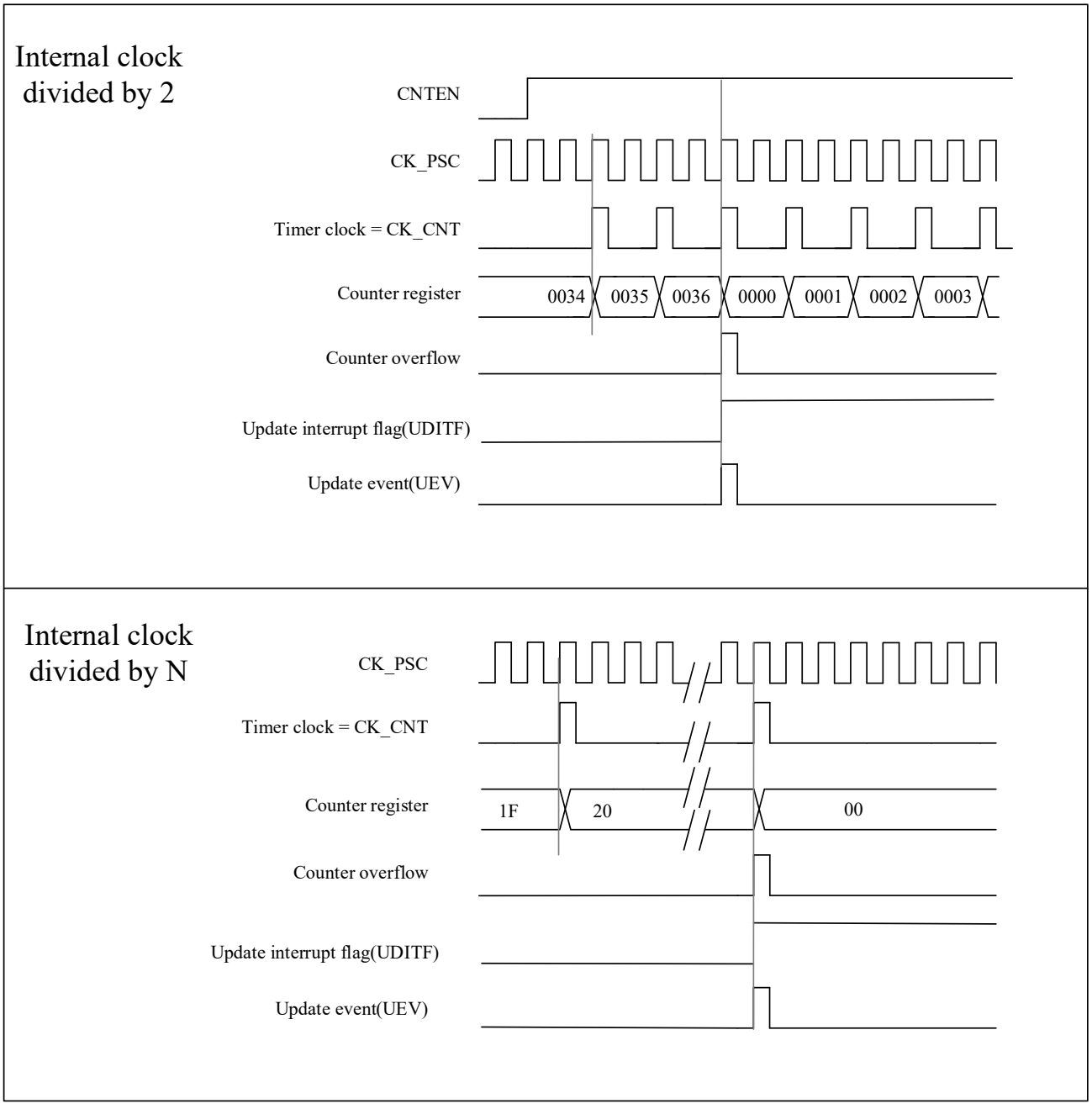

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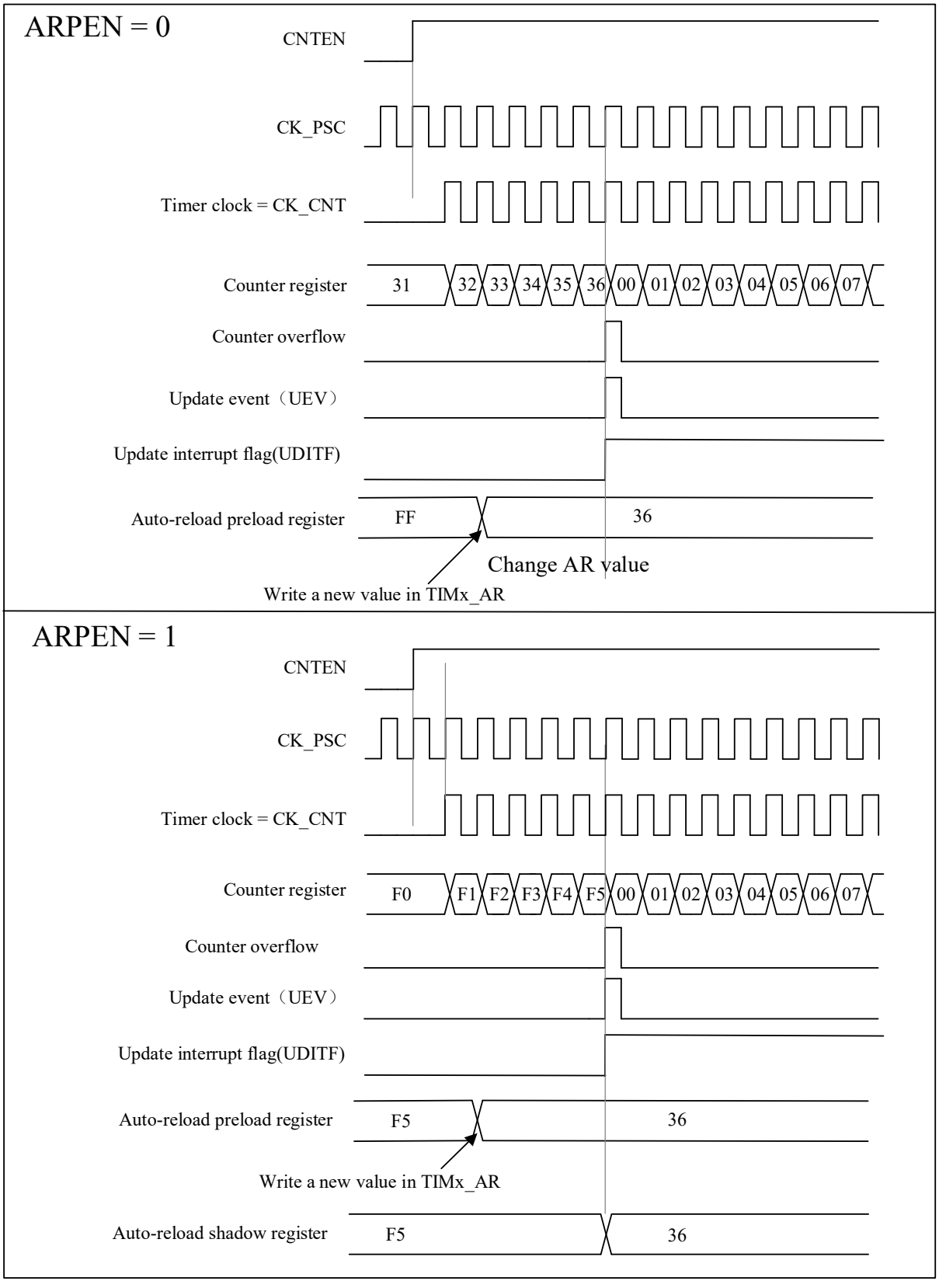
Figure 9-4 Timing Diagram of the Up-counting with Update Event when ARPEN=0/1



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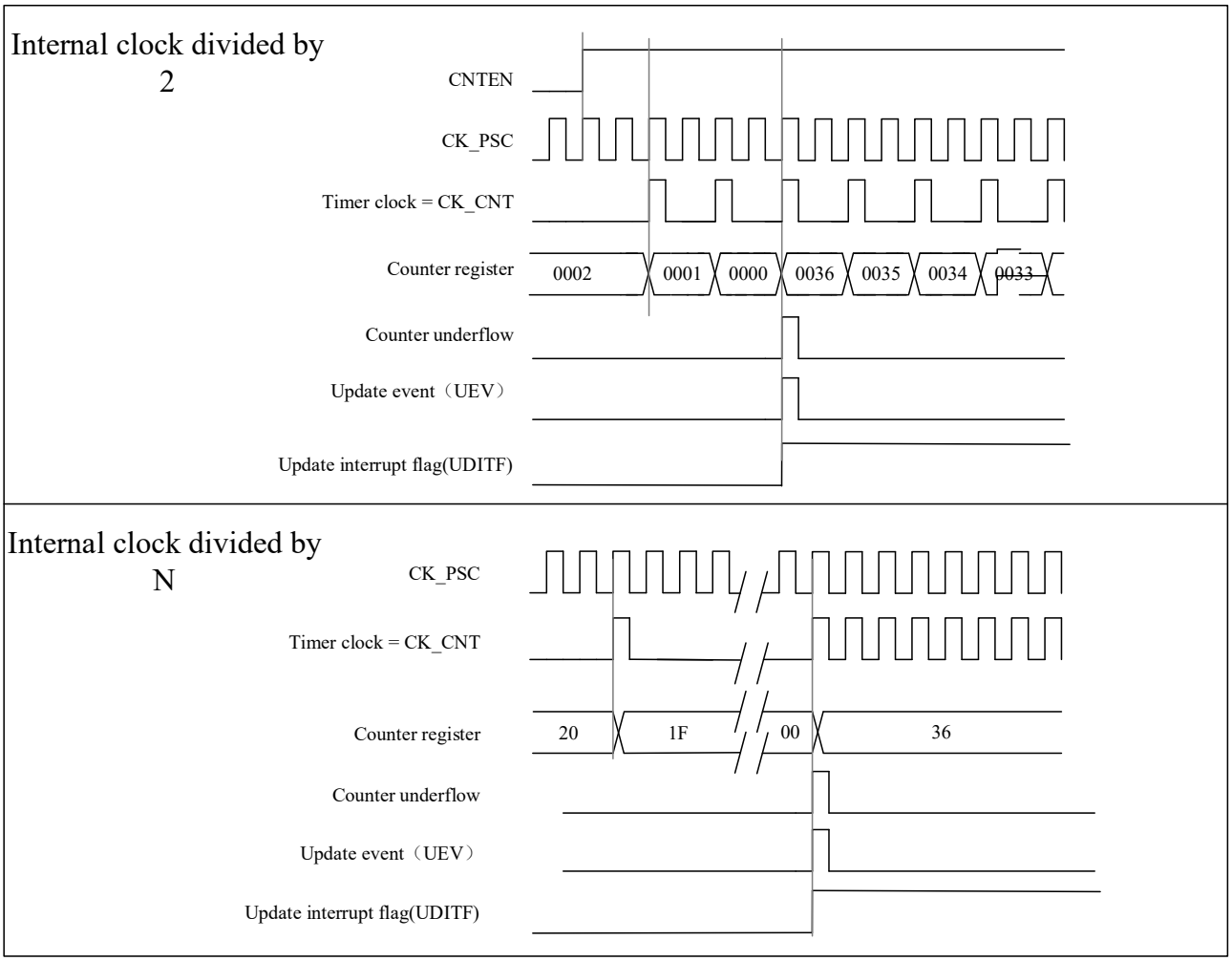
9.3.2.2 Down-counting mode

In down-counting mode, the counter decrements from the value of the register TIMx_AR to 0, then restart from the auto-reload value and generate a counter underflow event.

The process of configuring update events and updating registers in down-counting mode is the same as in up-counting mode, refer to Section 9.3.2.1.

The figure below shows some examples of the counter behavior and the update flags for different division factors in the down-counting mode.

Figure 9-5 Timing Diagram of the Down-counting with Internal Clock Divided Factor 2/N



9.3.2.3 Center-aligned mode

In center-aligned mode, the counter increments from 0 to the value (TIMx_AR) – 1 and generates a counter overflow event, then counts down from the auto-reload value (TIMx_AR) to 1 and generates a counter underflow event. Then the counter resets to 0 and starts counting up again.

In this mode, the TIMx_CTRL1.DIR direction bits have no effect and the count direction is updated and specified by hardware. Center-aligned mode is active when the TIMx_CTRL1. CAMSEL bit is not equal to "00".

An update event can be generated each time the counter overflows and underflows. Alternatively, an update event

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can also be generated by setting the TIMx_EVTGEN. UDGN bit (either by software or using a slave mode controller). In this case, the counter restarts from 0, and prescaler also restart from 0.

Note that if the update source is a counter overflow, the auto-reload is updated before reloading the counter.

Figure 9-6 Timing Diagram of the Center-aligned with Internal Clock Divided Factor 2/N

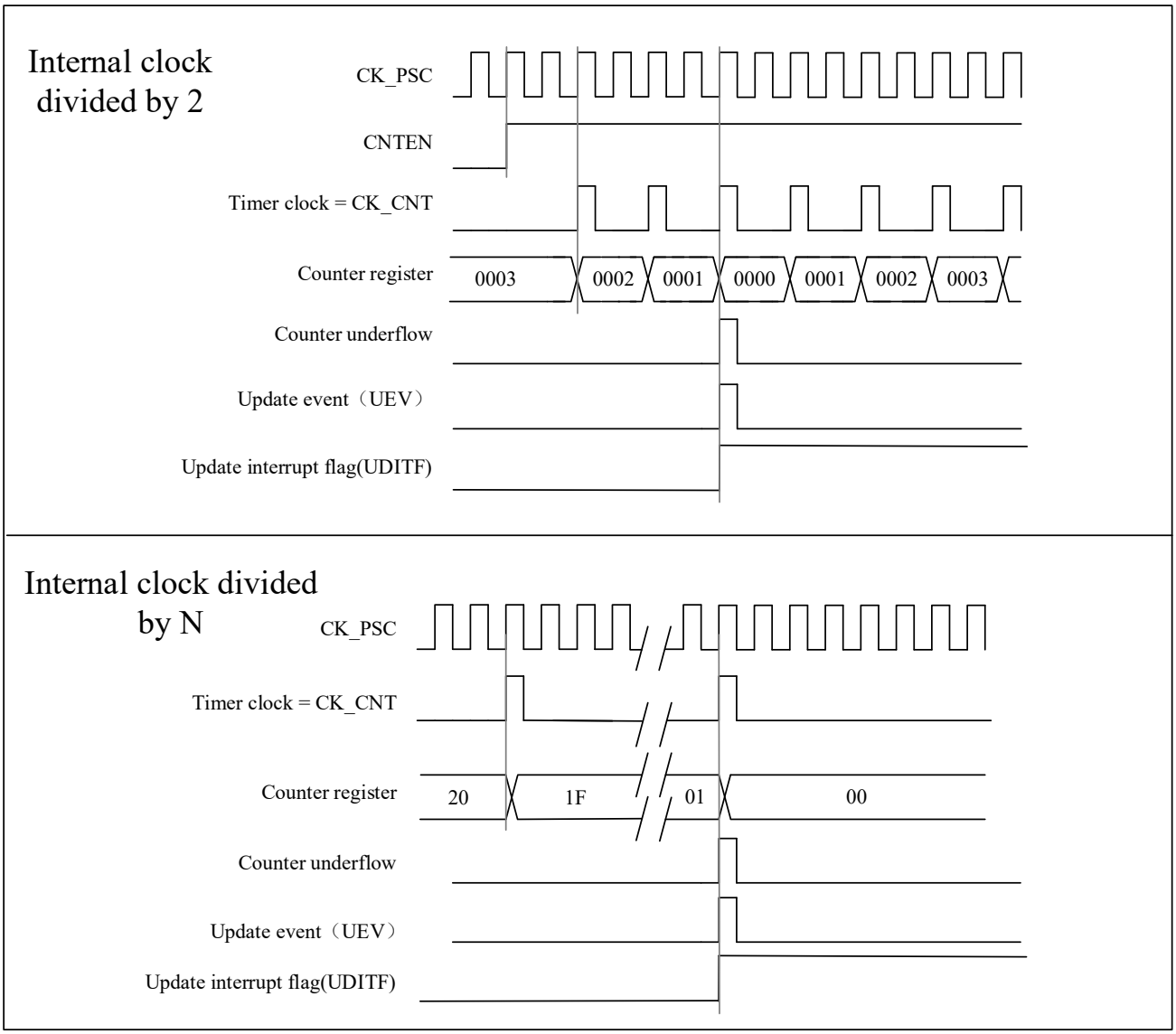

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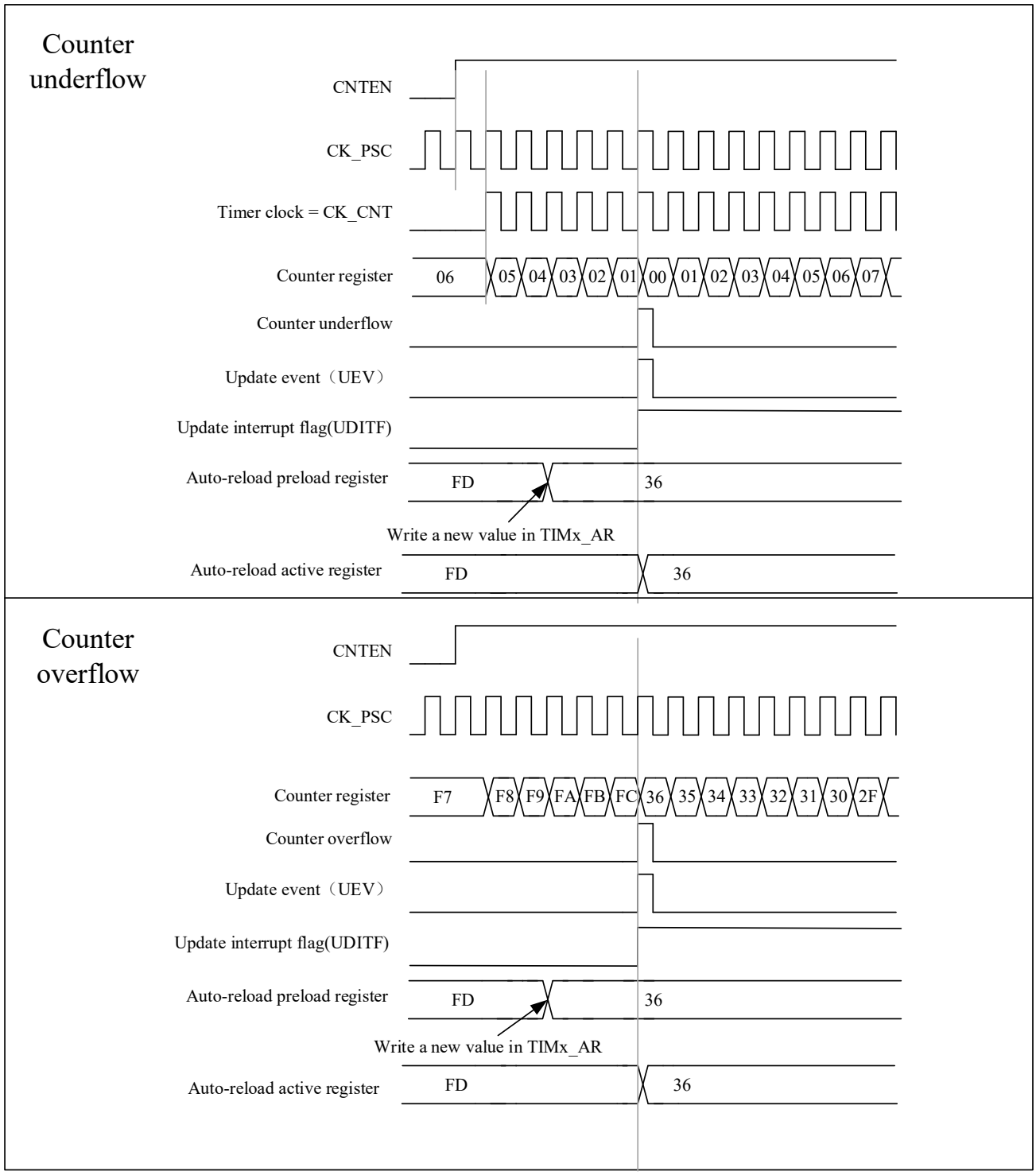
Figure 9-7 Center-aligned Sequence Diagram including Counter Overflows and Underflows (ARPEN = 1)



9.3.3 Clock Selection

- The internal clock of timer: CK_INT
- Two kinds of external clock mode:
  - external input pin

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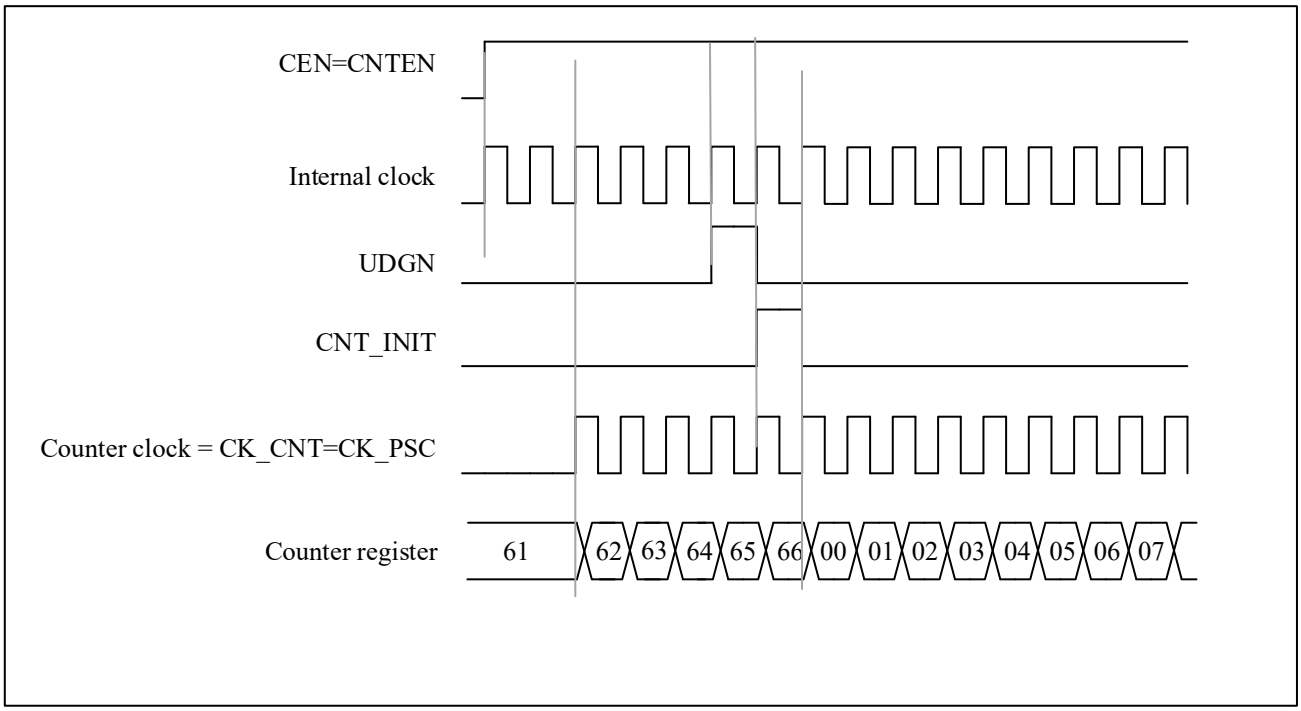
- external trigger input ETR

- Internal trigger input (ITRx): one timer is used as a prescaler for another timer.

9.3.3.1 Internal clock source (CK_INT)

When the TIMx_SMCTRL.SMSEL is equal to “000”, the slave mode controller is disabled. The three control bits (TIMx_CTRL1.CNTEN, TIMx_CTRL1. DIR, TIMx_EVTGEN. UDGN) can only be changed by software (except TIMx_EVTGEN. UDGN, which remains cleared automatically). As soon as the TIMx_CTRL1.CNTEN bit is written as '1' by software, the prescaler is clocked by the internal clock CK_INT.

Figure 9-8 Control Circuit in Normal Mode with Internal Clock Divided by 1



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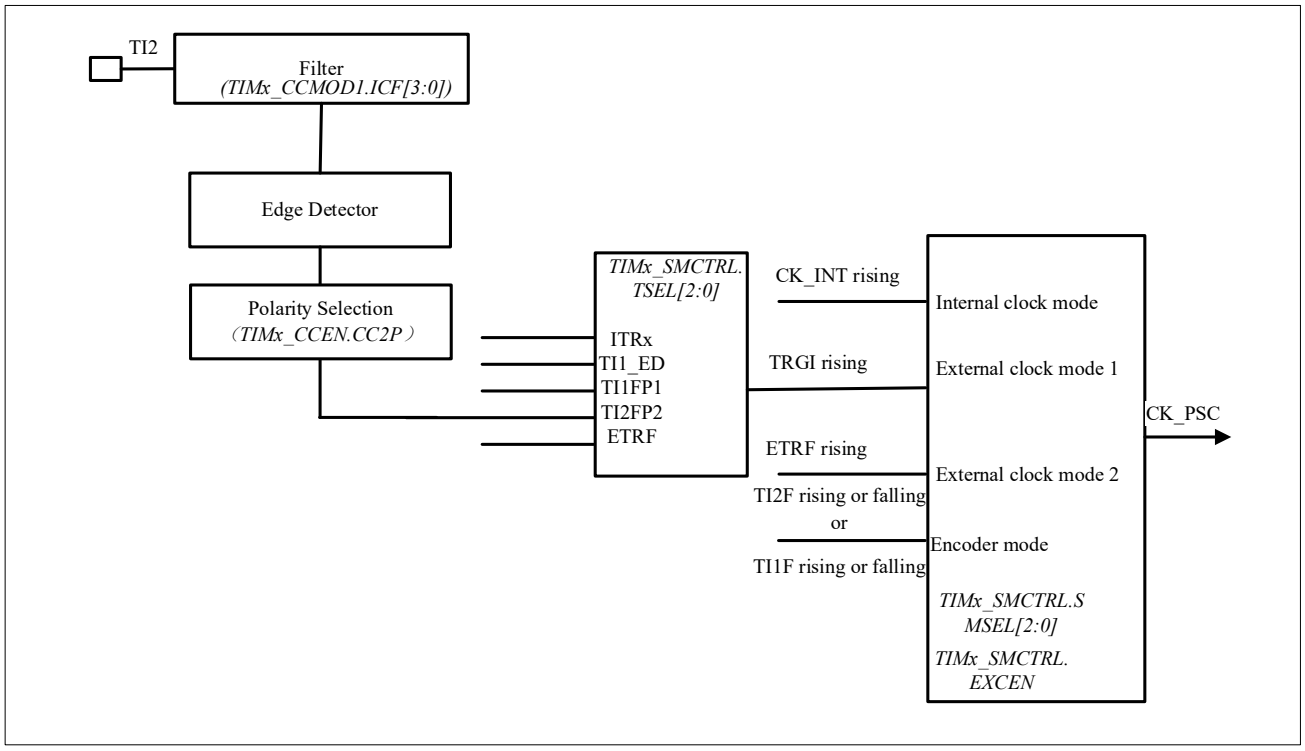
9.3.3.2 External clock source mode 1

Figure 9-9 TI2 External Clock Connection Example



This mode is selected by configuring TIMx_SMCTRL.SMSEL=111. The counter can be configured to count on the rising or falling edge of the clock at the selected input.

For example, to configure up-counting mode to count on the rising edge of the clock at the TI2 input, the configuration steps are as follows:

- Configure TIMx_CCMOD1.CC2SEL to '01'to configured CC2 channel as input, and IC2 is mapped to TI2
- Configure TIMx_CCEN.CC2P to '0' to select clock rising edge polarity
- Configure TIMx_CCMOD1.IC2F[3:0] (if filter is not needed, keep IC2F bit at '0000') to select input filter bandwidth
- Configure TIMx_SMCTRL.SMSEL to '111' to select timer external clock mode 1
- Configure TIMx_SMCTRL.TSEL to '110' to select TI2 as the trigger input source
- Configure TIMx_CTRL1.CNTEN to '1' to start the counter

Note: the capture prescaler is not used for triggering, so it does not need to be configured

When the rising edge of the timer clock occurs at TI2=1, the counter counts once and the TIMx_STS .TITF flag is set.

The delay between the rising edge of TI2 and the actual clock of the counter depends on the resynchronization circuit at the input of TI2.

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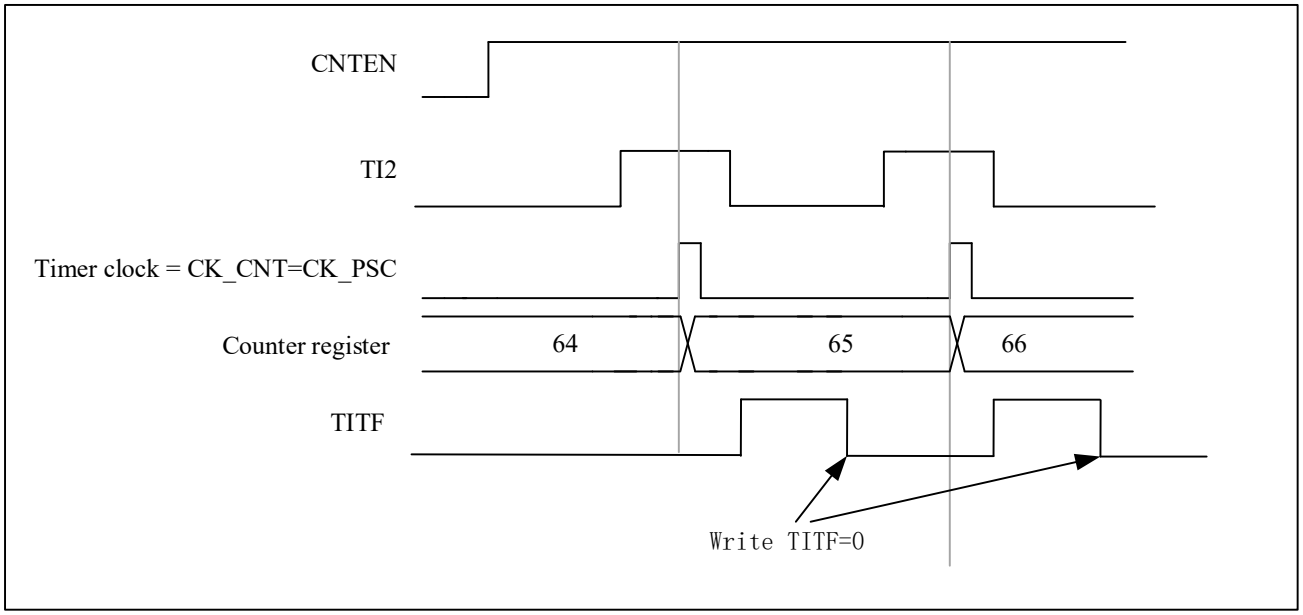
Figure 9-10 Control Circuit in External Clock Mode 1

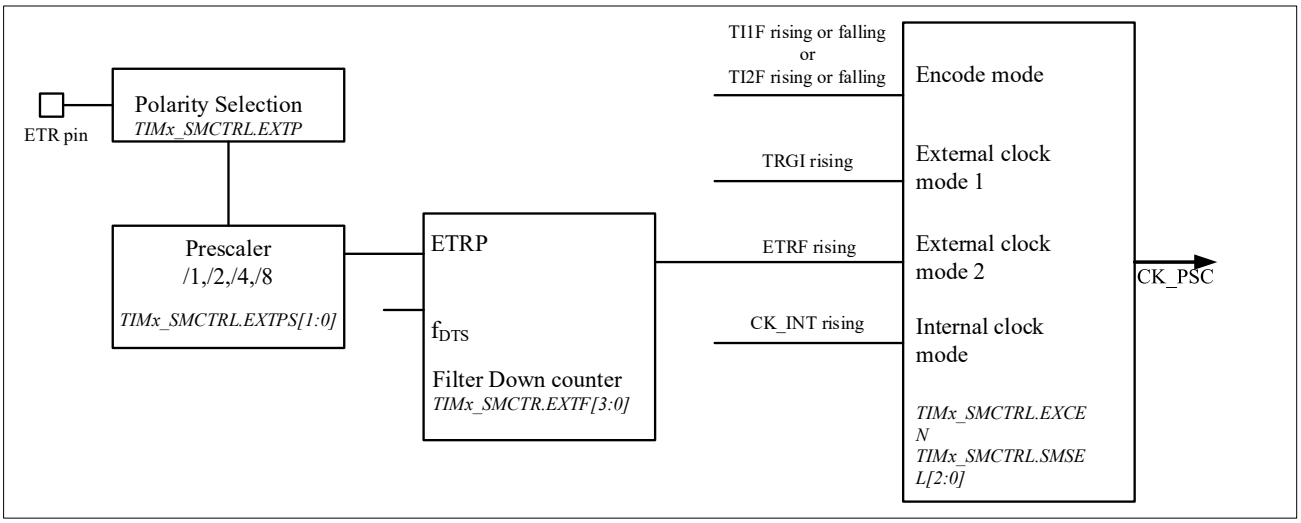


9.3.3.3 External clock source mode 2

This mode is selected by TIMx_SMCTRL .EXCEN equal to 1. The counter can count on every rising or falling edge of the external trigger input ETR.

The following figure is a schematic diagram of the external trigger input module in external clock source mode 2

Figure 9-11 External Trigger Input Block Diagram



For example, to configurate the up counter to count every 2 rising edges on ETR, use the following procedure:

- Since no filter is needed in this case, writeTIMx_SMCTRL .EXTF[3:0] to ‘0000’
- Configure the prescaler by writingTIMx_SMCTRL.EXTPS[1:0] to ‘01’
- Select the polarity of rising edge on ETR pin by setting TIMx_SMCTRL.EXTP to ‘0’
- External clock mode 2 is selected by setting TIMx_SMCTRL .EXCEN to ‘1’

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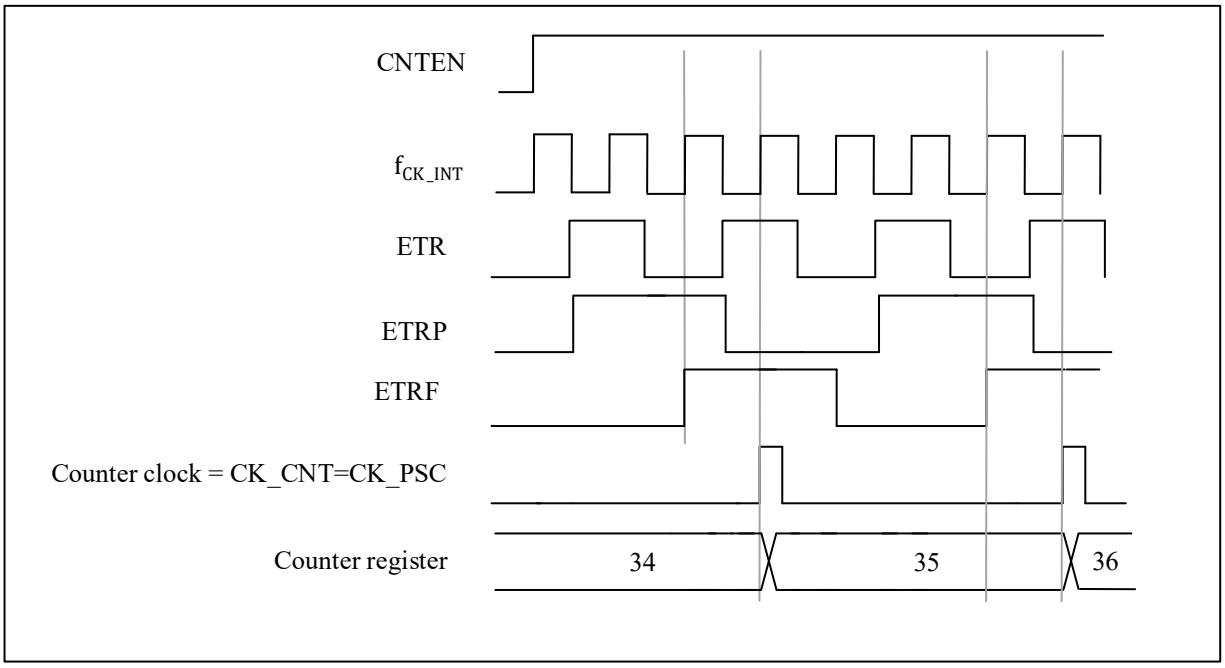
- Turn on the counter by setting TIMx_CTRL1. CNTEN to '1'

The counter counts every 2 rising edges of ETR. The delay between the rising edge of ETR and the actual clock to the counter is due to a resynchronization circuit on the ETRP signal.

Figure 9-12 Control Circuit in External Clock Mode 2



9.3.4 Capture/Compare Channels

The capture/compare channels include a capture/compare register and a shadow register. The input stage consists of digital filters, multiplexers and prescalers. The output stage includes comparator and output control.

The input signal TIx is sampled and filtered to generate the signal TIxF. A signal (TIxF_rising or TIxF_falling) is then generated by the edge detector withthe polarity select function, the polarity of which is selected by the TIMx_CCEN.CCxP bit. This signal can be used as a trigger input for the slave mode controller. At the same time, the signal ICx is sent to the capture register after frequency division. The following figure shows a block diagram of a capture/compare channel.

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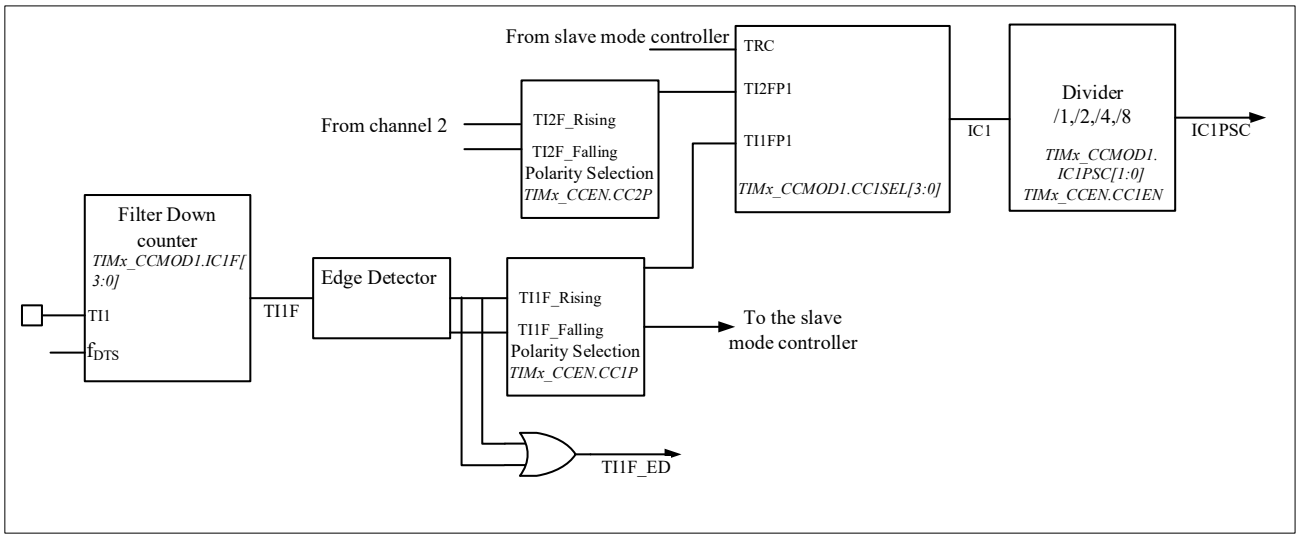
Figure 9-13 Capture/Compare Channel (Example: Channel 1 Input Stage)



The output stage generates an intermediate waveform OCxRef (active high) as reference. The polarity acts at the end of the chain.

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Figure 9-14 Capture/Compare Channel 1 Main Circuit

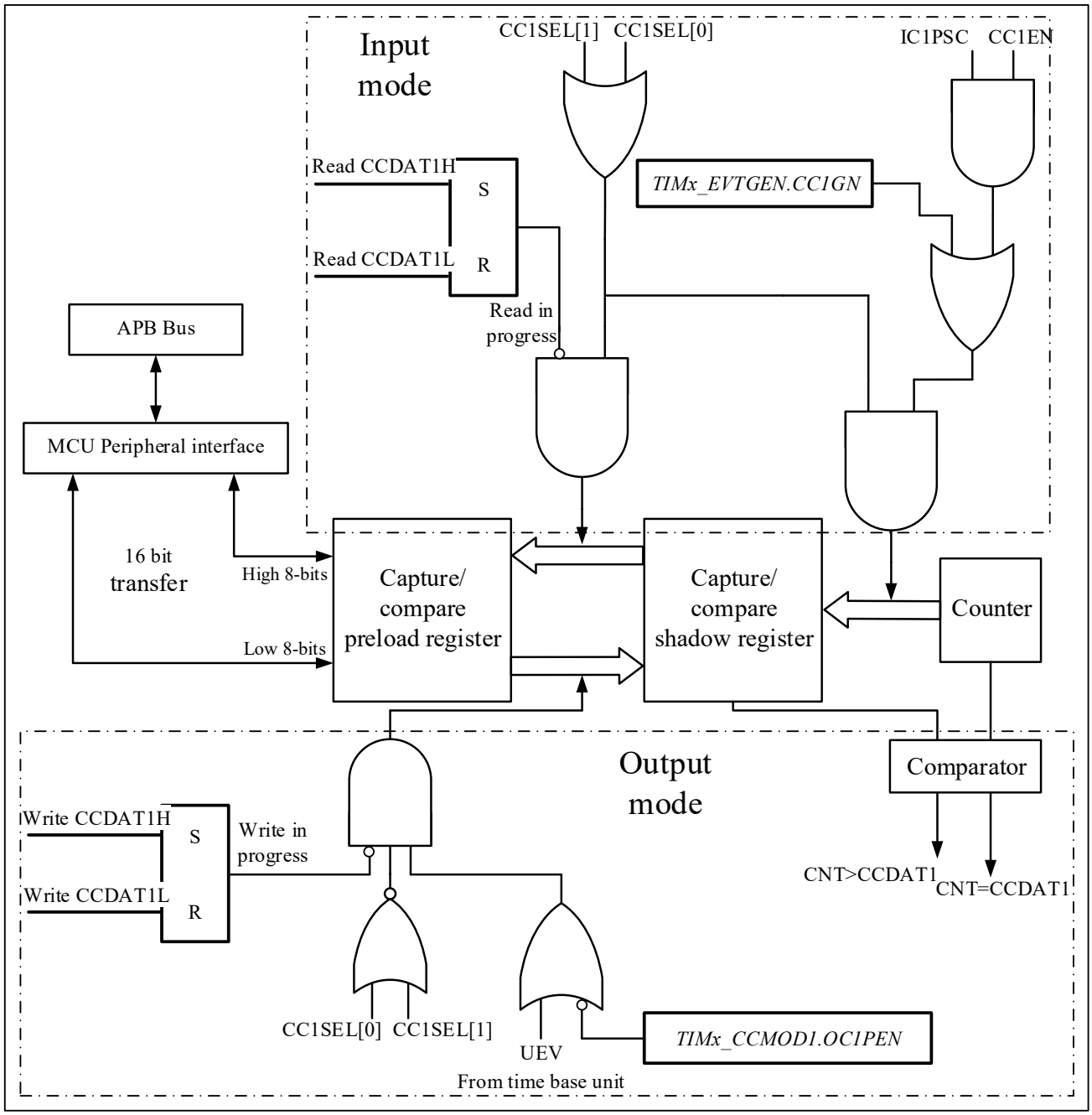

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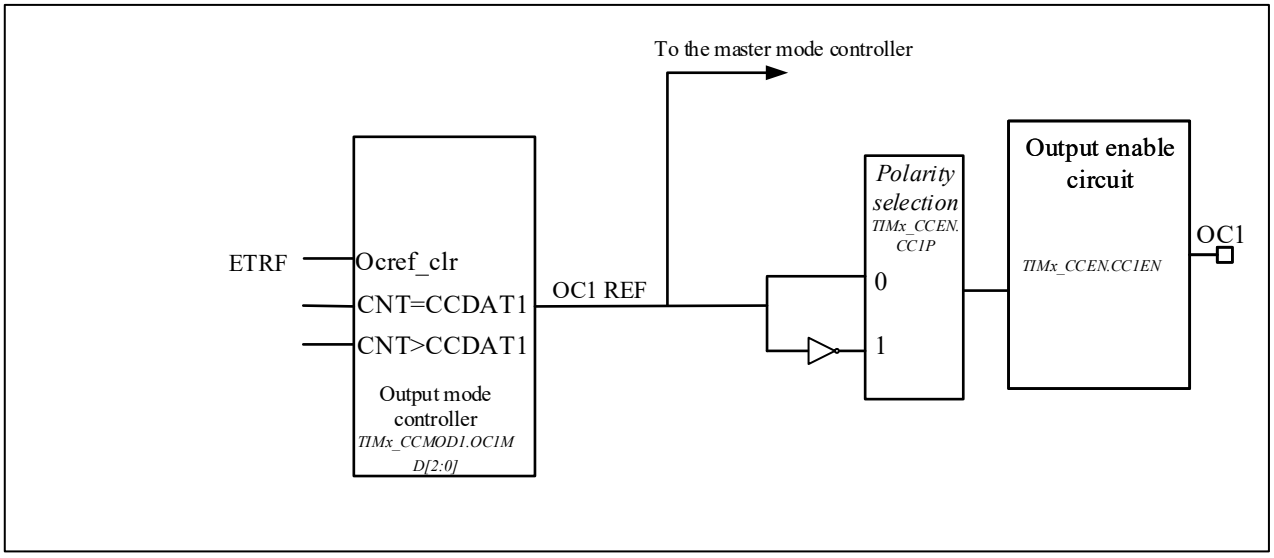
Figure 9-15 Output Part of Channelx (x = 1,2; Take Channel 1 as an Example)



Read and write always access preloaded registers when capturing/comparing. The two specific working processes are as follows:

In capture mode, the capture is actually done in the shadow register, and then the value in the shadow register is copied into the preload register.

In compare mode, as opposed to capture mode, the value of the preload register is copied into the shadow register, which is compared with the counter.

9.3.5 Input Capture Mode

In input capture mode, the TIMx_CCDATx registers are used to latch the counter value after the ICx signal is detected.

There is a capture interrupt flag TIMx_STS.CCxITF, which can trigger an interrupt if the corresponding interrupt enable is pulled high.

The TIMx_STS. CCxITF bit is set by hardware when a capture event occurs and is cleared by software or by reading the TIMx_CCDATx register.

The overcapture flag TIMx_STS.CCxOCF is set when the counter value is captured in the TIMx_CCDATx register and TIMx_STS.CC1ITF is already pulled high. Unlike the former, TIMx_STS.CCxOCF is cleared by writing 0 to it.

To achieve a rising edge of the TI1 input to capture the counter value into the TIMx_CCDAT1 register, the configuration flow is as follows:

- Select a valid input:

  Configure TIMx_CCMOD1.CC1SEL to '01'. At this time, the input is the CC1 channel, and IC1 is mapped to TI1.

- Define the input filter duration required for programming:

  Define the sampling frequency of the TI1 input and the length of the digital filter by configuring the TIMx_CCMODx.ICxF bits. Example: If the input signal jitters up to 5 internal clock cycles, we must choose a filter duration longer than these 5 clock cycles. When 8 consecutive samples (sampled at f_{DTS} frequency) with

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the new level are detected, we can validate the transition on TI1. Then configure TIMx_CCMOD1. IC1F to '0011'.

- By configuring TIMx_CCEN .CC1P=0, select the rising edge as the valid transition polarity on the TI1 channel.
- Configure the input prescaler. In this example, configure TIMx_CCMOD1.IC1PSC= '00' to disable the prescaler because we want to capture every valid transition.
- Enable capture by configuring TIMx_CCEN. CC1EN = '1'.

If needed, enable the related interrupt request by setting the TIMx_DINTEN.CC1IEN.

9.3.6 PWM Input Mode

There are some differences between PWM input mode and normal input capture mode, including:

- Two ICx signals are mapped to the same TIx input.
- The two ICx signals are active on edges of opposite polarity.
- Select one of two TIxFP signals as trigger input.
- The slave mode controller is configured in reset mode.

For example, the following configuration flow can be used to know the period and duty cycle of the PWM signal on TI1 (It depends on the frequency of CK_INT and the value of the prescaler).

- Configure TIMx_CCMOD1.CC1SEL to '01' to select TI1 as valid input for TIMx_CCDAT1.
- Configure TIMx_CCEN.CC1P to '0' to select the active polarity of filtered timer input 1(TI1FP1), active on the rising edge.
- Configure TIMx_CCMOD1.CC2SEL to '10' to select TI1 as valid input for TIMx_CCDAT2.
- Configure TIMx_CCEN.CC2P to '1' to select the valid polarity of filtered timer input 2(TI1FP2), active on the falling edge.
- Configure TIMx_SMCTRL.TSEL=101 to select filtered timer input 1 (TI1FP1) as valid trigger input.
- Configure TIMx_SMCTRL.SMSEL=100 to configure the slave mode controller to reset mode.
- Configure TIMx_CCEN. CC1EN=1 and TIMx_CCEN.CC2EN=1 to enable capture.

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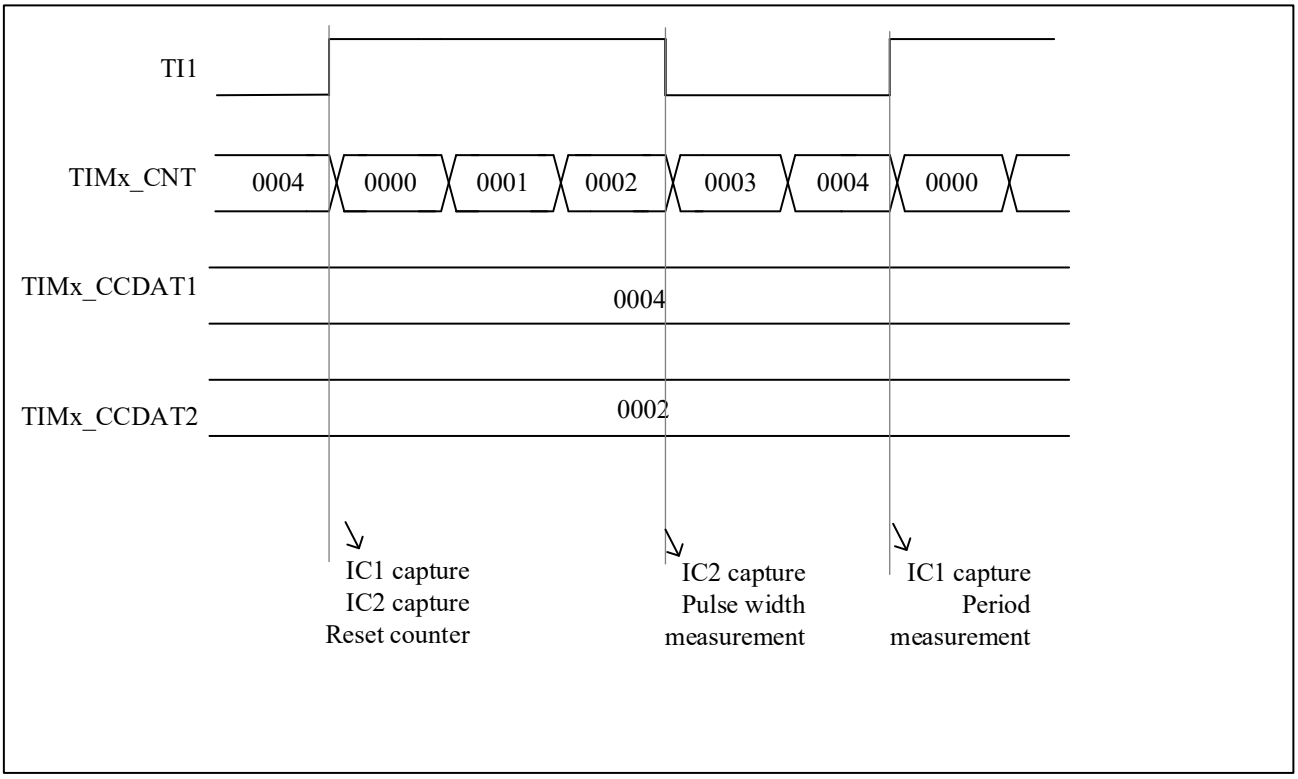
Figure 9-16 PWM Input Mode Timing



Because only filter timer input 1 (TI1FP1) and filter timer input 2 (TI2FP2) are connected to the slave mode controller, the PWM input mode can only be used with the TIMx_CH1/TIMx_CH2 signals.

9.3.7 Forced Output Mode

In output mode (TIMx_CCMODx.CCxSEL=00), software can force output compare signals to active or inactive level directly.

User can set TIMx_CCMODx. OCxMD=101 to force the output compare signal to active level. And the OCxREF will be forced high, OCx get opposite value to CCxP polarity bit. On the other hand, user can set TIMx_CCMODx. OCxMD=100 to force the output compare signal to low level.

The values of the TIMx_CCDATx shadow register and the counter still comparing with each other in this mode. And the flag still can be set. Therefore, the interrupt still can be sent.

The comparison between the output compare register TIMx_CCDATx and the counter TIMx_CNT has no effect on OCxREF. And the flag still can be set. Therefore, the interrupt still can be sent.

9.3.8 Output Compare Mode

User can use this mode to control the output waveform, or to indicate that a period of time has elapsed.

When the capture/compare register and the counter have the same value, the output compare function's operations are as follow:

- TIMx_CCMODx.OCxMD is for output compare mode, and TIMx_CCEN.CCxP is for output polarity. When the compare matches, if TIMx_CCMODx.OCxMD=000, the output pin will keep its level; if set TIMx_CCMODx.OCxMD=001, the output pin will be set active; if set TIMx_CCMODx.OCxMD=010, the

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output pin will be set inactive; if set TIMx_CCMODx.OCxMD=011, the output pin will be set to toggle.

- Set a flag in interrupt status register TIMx_STS.CCxITF.
- If user set TIMx_DINTEN.CCxIEN, a corresponding interrupt will be generated.

User can set TIMx_CCMODx.OCxPEN to choose capture/compare shawdow register using capture/compare preload registers(TIMx_CCDATx).

The time resolution is one count of the counter.

In one pulse mode, the output compare mode can also be used to output a single pulse.

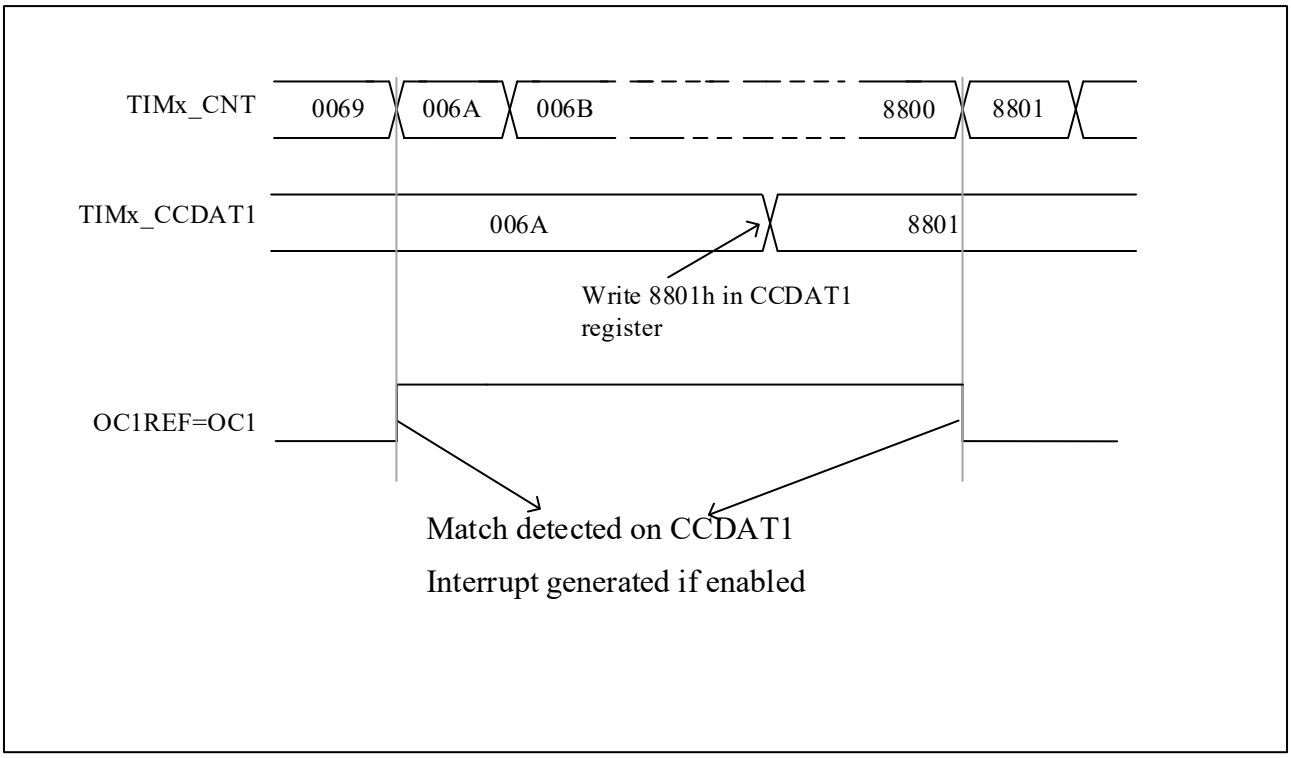
Here are the configuration steps for output compare mode:

- First of all, user should select the counter clock.
- Secondly, set TIMx_AR and TIMx_CCDATx with desired data.
- If user need to generate an interrupt, set TIMx_DINTEN.CCxIEN.
- Then select the output mode by set TIMx_CCEN.CCxP, TIMx_CCMODx.OCxMD, TIMx_CCEN.CCxEN, etc.
- At last, set TIMx_CTRL1.CNTEN to enable the counter.

User can update the output waveform by setting TIMx_CCDATx at any time, as long as the preload register is not enabled. Otherwise the TIMx_CCDATx shadow register will be updated at the next update event.

Here is an example.

Figure 9-17 Output Compare Mode, Toggle on OC1



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9.3.9 PWM Mode

User can use PWM mode to generate a signal with a duty cycle determined by the value of the TIMx_CCDATx register and a frequency determined by the value of the TIMx_AR register. Depending on the value of TIMx_CTRL1.CAMSEL, the TIM can generate PWM signal in edge-aligned mode or center-aligned mode.

User can select PWM mode 1 or PWM mode 2 by setting TIMx_CCMODx. OCxMD=110 or setting TIMx_CCMODx. OCxMD=111. To enable preload register, user must set corresponding TIMx_CCMODx.OCxPEN. And then set TIMx_CTRL1.ARPEN to auto-reload preload register eventually.

User can set polarity of OCx by setting TIMx_CCEN.CCxP. To enable the output of OCx, user need to set the combination of the value of CCxEN.

The values of TIMx_CNT and TIMx_CCDATx are always compared with each other when the TIM is under PWM mode.

Only when an update event occurs, the preload register will transfer to the shadow register. Therefore user must reset all the registers by setting TIMx_EVTGEN.UDGN before the counter starts counting.

9.3.9.1 PWM center-aligned mode

If user set TIMx_CTRL1.CAMSEL to 01, 10 or 11, the PWM center-aligned mode will be active. The setting of the compare flag depends on the value of TIMx_CTRL1.CAMSEL. There are three kinds of situation that the compare flag is set, only when the counter counts up, only when the counter counts down, or both when the counter counts up and counts down. User should not modify TIMx_CTRL1.DIR by software, as it is updated by hardware.

Examples of center-aligned PWM waveforms is as follows, and the settings of the waveform are: TIMx_AR=8, PWM mode 1, the compare flag is set when the counter counts down corresponding to TIMx_CTRL1. CAMSEL=01.

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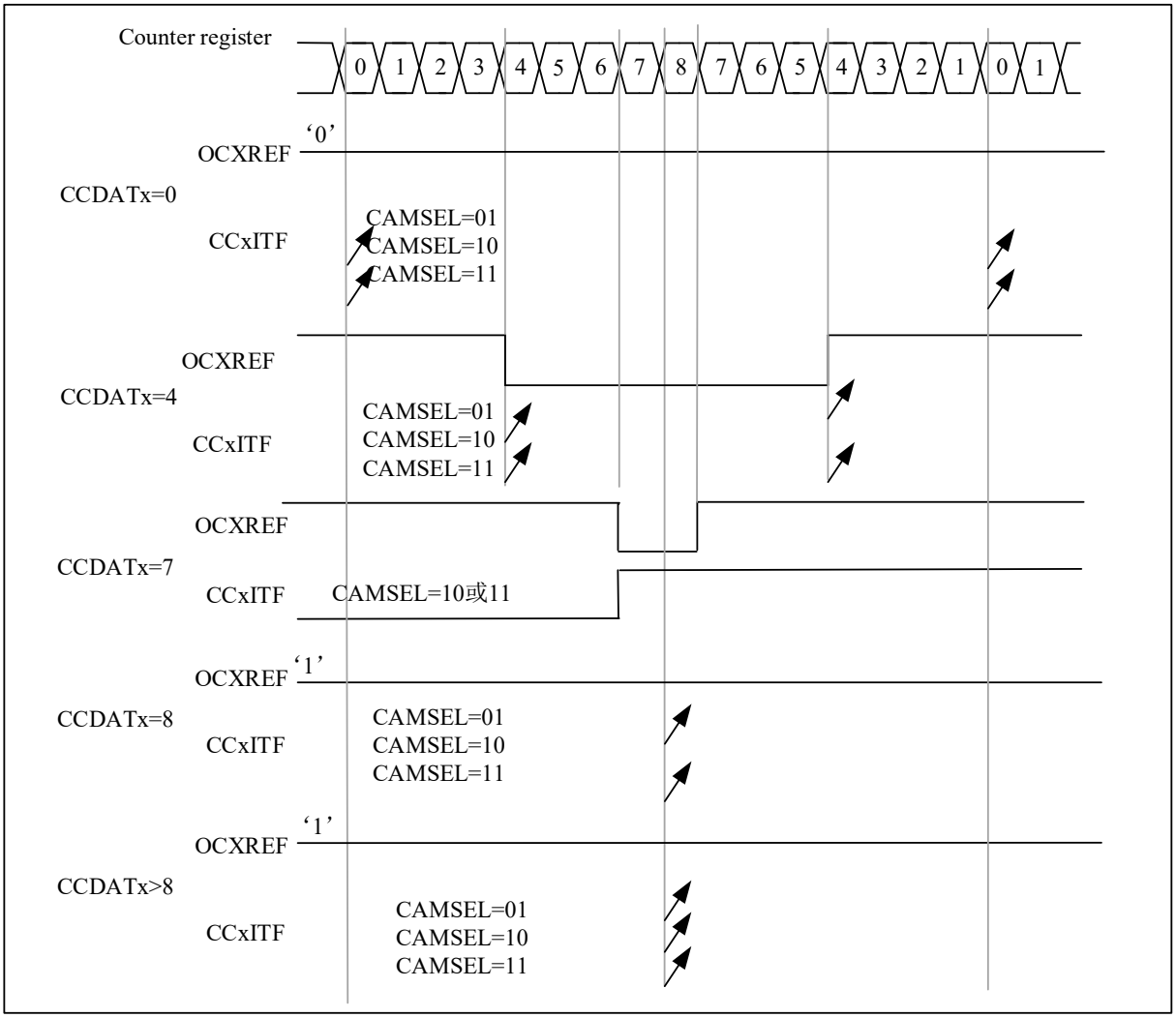
Figure 9-18 Center-aligned PWM Waveform (AR=8)



When using center-aligned mode, users should pay attention to the following considrations

- It depends on the value of TIMx_CTRL1.DIR that the counter counts up or down. Cautions that the DIR and CAMSEL bits should not be changed at the same time.
- User should not write the counter while running in center-aligned mode, otherwise it will cause unexpected results. Here are some example:
  - If the value written into the counter is 0 or is the value of TIMx_AR, the direction will be updated but the update event will not be generated.
  - If the value written into the counter is greater than the value of auto-reload, the direction will not be updated.
- For safety reasons, it is recommended that users set TIMx_EVTGEN.UDGN to generate an update by software before starting the counter, and dot not write the counter while it is running.

9.3.9.2 PWM edge-aligned mode

There are two kinds of configuration in edge-aligned mode, up-counting and down-counting.

- **Up-counting**

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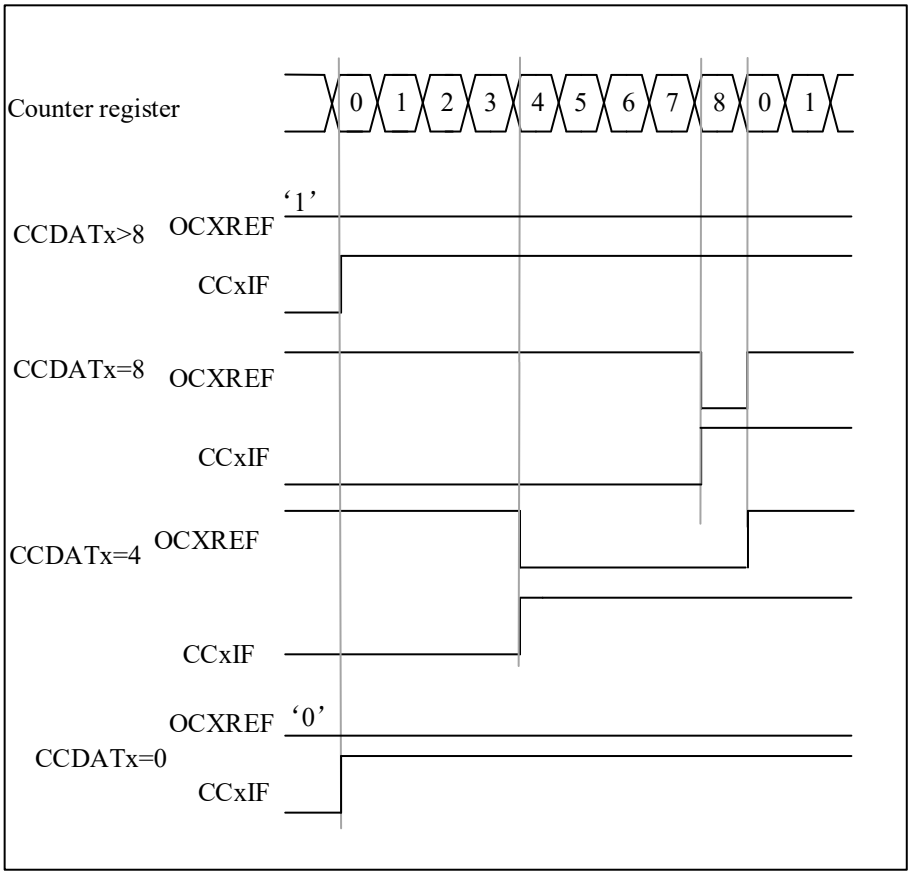
User can set TIMx_CTRL1.DIR=0 to make counter counts up.

Example for PWM mode1:

When TIMx_CNT < TIMx_CCDATx, the reference PWM signal OCxREF is high. Otherwise it will be low. If the compare value in TIMx_CCDATx is greater than the auto-reload value, the OCxREF will remains 1. Conversely, if the compare value is 0, the OCxREF will remain 0.

When TIMx_AR=8, the PWM waveforms are as follows.

Figure 9-19 Edge-aligned PWM Waveform (APR=8)



- **Down-counting**

User can set TIMx_CTRL1.DIR=1 to make counter counts down.

Example for PWM mode1.

When TIMx_CNT > TIMx_CCDATx, the reference PWM signal OCxREF is low. Otherwise it will be high. If the compare value in TIMx_CCDATx is greater than the auto-reload value, the OCxREF will remains 1.

Note: if the nth PWM cycle CCDATx shadow register >= AR value, the shadow register value of CCDATx in the (n+1)th PWM cycle is 0. At the moment when the counter is 0 in the (n+1)th PWM cycle, although the value of the counter = CCDATx shadow register = 0 and OCxREF = '0', no compare event will be generated.

9.3.10 One-pulse mode

In the one-pulse mode (ONEPM), a trigger signal is received, and a pulse t_{PULSE} with a programmable pulse width is generated after a programmable delay t_{DELAY}. The output mode needs to be configured as output compare mode or

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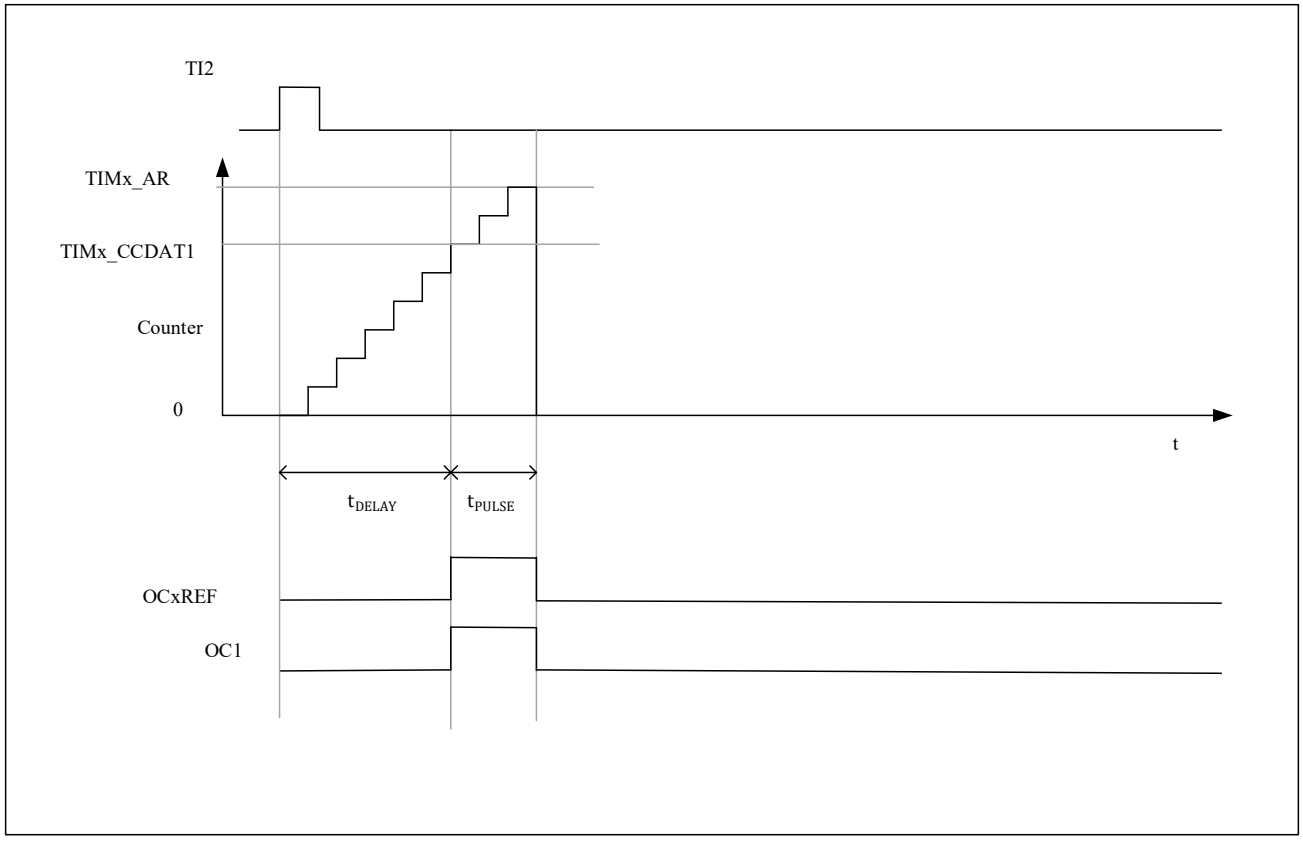
PWM mode. After selecting one-pulse mode, the counter will stop counting after the update event UEV is generated.

Figure 9-20 Example of One-pulse Mode



The following is an example of the one-pulse mode:

A rising edge trigger is detected from the TI2 input, and a pulse with a width of t_{PULSE} is generated on OC1 after a delay of t_{DELAY}.

1. Counter is configured as up-countingand counter TIMx_CNT < TIMx_CCDAT1 ≤ TIMx_AR;

2. TI2FP2 is mapped to TI2 by writing TIMx_CCMOD1.CC2SEL= ‘01’; TI2FP2 is configured for rising edge detection by writing TIMx_CCEN.CC2P= ‘0’;

3. TI2FP2 is configured as the trigger (TRGI) of the slave mode controller by writing TIMx_SMCTRL.TSEL= ‘110’; and T12FP2 is used to start the counter by writing TIMx_SMCTRL.SMSEL= ‘110’ (trigger mode);

4. The count value to be delayed (t_{DELAY}) is configured in TIMx_CCDAT1; TIMx_AR - TIMx_CCDAT1 is the count value of the pulse width t_{PULSE};

5. Configure TIMx_CTRL1.ONEPM=1 to enable single pulse mode; Configure TIMx_CCMOD1.OC1MD = ‘111’ to select PWM2 mode;

6. Wait for an external trigger event on TI2, and a one pulse waveform will be output on OC1;

9.3.10.1 Special case: OCx fast enable

In one-pulse mode, an edge is detected through the TIx input, and triggers the counter to count to the comparison value and then output a pulse. These operations limit the minimum delay t_{DELAY} that can be achieved.

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User can set TIMx_CCMODx.OCxFEN=1 to turn on OCx fast enable; After triggering the rising edge, the OCxREF signal will be forced to be converted to the same level as the comparison match occurs immediately, regardless of the comparison result. OCxFEN fast enable only takes effect when the channel mode is configured for PWM1 and PWM2 modes.

9.3.11 Clearing the OCxREF Signal on an External Event

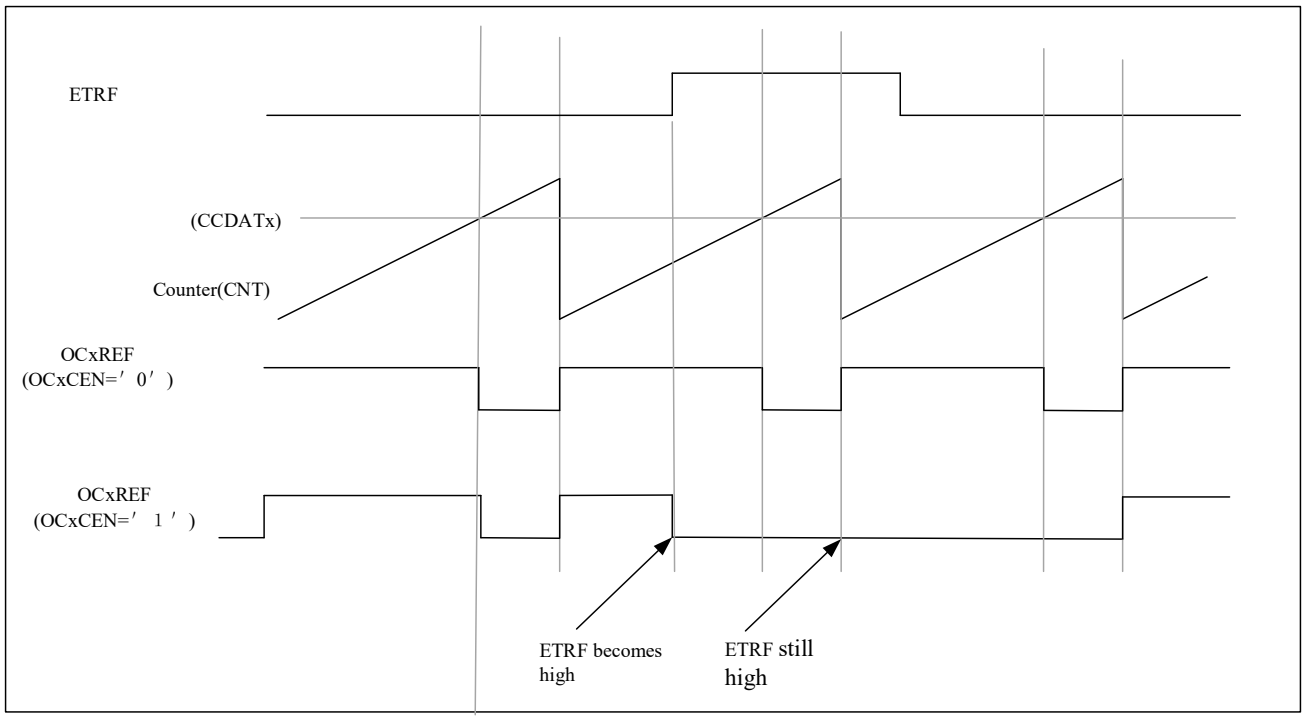
If TIMx_CCMODx.OCxCEN=1, high level of ETRF input can be used to driven the OCxREF signal to low, and the OCxREF signal will remain low until the next UEV happens. Only output compare and PWM modes can use this function. This cannot be used when it is in forced mode.

Example : to control the current, user can connect the ETR signal to the output of a comparator, and the operation for ETR should be as follow:

- Set TIMx_SMCTRL.EXTPS=00 to disable the external trigger prescaler.
- Set TIMx_SMCTRL.EXCEN=0 to disable the external clock mode 2.
- Set TIMx_SMCTRL.EXTP and TIMx_SMCTRL.EXTF to configure the external trigger polarity and external trigger filter according to the need.

Here is an example for the case that when ETRF input becomes high, the behavior of OCxREF signal for different value of OCxCEN. Timer is set to be in PWM mode in this case.

Figure 9-21 Clearing the OCxREF of TIMx



9.3.12 Debug Mode

When the microcontroller is in debug mode (the Cortex®-M0 core halted), depending on the DBG_CTRL.TIMx_STOP configuration in the PWR module, the TIMx counter can either continue to work normally

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or stop. For more details, refer to Section 3.4.9.

9.3.13 TIMx and External Trigger Synchronization

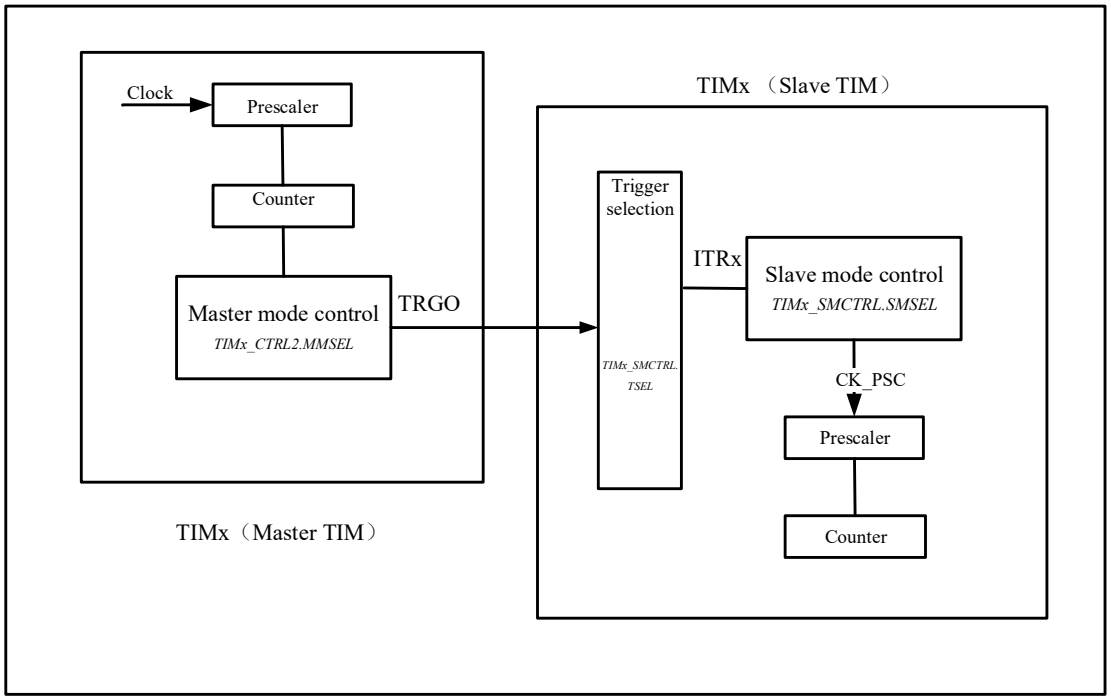
Same with advanced-control timer, refer to Section 8.3.15

9.3.14 Timer Synchronization

All TIMx timers are internally interconnected to each other. This implementation allows a master timer to provide trigger to reset, start, stop or provide a clock for the other slave timers. The master clock is used for internal counter and can be prescaled. Below figure shows a block diagram of timer interconnection.

The synchronization function does not support dynamic change of the interconnection. User should configure and enable the slave timer before enabling the master timer's trigger or clock.

Figure 9-22 Block Diagram of Timer Interconnection



9.3.14.1 Master timer as a prescaler for another timer

TIM1 acts as a prescaler for TIM3. TIM1 is maser, while TIM3 is slave.

User needs to do the following steps for this configuration.

- Set TIM1_CTRL2.MMSEL=' 010' to use the update event of TIM1 as trigger output.
- Configure TIM3_SMCTRL. TSEL= '000' to connect the TRGO of TIM1 to TIM3.
- Configure TIM3_SMCTRL.SMSEL = '111', so that the slave mode controller will be configured in external clock mode 1.
- Start TIM3 by setting TIM3_CTRL1. CNTEN = '1'.

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- Start TIM1 by setting TIM1_CTRL1. CNTEN = '1'.

Note: if user select OCx as the trigger output of TIM1 by configuring MMSEL = '1xx', OCx rising edge will be used to drive TIM3.

9.3.14.2 Master timer to enable another timer

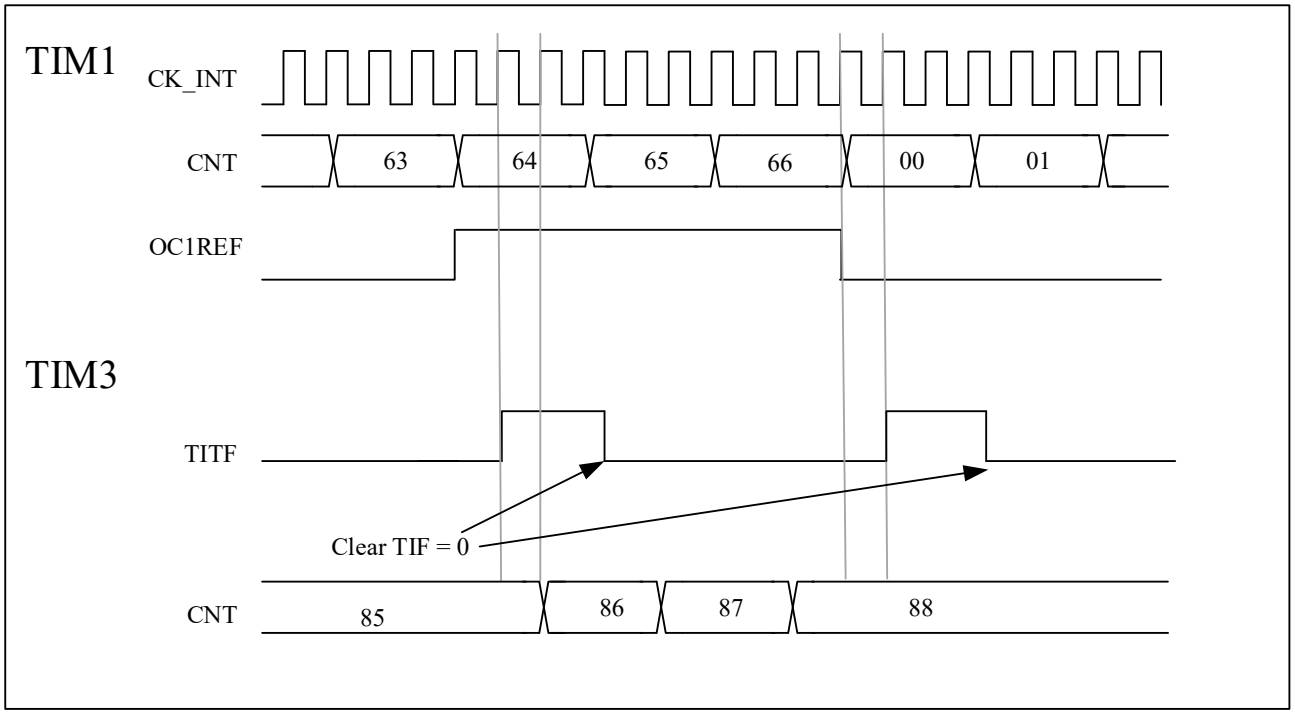
In this example, TIM3 is enabled by the output compare of TIM1. TIM3 counter will start to count after the OC1REF of TIM1 is high. Both counters are clocked based on CK_INT with a prescaler divide by 3 ($f_{CK\_CNT} = f_{CK\_INT}/3$).

The configuration steps are shown as below.

- Set TIM1_CTRL2.MMSEL='100' to use the OC1REF of TIM1 as trigger output.
- Configure TIM1_CCMOD1 register to configure the OC1REF output waveform.
- Set TIM3_SMCTRL.TSEL = '000' to connect TIM1 trigger output to TIM3.
- Set TIM3_SMCTRL.SMSEL= '101' to set TIM3 to gated mode.
- Set TIM3_CTRL1.CNTEN= '1' to start TIM3.
- Set TIM1_CTRL1.CNTEN= '1' to start TIM1.

Note: the TIM3 clock is not synchronized with the TIM1 clock; this mode only affects the TIM3 counter enable signal.

Figure 9-23 TIM3 Gated by OC1REF of TIM1



In the next example, gate TIM3 with enable signal of TIM1, and set TIM1.CTRL1.CNTEN = '0' to stop TIM1. TIM3 counts on the divided internal clock only when TIM1 is enable. Both counters are clocked based on CK_INT with a prescaler divide by 3 ($f_{CK\_CNT} = f_{CK\_INT}/3$).

The configuration steps are shown as below

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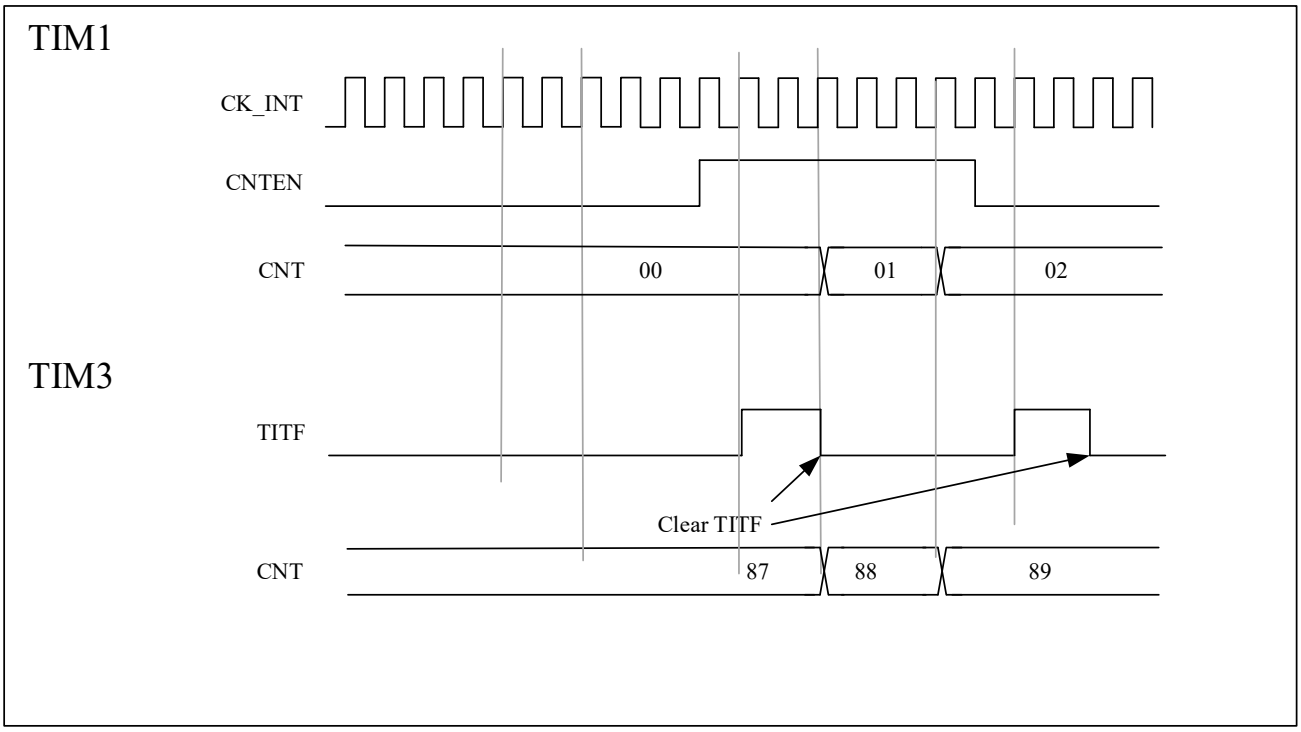
- Sett TIM1_CTRL2.MMSEL=’ 001’ to use the enable signal of TIM1 as trigger output
- Sett TIM3_SMCTRL.TSEL = ‘000’ to configure TIM3 to get the trigger input from TIM1
- Set TIM3_SMCTRL.SMSEL = ‘101’ to configure TIM3 in gated mode.
- Set TIM3_CTRL1.CNTEN= ‘1’ to start TIM3.
- Set TIM1_CTRL1.CNTEN= ‘1’ to start TIM1.
- Set TIM1_CTRL1.CNTEN= ‘0’ to stop TIM1.

Figure 9-24 TIM3 Gated by Enable Signal of TIM1



9.3.14.3 Master timer to start another timer

In this example, we can use update event as trigger source. TIM1 is master, while TIM3 is slave.

The configuration steps are shown as below:

- Set TIM1_CTRL2.MMSEL=’ 010’ to use the update event of TIM1 as trigger output
- Configure TIM1_AR register to set the output period.
- Set TIM3_SMCTRL .TSEL= ‘000’ to connect TIM1 trigger output to TIM3.
- Set TIM3_SMCTRL. SMSEL = ‘110’ to set TIM3 to trigger mode.
- Set TIM1_CTRL1.CNTEN=1 to start TIM1.

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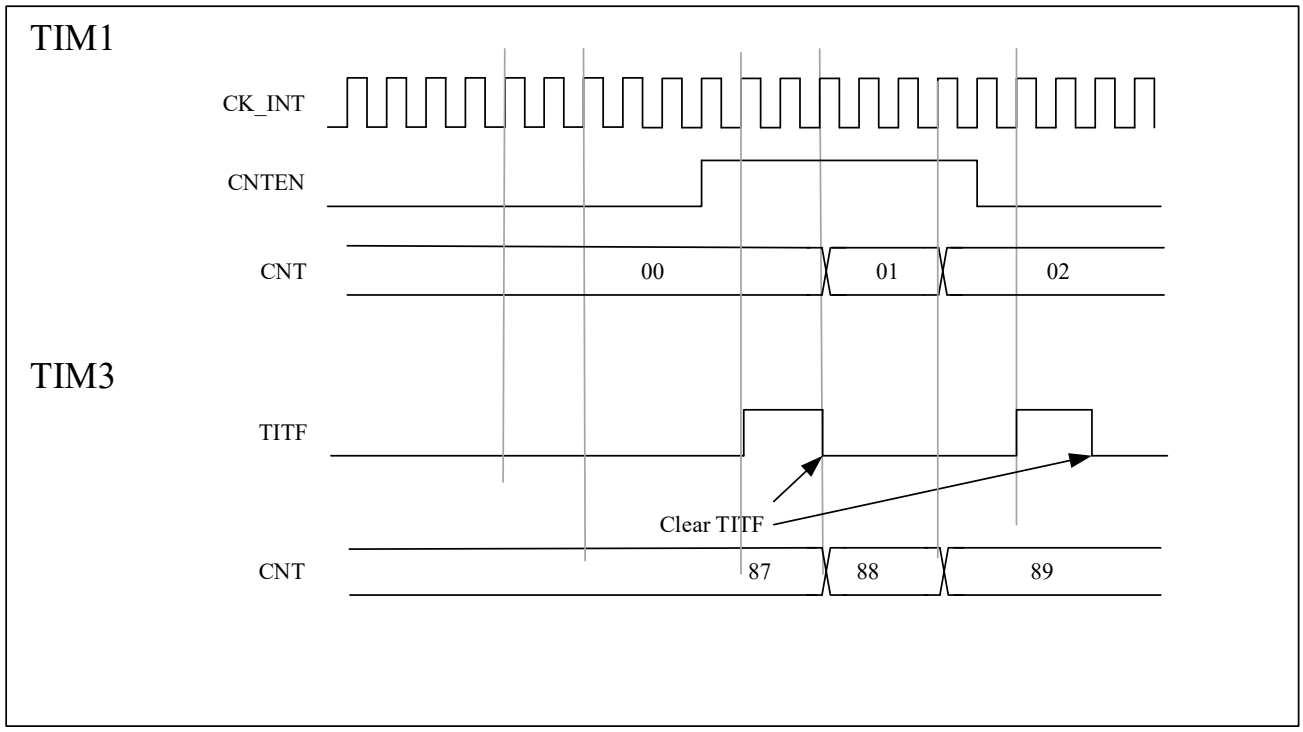
Figure 9-25 Trigger TIM3 with an Update of TIM1



9.3.14.4 Start 2 timers synchronously using an external trigger

In this example, TIM1 is enabled when TIM1's TI1 input rises, and TIM3 is enabled when TIM1 is enabled. To ensure the alignment of counters, TIM1 must be configured in master/slave mode. For TI1, TIM1 is the slave; for TIM3, TIM1 is the master.

The configuration steps are shown as below:

- Set TIM1.MMSEL = '001' to use the enable signal as trigger output
- Set TIM1_SMCTRL.TSEL = '100' to configure the TIM1 to slave mode and receive the trigger input of TI1.
- Sett TIM1_SMCTRL .SMSEL = '110' to configure TIM1 to trigger mode.
- Set TIM1_SMCTRL .MSMD = '1' to configure TIM1 to master/slave mode.
- Set TIM3_SMCTRL .TSEL = '000' to connect TIM1 trigger output to TIM3.
- Set TIM3_SMCTRL.SMSEL = '110' to configure TIM3 to trigger mode.

When TI1 rising edge arrives, both timers start counting synchronously according to the internal clock, and both TITF flags are set simultaneously.

The following figure shows a delay between CNTEN and CK_PSC of TIM1 in master/slave mode.

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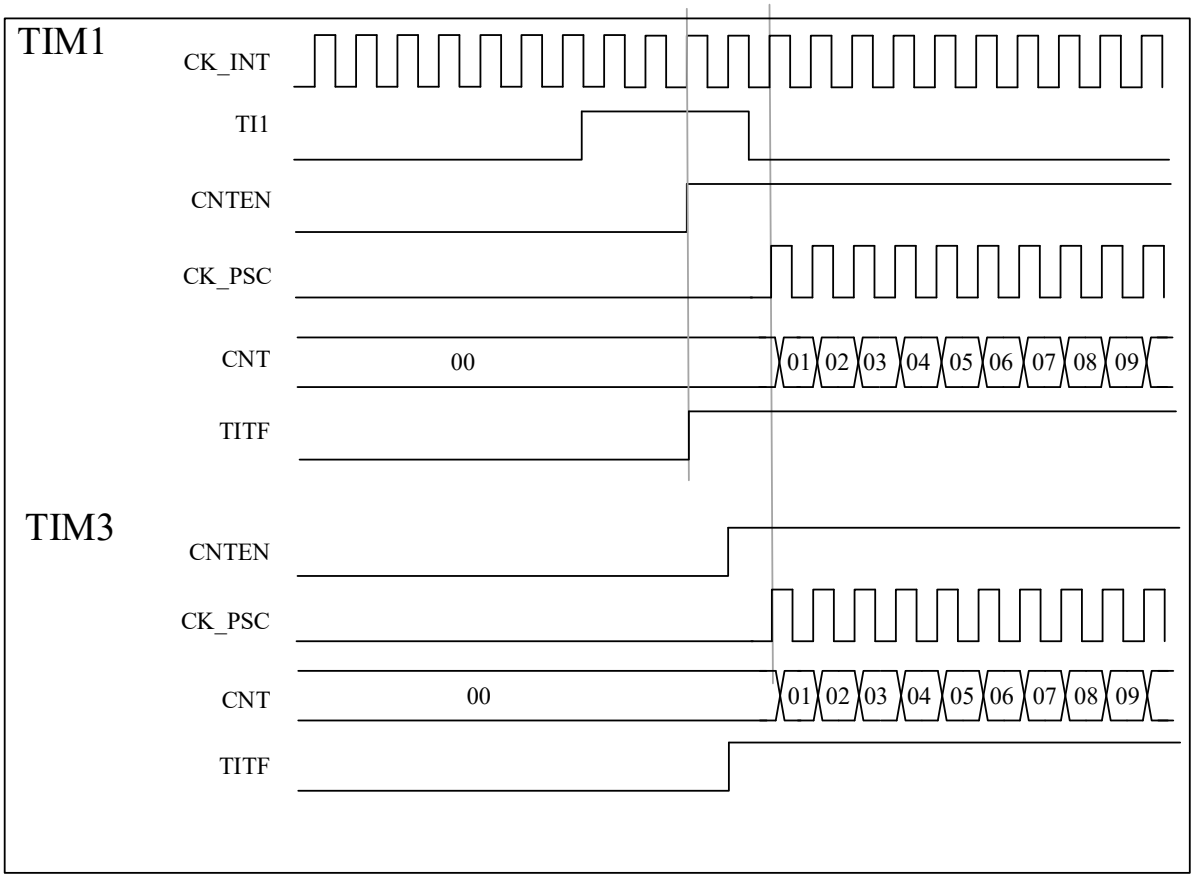
Figure 9-26 Triggers Timers 1 and 3 Using the TI1 Input of TIM1



9.4 TIMx Register Description(x=3)

9.4.1 Register Overview

Table 9-1 Register Overview

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
000h	TIMx_CTRL1	Reserved																CLRSEL	Reserved	Reserved	C2SEL	C1SEL	Reserved	CLKD[1:0]		ARPEN	CAMSEL[1:0]		DIR	ONEPM	UPRS	UPDIS	CNTEN
	Reset Value																	0			0	0		0	0	0	0	0	0	0	0	0	0
004h	TIMx_CTRL2	Reserved																							ETRSEL	TI1SEL	MMSEL[2:0]			Reserved			
	Reset Value																								0	0	0	0	0				
008h	TIMx_SMCTRL	Reserved																EXTP	EXCEN	EXTPS[1:0]			EXTF[3:0]			MSMD	TSEL[2:0]			Reserved	SMSEL[2:0]		
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0		0	0	0
00Ch	TIMx_DINTEN	Reserved																									TIEN	Reserved				CC2IEN	CC1IEN	UIEN
	Reset Value																										0				0	0	0

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010h	TIMx_STS	Reserved						CC2OCF	CC1OCF	Reserved		TITF	Reserved			CC2ITF	CC1ITF	UDITF
	Reset Value							0	0			0				0	0	0
014h	TIMx_EVTGEN	Reserved										TGN	Reserved			CC2GN	CC1GN	UDGN
	Reset Value											0				0	0	0
018h	TIMx_CCMOD1	Reserved	OC2CEN	OC2M[2:0]			OC2PEN	OC2FEN	CC2SEL[1:0]		OC1CEN	OC1M[2:0]			OC1PEN	OC1FEN	CC1SEL[1:0]	
	Reset Value		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	TIMx_CCMOD1	Reserved	IC2F[3:0]				IC2PSC[1:0]		CC2SEL[1:0]		IC1F[3:0]				IC1PSC[1:0]		CC1SEL[1:0]	
	Reset Value		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
020h	TIMx_CCEN	Reserved											CC2P	CC2EN	Reserved		CC1P	CC1EN
	Reset Value												0	0			0	0
024h	TIMx_CNT	Reserved	CNT[15:0]															
	Reset Value		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
028h	TIMx_PSC	Reserved	PSC[15:0]															
	Reset Value		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
02Ch	TIMx_AR	Reserved	AR[15:0]															
	Reset Value		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
030h	Reserved																	
034h	TIMx_CCDAT1	Reserved	CCDAT1[15:0]															
	Reset Value		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
038h	TIMx_CCDAT2	Reserved	CCDAT2[15:0]															
	Reset Value		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

9.4.2 Control Register 1 (TIMx_CTRL1)

Offset address: 0x00

Reset value: 0x0000 0000

31	16
Reserved	

15	14	12	11	10	9	8	7	6	5	4	3	2	1	0
CLRSEL	Reserved		C1SEL	Reserved	CLKD[1:0]		ARPEN	CAMSEL[1:0]		DIR	ONEPM	UPRS	UPDIS	CNTEN
rw			rw		rw		rw	rw		rw	rw	rw	rw	rw

Bit Field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained
15	CLRSEL	OCxREF clear selection 0: Select the external OCxREF clear from ETR 1: Select the internal OCxREF clear from comparator
14:12	Reserved	Reserved, the reset value must be maintained

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Bit Field	Name	Description
11	C1SEL	Channel 1 selection 0: Select external CH1 signal from IOM 1: Select internal CH1 signal from COMP
10	Reserved	Reserved, the reset value must be maintained
9:8	CLKD[1:0]	Clock division CLKD[1:0] indicates the division ratio between CK_INT (timer clock) and t_{DTS} (clock used for dead-time generator and digital filters (ETR, TIx)) 00: $t_{DTS} = t_{CK\_INT}$ 01: $t_{DTS} = 2 \times t_{CK\_INT}$ 10: $t_{DTS} = 4 \times t_{CK\_INT}$ 11: Reserved, do not use this configuration
7	ARPEN	ARPEN: Auto-reload preload enable 0: Shadow register disable for TIMx_AR register 1: Shadow register enable for TIMx_AR register
6:5	CAMSEL[1:0]	Center-aligned mode selection 00: Edge-aligned mode. TIMx_CTRL1.DIR specifies up-counting or down-counting. 01: Center-aligned mode 1. The counter counts in center-aligned mode, and the output compare interrupt flag bit is set to 1 when down-counting. 10: Center-aligned mode 2. The counter counts in center-aligned mode, and the output compare interrupt flag bit is set to 1 when up-counting. 11: Center-aligned mode 3. The counter counts in center-aligned mode, and the output compare interrupt flag bit is set to 1 when up-counting or down-counting. *Note: Switching from edge-aligned mode to center-aligned mode is not allowed when the counter is still enabled (TIMx_CTRL1.CNTEN = 1).*
4	DIR	Direction 0: Up-counting 1: Down-counting *Note: This bit is read-only when the counter is configured in center-aligned mode.*
3	ONEPM	One-pulse mode 0: Disable one-pulse mode. The counter counts are not affected when an update event occurs. 1: Enable one-pulse mode. The counter stops counting when the next update event occurs (clearing TIMx_CTRL1.CNTEN bit)
2	UPRS	Update request source This bit is used to select the UEV event sources by software. 0: If update interrupt is enabled, any of the following events will generate an update interrupt: – Counter overflow/underflow – The TIMx_EVTGEN.UDGN bit is set – Update generation from the slave mode controller 1: If update interrupt is enabled, only counter overflow/underflow will generate update interrupt

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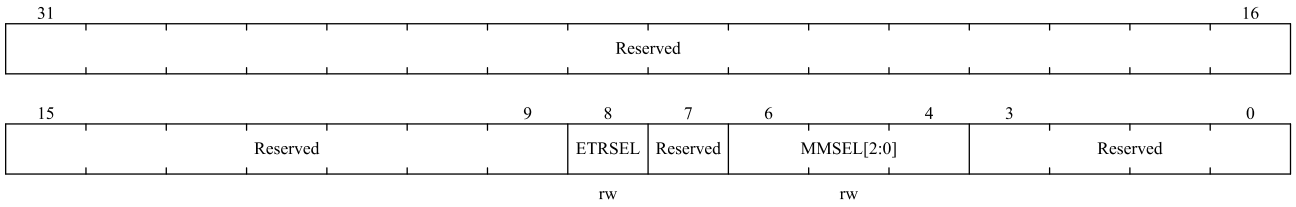
Bit Field	Name	Description
1	UPDIS	Update disable This bit is used to enable/disable the update event (UEV) events generation by software. 0: Enable UEV. And UEV will be generated if one of following condition been fulfilled: – Counter overflow/underflow – The TIMx_EVTGEN.UDGN bit is set – Update generation from the slave mode controller Shadow registers will update with preload value. 1: UEV disabled. No update event is generated, and the shadow registers (AR, PSC, and CCDATx) keep their values. If the TIMx_EVTGEN.UDGN bit is set or a hardware reset is issued by the slave mode controller, the counter and prescaler are reinitialized.
0	CNTEN	Counter Enable 0: Disable counter 1: Enable counter *Note: external clock, gating mode can only work after TIMx_CTRL1.CNTEN bit is set in the software. Trigger mode can automatically set TIMx_CTRL1.CNTEN bit by hardware*.

9.4.3 Control Register 2 (TIMx_CTRL2)

Offset address: 0x04

Reset value: 0x0000



Bit field	Name	Description
15:9	Reserved	Reserved, the reset value must be maintained
8	ETRSEL	External Triggered Selection storage (ETR Selection) 0: Select external ETR (from IOM) signal; 1: Reserved
7	Reserved	Reserved, the reset value must be maintained
6:4	MMSEL[2:0]	Master Mode Selection These 3 bits (TIMx_CTRL2. MMSEL [2:0]) are used to select the synchronization information (TRGO) sent to the slave timer in the master mode. Possible combinations are as follows: 000: Reset –When the TIMx_EVTGEN.UDGN is set or a reset is generated by the slave mode controller, a TRGO pulse occurs. And in the latter case, the signal on TRGO is delayed compared to the actual reset. 001: Enable - The TIMx_CTRL1.CNTEN bit is used as the trigger output (TRGO). Sometimes you need to start multiple timers at the same time or enable slave timer for a period of time. The counter enable signal is set when TIMx_CTRL1.CNTEN bit is set or the trigger input in gated mode is high.

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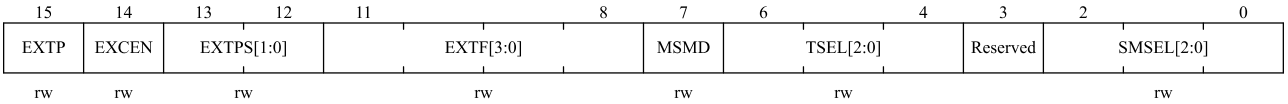
Bit field	Name	Description
		When the counter enable signal is controlled by the trigger input, there is a delay on TRGO except if the master/slave mode is selected (refer to the description of the TIMx_SMCTRL.MSMD bit). 010: Update - The update event is selected as the trigger output (TRGO). For example, a master timer clock can be used as a slave timer prescaler. 011: Compare pulse - Triggers the output to send a positive pulse (TRGO) when the TIMx_STS.CC1ITF is to be set (even if it is already high), when a capture or a comparison succeeds. 100: Compare - OC1REF signal is used as the trigger output (TRGO). 101: Compare - OC2REF signal is used as the trigger output (TRGO). Others: reserved
3:0	Reserved	Reserved, the reset value must be maintained

9.4.4 Slave Mode Control Register (TIMx_SMCTRL)

Offset address: 0x08

Reset value: 0x0000



Bit field	Name	Description
15	EXTP	External trigger polarity This bit is used to select whether the trigger operation is to use ETR or the inversion of ETR. 0: ETR active at high level or rising edge. 1: ETR active at low level or falling edge.
14	EXCEN	External clock enable This bit is used to enable external clock mode 2, and the counter is driven by any active edge on the ETRF signal in this mode. 0: External clock mode 2 disable. 1: External clock mode 2 enable. *Note 1: when external clock mode 1 and external clock mode 2 are enabled at the same time, the input of the external clock is ETRF.* *Note 2: the following slave modes can be used simultaneously with external clock mode 2: reset mode, gated mode and trigger mode; however, TRGI cannot connect to ETRF (TIMx_SMCTRL.TSEL ≠ '111').* *Note 3: setting the TIMx_SMCTRL.EXCEN bit has the same effect as selecting external clock mode 1 and connecting TRGI to ETRF (TIMx_SMCTRL.SMSEL = 111 and TIMx_SMCTRL.TSEL = 111).*
13:12	EXTPS[1:0]	External trigger prescaler The frequency of the external trigger signal ETRP must be at most 1/4 of TIMxCLK frequency. When a faster external clock is input, a prescaler can be used to reduce the frequency of ETRP. 00: Prescaler disable

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Bit field	Name	Description
		01: ETRP frequency divided by 2 10: ETRP frequency divided by 4 11: ETRP frequency divided by 8
11:8	EXTF[3:0]	External trigger filter These bits are used to define the frequency at which the ETRP signal is sampled and the bandwidth of the ETRP digital filtering. In effect, the digital filter is an event counter that generates a validate output after consecutive N events are recorded. 0000: No filter, sampling at f_{DTS} 0001: $f_{SAMPLING} = f_{CK\_INT}$, N = 2 0010: $f_{SAMPLING} = f_{CK\_INT}$, N = 4 0011: $f_{SAMPLING} = f_{CK\_INT}$, N = 8 0100: $f_{SAMPLING} = f_{DTS}/2$, N = 6 0101: $f_{SAMPLING} = f_{DTS}/2$, N = 8 0110: $f_{SAMPLING} = f_{DTS}/4$, N = 6 0111: $f_{SAMPLING} = f_{DTS}/4$, N = 8 1000: $f_{SAMPLING} = f_{DTS}/8$, N = 6 1001: $f_{SAMPLING} = f_{DTS}/8$, N = 8 1010: $f_{SAMPLING} = f_{DTS}/16$, N = 5 1011: $f_{SAMPLING} = f_{DTS}/16$, N = 6 1100: $f_{SAMPLING} = f_{DTS}/16$, N = 8 1101: $f_{SAMPLING} = f_{DTS}/32$, N = 5 1110: $f_{SAMPLING} = f_{DTS}/32$, N = 6 1111: $f_{SAMPLING} = f_{DTS}/32$, N = 8
7	MSMD	Master/ Slave mode 0: No action 1: Events on the trigger input (TRGI) are delayed to allow a perfect synchronization between the current timer (via TRGO) and its slaves. This is useful when several timers are required to be synchronized to a single external event.
6:4	TSEL[2:0]	Trigger selection These 3 bits are used to select the trigger input of the synchronous counter. 000: Internal trigger 0 (ITR0) 100: TI1 edge detector (TI1F_ED) 001: Internal trigger 1 (ITR1) 101: Filtered timer input 1(TI1FP1) 010: Internal trigger 2 (ITR2) 110: Filtered timer input 2 (TI2FP2) 011: Internal trigger 3 (ITR3) 111: External triggered Input (ETRF) For more details on ITRx, refer to Table 9-2 below. *Note: These bits must be changed only when not in use (e. g. TIMx_SMCTRL.SMSEL=000) to avoid false edge detection at the transition.*
3	Reserved	Reserved, the reset value must be maintained

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Bit field	Name	Description
2:0	SMSEL[2:0]	Slave mode selection When an external signal is selected, the active edge of the trigger signal (TRGI) is linked to the selected external input polarity (refer to input control register and control register description) 000: Disable slave mode. If TIMx_CTRL1.CNTEN = 1, the prescaler is driven directly by the internal clock. 001: reserved. 010: reserved. 011: reserved. 100: Reset mode. On the rising edge of the selected trigger input (TRGI), the counter is reinitialized and the shadow register is updated. 101: Gated mode. When the trigger input (TRGI) is high, the clock of the counter is enabled. Once the trigger input becomes low, the counter stops counting, but is not reset. In this mode, the start and stop of the counter are controlled. 110: Trigger mode. When a rising edge occurs on the trigger input (TRGI), the counter is started but not reset. In this mode, only the start of the counter is controlled. 111: External clock mode 1. The counter is clocked by the rising edge of the selected trigger input (TRGI). *Note: Do not use gated mode if TI1F_ED is selected as the trigger input (TIMx_SMCTRL.TSEL=100). This is because TI1F_ED outputs a pulse for each TI1F transition, whereas gated mode checks the level of the triggered input.*

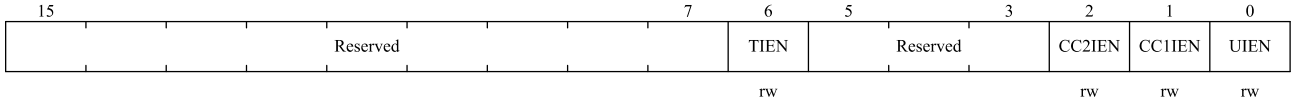
Table 9-2 TIMx Internal Trigger Connection

Slave timer	ITR0 (TSEL = 000)	ITR1 (TSEL = 001)	ITR2 (TSEL = 010)	ITR3 (TSEL = 011)
TIM3	TIM1	NA	NA	NA

9.4.5 Interrupt Enable Register (TIMx_DINTEN)

Offset address: 0x0C

Reset value: 0x0000



Bit field	Name	Description
15:7	Reserved	Reserved, the reset value must be maintained
6	TIEN	Trigger interrupt enable 0: Disable trigger interrupt 1: Enable trigger interrupt
5:3	Reserved	Reserved, the reset value must be maintained

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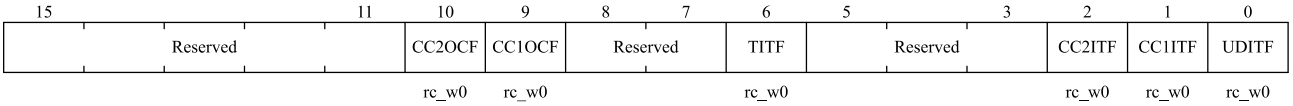
Bit field	Name	Description
2	CC2IEN	Capture/Compare 2 interrupt enable 0: Disable capture/compare 2 interrupt 1: Enables capture/compare 2 interrupt
1	CC1IEN	Capture/Compare 1 interrupt enable 0: Disable capture/compare 1 interrupt 1: Enables capture/comparing 1 interrupt
0	UIEN	Update interrupt enable 0: Disable update interrupt 1: Enables update interrupt

9.4.6 Status Register (TIMx_STS)

Offset address: 0x10

Reset value: 0x0000



Bit field	Name	Description
15:11	Reserved	Reserved, the reset value must be maintained
10	CC2OCF	Capture/Compare 2 overcapture flag Refer to TIMx_STS.CC1OCF description.
9	CC1OCF	Capture/Compare 1 overcapture flag This bit is set by hardware only when the corresponding channel is configured in input capture mode. This bit cleared by software writing 0. 0: No overcapture occurred 1: TIMx_STS.CC1ITF was already set when the value of the counter has been captured in the TIMx_CCDAT1 register.
8:7	Reserved	Reserved, the reset value must be maintained
6	TITF	Trigger interrupt flag This bit is set by hardware when an active edge is detected on the TRGI input when the slave mode controller is in a mode other than gated. This bit is set by hardware when any edge in gated mode is detected. This bit is cleared by software. 0: No trigger event occurred 1: Trigger interrupt occurred
5:3	Reserved	Reserved, the reset value must be maintained
2	CC2ITF	Capture/Compare 2 interrupt flag Refer to TIMx_STS.CC1ITF description.
1	CC1ITF	Capture/Compare 1 interrupt flag **When the corresponding channel of CC1 is in output mode:**

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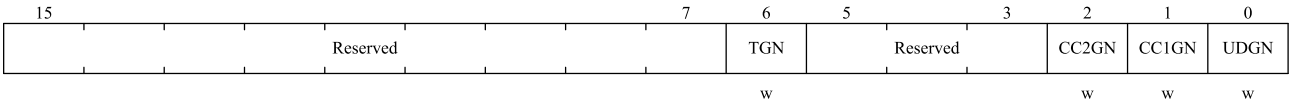
Bit field	Name	Description
		Except in center-aligned mode, this bit is set by hardware when the counter value is the same as the compare value (refer to TIMx_CTRL1.CAMSEL bit description). This bit is cleared by software. 0: No match occurred. 1: The value of TIMx_CNT is the same as the value of TIMx_CCDAT1. When the value of TIMx_CCDAT1 is greater than the value of TIMx_AR, the TIMx_STS.CC1ITF bit will go high if the counter overflows (in up-counting and up/down-counting modes) and underflows in down-counting mode. **When the corresponding channel of CC1 is in input mode:** This bit is set by hardware when the capture event occurs. This bit is cleared by software or by reading TIMx_CCDAT1. 0: No input capture occurred. 1: Input capture occurred. Counter value has captured in the TIMx_CCDAT1. An edge with the same polarity as selected has been detected on IC1.
0	UDITF	Update interrupt flag This bit is set by hardware when an update event occurs under the following conditions: – When TIMx_CTRL1.UPDIS = 0, overflow or underflow (An update event is generated). – When TIMx_CTRL1.UPRS = 0, TIMx_CTRL1.UPDIS = 0, and the TIMx_EVTGEN.UDGN bit is set by software to reinitialize the CNT. – When TIMx_CTRL1.UPRS = 0, TIMx_CTRL1.UPDIS = 0, and the counter CNT is reinitialized by the trigger event. (Refer to TIMx_SMCTRL Register description) This bit is cleared by software. 0: No update event occurred 1: Update interrupt occurred

9.4.7 Event Generation Register (TIMx_EVTGEN)

Offset address: 0x14

Reset values: 0 x0000



Bit Field	Name	Description
15:7	Reserved	Reserved, the reset value must be maintained.
6	TGN	Trigger generation This bit can generate a trigger event when set by software. And at this time TIMx_STS.TITF = 1, if the corresponding interrupt are enabled, the corresponding interrupt will be generated. This bit is automatically cleared by hardware. 0: No action 1: Generated a trigger event
5:3	Reserved	Reserved, the reset value must be maintained

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Bit Field	Name	Description
2	CC2GN	Capture/Compare 2 generation Refer to TIMx_EVTGEN.CC1GN description.
1	CC1GN	Capture/Compare 1 generation This bit can generate a capture/compare event when set by software. This bit is automatically cleared by hardware. When the corresponding channel of CC1 is in output mode: The TIMx_STS.CC1ITF flag will be pulled high, if the corresponding interrupt is enabled, and the corresponding interrupt will be generated. When the corresponding channel of CC1 is in input mode: TIMx_CCDAT1 will capture the current counter value, and the TIMx_STS.CC1ITF flag will be pulled high, if the corresponding interrupt are enabled. If The IMx_STS.CC1ITF is already pulled high, pull TIMx_STS.CC1OCF high. 0: No action 1: Generated a CC1 capture/compare event
0	UDGN	Update generation This bit can generate an update event when set by software. At this time the counter will be reinitialized, and the prescaler counter will be cleared, the counter will be cleared in center-aligned or up-counting mode, but take the value of the TIMx_AR register in down-counting mode. This bit is automatically cleared by hardware. 0: No action 1: Generated an update event

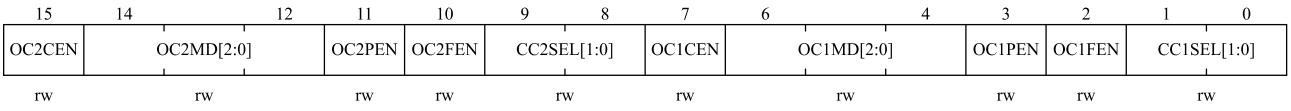
9.4.8 Capture/Compare Mode Register 1 (TIMx_CCMOD1)

Offset address: 0x18

Reset value: 0x0000

Channels can be used for input (capture mode) or output (compare mode), and the direction of the channel is defined by the corresponding CCxSEL bit. The other bits of the register act differently in input and output modes. OCx describes the function of a channel in output mode, ICx describes the function of a channel in input mode. Hence, please note that the same bit can have different meanings for output mode and for input mode.

Output compare mode:



Bit Field	Name	Description
15	OC2CEN	Output Compare 2 clear enable
14:12	OC2MD[2:0]	Output Compare 2 mode
11	OC2PEN	Output Compare 2 preload enable
10	OC2FEN	Output Compare 2 fast enable

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Bit Field	Name	Description
9:8	CC2SEL[1:0]	Capture/compare 2 selection These bits are used to select the input/output and input mapping of the channel 00: CC2 channel is configured as output 01: CC2 channel is configured as input, IC2 is mapped on TI2 10: CC2 channel is configured as input, IC2 is mapped on TI1 11: CC2 channel is configured as input, IC2 is mapped on TRC. This mode is only active when the internal trigger input is selected by TIMx_SMCTRL.TSEL. *Note: CC2SEL is writable only when the channel is off (TIMx_CCEN.CC2EN = 0).*
7	OC1CEN	Output Compare 1 clear enable 0: OC1REF is not affected by ETRF input level 1: OC1REF is cleared immediately when the ETRF input level is detected as high
6:4	OC1MD[2:0]	Output compare 1 mode These bits are used to manage the output reference signal OC1REF, which determines the values of OC1 and OC1N, and is valid at high levels, while the active levels of OC1 and OC1N depend on the TIMx_CCEN.CC1P and TIMx_CCEN.CC1NP bits. 000: Frozen. Comparison between TIMx_CCDAT1 register and counter TIMx_CNT has no effect on OC1REF signal. 001: Set channel 1 to the active level on match. When TIMx_CCDAT1 = TIMx_CNT, OC1REF signal will be forced high. 010: Set channel 1 as inactive level on match. When TIMx_CCDAT1 = TIMx_CNT, OC1REF signal will be forced low. 011: Toggle. When TIMx_CCDAT1 = TIMx_CNT, OC1REF signal will be toggled. 100: Force to inactive level. OC1REF signal is forced low. 101: Force to active level. OC1REF signal is forced high. 110: PWM mode 1 - In up-counting mode, if TIMx_CNT < TIMx_CCDAT1, OC1REF signal of channel 1 is high, otherwise it is low. In down-counting mode, if TIMx_CNT > TIMx_CCDAT1, OC1REF signal of channel 1 is low, otherwise it is high. 111: PWM mode 2 - In up-counting mode, if TIMx_CNT < TIMx_CCDAT1, OC1REF signal of channel 1 is low, otherwise it is high. In down-counting mode, if TIMx_CNT > TIMx_CCDAT1, OC1REF signal of channel 1 is high, otherwise it is low. *Note 1: In PWM mode 1 or PWM mode 2, the OC1REF level changes only when the comparison result changes or when the output compare mode is switched from frozen mode to PWM mode.*
3	OC1PEN	Output compare 1 preload enable 0: Disable preload function of TIMx_CCDAT1 register. Supports write operations to TIMx_CCDAT1 register at any time, and the written value is effective immediately. 1: Enable preload function of TIMx_CCDAT1 register. Only read and write access to preload registers. When an update event occurs, the value of TIMx_CCDAT1 is loaded into the active register. *Note : only when TIMx_CTRL1.ONEPM = 1(In one-pulse mode), PWM mode can be used without verifying the preload register, otherwise no other behavior can be predicted.*

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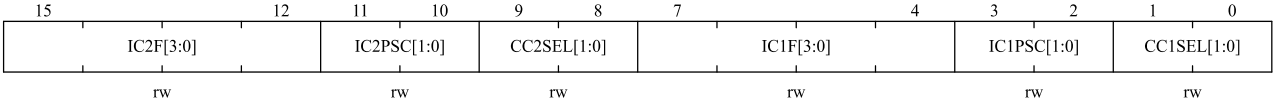
Bit Field	Name	Description
2	OC1FEN	Output compare 1 fast enable This bit is used to speed up the response of the CC output to the trigger input event. 0: CC1 behaves normally depending on the counter and CCDAT1 values, even if the trigger is ON. The minimum delay for activating CC1 output when an edge occurs on the trigger input is 5 clock cycles. 1: An active edge of the trigger input acts like a comparison match on CC1 output. Therefore, OC is set to the comparison level regardless of the comparison result. The delay time for sampling the trigger input and activating the CC1 output is reduced to 3 clock cycles. OCxFEN only works if the channel is configured in PWM1 or PWM2 mode.
1:0	CC1SEL[1:0]	Capture/Compare 1 selection These bits are used to select the input/output and input mapping of the channel 00: CC1 channel is configured as output 01: CC1 channel is configured as input, IC1 is mapped on TI1 10: CC1 channel is configured as input, IC1 is mapped on TI2 11: CC1 channels are configured as inputs and IC1 is mapped to TRC. This mode is only active when the internal trigger input is selected by TIMx_SMCTRL.TSEL. *Note: CC1SEL is writable only when the channel is off (TIMx_CCEN.CC1EN = 0).*

Input capture mode:



Bit Field	Name	Description
15:12	IC2F[3:0]	Input capture 2 filter
11:10	IC2PSC[1:0]	Input capture 2 prescaler
9:8	CC2SEL[1:0]	Capture/Compare 2 selection These bits are used to select the input/output and input mapping of the channel 00: CC2 channel is configured as output 01: CC2 channel is configured as input, IC2 is mapped on TI2 10: CC2 channel is configured as input, IC2 is mapped on TI1 11: CC2 channel is configured as input, IC2 is mapped on TRC. This mode is only active when the internal trigger input is selected by TIMx_SMCTRL.TSEL. *Note: CC2SEL is writable only when the channel is off (TIMx_CCEN.CC2EN = 0).*
7:4	IC1F[3:0]	Input capture 1 filter These bits are used to define sampling frequency of TI1 input and the length of digital filter. The digital filter is an event counter that generates an output transition after N events are recorded. 0000: No filter, sampling at f_{DTS} frequency 0001: $f_{SAMPLING} = f_{CK\_INT}$, N = 2 0010: $f_{SAMPLING} = f_{CK\_INT}$, N = 4 0011: $f_{SAMPLING} = f_{CK\_INT}$, N = 8

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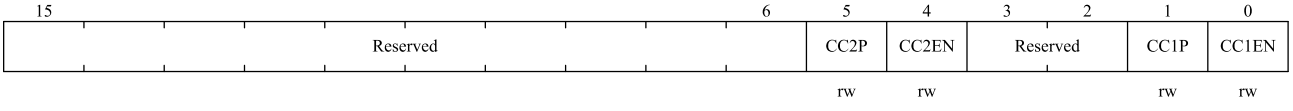
Bit Field	Name	Description
		0100: $f_{SAMPLING} = f_{DTS}/2$, N = 6 0101: $f_{SAMPLING} = f_{DTS}/2$, N = 8 0110: $f_{SAMPLING} = f_{DTS}/4$, N = 6 0111: $f_{SAMPLING} = f_{DTS}/4$, N = 8 1000: $f_{SAMPLING} = f_{DTS}/8$, N = 6 1001: $f_{SAMPLING} = f_{DTS}/8$, N = 8 1010: $f_{SAMPLING} = f_{DTS}/16$, N = 5 1011: $f_{SAMPLING} = f_{DTS}/16$, N = 6 1100: $f_{SAMPLING} = f_{DTS}/16$, N = 8 1101: $f_{SAMPLING} = f_{DTS}/32$, N = 5 1110: $f_{SAMPLING} = f_{DTS}/32$, N = 6 1111: $f_{SAMPLING} = f_{DTS}/32$, N = 8
3:2	IC1PSC[1:0]	Input capture 1 prescaler These bits are used to select the ratio of the prescaler for IC1 (CC1 input). When TIMx_CCEN.CC1EN = 0, the prescaler will be reset. 00: No prescaler, capture is done each time an edge is detected on the capture input 01: Capture is done once every 2 events 10: Capture is done once every 4 events 11: Capture is done once every 8 events
1:0	CC1SEL[1:0]	Capture/Compare 1 selection These bits are used to select the input/output and input mapping of the channel 00: CC1 channel is configured as output 01: CC1 channel is configured as input, IC1 is mapped on TI1 10: CC1 channel is configured as input, IC1 is mapped on TI2 11: CC1 channel is configured as input, IC1 is mapped to TRC. This mode is only active when the internal trigger input is selected by TIMx_SMCTRL.TSEL. *Note: CC1SEL is writable only when the channel is off (TIMx_CCEN.CC1EN = 0).*

9.4.9 Capture/Compare Enable Register (TIMx_CCEN)

Offset address: 0x20

Reset value: 0x0000



Bit Field	Name	Description
15:6	Reserved	Reserved, the reset value must be maintained.
5	CC2P	Capture/Compare 2 output polarity Refer to TIMx_CCEN.CC1P description.
4	CC2EN	Capture/Compare 2 output enable Refer to TIMx_CCEN.CC1EN description.
3:2	Reserved	Reserved, the reset value must be maintained

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Bit Field	Name	Description
1	CC1P	Capture/Compare 1 output polarity When the corresponding channel of CC1 is in output mode: 0: OC1 active high 1: OC1 active low When the corresponding channel of CC1 is in input mode: At this time, this bit is used to select whether IC1 or the inverse signal of IC1 is used as the trigger or capture signal. 0: non-inverted: Capture action occurs when IC1 generates a rising edge. When used as external trigger, IC1 is non-inverted. 1: inverted: Capture action occurs when IC1 generates a falling edge. When used as external trigger, IC1 is inverted. *Note: if TIMx_BKDT.LCKCFG = 3 or 2, these bits cannot be modified.*
0	CC1EN	Capture/Compare 1 output enable When the corresponding channel of CC1 is in output mode: 0: Disable - Disable output OC1 signal. 1: Enable - Enable output OC1 signal. When the corresponding channel of CC1 is in input mode: At this time, this bit is used to disable/enable the capture function. 0: Disable capture 1: Enable capture

Table 9-3 Output Control Bits of Standard OCx Channel

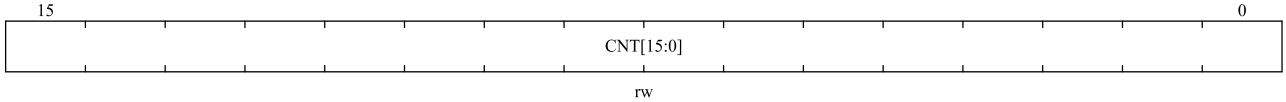
CCxEN	OCx output status
0	Disable output (OCx=0)
1	OCx = OCxREF + polarity

Note: the state of external I/O pins connected to standard OCx channels depend on the OCx channel state and GPIO and AFIO registers.

9.4.10 Counter (TIMx_CNT)

Offset address: 0x24

Reset value: 0x0000



Bit field	Name	Description
15:0	CNT[15:0]	Counter value

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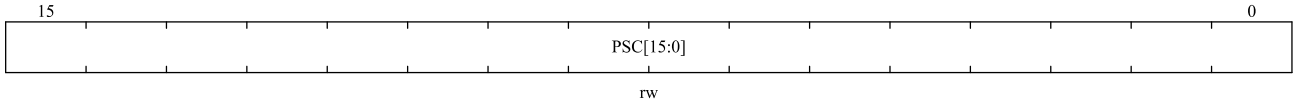
9.4.11 Prescaler (TIMx_PSC)

Offset address: 0x28

Reset value: 0x0000

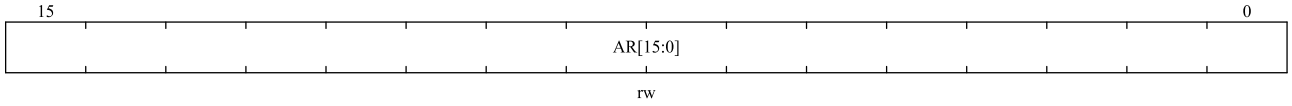


Bit field	Name	Description
15:0	PSC[15:0]	Prescaler value Counter clock $f_{CK\_CNT} = f_{CK\_PSC}/$ (PSC [15:0] +1). Each time an update event occurs, the PSC value is loaded into the active prescaler register.

9.4.12 Auto-reload Register (TIMx_AR)

Offset address: 0x2C

Reset values: 0xFFFF

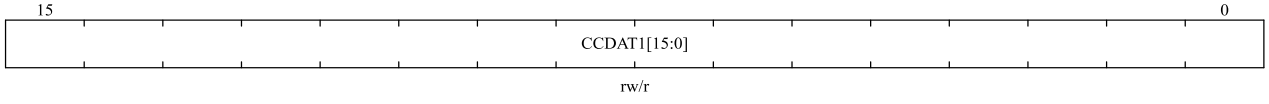


Bit field	Name	Description
15:0	AR[15:0]	Auto-reload value These bits define the value that will be loaded into the actual auto-reload register. Refer to Section 8.3.1 for more details. When the TIMx_AR.AR [15:0] value is null, the counter does not work.

9.4.13 Capture/Compare Register 1 (TIMx_CCDAT1)

Offset address: 0x34

Reset value: 0x0000



Bit field	Name	Description
15:0	CCDAT1[15:0]	Capture/Compare 1 value • CC1 channel is configured as output: CCDAT1 contains the value to be compared to the counter TIMx_CNT, signaling on the OC1 output.

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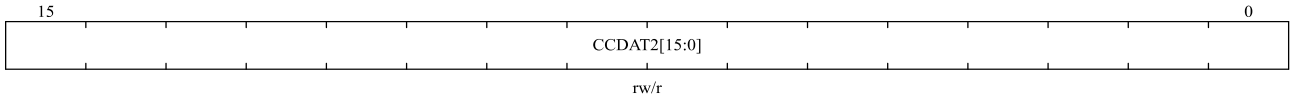
Bit field	Name	Description
		If the preload feature is not selected in TIMx_CCMOD1.OC1PEN bit, the written value is immediately transferred to the active register. Otherwise, this preloaded value is transferred to the active register only when an update event occurs. • CC1 channel is configured as input: CCDAT1 contains the counter value transferred by the last input capture 1 event (IC1). When configured as input mode, register CCDAT1 is only readable. When configured as output mode, register CCDAT1 is readable and writable.

9.4.14 Capture/Compare Register 2 (TIMx_CCDAT2)

Offset address: 0x38

Reset value: 0x0000



Bit field	Name	Description
15:0	CCDAT2[15:0]	Capture/Compare 2 values • CC2 channel is configured as output: CCDAT2 contains the value to be compared to the counter TIMx_CNT, signaling on the OC2 output. If the preload feature is not selected in TIMx_CCMOD1.OC2PEN bit, the written value is immediately transferred to the active register. Otherwise, this preloaded value is transferred to the active register only when an update event occurs. • CC2 channel is configured as input: CCDAT2 contains the counter value transferred by the last input capture 2 event (IC2). When configured as input mode, register CCDAT2 is only readable. When configured as output mode, register CCDAT2 is readable and writable.

10 Basic Timer (TIM6)

10.1 Basic Timer Introduction

The basic timer contains a 16-bit counter, it also provides the ability to wake the system from a low-power mode.

10.2 Main Features of Basic Timer

- 16-bit auto-reload up-counting counter.
- 16-bit programmable prescaler. (The prescaler factor can be configured with any value between 1 and 65536)
- The events that generate the interrupt are as follows:

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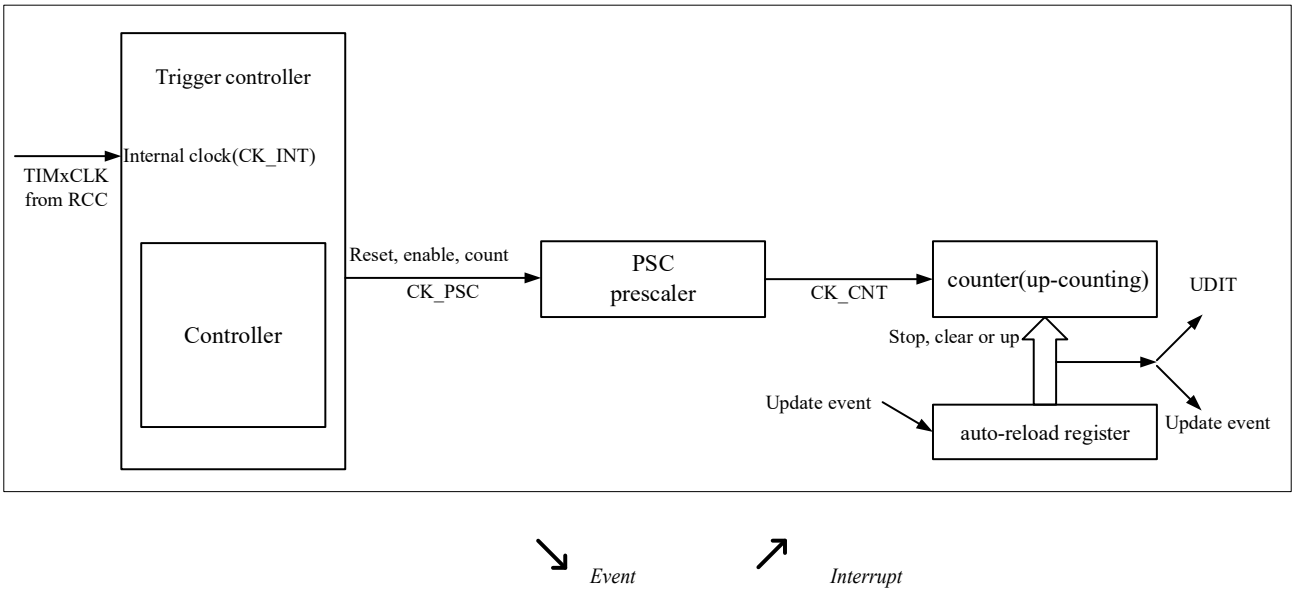
– Update event

- Support STOP mode wake-up: when the clock source is configured as LSI, STOP mode can be waken up by updating interrupts (connected to EXTI19).

Figure 10-1 TIM6 Block Diagram



10.3 Basic Timers Description

10.3.1 Time-base Unit

The time-base unit mainly includes: prescaler, counter and auto-reload. When the time base-unit is operating, the software can read and write the corresponding registers (TIMx_PSC, TIMx_CNT and TIMx_AR) at any time.

Note: When the clock source is configured for LSI, TIMx_CNT does not support writes.

Depending on the setting of the auto-reload preload enable bit (TIMx_CTRL1.ARPEN), the value of the preload register is transferred to the shadow register immediately or at each update event UEV. when TIMx_CTRL1.UPDIS=0, an update event is generated when the counter reaches the overflow condition or the software settings TIMx_EVTGEN.UDGN bit. The counter CK_CNT is valid only when the TIMx_CTRL1.CNTEN bit is set. The counter starts counting one clock cycle after the TIMx_CTRL1.CNTEN bit is set.

10.3.1.1 Prescaler description

The TIMx_PSC register consists of a 16-bit counter that can be used to divide the counter clock frequency by any factor between 1 and 65536. It can be changed on the fly as this register is buffered. The new prescaler value is only taken into account at the next update event.

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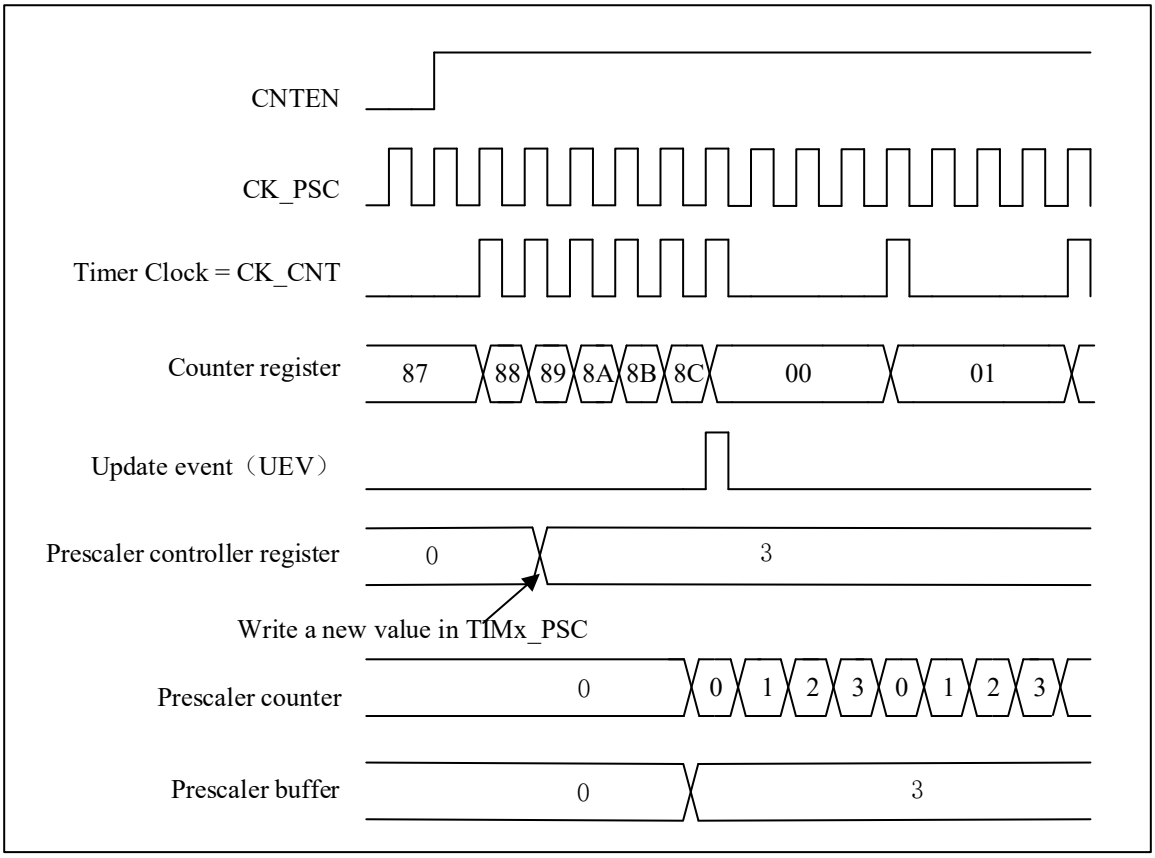
Figure 10-2 Counter Timing Diagram with Prescaler Division Change from 1 to 4



10.3.2 Counter Mode

10.3.2.1 Up-counting mode

In up-counting mode, the counter will count from 0 to the value of the register TIMx_AR, then it resets to 0 and generate a counter overflow event.

If the TIMx_CTRL1.UPRS bit (select update request) and the TIMx_EVTGEN.UDGN bit are set, an update event (UEV) will be generated, but without setting TIMx_STS.UDITF by hardware. Therefore, no update interrupts requests are generated. This is to avoid generating both update and capture interrupts when clearing the counter on the capture event.

Depending on the update request source configured in the TIMx_CTRL1.UPRS, when an update event occurs, all registers are updated and the TIMx_STS.UDITF is set:

- Update auto-reload shadow register with preload value(TIMx_AR), when TIMx_CTRL1.ARPEN = 1.
- The prescaler shadow register is reloaded with the preload value(TIMx_PSC)

To avoid updating the shadow registers when new values are written to the preload registers,the UEV can be disabled by setting TIMx_CTRL1.UPDIS=1.

When an update event occurs, the counter will still be cleared and the prescaler counter will also be set to 0 (but the prescaler value will remain unchanged).

The figure below shows some examples of the counter behavior and the update flags for different division factors in

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the up-counting mode.

Figure 10-3 Timing Diagram of Up-counting with Internal Clock Divider Factor = 2/N

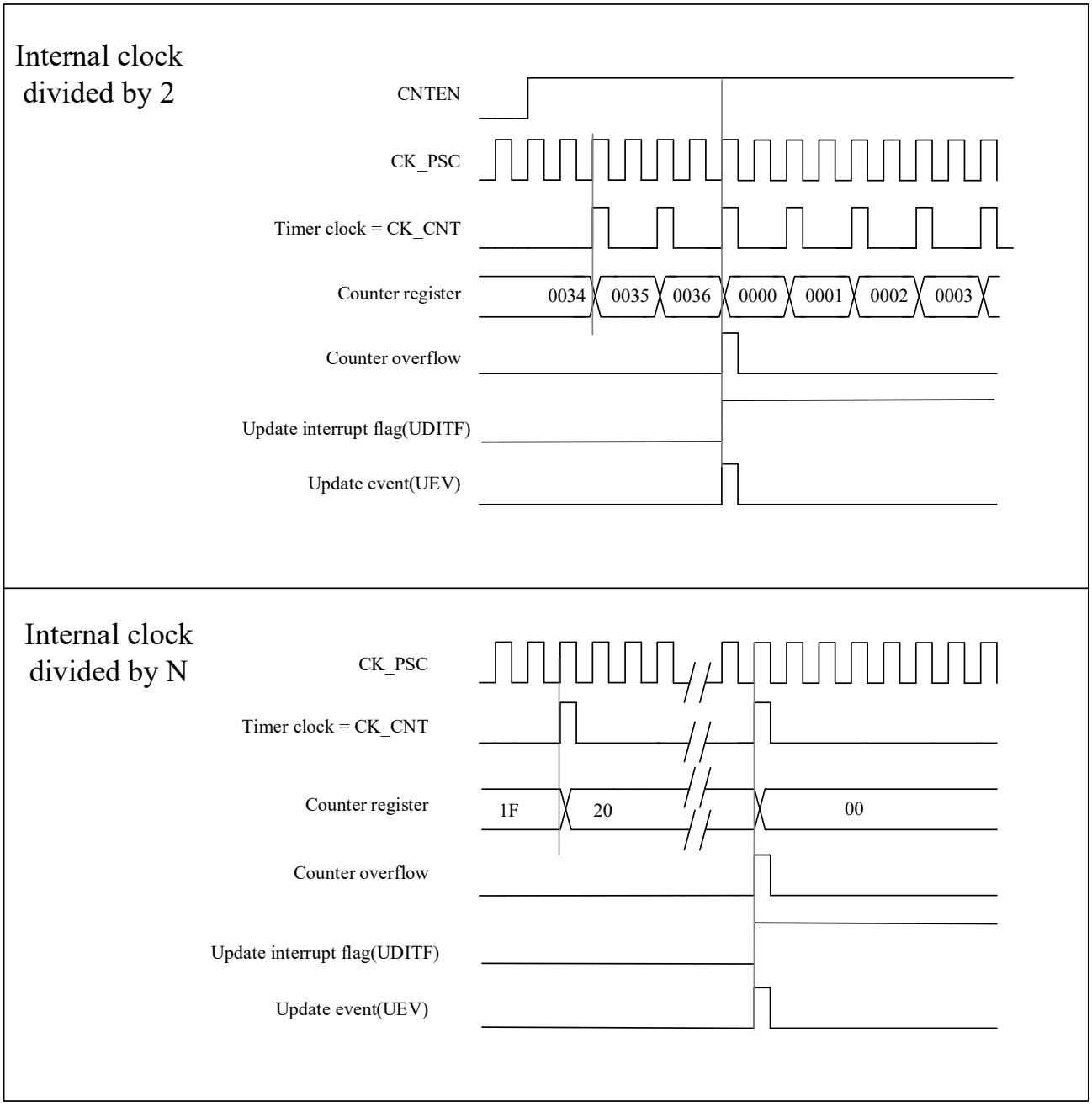

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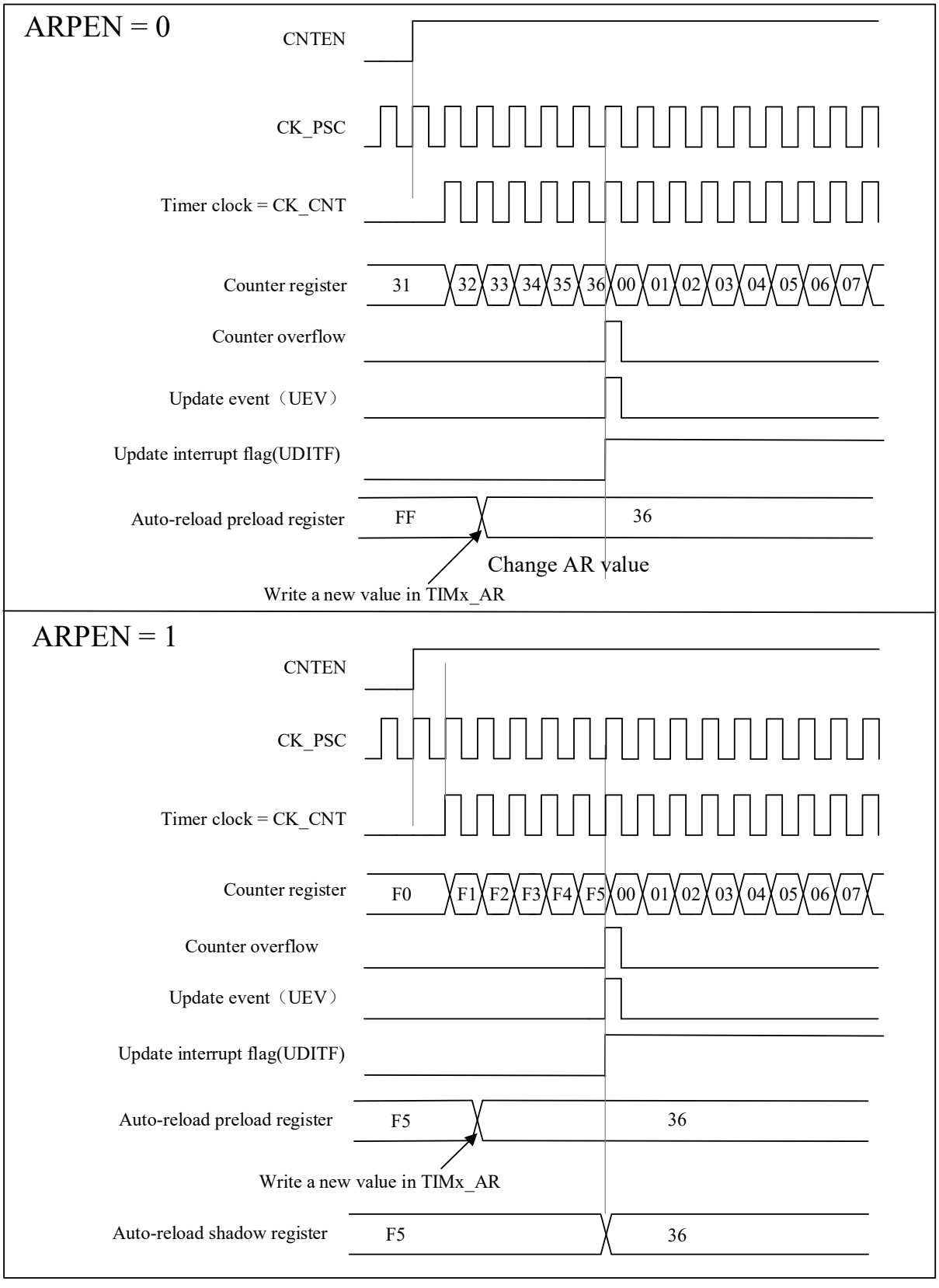
Figure 10-4 Timing Diagram of the Up-counting with Update Evnt when ARPEN=0/1



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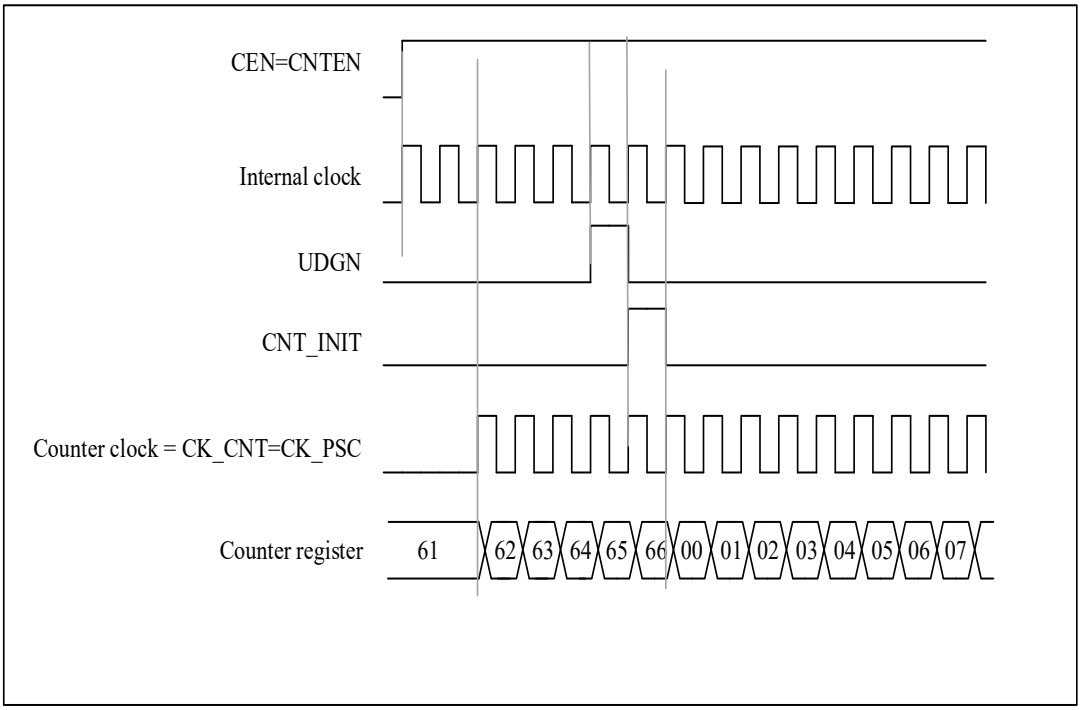
10.3.3 Clock Selection

- The internal clock of timers: CK_INT

10.3.3.1 Internal clock source (CK_INT)

As soon as the TIMx_CTRL1.CNTEN bit is written as '1' by software, the prescaler is clocked by the internal clock CK_INT.

Figure 10-5 Control Circuit in Normal Mode with Internal Clock Divided by 1



10.3.4 Debug Mode

When the microcontroller is in debug mode (the Cortex®-M0 core halted), depending on the DBG_CTRL.TIM6STP configuration in the PWR module, the TIM6 counter can either continue to work normally or stop. For more details, refer to Section 3.4.9.

10.4 TIMx Register(x=6)

For abbreviations used in registers, refer to Section 1.1

These peripheral registers can be operated as half word (16-bits) or word (32-bits).

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10.4.1 Register Overview

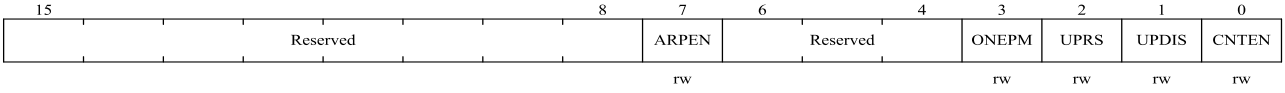
Table 10-1 Register Overview

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
000h	TIMx_CTRL1	Reserved																								ARPEN	Reserved			ONEPM	UPRS	UPDIS	CNTEN
	Reset Value																									0				0	0	0	0
004h ~ 008h	Reserved																																
00Ch	TIMx_DINTEN	Reserved																															UIEN
	Reset Value																																0
010h	TIMx_STS	Reserved																															UDITF
	Reset Value																																0
014h	TIMx_EVTGEN	Reserved																															UDGN
	Reset Value																																0
018h ~ 020hh	Reserved																																
024h	TIMx_CNT	Reserved																CNT[15:0]															
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
028h	TIMx_PSC	Reserved																PSC[15:0]															
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
02Ch	TIMx_AR	Reserved																AR[15:0]															
	Reset Value																	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

10.4.2 Control Register 1 (TIMx_CTRL1)

Offset address: 0x00

Reset value: 0x0000



Bit Field	Name	Description
15:8	Reserved	Reserved, the reset value must be maintained
7	ARPEN	ARPEN: Auto-reload preload enable 0: Shadow register disable for TIMx_AR register

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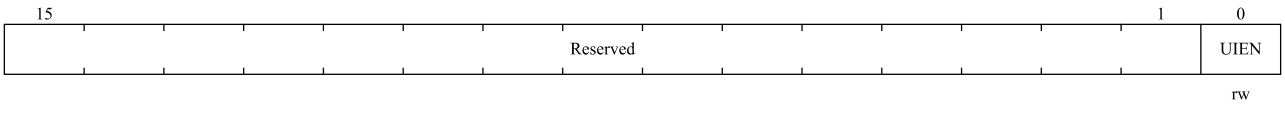
Bit Field	Name	Description
		1: Shadow register enable for TIMx_AR register
6:4	Reserved	Reserved, the reset value must be maintained
3	ONEPM	One-pulse mode 0: Disable one-pulse mode. The counter counts are not affected when an update event occurs. 1: Enable one-pulse mode. The counter stops counting when the next update event occurs (clearing TIMx_CTRL1.CNTEN bit)
2	UPRS	Update request source This bit is used to select the UEV event sources by software. 0: If update interrupt request is enabled, any of the following events will generate an update interrupt request: Counter overflow The TIMx_EVTGEN.UDGN bit is set 1: If update interrupt request is enabled, only counter overflow will generate update interrupt request
1	UPDIS	Update disable This bit is used to enable/disable the update event (UEV) events generation by software. 0: Enable UEV. UEV will be generated if one of following condition been fulfilled: Counter overflow The TIMx_EVTGEN.UDGN bit is set Shadow registers will update with preload value. 1: UEV disabled. No update event is generated, and the shadow registers (AR, PSC) keep their values. If the TIMx_EVTGEN.UDGN bit is set, the counter and prescaler are reinitialized.
0	CNTEN	Counter Enable 0: Disable counter 1: Enable counter

10.4.3 Interrupt Enable Register (TIMx_DINTEN)

Offset address: 0x0C

Reset value: 0x0000



Bit field	Name	Description
15:1	Reserved	Reserved, the reset value must be maintained
0	UIEN	Update interrupt enable 0: Disable update interrupt 1: Enables update interrupt

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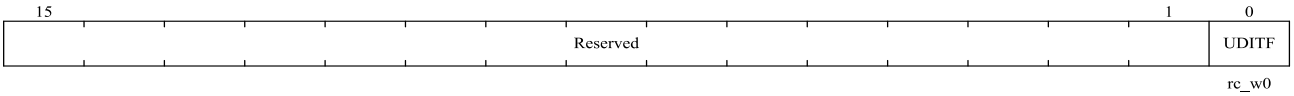
10.4.4 Status Register (TIMx_STS)

Offset address: 0x10

Reset value: 0x0000

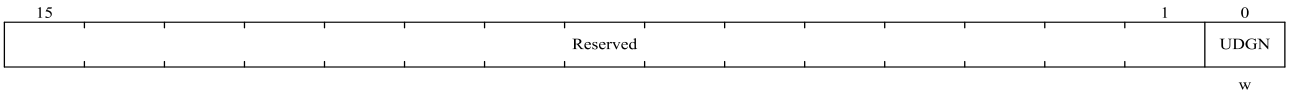


Bit Field	Name	Description
15:1	Reserved	Reserved, the reset value must be maintained
0	UDITF	Update interrupt flag This bit is set by hardware when an update event occurs under the following conditions: -When TIMx_CTRL1.UPDIS = 0, and counter value overflow. -When TIMx_CTRL1.UPDIS = 0 and TIMx_CTRL1.UPRS = 0, and the TIMx_EVTGEN.UDGN bit is set by software to reinitialize the CNT. This bit is cleared by software. 0: No update event occurred 1: Update interrupt occurred

10.4.5 Event Generation Register (TIMx_EVTGEN)

Offset address: 0x14

Reset values: 0 x0000



Bit Field	Name	Description
15:1	Reserved	Reserved, the reset value must be maintained.
0	UDGN	Update generation Software can set this bit to update configuration register value and hardware will clear it automatically. 0: No effect. 1: Timer counter will restart and all shadow register will be updated. It will restart prescaler counter also.

10.4.6 Counter (TIMx_CNT)

Offset address: 0x24

Reset value: 0x0000

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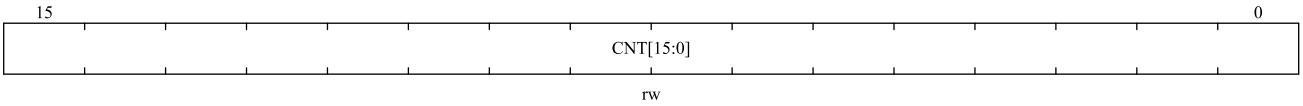
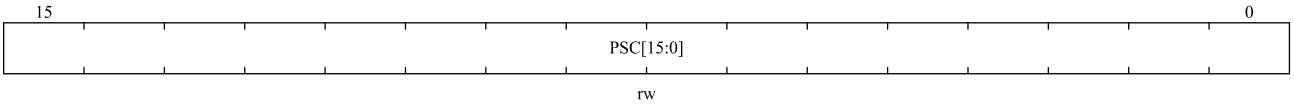


Bit field	Name	Description
15:0	CNT[15:0]	Counter value *Note: when the clock source is configured for LSI, TIMx_CNT does not support writes*

10.4.7 Prescaler (TIMx_PSC)

Offset address: 0x28

Reset value: 0x0000

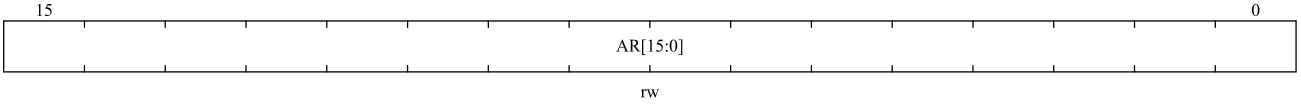


Bit field	Name	Description
15:0	PSC[15:0]	Prescaler value PSC register value will be updated to prescaler register at update event. Counter clock frequency is input clock frequency divide PSC + 1.

10.4.8 Automatic Reload Register (TIMx_AR)

Offset address: 0x2C

Reset values: 0xFFFF



Bit field	Name	Description
15:0	AR[15:0]	Auto-reload value These bits define the value that will be loaded into the actual auto-reload register. refer to Section 10.3.1 for more details. When the TIMx_AR.AR [15:0] value is null, the counter does not work.

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11 Independent Watchdog (IWDG)

11.1 IWDG Introduction

The N32G003 has built-in independent watchdog (IWDG) timer to solve the problems caused by software errors. The watchdog timer is very flexible to use, which improves the security of the system and the accuracy of timing control.

The Independent Watchdog (IWDG) is driving by low-speed internal clock (LSI clock) running at 32 KHz, which will still running even dead loop or MCU stuck is happening. This can provide higher safety level, timing accuracy and flexibility of watchdog. It can reset and resolve system malfunctions due to software failure. The IWDG is best suited for applications that require the watchdog to run as a totally independent process outside the main application, but have lower timing accuracy constraints.

When the power control register PWR_CTRL.IWDGRSTEN bit is '1' and the IWDG counter reaches 0, a system reset will be generated (if this bit is '0', the IWDG will count but not reset). IWDG reset can also be used for low power wake up.

Note: This chapter is based on the system default value PWR_CTRL.IWDGRSTEN = 1.

11.2 IWDG Main Features

- A 12-bit down-counter that runs independently
- The initial count value of the down-counter can be configured, and the pre-frequency can be configured
- After the watchdog is enabled, a system reset occurs when the down-counter reaches 0x000
- Reset enable is configurable
- Support software/hardware startup
- Can choose to stop counting or work normally in debug mode
- Support low power consumption mode: you can choose to work or freeze in STOP mode

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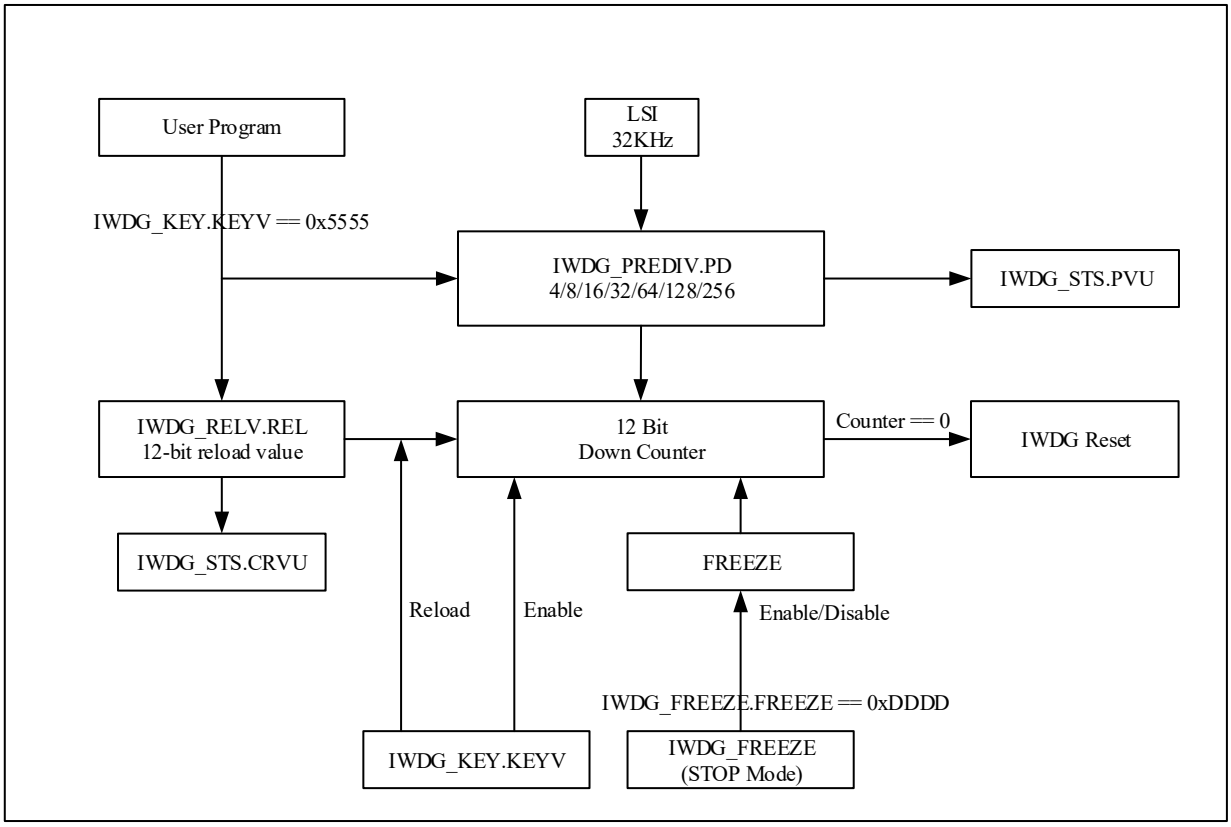
11.3 IWDG Function Description

Figure 11-1 Functional Block Diagram of the Independent Watchdog Module



To enable IWDG, we need to write 0xCCCC to IWDG_KEY.KEYV[15:0] bits. Counter starts counting down from reset value (0xFFF). When counter counts to 0x000, it generates a reset signal (IWDG_RESET) to MCU. Writing 0xDDDD to IWDG_FREEZE enables the IWDG freeze function, which can be configured to make the IWDG counter work or stop in STOP mode. Other than that, as long as 0xAAAA (reload request) is written to IWDG_KEY.KEYV[15:0] bits before reset, the counter value is set to the reload value in the IWDG_RELV.REL[11:0] bits and prevents the watchdog from resetting the entire device.

If the "hardware watchdog timer" function is enabled through the option byte, the watchdog will automatically start running after the system is powered on and will generate a system reset, unless the software reloads the counter before it reaches ‘0’.

11.3.1 Register Access Protection

IWDG_PREDIV and IWDG_RELV registers are write protected. To modify the value of those two registers, user needs to write 0x5555 to IWDG_KEY.KEYV[15:0] bits. Writing other value enables write protections again. IWDG_STS.PVU indicates whether the pre-scaler value update is on going. IWDG_STS.CRVU indicates whether the IWDG is updating the reload value. The hardware sets the IWDG_STS.PVU bit and/or IWDG_STS.CRVU bit when the pre-scaler value and/or reload value is updating. After the pre-scaler value and/or reload value update is complete, the hardware clears the IWDG_STS.PVU bit and/or IWDG_STS.CRVU bit.

The reload operation (IWDG_KEY.KEYV[15:0] is configured with value of 0xAAAA) will also cause the registers to become write protected again.

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11.3.2 Debug Mode

In debug mode (Cortex®-M0 core stops), IWDG counter will either continue to work normally or stop, depending on DBG_CTRL.IWDG_STOP bit in PWR module. If this bit is set to '1', the counter stops. The counter works normally when the bit is '0'. For details, refer to Section 3.3.2 Peripheral Debugging Support.

11.3.3 Low Power Consumption

The working clock of IWDG can be controlled by configuring the IWDG_FREEZE register to ensure the IWDG is suspended in the STOPmode. Refer to the Section 11.5.6 IWDG Freeze register for details.

11.4 User Interface

User interface of IWDG contains 5 registers: Key Register (IWDG_KEY), Pre-scale Register (IWDG_PREDIV), Reload Register (IWDG_RELV), Freeze Register(IWDG_FREEZE) and Status Register (IWDG_STS).

11.4.1 Operate Process

When IWDG is enable from software reset (by writing 0xAAAA to IWDG_KEY.KEYV[15:0] bits) or hardware reset (by clearing FLASH_OB.WDG_SW bit). It starts counting down from 0xFFF. Down counting gap is determined by pre-scale LSI clock. Once the counter is reloaded, each new round will start from the value in IWDG_RELV.REL[11:0] instead of 0xFFF.

When program is running normally, software needs to feed IWDG before counter reaches 0x000 and starts a new round of down counting. When counter reaches 0x000, this indicates program malfunction. IWDG generates reset signal under this circumstance.

If user wants to configure IWDG pre-scaler and reload value register, it needs to write 0x5555 to IWDG_KEY.KEYV[15:0] first, then confirm IWDG_STS.CRVU bit and IWDG_STS.PVU bit. IWDG_STS.CRVU bit indicates reload value update is ongoing, IWDG_STS.PVU indicates pre-scale divider ratio is updating. Only when those two bit are 0 then user can update corresponding value. When update is on-going, hardware sets corresponding bit to 1. At this time, reading IWDG_PREDIV.PD[2:0] or IWDG_RELV.REL[11:0] is invalid since data needs to be synchronized to LSI clock domain. The value read from IWDG_PREDIV.PD[2:0] or IWDG_RELV.REL[11:0] will be valid after hardware clears the IWDG_STS.PVU bit or IWDG_STS.CRVU bit.

If the application uses more than one reload value or pre-scaler value, it must wait until the IWDG_STS.CRVU bit is reset before changing the reload value, the same as changing the pre-scaler value. However, after updating the pre-scale and/or the reload value, it is not necessary to wait until IWDG_STS.CRVU bit and/or IWDG_STS.PVU bit are reset before continuing code execution (even in case of low-power mode entry, the write operation is taken into account and will complete).

Pre-scale register and reload register control the time that generates reset, as shown in Table 11-1.

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Table 11-1 IWDG Overtime Time at 32kHz

Prescaler Divider	IWDG_ PREDIV [2:0]	Min Timeout (ms) (IWDG_PELV11:0]=0)	Max Timeout (ms) (IWDG_PELV[11:0]=0xFFF)
/4	000	0.125	512
/8	001	0.25	1024
/16	010	0.5	2048
/32	011	1	4096
/64	100	2	8192
/128	101	4	16384
/256	11x	8	32768

11.4.2 IWDG Configuration Flow

Software flow:

1. Write 0x5555 to IWDG_KEY.KEYV[15:0] bits to enable write access of IWDG_PREDIV and IWDG_RELV registers.
2. Check IWDG_STS.PVU bit and IWDG_STS.CRVU bit. If they are 0, continue next step.
3. Configure IWDG_PREDIV.PD[2:0] bits to select pre-scale value.
4. Configure IWDG_RELV.REL[11:0] bits to reload value.
5. Write 0xAAAA to IWDG_KEY.KEYV[15:0] bits to upload counter with reload value.
6. Configure the IWDG_FREEZE register
7. Write 0xCCCC to IWDG_KEY.KEYV[15:0] bits to start the watchdog

If user needs to modify the prescaler value and reload value, repeat steps 1 to 5; if not, just feed the dog with step 5 at regular intervals.

11.5 IWDG Registers

11.5.1 IWDG Register Map

Table 11-2 IWDG Register Map and Reset Values

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
000h	IWDG_KEY	Reserved																KEYV[15:0]															
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
004h	IWDG_PREDIV	Reserved																													PD[2:0]		
	Reset Value																														0	0	0
008h	IWDG_RELV	Reserved																REL[11:0]															
	Reset Value																	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
00Ch	IWDG_STS	Reserved																														CRVU	PVU
	Reset Value																															0	0

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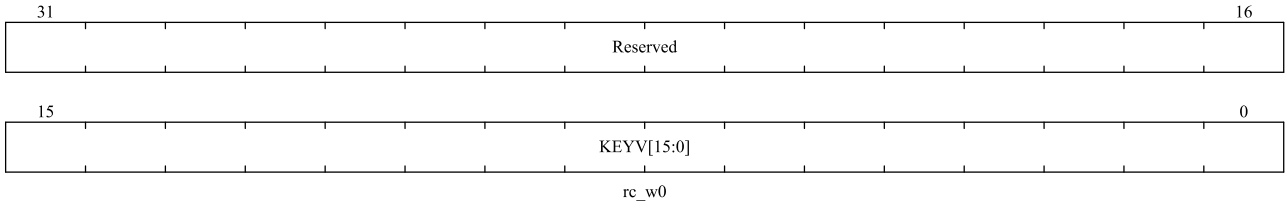
Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
010h	IWDG_FREEZE	Reserved																															FREEZE
	Reset Value																																0

11.5.2 IWDG Key Register (IWDG_KEY)

Address offset: 0x00

Reset value: 0x0000 0000

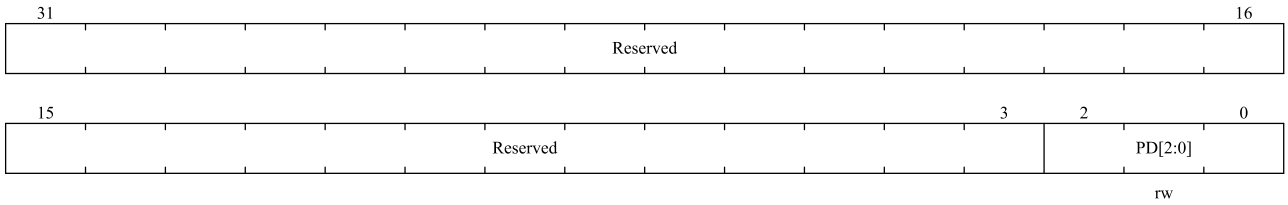


Bit Field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained.
15:0	KEYV[15:0]	Key value register: only certain value will serve particular function. **0xCCCC:** Start watch dog counter, and does not have any effect if hardware watchdog is enable. (if hardware watchdog is selected, it is not limited by this command word) **0xAAAA:** Reload counter with REL value in IWDG_RELV register to prevent reset. **0x5555:** Disable write protection of IWDG_PREDIV and IWDG_RELV register

11.5.3 IWDG Pre-scaler Register (IWDG_PREDIV)

Address offset: 0x04

Reset value: 0x0000 0000



Bit Field	Name	Description
31:3	Reserved	Reserved, the reset value must be maintained.
2:0	PD[2:0]	Pre-frequency division factor With write access protection when IWDG_KEY.KEYV[15:0] is not 0x5555. The IWDG_STS.PVU bit must be 0 otherwise PD [2:0] value cannot be changed. Divide number is as follow: 000: Prescaler divider =4 001: Prescaler divider =8 010: Prescaler divider =16 011: Prescaler divider =32

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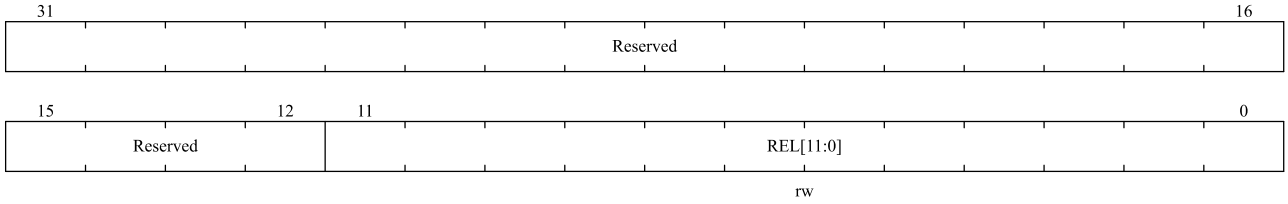
		100: Prescaler divider =64 101: Prescaler divider =128 11x: Prescaler divider =256 *Note: Reading this register will return the pre-divided value from the VDD voltage domain. If a write operation is in progress, the read-back value may be invalid. Therefore, the read value is valid only when the IWDG_STS.PVU bit is '0'.*

11.5.4 IWDG Reload Register (IWDG_RELV)

Address offset: 0x08

Reset value: 0x0000 0FFF

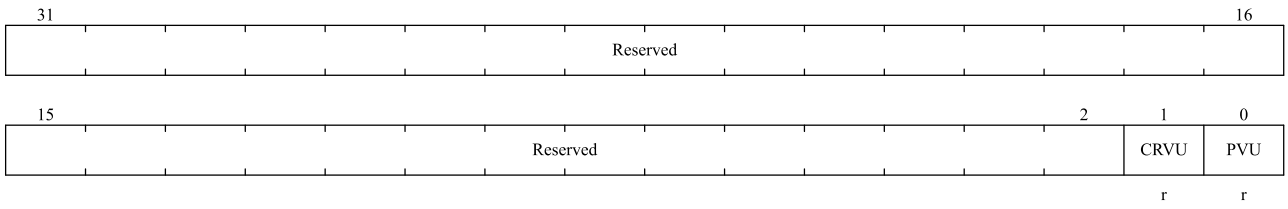


Bit Field	Name	Description
31:12	Reserved	Reserved, the reset value must be maintained.
11:0	REL[11:0]	Watchdog counter reload value. With write protection. Defines the reload value of the watchdog counter, which is loaded to the counter every time 0xAAAA is written to IWDG_KEY.KEYV[15:0] bits. The counter then starts to count down from this value. The watchdog timeout period can be calculated from this reloading value and the clock pre-scaler value, refer to Table 11-1. This register can only be modified when the IWDG_STS.CRVU bit is '0'. *Note: reading this register will return the reload value from the VDD voltage domain. If a write operation is in progress, the read-back value may be invalid. Therefore, the read value is valid only when the IWDG_STS.CRVU bit is '0'.*

11.5.5 IWDG Status Register (IWDG_STS)

Address offset: 0x0C

Reset value: 0x0000 0000



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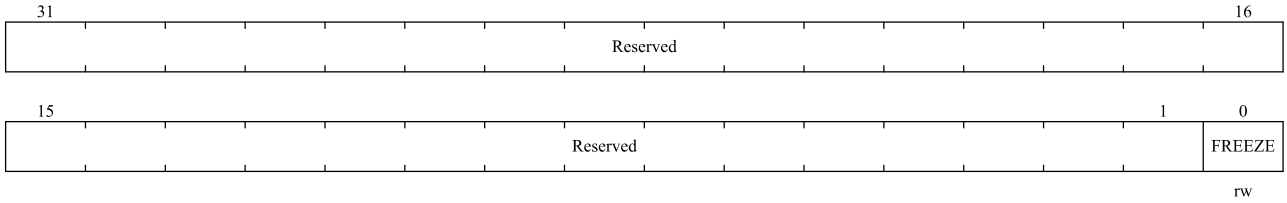
Bit Field	Name	Description
31: 2	Reserved	Reserved, the reset value must be maintained.
1	CRVU	Watchdog reload value update This bit indicates an update of reload value is ongoing. Set and clear by hardware(up to 5 RC cycles of 32kHz). Software can only try to change IWDG_RELV.REL[11:0] value when IWDG_KEY.KEYV[15:0] bits' value is 0x5555 and this bit is 0.
0	PVU	Watchdog prescaler value update This bit indicates an update of pre-scaler value is ongoing. Set and clear by hardware(up to 5 RC cycles of 32kHz). Software can only try to change IWDG_PREDIV.PD[2:0] value when IWDG_KEY.KEYV[15:0] bits' value is 0x5555 and this bit is 0.

11.5.6 IWDG Freeze Register (IWDG_FREEZE)

Address offset: 0x010

Reset value: 0x0000 0000



Bit Field	Name	Description
31:1	Reserved	Reserved, the reset value must be maintained.
0	FREEZE	STOP mode freeze function 1. The initial value of IWDG_FREEZE.FREEZE bit is 0x00; 2. When writing 0xDDDD to this address, IWDG_FREEZE.FREEZE flips once and becomes 1, and controls counter stops after entering STOP mode. 3. When 0xDDDD is written to the address again, IWDG_FREEZE.FREEZE flips once and becomes 0, and controls counter continues to count after entering STOP mode. 4. And so on The current value of IWDG_FREEZE.FREEZE can be determined by reading the freeze register firstly, and then the switch freeze operation can be performed.

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12 Analog To Digital Conversion (ADC)

12.1 ADC Introduction

The 12-bit ADC is a high-speed analog-to-digital converter using successive approximation. It can measure 10 channel signal sources. It has 9 external and 1 internal channels. Each channel of the A/D conversion performed in single, continuous or scan mode. ADC measurements are stored (left-aligned/ right-aligned) in 16-bit data registers. The application detects the input voltage within user-defined high/low thresholds by analog watchdog and the maximum frequency of the input clock to the ADC is 24MHz.

12.2 Main Features

- Supports 1 ADC, supports single-ended inputs, and can measure 9 external and 1 internal sources
- Supports 12-bit resolution with a maximum sampling rate of 1MSPS
- ADC clock source is divided into working clock source and timing clock source
  - HSI as the ADC_CLK working clock source with a maximum frequency of 24MHz.
  - HSI as the ADC_1MCLK timing clock source for internal timing functions, and the frequency must be configured to 1MHz.
- Supports timer trigger ADC sampling
- Interrupts at the end of conversion, and simulated watchdog events
- Support 2 conversion modes
  - Single conversion
  - Continuous conversion
- Scan mode supports up to any 5 channels, and each channel has an independent result data register buffer
- All channel sampling intervals can be programmed uniformly
- Regular conversion has external triggering options
- ADC power supply requirements: 2.4V to 5.5V
- ADC input range: $0 \leq V_{IN} \leq V_{DD}$

12.3 ADC Function Description

Below is a block diagram of an ADC module. Table 12-1 shows the description of ADC pins.

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Figure 12-1 Block Diagram of ADC

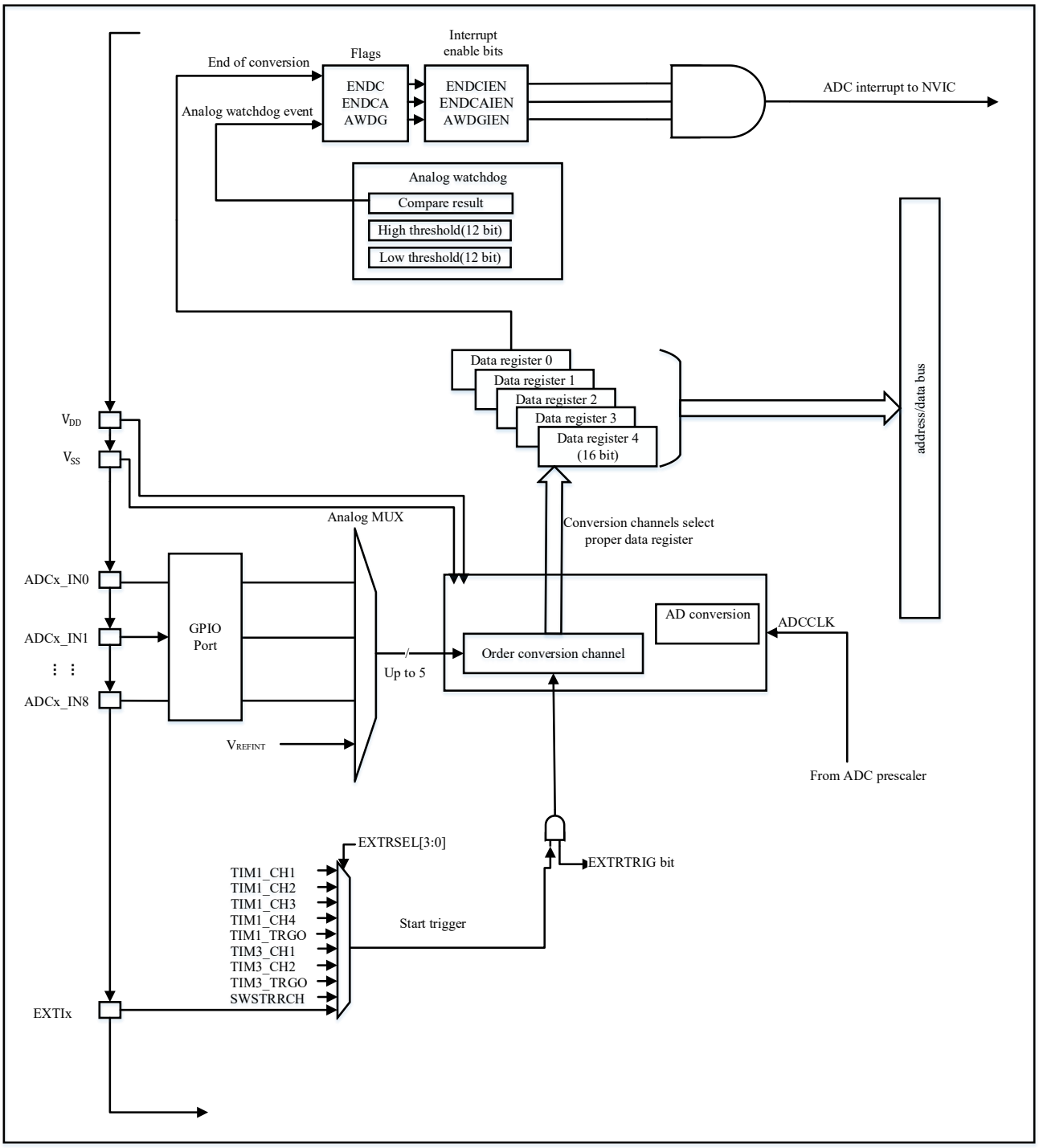

Table 12-1 ADC Pins

Name	Signal Types	Annotations
V_{DD}	Input, analog power supply	Equivalent to V_{DD} analog power supply and: $2V \le V_{DD} \le 5.5$ V
V_{SS}	Input, analog power supply ground	Equivalent to V_{SS} analog power supply ground
ADCx_IN[8:0]	Analog input signal	9 analog external input channels

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12.3.1 ADC Clock

An ADC requires three clocks, ADC_CLK, HCLK, and ADC_1MCLK.

- HCLK is used for the register access.
- ADC_CLK is the working clock of ADC.
- ADC_1MCLK is used for internal timing function, configured in RCC, and its frequency must be configured to 1M

Note:

1. *The ADC_CLK frequency division factor can be configured with maximum frequency of 24MHz. The ADC_CLK frequency division factor can be 1,2,3,4,6,8,10,12,24,32*

12.3.2 ADC Switch Control

User can proceed to the next step only after the power-up process is complete by polling the ADC_CTRL3.RDY bit.

User can set the ADC_CTRL2.ON bit to turn on the ADC. When the ADC_CTRL2.ON bit is set for the first time, it wakes up the ADC from the power-off state. After a power-on delay of ADC (t_{STAB}), the conversion begins when the ADC_CTRL2.ON bit is set again.

The conversion can be stopped by clearing the ADC_CTRL2.ON bit and placing the ADC in power-off mode. In this mode, the ADC consumes almost no power consumption (just a few μA). Power-down state of ADC can be checked by polling the ADC_CTRL3.PDRDY bit.

When the ADC is disabled, the default mode is power-down.

12.3.3 Channel Selection

Each channel can be configured as a regular sequence. A series of conversions can be performed in any order on any number of channels. For example, the conversion can be completed in the following order: channel 3, channel 8, channel 2, channel 1, channel 0.

The regular sequence consists of multiple conversions, up to a maximum of 5. The ADC_DATx.SEQx[3:0] bits specify the regular channels and their conversion sequence. The ADC_CTRL2.LEN[2:0] bits specify the regular channel sequence length.

Note: During conversion, changes to the ADC_DATx.SEQx[3:0] are prohibited; the ADC_DATx.SEQx[3:0] bits can only be changed when the ADC is idle.

12.3.4 Internal Channel

The V_{REFINT} is connected with channel ADC_IN9.

Internal channels can be converted by regular channels.

12.3.5 Single Conversion Mode

The ADC can enter the single conversion mode by configuring ADC_CTRL2.CTU to 0. In this mode, external triggering or setting ADC_CTRL2.ON=1 can start the ADC to start conversion, and the ADC only performs signleconversion.

After the conversion starts, when a regular channel conversion is completed, the regular channel end of

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conversionflag (ADC_STS.ENDC) will be set to 1. If the regular channel end of conversion interrupt enable (ADC_CTRL1.ENDCIEN) bit is set to 1, an interrupt will be generated, and the converted data will be stored in the ADC_DATx.DAT[15:0] register.

After single conversion, the ADC stops.

12.3.6 Continuous Conversion Mode

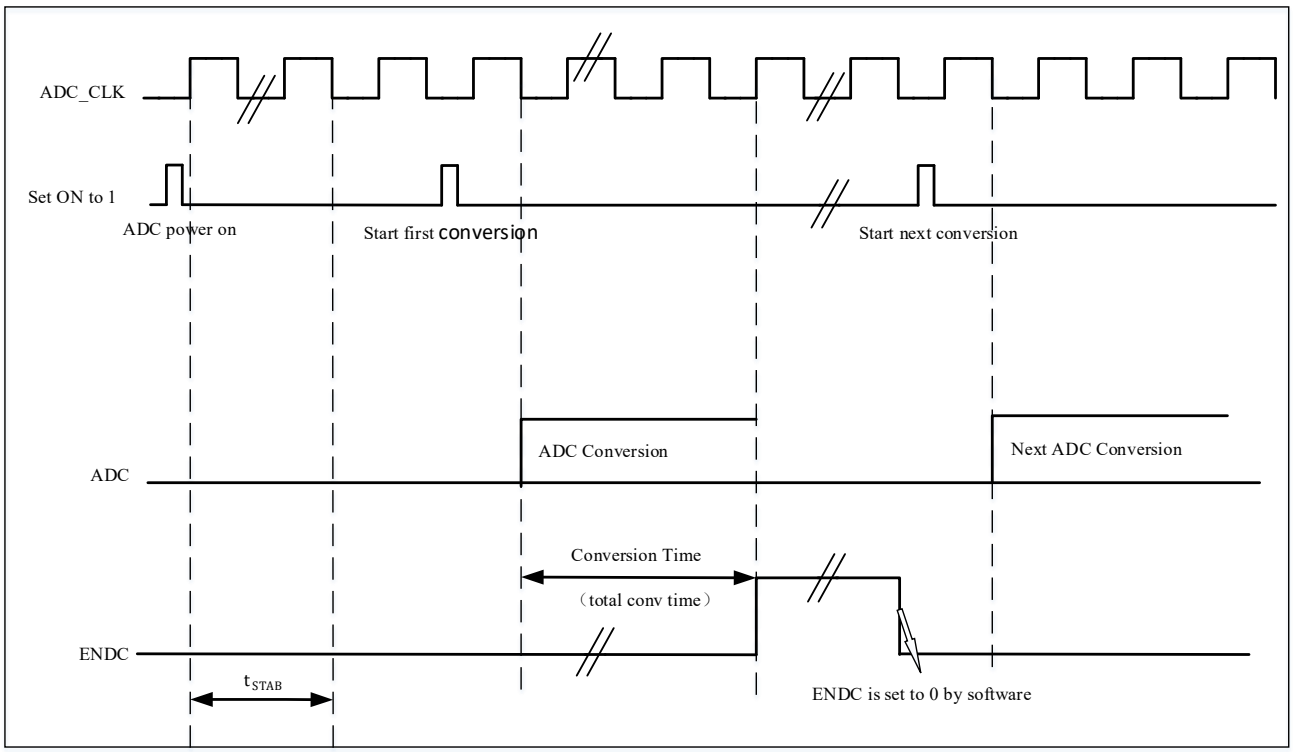
The ADC can enter the continuous conversion mode by configuring ADC_CTRL2.CTU to 1. In this mode, external triggering or setting ADC_CTRL2.ON to 1 can start the ADC conversion, and the ADC will continuously convert the selected channels.

After the conversion starts, when a regular channel conversion is completed, the regular channel end of conversion flag (ADC_STS.ENDC) will be set to 1. If the regular channel end of conversion interrupt enable bit (ADC_CTRL1.ENDCIEN) is set to 1, an interrupt will be generated. The converted data will be stored in the ADC_DATx.DAT[15:0] register.

12.3.7 Timing Diagram

When ADC_CTRL2.ON is set to 1 for the first time, the ADC is powered on. After the ADC is powered on, the ADC needs a certain time(tSTAB) to ensure its stability. After the ADC is stabilized, ADC_CTRL2.ON is set to 1. At this time, set ADC_CTRL2.ON to 1 again through software to start the conversion. After 24 cycles, the end of conversion flag will be set to 1 after the conversion is completed.

Figure 12-2 Timing Diagram



12.3.8 Analog Watchdog

The analog watchdog can be enabled on the regular channel by setting ADC_CTRL1.AWDGERCH to 1. The high

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threshold of the analog watchdog can be set by configuring ADC_WDGHIGH.HTH, and the low threshold of the analog watchdog can be set by configuring ADC_WDGLOW.LTH. The threshold of the analog watchdog independent of data alignment, because the comparison of the ADC's conversion value with the threshold is done before the alignment . When the value of ADC analog conversion is higher than the high threshold of the analog watchdog or lower than the low threshold of the analog watchdog, the analog watchdog flag (ADC_STS.AWDG) will be set to 1. If ADC_CTRL1.AWDGIEN has been configured to 1, an interrupt will be generated at this time. The analog watchdog can be controlled for one or more channels by configuring ADC_CTRL1.AWDSGSGLEN and ADC_CTRL1.AWDGCH[3:0].

Table 12-2 Analog Watchdog Channel Selection

Channel	ADC_CTRL1 Register Control Bit	
	AWDGSGLEN	AWDGERCH
All regular channels	0	1
Single regular channel	1	1

12.3.9 Scan Mode

By configuring ADC_CTRL1.SCAMD to 1, the scan mode can be turned on, and the ADC will scan and convert all the channels selected in ADC_DATx.SEQx[3:0]. Each sequence can select any channel for conversion. After the conversion is started, the channels will be converted sequentially one by one, supporting up to 5 conversion sequences. If ADC_CTRL2.CTU is 1 at this time, the conversion will be restarted from the first channel of the conversion sequence after the conversion of all selected channels is completed.

12.4 Data Aligned

There are two alignment methods for data storage after conversion: left-aligned and right-aligned. The alignment can be set by the ADC_CTRL2.ALIG bit. ADC_CTRL2.ALIG = 0 is right-aligned, while ADC_CTRL2.ALIG = 1 is left-aligned, as shown in following tables.

Table 12-3 Right-align data

0	0	0	0	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

Table 12-4 Left-align data

D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	0	0	0	0

12.5 Programmable Channel Sampling Time

Specify the number of sampling cycles of ADC in ADC_SAMPT.SAMP[4:0], and then the ADC samples the input voltage in the specified sampling cycle. For different channels, Sampling intervals can be programmed uniformly. The total conversion time is calculated as follows:

$$T_{CONV} = \text{Sampling time} + 12 \text{ cycles}$$

Example:

With ADCCLK=24MHz, the sampling time is 12 cycles and resolution is 12bit, the total conversion time is "12 +

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12" ADCCLK Cycles, that is:

$$T_{CONV} = 12 + 12 = 24 \text{ cycle} = 1\mu s$$

Note: All ADC channels share a channel sample time configuration.

12.6 Externally Triggered Conversion

For the regular sequence, software sets the ADC_CTRL2.EXTRTRIG bit to 1, then the regular channel can use the rising edge of the external event to trigger the start conversion, and then the software sets the ADC_CTRL2.EXTRSEL[3:0] bits to select the external trigger source of the regular sequence. The external trigger source selection is shown in the table below. User can set the AFIO _CFG.EXTI_ETRR[4:0] bits to select EXTI line as the external trigger source, or start the regular channel conversion by setting ADC_CTRL2.SWSTRRCH to 1 if SWSTRRCH is seleted as the external trigger source.

Table 12-5 ADC is Used for External Triggering of Regular Channels

EXTRSEL[3:0]	Trigger Source	Type
0000	TIM1_CC1 event	Internal signal from the on-chip timer
0001	TIM1_CC2 event	
0010	TIM1_CC3 event	
0011	TIM1_CC4 event	
0100	TIM1_ TRGO event	
0101	TIM3_TRGO event	
0110	TIM3_CC1 event	
0111	TIM3_CC2 event	
1000	EXTI line event	External pin/internal signal from on-chip timer
1001	SWSTRRCH	Software control bit

12.7 ADC interrupt

ADC interrupts can be from an end of conversion of regular sequence, an analog watchdog event when input voltage exceeds the threshold, any end of regular channel conversion. These interrupts have independent interrupt enable bits.

There is a status flag in the ADC_STS register, without interrupt associated with this flag in the ADC: regular sequence channel conversion started (STR)

Table 12-6 ADC Interrupt

Interrupt Event	Event Flags	Enable Eontrol Bit
Regular sequence conversion is complete	ENDC	ENDCIEN
Analog watchdog status bit is set	AWDG	AWDGIEN
Any regular channel interruption is enabled	ENDCA	ENDCAIEN

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12.8 ADC Registers

12.8.1 ADC Registers

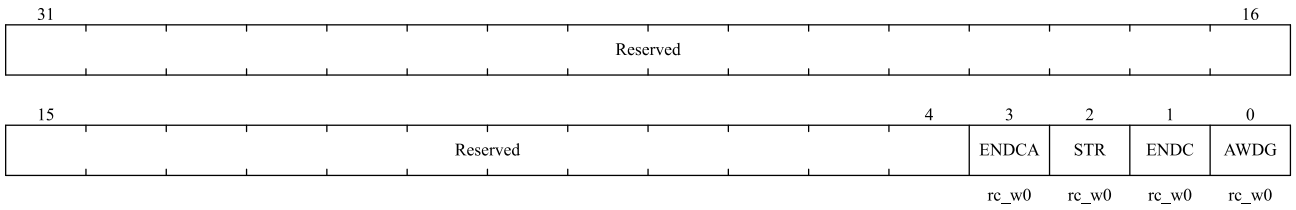
Table 12-7 Register Overview

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
000h	ADC_STS	Reserved																												ENDCA	STR	ENDC	AWDG
	Reset Value																													0	0	0	0
004h	ADC_CTRL1	Reserved																							TEST_EN	AWDGEN	AWDGSGLEN	AWDGIEN	ENDCIEN	AWDGCH[3:0]			
	Reset Value																								0	0	0	0	0	0	0	0	0
008h	ADC_CTRL2	Reserved																			COV_MODE	LEN[2:0]			SWSTART	EXTRTRIG	EXTRSEL[3:0]			ALIG	CONT	ON	
	Reset Value																				0	0	0	0	0	0	0	0	0	0	0	0	0
00Ch	ADC_CTRL3	Reserved																										ENDCAIEN	PDRDY	RDY	BUF_READY	BUF_EN	Reserved
	Reset Value																											0	1	0	0	0	
010h	ADC_SAMP	Reserved																												SAMP[4:0]			
	Reset Value																													0	0	0	0	0
014h	ADC_WDGHIGH	Reserved																			HTH[11:0]												
	Reset Value																				1	1	1	1	1	1	1	1	1	1	1	1	1
018h	ADC_WDGLOW	Reserved																			LTH[11:0]												
	Reset Value																				0	0	0	0	0	0	0	0	0	0	0	0	0
01Ch	ADC_DAT0	Reserved												SEQ0[19:16]				DAT0[15:0]															
	Reset Value													0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
020h	ADC_DAT1	Reserved												SEQ1[19:16]				DAT1[15:0]															
	Reset Value													0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
024h	ADC_DAT2	Reserved												SEQ2[19:16]				DAT2[15:0]															
	Reset Value													0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
028h	ADC_DAT3	Reserved												SEQ3[19:16]				DAT3[15:0]															
	Reset Value													0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
02Ch	ADC_DAT4	Reserved												SEQ4[19:16]				DAT4[15:0]															
	Reset Value													0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

12.8.2 ADC Status Register (ADC_STS)

Address offset: 0x00

Reset value: 0x0000 0000



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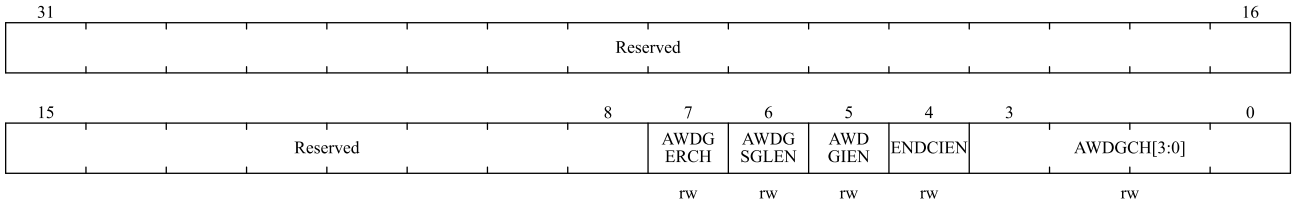
Bit Field	Name	Description
31:4	Reserved	Reserved,the reset value must be maintained.
3	ENDCA	Any channel End of conversion Flag This bit is set by hardware at the end of regular channel conversion and cleared by software. 0: The conversion is not complete; 1: The conversion is complete.
2	STR	Regular channel start flag This bit is set by hardware at the start of regular channel conversion and cleared by software. 0: Regular channel conversion has not started. 1: Regular channel conversion has started.
1	ENDC	End of conversion This bit is set by hardware at the end of channel sequence conversion and cleared by software 0: the conversion is not complete. 1: The conversion is complete.
0	AWDG	Analog watchdog flag This bit is set by hardware and cleared by software when converted voltage values are outside the range defined by the ADC_WDGHIGH.HTH and ADC_WDGLOW.LTH registers 0: No simulated watchdog event occurs; 1: The simulated watchdog event occurs.

12.8.3 ADC Control Register 1 (ADC_CTRL1)

Address offset: 0x04

Reset value: 0x0000 0000



Bit Field	Name	Description
31:8	Reserved	Reserved,the reset value must be maintained.
7	AWDGERCH	Analog watchdog enable on regular channels This bit is set and cleared by the software. 0: Disables analog watchdog on regular channel. 1: Use analog watchdog on regular channels.
6	AWDGSGLEN	Enable the watchdog on a single channel in scan mode This bit is set and cleared by software to enable or disable analog watchdog functions on channels specified by ADC_CTRL1.AWDGCH[3:0] 0: Use watchdog on all channels. 1: Use watchdog on single channel.

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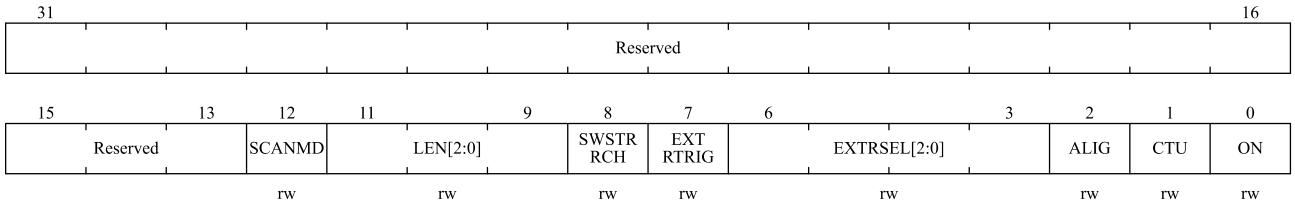
Bit Field	Name	Description
5	AWDGIEN	Analog watchdog interrupt enable This bit is set and cleared by software to disallow or allow interrupt generated by simulated watchdog.In scan mode, if the watchdog detects an out-of-range value, the scan is aborted only when that bit is set. 0: Disable analog watchdog interruption. 1: Enable analog watchdog interruption.
4	ENDCIEN	Interrupt enable for any channels This bit is set and cleared by the software to disallow or allow interrupts to occur after the regular channel conversion ends. 0: Disable ENDC interruption. 1: Enable ENDC interruption.
3:0	AWDGCH[3:0]	Analog watchdog channel select bits These bits are set and cleared by software. They select the input channel to be guarded by the analog watchdog. 0000: ADC analog Channel0 0001: ADC analog Channel1 .... 1001: ADC analog Channel9 Reserved all other values.

12.8.4 ADC Control Register 2 (ADC_CTRL2)

Address offset: 0x08

Reset value: 0x0000 0000



Bit Field	Name	Description
31:13	Reserved	Reserved,the reset value must be maintained.
12	SCANMD	Scan mode This bit is set and cleared by the software to enable or disable scan mode. In scan mode, the conversion is made by ADC_DATx.ADC_SEQx[3:0] register. 0: Disable scan mode. 1: Enable scan mode. *Note: if the ADC_CTRL1.ENDCIEN bits are set separately, ADC_STS.ENDC interrupts occur only after the last channel has been converted.*
11:9	LEN[2:0]	Channel sequence length These bits are written by software to define the total number of conversions in the

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Bit Field	Name	Description
		channel conversion sequence. 000: 1 conversion 001: 2 conversions 010: 3 conversions 011: 4 conversions 100: 5 conversions
8	SWSTRRCH	Start conversion of channels This bit is set by software to start conversion and cleared by hardware as soon as conversion starts. It starts a conversion of a group of channels if SWSTRRCH is selected as trigger event by the ADC_CTRL2.EXTRSEL[3:0] bits. 0: Reset state 1: Starts conversion of channels
7	EXTRTRIG	External trigger conversion mode for channels This bit is set and cleared by software to enable or disable external triggering events that can initiate channel group conversion. 0: Start conversion without external events; 1: Use an external event to start the conversion.
6:3	EXTRSEL[3:0]	External event select for regular sequence These bits select external events to start the regular sequence conversion The triggering configuration of ADC is as follows: 0000: Timer 1 CC1 event 0001: Timer 1 CC2 event 0010: Timer 1 CC3 event 0011: Timer 1 CC4 event 0100: Timer 1 TRGO event 0101: Timer 3 TRGO event 0110: Timer 3 CC1 event 0111: Timer 3 CC2 event 1000: EXTI line 1001: SWSTRRCH
2	ALIG	Data alignment This bit is set and cleared by the software. 0: Right-aligned; 1: Left-align.
1	CTU	Continuous conversion This bit is set and cleared by the software.If this bit is set, the conversion continues until the bit is cleared. 0: single conversion mode. 1: Continuous conversion mode.

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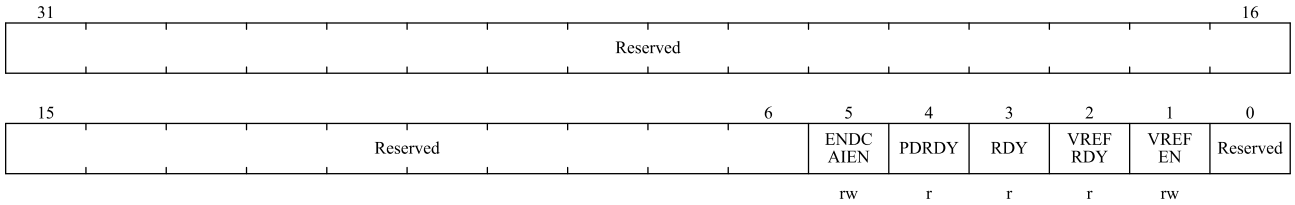
Bit Field	Name	Description
0	ON	A/D Converter ON/OFF This bit is set and cleared by the software.When the bit is' 0 ', writing '1' will wake the ADC from power-off mode. When the bit is' 1 ', writing '1' starts the conversion.The application should note that there is a delay t between the time the converter is powered on and the time the conversion begins t_{STAB}, refer to Figure 12-2. 0: close ADC conversion and enter power off mode; 1: Start ADC and start conversion. *Note: if there are other bits changed in this register along with ON, the conversion will not be triggered.This is to prevent the wrong conversion from being triggered.*

12.8.5 ADC Control Register 3 (ADC_CTRL3)

Address offset: 0x0C

Reset value: 0x0000 0040



Bit Field	Name	Description
31:6	Reserved	Reserved,the reset value must be maintained.
5	ENDCAIEN	Interrupt enable for any channels This bit is set and cleared by the software to enable/disable channel conversion to end the interrupt 0: ADC_STS.ENDCA interrupt is disabled 1: ADC_STS.ENDCA interrupt is enabled
4	PDRDY	ADC power down ready 0: ADC is powered on 1: ADC is powered down
3	RDY	ADC Ready 0: Not ready 1: Get ready
2	VREFRDY	VREFINT_READY ADC internal input buffer ready status, software must check this status bit before measuring VREFINT 0: VREFINT not ready 1: VREFINT is ready
1	VREFEN	VREFINT Enable ADC internal input buffer is enabled, software must enable this bit before measuring VREFINT 0: Disable VREFINT measurement 1: Enable VREFINT measurement

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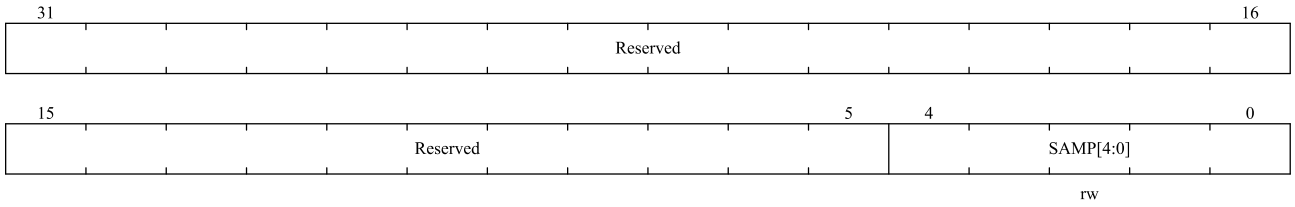
Bit Field	Name	Description
0	Reserved	Reserved,the reset value must be maintained.

12.8.6 ADC Sampling Time Register (ADC_ SAMPT)

Address offset: 0x10

Reset value: 0x0000 0000



Bit Field	Name	Description
31:5	Reserved	Reserved,the reset value must be maintained.
4:0	SAMP[4:0]	Channel sample time selection These bits are written by software to select the sample time for channel. During sample cycles channel selection bits must remain unchanged. 00000: reserved 00001: 8 cycles(only set for working clock of 20MHz,the frequency of HSI is 40MHz) 00010: 12 cycles 00011: 14 cycles 00100: 20 cycles 00101: 26 cycles 00110: 30 cycles 00111: 42 cycles 01000: 56 cycles 01001: 72 cycles 01010: 88 cycles 01011: 120 cycles 01100: 182 cycles 01101: 240 cycles 01110: 380 cycles 01111: 760 cycles 10000: 1520 cycles 10001: 3040 cycles

12.8.7 ADC Watchdog High Threshold Register (ADC_WDGHIGH)

Address offset: 0x14

Reset value: 0x00000FFF

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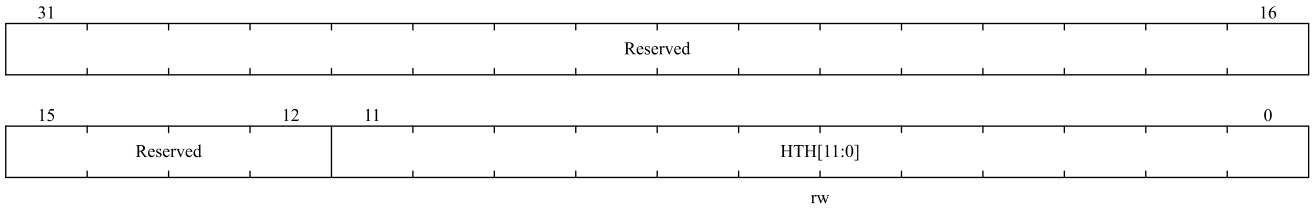
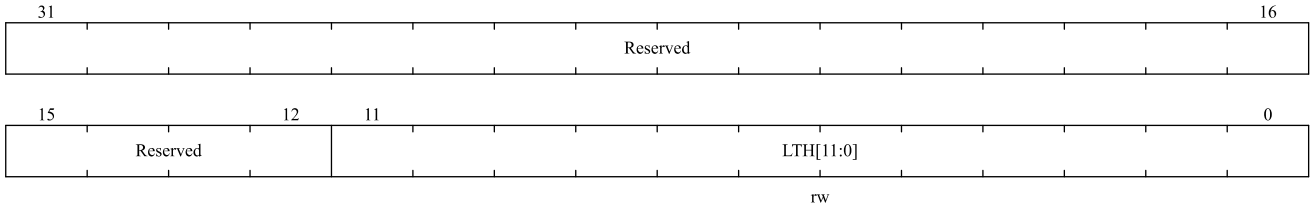


Bit Field	Name	Description
31:12	Reserved	Reserved,the reset value must be maintained.
11:0	HTH[11:0]	Analog watchdog high threshold These bits define the high threshold for simulating a watchdog.

12.8.8 ADC Watchdog Low Threshold Register (ADC_WDGLOW)

Address offset: 0x18

Reset value: 0x0000 0000

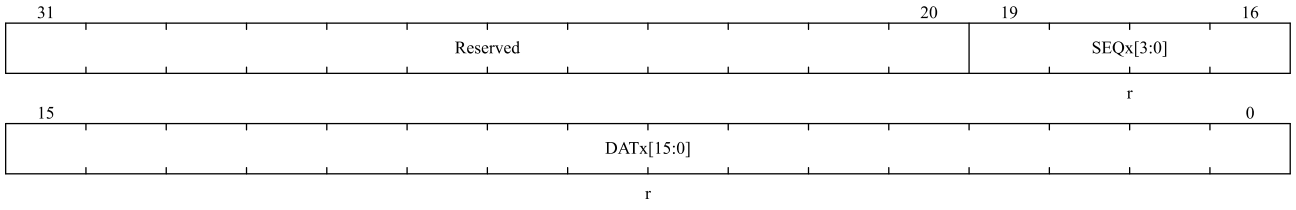


Bit Field	Name	Description
31:12	Reserved	Reserved,the reset value must be maintained.
11:0	LTH[11:0]	Analog watchdog low threshold These bits define the lower threshold for simulating a watchdog.

12.8.9 ADC Regular Data Register x (ADC_DATx) (x= 0..4)

Address offset: 0x1C-0x2C

Reset value: 0x0000 0000



Bit Field	Name	Description
31:20	Reserved	Reserved,the reset value must be maintained.
19:16	SEQx[3:0]	Conversion channel of selecting proper data register 0000: channel 0

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Bit Field	Name	Description
		… 1001: channel 9 Others: reserved
15:0	DATx[15:0]	Regular data for conversions These bits are read-only and contain the conversion results of the regular channel.The data is left-aligned or right-aligned.

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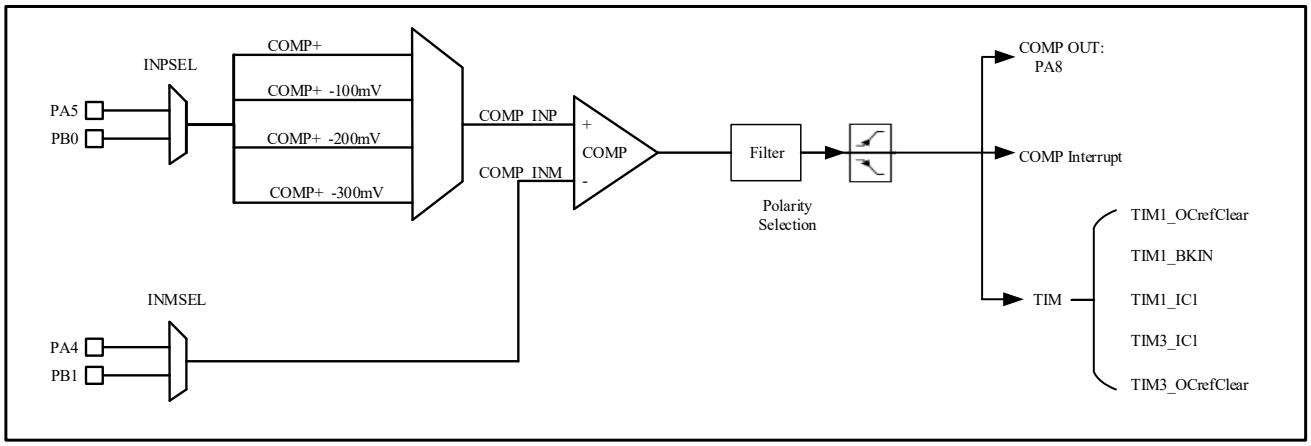
13 Comparator (COMP)

The COMP module is used to compare the analog voltages of two inputs and output high/low levels based on the comparison results.When the input voltage of "INP" is higher than the input voltage of "INM", the comparator output is high; when the input voltage of "INP" is lower than the input voltage of "INM", the comparator output is low.

13.1 COMP System Connection Block Diagram

The COMP module supports an independent comparator, which is connected to the APB bus.

Figure 13-1 Comparator System Connection Diagram



13.2 COMP Features

- Operating votage range: 2.4~5.5V
- A comparator with substraction, supports positive port input voltage(500mV~VDD-200mV) subtracting a reference voltage(300/200/100/0mV)
- Supports filter clock
- Output polarity can be configured as high and low
- The hysteresis can be configured with none, low, medium, or high
- The comparison result can be output to the I/O port or trigger timer, which is used to capture events, OCREF_CLR events, brake events, and generate interrupts
- Input channels can select I/O ports
- Can be configured with read-only or read-write, and can be unlocked only after a reset
- Supports blanking, configurable blanking source
- Filter window size can be configured
- Filter threshold size can be configured
- Filter sampling frequency can be configured

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13.3 COMP Configuration Process

The complete configuration items are as follows. If the default configuration is used, skip the corresponding configuration items.

1. Configure hysteresis level COMP_CTRL.HYST[1:0].
2. Configure the output polarity COMP_CTRL.POL.
3. Configure input selection, comparator positive COMP_CTRL.INPSEL, negative COMP_CTRL.INMSEL.
4. Configure the subtraction value at the positive input COMP_CTRL.CMPVOS[1:0].
5. Configure output selection COMP_CTRL.OUTTRG[2:0].
6. Configure the blanking source COMP_CTRL.BLKING.
7. Configure the filter sampling window COMP_FILC.SAMPW[4:0].
8. Configure the threshold COMP_FILC.THRESH[4:0] (Threshold should be greater than COMP_FILC.SAMPW[4:0]/2).
9. Configure the filter sampling frequency (for timer applications, sampling frequency should be greater than 5MHz).
10. Enable COMP_FILC.FILEN filter.
11. Enable COMP_CTRL.EN on the comparator.

Note: For the above steps, the filter should be enabled first and then the comparator should be enabled. The comparator should be enabled after the filtering (if enabled) is configured and enabled. In addition, when the comparator control register is locked, it can only be unlocked by reset.

13.4 COMP Working Mode

13.4.1 Independent Comparator

One comparator can be configured independently to complete the comparator functions. The output of the comparator can be output to I/O ports. The comparator supports different remapping ports. And the output of the comparator can be selected and connected to the corresponding port by configuration.

The comparator output supports triggering events, for example, it can be configured as timer 1 brake function.

Note: Refer to the comparator interconnection for specific configuration

13.5 Comparator Interconnection

For interconnection of comparator output ports, please refer to the AFIO remapping chapter on IO multiplexing function in GPIOx_AFL/AFH.

The comparator INP pins have the following configuration:

INPSEL	COMP
0	PB0

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INPSEL	COMP
1	PA5

The comparator INM pins have the following configuration:

INMSEL	COMP
0	PB1
1	PA4

The signals of TRIG output by the comparator have the following interconnections:

TRIG	COMP
000	NC
001	TIM1_BKIN
010	TIM1_IC1
011	TIM1_OCrefclear
100	TIM3_IC1
101	TIM3_OCrefclear
Other	--

13.6 Interrupts

COMP supports interrupt response. There are two types of interrupts.

- The polarity of COMP_CTRL.POL is not reversed and the interrupt is enabled. When INPSEL > INMSEL, the comparator interrupt will be generated when COMP_CTRL.OUT is set to 1 by hardware.
- The polarity of COMP_CTRL.POL is reversed and the interrupt is enabled. When INPSEL < INMSEL, the comparator interrupt will be generated when COMP_CTRL.OUT is set to 1 by hardware.

13.7 COMP Registers

13.7.1 COMP Registers

Table 13-1 Register Overview

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
000h	COMP_INTEN	Reserved																															CMPIEN
	Reset Value																																0
004h	COMP_INTSTS	Reserved																															CMPIS
	Reset Value																																0
008h	Reserved																																
00Ch	COMP_LOCK	Reserved																															CMPLK
	Reset Value																																0

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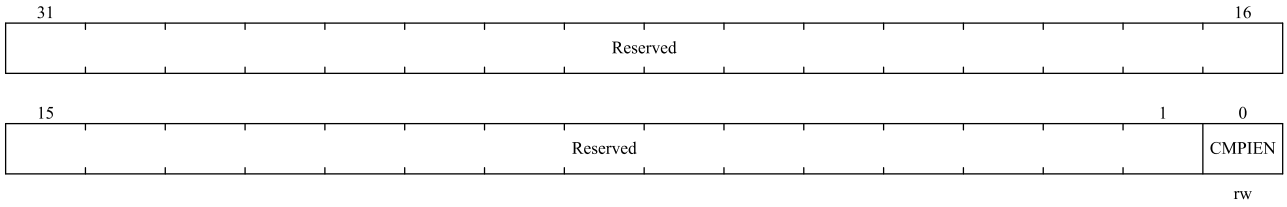
Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
010h	COMP_CTRL	Reserved														OUT	Reserved		BLKING	HYST[1:0]		POL	Reserved	OUTTRG[2:0]			Reserved		CMPVOS[1:0]		INPSEL	INMSEL	EN
	Reset Value															0			0	0	0	0		0	0	0			0	0	0	0	0
014h	COMP_FILC	Reserved																					SAMPW[4:0]						THRESH[4:0]				FILEN
	Reset Value																						0	0	0	0	0	0	0	0	0	0	0
018h	COMP_FILP	Reserved																	CLKPSC[15:0]														
	Reset Value																		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
01Ch ~ 03Ch	Reserved																																

13.7.2 COMP Interrupt Enable Register (COMP_INTEN)

Address offset :0x00

Reset value :0x0000 0000

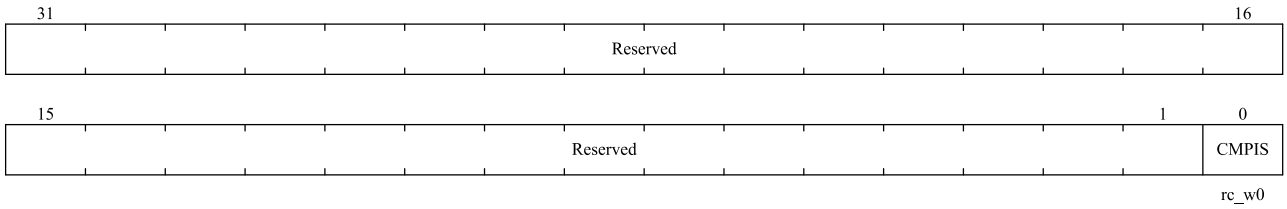


Bit Field	Name	Description
31:1	Reserved	Reserved,the reset value must be maintained.
0	CMPIEN	Comparator interrupt enable register. 0: Disable 1: Enable

13.7.3 COMP Interrupt Status Register (COMP_INTSTS)

Address offset :0x04

Reset value :0x0000 0000



Bit Field	Name	Description
31:1	Reserved	Reserved,the reset value must be maintained.
0	CMPIS	The status of comparator is interrupted

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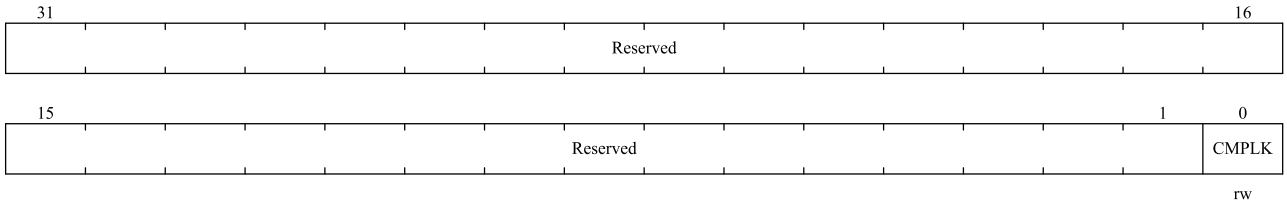
Bit Field	Name	Description
31:1	Reserved	Reserved,the reset value must be maintained.
		Write 0 to clear

13.7.4 COMP Lock Register (COMP_LOCK)

Address offset :0x0C

Reset value :0x0000 0000

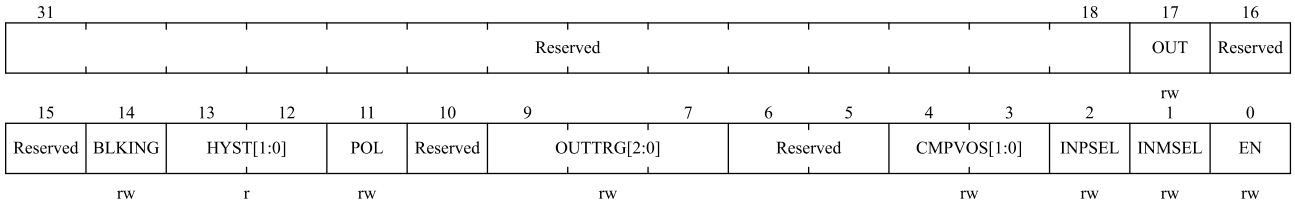


Bit Field	Name	Description
31:1	Reserved	Reserved,the reset value must be maintained.
0	CMPLK	This bit can only be reset then written once by software. If software is set to 1, the COMP_CTRL register will become a read-only register. 0: COMP_CTRL\ COMP_FIL\ COMP_FILP is read-write. 1: COMP_CTRL\ COMP_FIL\ COMP_FILP is read-only.

13.7.5 COMP Control Register (COMP_CTRL)

Address offset :0x10

Reset value :0x0000 0000



Bit Field	Name	Description
31:18	Reserved	Reserved,the reset value must be maintained.
17	OUT	This read-only bit is COMP output state. 0: Output is low 1: Output is high
16:15	Reserved	Reserved,the reset value must be maintained.
14	BLKING	Comparator output is selected by blanking source control 0: No blanking 1: TIM1 OC5 selected as blanking source
13:12	HYST[1:0]	These bits control the hysteresis level. 00: No hysteresis 01: Low hysteresis

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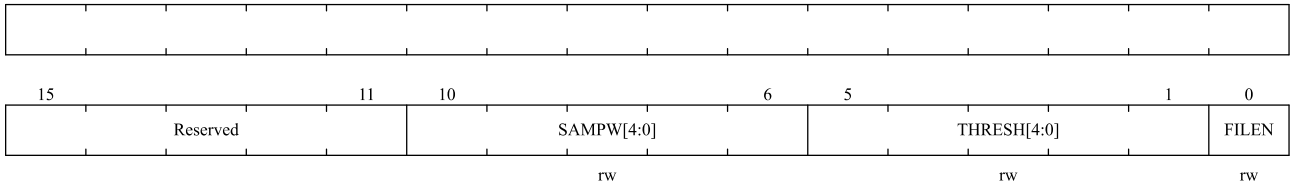
Bit Field	Name	Description
		10: Moderate hysteresis 11: High hysteresis
11	POL	This bit is used to invert the COMP output. 0: Output is not reversed 1: Output is reversed
10	Reserved	Reserved,the reset value must be maintained.
9:7	OUTTRG[2:0]	These bits select which Timer input must be connected with the COMP output. 000: Reserved 001: TIM1_BKIN 010: TIM1_IC1 011: TIM1_OCrefclear 100: TIM3_IC1 101: TIM3_OCrefclear
6:5	Reserved	Reserved,the reset value must be maintained.
4:3	CMPVOS[1:0]	the subtraction value at the positive end. 00: no subtract 01: subtract 100mv 10: subtract 200mv 11: subtract 300mv
2	INPSEL	COMP positive input select 0: PB0 1: PA5
1	INMSEL	COMP negative input select 0: PB1 1: PA4
0	EN	This bit switches COMP ON/OFF. 0: Disable 1: Enable

13.7.6 COMP Filter Control Register (COMP_FILC)

Address offset :0x14

Reset value :0x0000 0000



Bit Field	Name	Description
31:11	Reserved	Reserved,the reset value must be maintained.
10:6	SAMPW[4:0]	Sampling window size of low pass filter, sampling window = SAMPW + 1.

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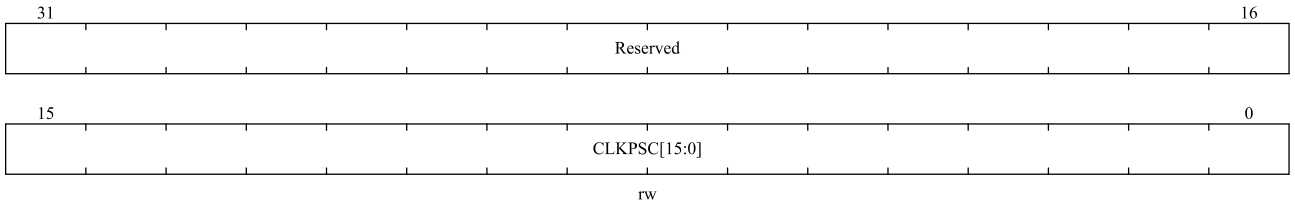
Bit Field	Name	Description
5:1	THRESH[4:0]	Low pass filter threshold, the value must be greater than SAMPW / 2
0	FILEN	Filter enable bit 0: Disable 1: Enable

13.7.7 COMP Filter Clock Register (COMP_FILP)

Address offset :0x18

Reset value :0x0000 0000



Bit Field	Name	Description
31:16	Reserved	Reserved,the reset value must be maintained.
15:0	CLKPSC[15:0]	Low pass filter sampling clock predivision, system clock frequency division = CLKPSC + 1. 0: Every clock 1: Every 2 clocks 2: Every 3 clocks ... 65535: Every 65536 clocks

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14 Inter-integrated Circuit Bus(I^2C)

14.1 Introduction

The I^2C(Inter-Integrated Circuit) bus is a widely used bus structure that consists of only two bidirectional lines: namely data bus SDA and clock bus SCL. All devices compatible with I^2C bus can communicate directly with each other through I^2C bus with these two lines.

I^2C interface connects microcontroller and serial I^2C bus, which can be used for communication between MCU and external I^2C devices. It supports standard speed mode and fast mode with CRC calculation and verification. It also provides multi-master function to control all I^2C bus specific timing, protocol, arbitration.

14.2 Main Features

- Same interface can be used for both master and slave functions
- Parallel-bus to I^2C protocol converter
- Supports 7-bit/10-bit address mode and broadcast addressing
- As I^2C master device, it can generate clock, start and stop signal
- As I^2C slave device, it supports programmable address detection, stop bit detection function
- Supports standard speed mode(up to 100 kHz) , fast mode(up to 400 kHz) and fast plus mode(up to 1MHz)
- Supports interrupt vector: byte transfer successfully interrupt and error event interrupt
- Optional clock stretching function
- Optional PEC (Packet Error Check) generation and verification
- Programmable analog and digital noise filters

14.3 Function Description

The I^2C interface is connected to I^2C bus through data pin (SDA) and clock pin (SCL) to communicate with external devices. It can be connected to standard (up to 100kHz) or fast (up to 400kHz) or fast$^+$ (up to 1MHz) I^2C bus. I^2C module converts data from serial to parallel when receiving, and converts data from parallel to serial when transmitting. It supports interrupt mode, and user can enable or disable interrupt according to their needs.

14.3.1 SDA And SCL Line Control

The I^2C module has two interface lines: serial data line (SDA) and serial clock line (SCL). Devices connecte to the bus and exchange information to each other through these two wires. Both SDA and SCL are bidirectional lines, connected to positive power supply with a pull-up resistor. When the bus is idle, both lines are high level. The output of device which is connected to the bus must have open drain or open collector to provide wired-AND functionality. The data on I^2C bus can reach 100 kbit/s in standard mode and 1000 kbit/s in fast mode. Since devices of different processors may be connected to the I^2C bus, the levels of logic '0' and logic '1' are not fixed and depend on the actual level of VDD.

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If the clock stretching is allowed, the SCL line is pulled low which can avoid the overrun error during reception and the underrun error during transmission.

For example, in the transmission mode, if the transmit data register is empty and the byte transfer finish bit is set (I2C_STS1.TXDATE = 1, I2C_STS1.BSF = 1), the I²C interface keeps the clock line low before transmission to wait for the software to read STS1 and write the data into the data register (both buffer and shift register are empty); In the receive mode, if the data register is not empty and the byte transfer finish bit is set (I2C_STS1.RXDATNE = 1, I2C_STS1.BSF = 1), the I²C interface keeps the clock line low after receiving the data byte, waiting for the software to read STS1, and then read the data register(buffer and shift register are full).

If clock stretching is disable in slave mode, if the receive data register is not empty (I2C_STS1.RXDATNE = 1) in the receive mode, and the data has not been read before receiving the next byte, an overrun error will issue and the last word byte will be discarded. In transmit mode, if the transmit data register is empty (I2C_STS1.TXDATE = 1), and no new data is written into the data register before the next byte must be sent, an underrun error will issue. The same byte will be send repeatedly. In this case, duplicate write conflicts are not controlled.

14.3.2 Software Communication Process

The data transmission of I²C device is divided into master and slave. Master is the device responsible for initializing the transmission of data on the bus and generating clock signal. At this time, any addressed device is a slave. Whether the I²C device is a master or a slave, it can transmit or receive data. Therefore, the I²C interface supports four operation modes:

- Slave transmitter mode
- Slave receiver mode
- Master transmitter mode
- Master receiver mode

After system reset, I²C works in slave mode by default. The I²C interface is configured by software to send a start bit on the bus, and then the interface automatically switches from the slave mode to the master mode. When arbitration is lost or a stop signal is generated, the interface will switched to the slave mode from the master mode.

The functional block diagram of I²C interface is shown in the figure below.

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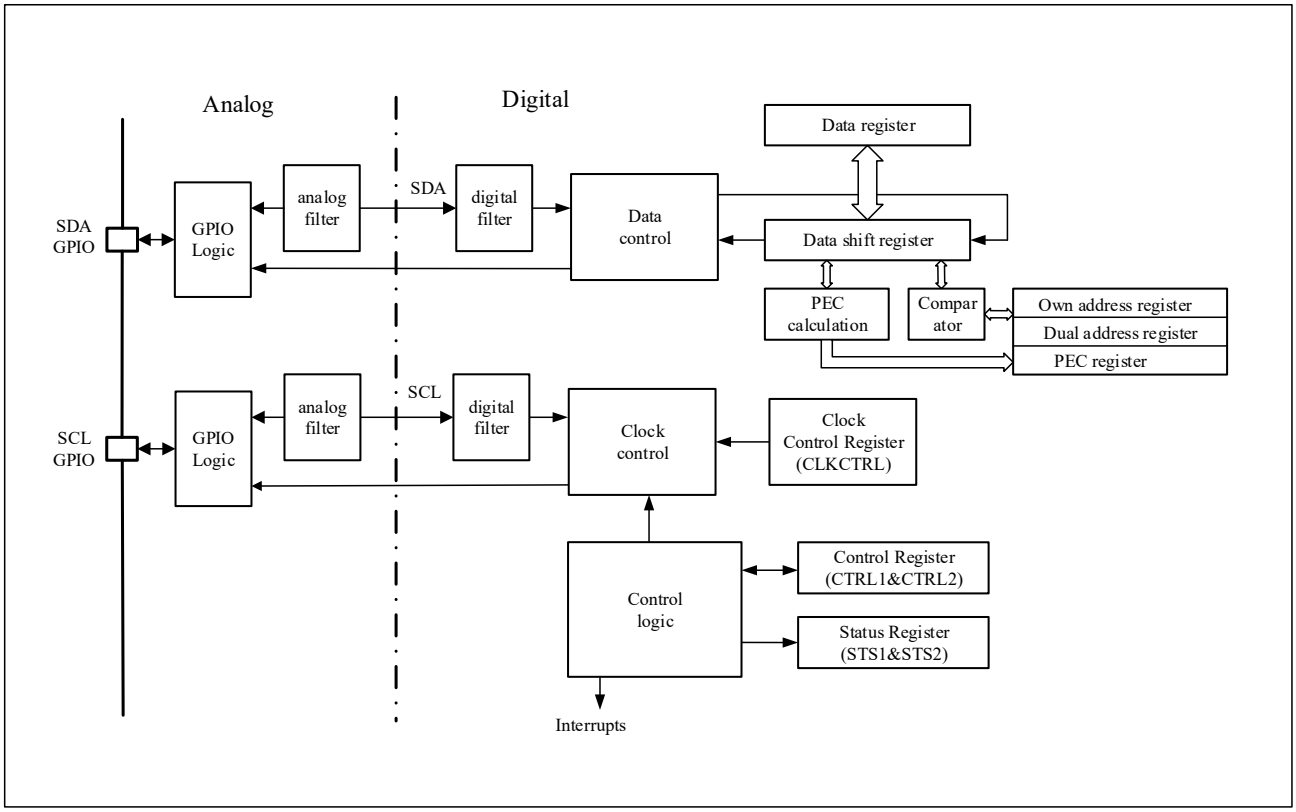
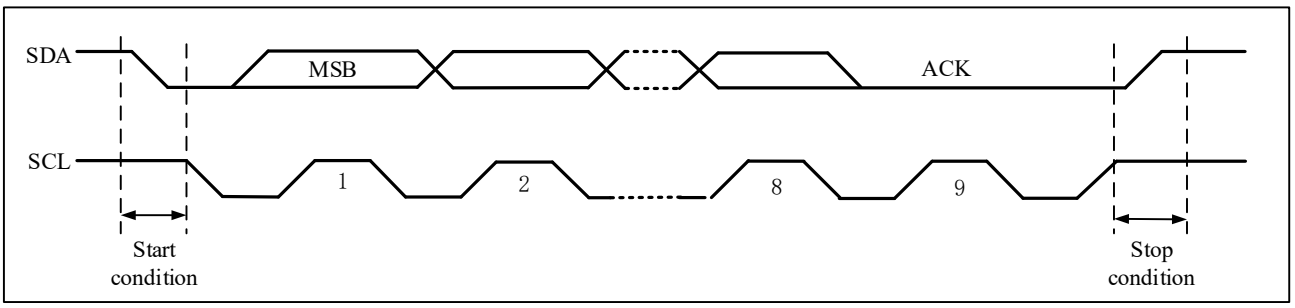
Figure 14-1 I²C Functional Block Diagram



14.3.2.1 Start and stop conditions

All data transfers always start with the start bit and end with the stop bit. The start and stop conditions are generated by software in the master mode. Start bit is a level conversion from high to low on SDA line when SCL is high. Stop bit is a level conversion from low to high on SDA line when SCL is high, as shown in the figure below.

Figure 14-2 I²C Bus Protocol



14.3.2.2 Clock synchronization and arbitration

The I²C module supports multi-master arbitration, which means two masters can start transferring data on an idle bus at the same time. So some mechanisms are needed to decide which master takes control of the bus, which is usually done through clock synchronization and arbitration.

I²C module has two key features:

- SDA and SCL are open-drain circuit structures, and the signal "wire-AND" logic is realized through an external

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pull-up resistor.

- SDA and SCL pins will also detect the level on the pin while outputting the signal to check whether the output is consistent with the previous output.

This provides the hardware basis for "Clock Synchronization" and "Bus Arbitration".

The I²C device on the bus is to output logic 0 by "grounding the line". Based on the characteristics of the I²C bus, if one device transmits logic 0 and the other transmits logic 1, then the line sees only logic 0, so there is no possibility of level conflicts on the line.

The physical connection of the bus allows the master to read data while writing data to the bus. In this way, when two masters are competing for the bus, the one that transmits logic 0 does not know the occurrence of the competition. Only the one that transmits logic 1 will find the conflict (when writing a logic 1, but read 0) and exit the competition.

Clock synchronization

Multiple masters can generate clocks on an idle bus at the same time. The high-to-low switching of the SCL line causes the devices to begin counting their low-level periods, and once the device's clock goes low, it keeps the SCL line in this state until the high-level of the clock is reached. However, if another clock is still in the low period, the low-to-high switch of this clock will not change the state of the SCL line. Therefore, the SCL line is kept low by the device with the longest low-level period. A device with a short low-level period will enter a high-level wait state.

When all related devices have counted their low-level periods, the clock line is released and goes high-level, after which there is no difference in the state of the device clock and SCL lines, and all devices will begin counting their high-level periods, the device that completes the high-level period first will pull the SCL line low again.

In this way, the low-level period of the generated synchronous SCL clock is determined by the device with the longest low-level clock period, and the high-level period is determined by the device with the shortest high-level clock period.

Arbitration

Arbitration, like synchronization, is to resolve bus control conflicts in the case of multiple masters. The arbitration process has nothing to do with the slave. When the two masters both produce a valid start bit when the bus is idle, in this case, it is necessary to decide which master will complete the data transmission. This is the process of arbitration.

Each master controller does not have the priority level of controlling the bus, which is all determined by arbitration. The bus control is determined and carried out bit by bit. They follow the principle of "low level first", that is, whoever transmits the low level first will control the bus. During the arbitration of each bit, when SCL is high, each master checks whether its own SDA level is the same as that sent by itself. In theory, if the content transmitted by two master is exactly the same, they can successfully transmit without errors. If a master sends a high level but detects that the SDA line is low, it considers that it has lost arbitration and shuts down its SDA output driver, while the other master continues to complete its own transmission.

14.3.2.3 I²C data communication flow

Each I²C device is identified by a unique address. According to the device function, they can be either a transmitter or a receiver.

The I²C master is responsible for generating the start bit and the end bit in order to start and end a transmission, and is responsible for generating the SCL clock.

The I²C module supports 7-bit and 10-bit addresses, and the user can configure the address of the I²C slave through

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software. After the I²C slave detects the start bit on the I²C bus, it starts to receive the address from the bus, and compares the received address with its own address. Once the two addresses are matched, the I²C slave will send an acknowledgement (ACK) and respond to subsequent commands on the bus: transmit or receive the requested data. In addition, if the software opens a broadcast call, the I²C slave always transmits a confirmation response to a broadcast address (0x00).

Data and address are transmitted in 8-bit width, with the most significant bit first. The 1 or 2 bytes following the start condition is the address (1 byte in 7-bit mode, 2 bytes in 10-bit mode). The address is only sent in master mode. During the 9th clock period after 8 clocks of a byte transmission, the receiver must send back an acknowledge bit (ACK) to the transmitter, as shown in the Figure 14-2 I2C Bus Protocol.

Software can enable or disable acknowledgement (ACK), and can set the I²C interface address (7-bit, 10-bit address or broadcast call address).

14.3.2.4 I²C slave transmission mode

In slave mode, the transmission reception flag bit (I2C_STS2.TRF) indicates whether it is currently in receiver mode or transmission mode. When sending data to I²C bus in transmission mode, the software should follow the following steps:

1. First, enable I²C peripheral clock and configure the related register in I2C_CTRL2, ensuring the correct I2C timing. After these two steps are completed, I²C runs in slave mode, waiting for receiving start bit and address.
2. I²C slave receives a start bit first, and then receives a matching 7-bit or 10-bit address. I²C hardware will set the I2C_STS1.ADDRF(received address and matched its own address). The software should poll this bit regularly or monitor this bit with a interrupt. After this bit is set, the software reads I2C_STS1 register and then reads I2C_STS2 register to clear the I2C_STS1.ADDRF bit. If the address is in 10-bit format, the I²C master should then generate a START and send an address header to the I²C bus. After detecting START and the following address header, the slave will continue to set I2C_STS1.ADDRF bit. The software continues to read I2C_STS1 register and read I2C_STS2 register to clear the I2C_STS1.ADDRF bit for the second time.
3. I²C enters the data sending state, and now shift register and data register I2C_DAT are all empty, so the hardware will set the I2C_STS1.TXDATE(transmitter data register empty). At this time, the software can write the first byte data to I2C_DAT register, however, because the byte of the I2C_DAT register is immediately moved into the internal shift register, the I2C_STS1.TXDATE bit is not cleared to zero. When the shift register is not empty, I²C starts to send data to I²C bus.
4. During the transmission of the first byte, the software writes the second byte to I2C_DAT. At this time, since neither the I2C_DAT register nor the shift register is empty, the I2C_STS1.TXDATE bit is cleared to 0.
5. After the first byte is transmitted, I2C_STS1.TXDATE is set again. The software writes the third byte to I2C_DAT, and at the same time, the I2C_STS1.TXDATE bit is cleared. After that, as long as there is still data to be sent and I2C_STS1.TXDATE is set to 1, the software can write a byte to I2C_DAT register.
6. During the sending of the second last byte, the software writes the last data to the I2C_DAT register to clear the I2C_STS1.TXDATE flag bit, and then the I2C_STS1.TXDATE status is no longer concerned. The I2C_STS1.TXDATE bit is set after the second last byte is sent until the stop end bit is detected.
7. According to the I²C protocol, the I²C master will not send a ACK to the last byte received. Therefore, after the last byte is sent, the I2C_STS1.ACKFAIL bit (acknowledge fail) of the I²C slave will be set to notify the software

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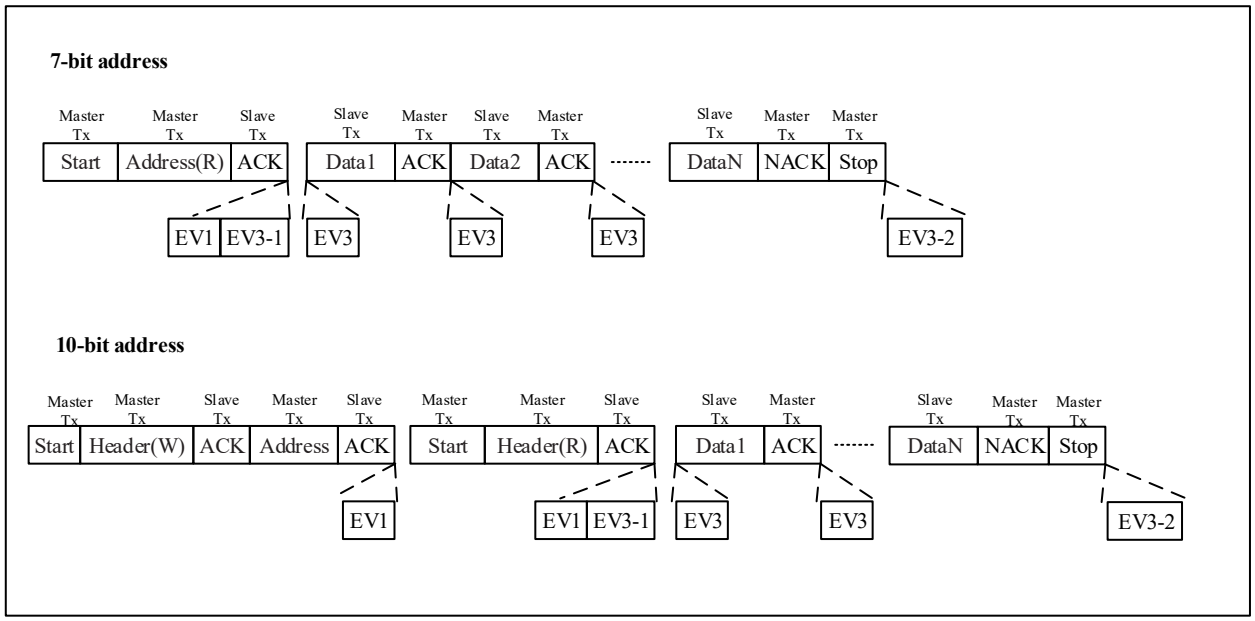
of the end of transmitting. The software writes 0 to the I2C_STS1.ACKFAIL bit to clear this bit.

Figure 14-3 Slave Transmitter Transfer Sequence Diagram



Instructions:

1. EV1: I2C_STS1.ADDRF = 1, read STS1 and then STS2 to clear the event.
2. EV3-1: I2C_STS1.TXDATE=1, write DAT (shift register and data register are both empty).
3. EV3: I2C_STS1.TXDATE=1, write DAT to clear the event (Shift register is not empty, while data register is empty).
4. EV3-2: I2C_STS1.ACKFAIL=1, write "0" to clear the event.

Notes:

(1) EV1 and EV3-1 event prolongs the low SCL time until the end of the corresponding software sequence.

(2) The software sequence of EV3 must be completed before the end of the current byte transfer.

14.3.2.5 I²C slave receiving mode

When receiving data in slave mode, the software should operate as follows:

1. First, enable I²C peripheral clock and configure the related register in I2C_CTRL2 ensuring the correct I²C timing. After these two steps are completed, I²C runs in slave mode, waiting for receiving start bit and address.
2. After receiving the START condition and the matched 7-bit or 10-bit address, I²C hardware will set I2C_STS1.ADDRF bit(the address received and matched with its own address) to 1. This bit should be detected by software polling or interrupt. After it is set, the software clears the I2C_STS1.ADDRF bit by reading I2C_STS1 register first and then I2C_STS2 register. Once the I2C_STS1.ADDRF bit is cleared, the I2C slave starts to receive data from the I²C bus.
3. When the first byte is received, the I2C_STS1.RXDATNE bit (the received data is not empty) is set to 1 by hardware. If the I2C_CTRL2.EVTINTEN and I2C_CTRL2.BUFINTEN bits are set, an interrupt is generated. The software should check this bit by polling or interrupt. Once it is set, the software can read the first byte of

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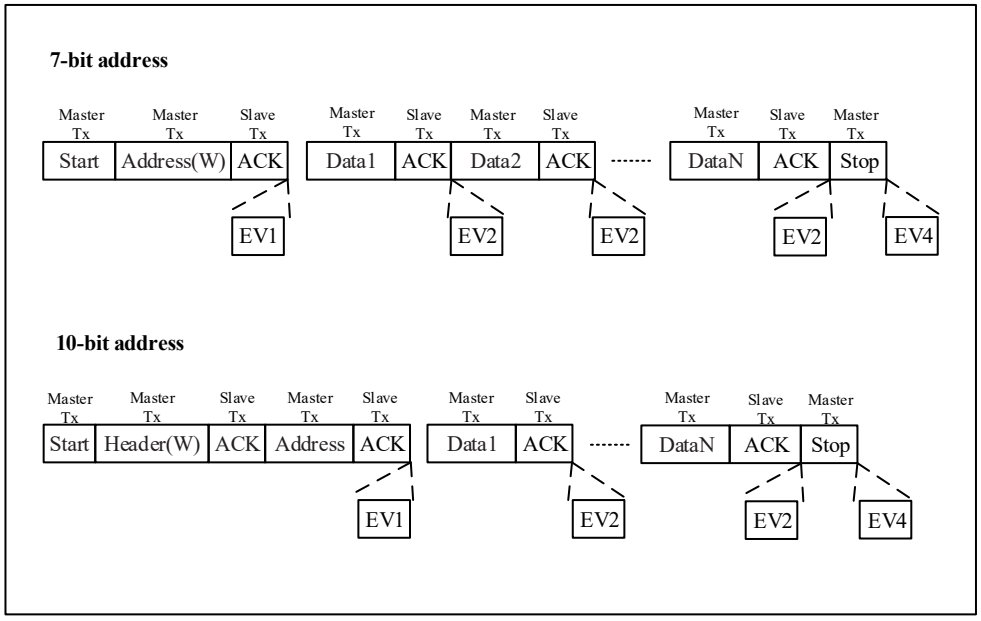
I2C_DAT register, and then the I2C_STS1.RXDATNE bit is cleared to 0. Note that if the I2C_CTRL1.ACKEN bit is set, after receiving a byte, the slave should generate a response pulse.

4. At any time, as long as the I2C_STS1.RXDATNE bit is set to 1, the software can read a byte from the I2C_DAT register. When the last byte is received, I2C_STS1.RXDATNE is set to 1 and the software reads the last byte.

5. When the slave detects the STOP bit on I²C bus, I2C_STS1.STOPF is set to 1, and if the I2C_CTRL2.EVTINTEN bit is set, an interrupt will be generated. The software clears the I2C_STS1.STOPF bit by reading the I2C_STS1 register before writing the I2C_CTRL1 register (refer to EV4 in the following figure).

Figure 14-4 Slave Receiver Transfer Sequence Diagram



Instructions:

1. EV1: I2C_STS1.ADDRF = 1, read STS1 and then STS2 to clear the event.
2. EV2: I2C_STS1.RXDATNE =1, read DAT to clear this event.
3. EV4: I2C_STS1.STOPF=1, read STS1 and then write the CTRL1 register to clear this event.

Notes:

(1) EV1 event prolongs the low SCL time until the end of the corresponding software sequence.

(2) The software sequence of EV2 must be completed before the end of the current byte transmission.

14.3.2.6 I²C master transmission mode

In the master mode, the I²C interface starts data transmission and generates a clock signal. Serial data transmission always starts with a start condition and ends with a stop condition. When the start condition is generated on the bus through the START bit, the device enters the master mode.

When sending data to I²C bus in master mode, the software should operate as follows:

1. First, enable the I²C peripheral clock, and configure the related registers in I2C_CTRL2 to ensure the correct I²C timing. When these two steps are completed, I²C runs in the slave mode by default, waiting for receiving the start bit and address.

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2. When BUSY=0, set I2C_CTRL1.STARTGEN bit to 1, and the I²C interface will generate a start condition and switch to the master mode (I2C_STS2.MSMODE=1).

3. Once the start condition is issued, I²C hardware will set I2C_STS1.STARTBF bit(START bit flag)and then enters the master mode. If the I2C_CTRL2.EVTINTEN bit is set, an interrupt will be generated. Then the software reads the I2C_STS1 register and then writes a 7-bit address bit or a 10-bit address bit with an address header to the I2C_DAT register to clear the I2C_STS1.STARTBF bit. After the I2C_STS1.STARTBF bit is cleared to 0, I²C master starts transmitting addresses or address headers to I²C bus.

   In 10-bit address mode, sending a header sequence will generate the following events:

   1) I2C_STS1.ADDR10F bit is set by hardware, and if I2C_CTRL2.EVTINTEN bit is set, an interrupt is generated. Then the master reads the STS1 register, and then writes the second address byte into the DAT register.

   2) I2C_STS1.ADDRF bit is set by hardware, and if I2C_CTRL2.EVTINTEN bit is set, an interrupt is generated. Then the master reads the STS1 register, followed by the STS2 register.

      Note: in the transmitter mode, the master device first transmits the header byte (11110xx0) and then transmits the lower 8 bits of the slave address. (where xx represents the highest 2 bits of the 10-bit address).

      In the 7-bit address mode, only one address byte needs to be sent out. Once the address byte is sent out:

   3) I2C_STS1.ADDRF bit is set by hardware, and if I2C_CTRL2.EVTINTEN bit is set, an interrupt is generated. Then the master device waits for reading the STS1 register once, followed by reading the STS2 register.

   Note: in the transmitter mode, the master transmits the slave address with lowest bit reset.

   Note: in 7-bit address mode, don't set the slave address to 0xF0 to prevent the I2C_STS1.ADDR10F bit from being set by hardware.

4. After the 7-bit or 10-bit address bit is transmitted, the I²C hardware sets the I2C_STS1.ADDRF bit (address has been sent) to 1. If the I2C_CTRL2.EVTINTEN bit is set, an interrupt is generated. The software can clear I2C_STS1.ADDRF bit by reading the I2C_STS1 register and then the I2C_STS2 register.

5. I²C enters the data transmission state. Because the shift register and the data register (I2C_DAT) are empty, the hardware sets the I2C_STS1.TXDATE bit (transmission data empty) to 1, and then the software writes the first byte of data to the I2C_DAT register. However, because the byte written into the I2C_DAT register is immediately moved into the internal shift register, the I2C_STS1.TXDATE bit will not be cleared at this time. Once the shift register is not empty, I2C starts transmitting data to the bus.

6. During the transmission of the first byte, the software writes the second byte to I2C_DAT, and I2C_STS1.TXDATE is cleared at this time. At any time, as long as there is data waiting to be transmitted and the I2C_STS1.TXDATE bit is set to 1, the software can write a byte to the I2C_DAT register.

7. In the process of transmitting second last byte, the software writes the last byte to I2C_DAT to clear the I2C_STS1.TXDATE flag. After that, there is no need to care about the status of the I2C_STS1.TXDATE bit. The I2C_STS1.TXDATE bit will be set after the second last byte is transmitted, and will be cleared when the stop bit (STOP) is transmitted.

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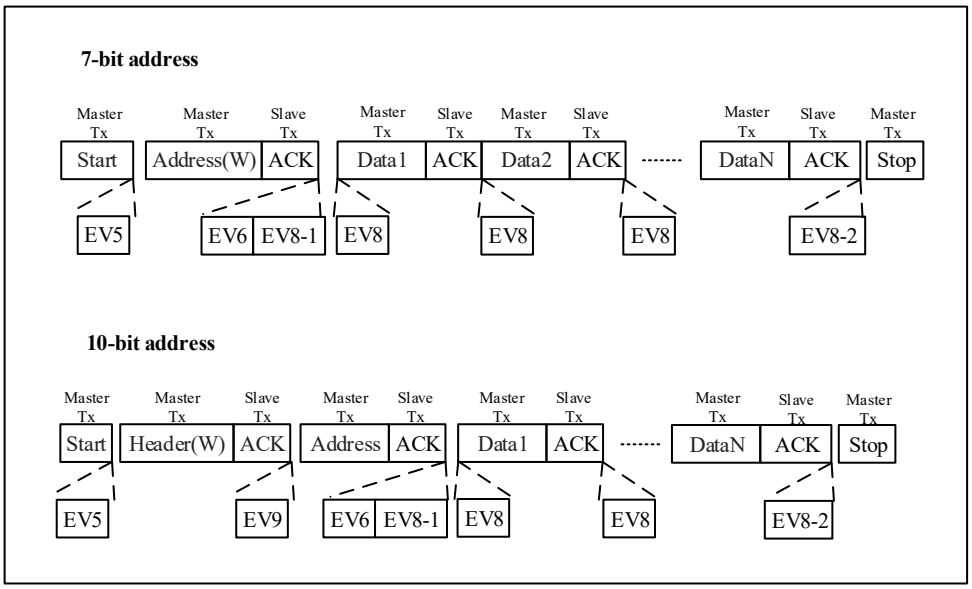
8. After the last byte is sent, because the shift register and the I2C_DAT register are empty at this time, the I2C master sets the I2C_STS1.BSF bit (byte transmission end), and the I²C interface will keep SCL low before clearing the I2C_STS1.BSF bit. After reading I2C_STS1, writing to the I2C_DAT register will clear the I2C_STS1.BSF bit. The software sets the I2C_CTRL1.STOPGEN bit at this time to generate a stop condition, and then the I²C interface will automatically return to the slave mode (I2C_STS2.MSMODE bit is cleared).

Figure 14-5 Master Transmitter Transfer Sequence Diagram



Instructions:

1. EV5: I2C_STS1.STARTBF = 1, read STS1 and write the address to the DAT register to clear the event.
2. EV6: I2C_STS1.ADDRF = 1, read STS1 and then STS2 to clear the event.
3. EV8_1: I2C_STS1.TXDATE = 1, write DAT register (Shift register and data register are both empty).
4. EV8: I2C_STS1.TXDATE = 1, write to DAT register will clear the event (Shift register is not empty, while data register is empty).
5. EV8_2: I2C_STS1.TXDATE = 1, I2C_STS1.BSF = 1, request to set STOP bit. These two events are cleared by the hardware when a stop condition is generated.
6. EV9: I2C_STS1.ADDR10F = 1, read STS1 and then write to DAT register to clear the event.

Notes:

(1) EV5, EV6, EV9, EV8_1 and EV8_2 event prolonged the low SCL time until the end of the corresponding software sequence.

(2) The software sequence of EV8 must be completed before the end of the current byte transfer.

(3) When I2C_STS1.TXDATE or I2C_STS1.BSF bit is set, stop condition should be arranged when EV8_2 occurs.

14.3.2.7 I²C master receiving mode

The I²C interface supports BYTENUM byte control mode. In the master receiving mode, after configuring the number of bytes received, the hardware automatically ends the communication, without software intervention to

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configure NACK and send START/STOP conditions. Of course, normal master receive mode can be used.

In master mode, software receiving data from I²C bus should follow the following steps:

1. First, enable the I²C peripheral clock and configure the related registers in I2C_CTRL2, in order to ensure that the correct I²C timing is output. After enabling and configuring, I²C runs in slave mode by default, waiting to receive the START bit and address.

   Note: to enable master receive byte control, after enabling the I²C peripheral clock in this step, user need to configure the number of bytes to received through I2C_BYTENUM.BYTENUM and select the master to send START or STOP conditions after the receive is finish through I2C_BYTENUM.RXFSEL.

2. When BUSY=0, set the I2C_CTRL.STARTGEN bit, and the I²C interface will generate a start condition and switch to the master mode (I2C_STS2.MSMODE bit is set to 1).

3. Once the start condition is issued, the I²C hardware sets I2C_STS1.STARTBF(START bit flag) and enters the master mode. If the I2C_CTRL2.EVTINTEN bit is set to 1, an interrupt will be generated. Then the software reads the I2C_STS1 register and then writes a 7-bits address or a 10-bits address with an address header to the I2C_DAT register, in order to clear the I2C_STS1.STARTBF bit. After the I2C_STS1.STARTBF bit is cleared to 0, I²C master begins to transmit the address or address header to the I²C bus.
   In 10-bits address mode, sending a header sequence will generate the following events:
   1) When the I2C_STS1.ADDR10F bit is set to 1 by hardware, if the I2C_CTRL2.EVTINTEN bit is set to 1, an interrupt will be generated. Then the master device reads the STS1 register, and then writes the second byte of address into the DAT register.
   2) When the I2C_STS1.ADDRF bit is set to 1 by hardware, if the I2C_CTRL2.EVTINTEN bit is set to 1, an interrupt will be generated. Then the master device reads the STS1 register and the STS2 register in sequence.

      Note: in the receiving mode, the master device sends the header byte (11110xx0) firstly, then sends the lower 8 bits of the slave address, and then resends a start condition followed by the header byte (11110xx1) (where xx represents the highest 2 digits of the 10-bits address).

   In the 7-bits address mode, only one address byte needs to be sent, once the address byte is sent:

   3) When the I2C_STS1.ADDRF bit is set to 1 by hardware, if the I2C_CTRL2.EVTINTEN bit is set to 1, an interrupt will be generated. Then the master device waits to read the STS1 register once, and then reads the STS2 register.

   Note: in the receiving mode, the master device sets the lowest bit as '1' when sending the slave address.

   Note: in 7-bit address mode, don't set the slave address to 0xF0 to prevent the I2C_STS1.ADDR10F bit from being set by hardware.

4. After the 7-bits or 10-bits address is sent, the I²C hardware sets the I2C_STS1.ADDRF bit (address has been sent) to 1. If the I2C_CTRL2.EVTINTEN bit is set to 1, an interrupt will be generated. The software clears the I2C_STS1.ADDRF bit by reading the I2C_STS1 register and the I2C_STS2 register in sequence. If in the 10-bit address mode, software should set the I2C_CTRL1.STARTGEN bit again to regenerate a START condition. After the START condition is generated, the I2C_STS1.STARTBF bit will be set. The software should clear the I2C_STS1.STARTBF bit by reading I2C_STS1 firstly and then writing the address header to I2C_DAT, and then the address header is sent to the I²C bus, and I2C_STS1.ADDRF is set to 1 again. The software should

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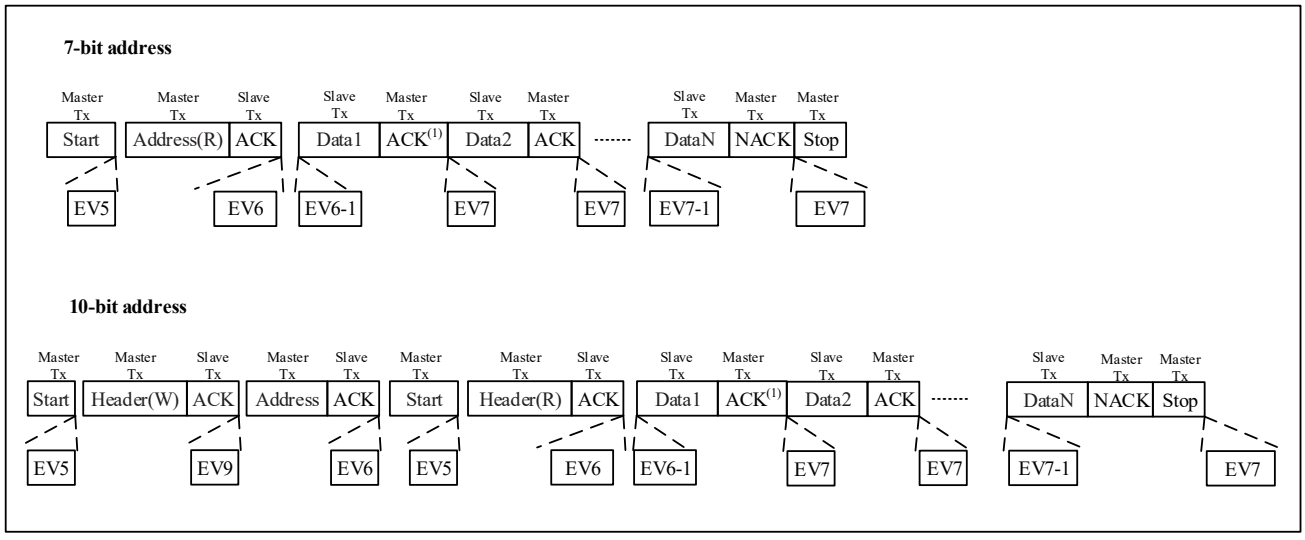
clear the I2C_STS1.ADDRF bit again by reading I2C_STS1 and I2C_STS2 in sequence.

5. After sending the address and clearing the I2C_STS1.ADDRF bit, the I²C interface enters the master receiving mode. In this mode, the I²C interface receives data bytes from the SDA line and sends them to the DAT register through the internal shift register. Once the first byte is received, the hardware will set the I2C_STS1.RXDATNE bit (not empty flag bit of received data) to 1, and if the I2C_CTRL1.ACKEN bit is set to 1, an acknowledge pulse will be sent. At this time, the software can read the first byte from the I2C_DAT register, and then the I2C_STS1.RXDATNE bit is cleared to 0. After that, as long as I2C_STS1.RXDATNE is set to 1, the software can read a byte from the I2C_DAT register.
6. The master device sends a NACK after receiving the last byte from the slave device. After receiving the NACK, the slave device releases the control of SCL and SDA lines; the master device can send a stop/restart condition. In order to generate a NACK pulse after receiving the last byte, the software should clear the I2C_CTRL1.ACKEN bit immediately after receiving the second last byte (N-1). In order to generate a stop/restart condition, the software must set the I2C_CTRL1.STOPGEN bit or I2C_CTRL1.STARTGEN to 1 after reading the second last data byte. This process needs to be completed before the last byte is received to ensure that the NACK is sent for the last byte.
   Note: if the master receive byte control is enabled earlier, steps 6 and 7 can be ignored, the software only needs to read the bytes according to the receive flag, and the hardware will automatically send NACK and START/STOP conditions after the the receive is finish.
7. After the last byte is received, the I2C_STS1.RXDATNE bit is set to 1, and the software can read the last byte. Since I2C_CTRL1.ACKEN has been cleared to 0 in the previous step, I²C no longer sends ACK for the last byte, and generates a STOP bit after the last byte is sent.

Note: in normal master receive mode, the above steps require the number of bytes N>1. If N=1, step 6 should be executed after step 4, and it needs to be completed before the reception of byte is completed.

Figure 14-6 Master Receiver Transfer Sequence Diagram



Instructions:

1. EV5: I2C_STS1.STARTBF=1, read STS1 and then write the address into the DAT register to clear this event.
2. EV6: I2C_STS1.ADDRF=1, read STS1 and STS2 in sequence to clear this event. In the 10-bits master receiving mode, the I2C_CTRL1.STARTGEN should be set to 1 after this event.
3. EV6_1: There is no corresponding event flag. Just after EV6 (that is after clearing I2C_STS1.ADDRF), the

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generation bits for acknowledge and stop condition should be cleared.

4. EV7: I2C_STS1.RXDATNE=1, read the DAT register to clear this event.
5. EV7_1: I2C_STS1.RXDATNE =1, read the DAT register to clear this event. Set I2C_CTRL1.ACKEN=0 and I2C_CTRL1.STOPGEN=1.
6. EV9: I2C_STS1.ADDR10F=1, read STS1 and then write to the DAT register to clear this event.

Notes:

(1) If a single byte is received, it is NA.

(2) EV5, EV6, and EV9 events extend the low SCL time until the corresponding software sequence ends.

(3) The EV7 software sequence shall be completed before the end of the current byte transmission.

(4) The software sequence of EV6_1 or EV7_1 shall be completed before the ACK pulse of the current transmission byte.

14.3.3 Error Conditions Description

I²C errors mainly include bus error, acknowledge fail, arbitration loss, overrun\underrun error. These errors may cause communication failure.

14.3.3.1 Acknowledge failure(ACKFAIL)

When the interface detects that acknowledgement bit does not match the expectation, it will generate an acknowledge fail error, and I2C_STS1.ACKFAIL bit is set. An interrupt will be generated, if I2C_CTRL2.ERRINTEN bit is set to 1.

When transmitter receives a NACK, the communication must be reset: if in slave mode, hardware will release the bus; if in master mode, it must generate a stop condition from software.

14.3.3.2 Bus error(BUSERR)

when address or data is transmissing, if I²C interface receive external stop or start condition, a bus error is generated, and I2C_STS1.BUSERR bit is set. An interrupt will be generated, if I2C_CTRL2.ERRINTEN bit is set to 1.

In master mode, the hardware does not release bus, as the same time it done not affect the current transmission status. It is up to software to abort or not the current transmission.

In slave mode, data is discarded in transmission and the bus is released by hardware. There are two situations: if an error start condition is detected, the slave device considers a restart condition and waits for an address or a stop condition. If an error stop condition is detected, the slave device operates as a normal stop condition and the hardware releases the bus.

14.3.3.3 Arbitration lost(ARLOST)

If arbitration lost is detected, an arbitration lost occurs with I2C_STS1.ARLOST bit set, and hardware release the bus. An interrupt will be generated, if I2C_CTRL2.ERRINTEN bit is set to 1.

I²C interface will go to slave mode automatically(I2C_STS2.MSMODE bit is cleared). When the I²C interface lost the arbitration, it can not acknowledge to its slave address in the same transfer, but it can acknowledge it after a repeat start condition from winning master.

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14.3.3.4 Overrun/Underrun error(OVERRUN)

In slave mode, Overrun/Underrun error can easily occur if clock stretching is disable.

When I²C interface has received a byte(I2C_STS1.RXDATNE=1), and I2C_DAT register still have previous byte has not been read, it will occurs an overrun error. In this situation, the last received data is discarded; Software should clear I2C_STS1.RXDATNE bit, and the transmitter should retransmit last byte.

In slave transmission mode, if clock stretching is disabled, an underrun error occurs when the current byte has been sent but the data register remains empty (I2C_STS1.TXDATE=1). In this situation, the previous byte in the I2C_DAT register is transmitted repeatedly; User should make sure that in the event of an underrun error, the receiver discard repeatedly byte. The transmitter should update the I2C_DAT register at the specified time according to the I²C bus standard.

During transmitting the first byte, I2C_DAT register must be written after I2C_STS1.ADDRF bit is cleared and the before the first SCL rising edge. If no possible, receiver must discard the first byte.

14.3.4 Packet Error Check

Setting the I2C_CTRL1.PECEN bit to 1 enables the PEC function. PEC uses CRC-8 algorithm to calculate all information bytes including address and read/write bits. It can improve the reliability of communication. The CRC-8 polynomial uses by the PEC calculator is $C(x) = x^8 + x^2 + x + 1$.

In transmission mode, software sets I2C_CTRL1.PEC bit after the last I2C_STS1.TXDATE event, and then PEC will be transmitted after the last byte. While in receiving mode, software sets I2C_CTRL1.PEC bit after the last I2C_STS1.RXDATNE event, and then receives the PEC byte and compares the received PEC byte to the internally calculated PEC value. If it is not equal to the internally calculated PEC value, the receiver needs to send a NACK. If it is master receiving mode, NACK will be sent after PEC regardless of the calculated result. Note that I2C_CTRL1.PEC bit must be set before receiving the ACK pulse of the current byte.

When arbitration is lost, PEC calculation is invalid.

14.3.5 Noise Filter

The I²C interface standard requires the ability to filter spikes of 50ns on SCL/SDA, hence analog filter and digital filter are added in design. By default, analog filter are enable and can be disable by setting I2C_TMRISE.SCLAFENN/SDAAFENN. The spike filtering width of analog filter can be configured by setting I2C_TMRSE.SCLAFE/SDAAFW with the width of 5ns, 15ns, 25ns, 35ns. Digital filter can be enabled by setting I2C_TMRISE.SCLDFW/SDADFW to a non-zero values. The max width of digital/analog filter is (SCLDEW[3:0] or SDADFW[3:0])*T_{PCLK}. Enabling the digital filter will increase the hold time of SDA by an amount equal to (SDADFW[3:0]+1)*T_{PCLK}.

14.4 Interrupt Request

All I²C interrupt requests are listed in the following table.

Table 14-1 I²C Interrupt Request

Interrupt Function	Interrupt Event	Event Flag	Set Control Bit
I²C event interrupt	Start bit sent (master)	STARTBF	EVTINTEN
	Address sent (master) or	ADDRF	

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Interrupt Function	Interrupt Event	Event Flag	Set Control Bit
	address matched (slave)		
	10-bit header sent (master)	ADDR10F	
	Received stop (slave)	STOPF	
	Data byte transfer finish	BSF	
	Receive buffer is not empty.	RXDATNE	EVTINTEN and BUFINTEN
	Transmit buffer is empty.	TXDATE	
I^2C error interrupt	Bus error	BUSERR	ERRINTEN
	Lost arbitration (master)	ARLOST	
	Acknowledge fail	ACKFAIL	
	Overrun/underrun	OVERRUN	
	PEC error	PECERR	

Notes:

(1) STARTBF, ADDRF, ADDR10F, STOPF, BSF, RXDATNE and TXDATE are merged into a interrupt channel through logical OR.

(2) BUSERR, ARLOST, ACKFAIL, OVERRUN and PECERR are merged into a interrupt channel through logical OR.

14.5 I^2C Registers

These peripheral registers can be operated by half word (16 bits) or word (32 bits)

14.5.1 I^2C Register Overview

Table 14-2 I^2C Register Overview

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
000h	I2C_CTRL1	Reserved																SWRESET	Reserved		PEC	ACKPOS	ACKEN	STOPGEN	STARTGEN	NOEXTEND	GCEN	PECEN	Reserved				EN
	Reset Value																	0			0	0	0	0	0	0	0	0					0
004h	I2C_CTRL2	Reserved																					BUFINTEN	EVTINTEN	ERRINTEN	Reserved		CLKFREQ[5:0]					
	Reset Value																						0	0	0			0	0	0	0	0	0
008h	I2C_OADDR1	Reserved																ADDRMODE	Reserved	Reserved				ADDR[9:8]		ADDR[7:1]							ADDR0
	Reset Value																	0						0	0	0	0	0	0	0	0	0	0
00Ch	I2C_OADDR2	Reserved																								ADDR2[7:1]							DUALEN
	Reset Value																									0	0	0	0	0	0	0	0
010h	I2C_DAT	Reserved																								DATA[7:0]							
	Reset Value																									0	0	0	0	0	0	0	0
014h	I2C_STS1	Reserved																			PECERR	OVERRUN	ACKFAIL	ARLOST	BUSERR	TXDATE	RXDATNE	Reserved	STOPF	ADDR10F	BSF	ADDRF	STARTBF
	Reset Value																				0	0	0	0	0	0	0		0	0	0	0	0

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Offset	Register		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
018h	I2C_STS2	Reserved	PECVAL[7:0]								DUALFLAG	Reserved		GCALLADDR	Reserved	TRF	BUSY	MSMODE
	Reset Value		0	0	0	0	0	0	0	0	0			0		0	0	0
01Ch	I2C_CLKCTRL	Reserved	FSMODE	DUTY	Reserved		CLKCTRL[11:0]											
	Reset Value		0	0			0	0	0	0	0	0	0	0	0	0	0	0
020h	I2C_TMRISE	Reserved											TMRISE[5:0]					
	Reset Value												0	0	0	0	1	0
024h	I2C_GFLTRCTRL	Reserved			SCLAFENN	SCLAFW[1:0]		SDAAFENN	SDAAFW[1:0]		SCLDFW[3:0]				SDADFW[3:0]			
	Reset Value				0	0	0	0	0	0	0	0	0	0	0	0	0	0
028h	I2C_BYTENUM	Reserved	BYTENUMEN	RXFSEL	BYTENUM[13:0]													
	Reset Value		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

14.5.2 I²C Control Register 1 (I2C_CTRL1)

Address offset: 0x00

Reset value: 0x0000

15	14	13	12	11	10	9	8	7	6	5	4			1	0
SW RESET	Reserved		PEC	ACK POS	ACKEN	STOP GEN	START GEN	NO EXTEND	GCEN	PECEN	Reserved				EN
rw			rw	rw	rw	rw	rw	rw	rw	rw					rw

Bit Field	Name	Description
15	SWRESET	Software reset Make sure the I²C bus is idle before resetting this bit. 0:I²C not under reset state; 1:I²C under reset state. *Note: this bit can be used when the I2C_STS2.BUSY bit is set to 1 and no stop condition is detected on the bus.*
14:13	Reserved	Reserved, the reset value must be maintained
12	PEC	Packet error checking It can be set or cleared by software. It will be cleared by hardware when PEC has been transferred, or detect start or stop condition, or when I2C_CTRL1.EN=0. 0: No PEC transfer 1: PEC transfer. *Note: when arbitration is lost, the calculation of PEC is invalid.*
11	ACKPOS	Acknowledge/PEC Position (for data reception) It can be set or cleared by software. Or when I2C_CTRL1.EN=0, it will be cleared by hardware. 0: I2C_CTRL1.ACKEN bit determines whether to send an ACK to the byte currently being received; I2C_CTRL1.PEC bit indicates that the byte in the current shift register is PEC.

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Bit Field	Name	Description
		1: I2C_CTRL1.ACKEN bit determines whether to send an ACK to the next received byte; I2C_CTRL1.PEC bit indicates that the next byte received in the shift register is PEC. *Note: ACKPOS bit can only be used in 2-byte receiving configuration and must be configured before receiving data.* *To NACK second byte, the I2C_CTRL1.ACKEN bit must be cleared after the I2C_STS1.ADDRF bit is cleared.* *To detect the PEC of the second byte, the I2C_CTRL1.PEC bit must be set after the ACKPOS bit is configured and during the ADDR extend event.*
10	ACKEN	Acknowledge enable It can be set or cleared by software. Or when I2C_CTRL1.EN equals to 0, it will be cleared by hardware. 0: No acknowledge send; 1: Send an acknowledge after receiving a byte(matched address or data)
9	STOPGEN	Stop generation It can be set or cleared by software. Or it will be cleared by hardware when a stop condition is detected. In the master mode: 0: No stop condition generates; 1: Generate a stop condition. In the slave mode: 0: No stop condition generates; 1: Release SCL and SDA lines after the current byte. *Note: when the STOPGEN, STARTGEN or PEC bit is set, the software should not take any write operation to I2C_CTRL1 until this bit is cleared by hardware. Otherwise, the STOPGEN, STARTGEN or PEC bits may be set twice.*
8	STARTGEN	Start generation It can be set or cleared by software. Or it will be cleared by hardware when the start condition is transferred or I2C_CTRL1.EN=0. 0: No start condition generates; 1: Generate a start conditions.
7	NOEXTEND	Clock extending disable (Slave mode) This bit determines whether to pull SCL low when the data is not ready(I2C_STS1.ADDRF or I2C_STS1.BSF flag is set) in slave mode, and is cleared by software reset 0: Enable Clock extending. 1: Disable Clock extending.
6	GCEN	General call enable 0: Disable General call. not acknowledge(NACK) the address 00h; 1: Enable General call. acknowledge(ACK) the address 00h.
5	PECEN	PEC enable 0: Disable PEC module; 1: Enable PEC module.
4:1	Reserved	Reserved, the reset value must be maintained.

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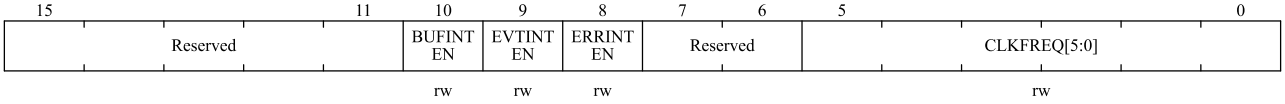
Bit Field	Name	Description
0	EN	I2C Peripheral enable 0: Disable I²C module; 1: Enable I²C module *Note: if this bit is cleared when communication is in progress, the I²C module is disabled and returns to the idle state after the current communication ends, and all bits will be cleared.* *In master mode, this bit must never be cleared until the communication has ended.*

14.5.3 I²C Control Register 2 (I2C_CTRL2)

Address offset: 0x04

Reset value: 0x0000



Bit Field	Name	Description
15:11	Reserved	Reserved, the reset value must be maintained.
10	BUFINTEN	Buffer interrupt enable 0: When I2C_STS1.TXDATE=1 or I2C_STS1.RXDATNE=1, any interrupt is not generated. 1: If I2C_CTRL2.EVTINTEN= 1,when I2C_STS1.TXDATE=1 or I2C_STS1.RXDATNE= 1, interrupt will be generated.
9	EVTINTEN	Event interrupt enable 0: Disable event interrupt; 1: Enable event interrupt This interrupt is generated when: I2C_STS1.STARTBF = 1 (Master) I2C_STS1.ADDR F = 1 (Master/Slave) I2C_STS1.ADD10F = 1 (Master) I2C_STS1.STOPF = 1 (Slave) I2C_STS1.BSF = 1 with no I2C_STS1.TXDATE or I2C_STS1.RXDATNE event I2C_STS1.TXDATE = 1 when I2C_CTRL2.BUFINTEN = 1 I2C_STS1.RXDATNE = 1 when I2C_CTRL2.BUFINTEN = 1
8	ERRINTEN	Error interrupt enable 0: Disable error interrupt; 1: Enable error interrupt. This interrupt is generated when: I2C_STS1.BUSERR = 1; I2C_STS1.ARLOST = 1; I2C_STS1.ACKFAIL = 1; I2C_STS1.OVERRUN = 1; I2C_STS1.PECERR = 1
7:6	Reserved	Reserved, the reset value must be maintained.
5:0	CLKFREQ[5:0]	I²C Peripheral clock frequency

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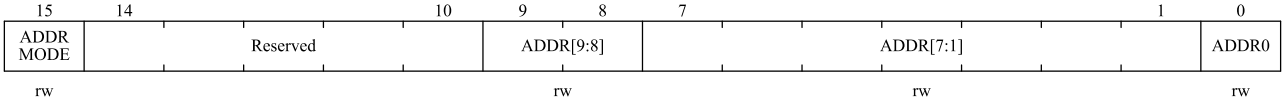
Bit Field	Name	Description
		CLKFREQ[5:0] should be the APB clock frequency to generate the correct timming. 000000: Disable 000001: Disable 000010: 2MHz 000011: 3MHz ... 110000: 48MHz 110001~111111: Disable.

14.5.4 I²C Own Address Register 1 (I2C_OADDR1)

Address offset: 0x08

Reset value: 0x0000

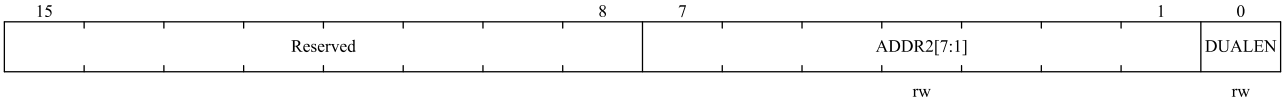


Bit Field	Name	Description
15	ADDRMODE	Addressing mode (slave mode) 0: 7-bit slave address 1: 10-bit slave address
14	Reserved	Must always be kept as' 1' by the software.
13:10	Reserved	Reserved, the reset value must be maintained.
9:8	ADDR[9:8]	Interface address 9~8 bits of the address. *Note: don't care these bits in 7-bit address mode*
7:1	ADDR[7:1]	Interface address 7~1 bits of the address.
0	ADDR0	Interface address 0 bit of the address. *Note: don't care these bits in 7-bit address mode*

14.5.5 I²C Own Address Register 2 (I2C_OADDR2)

Address offset: 0x0C

Reset value: 0x0000



Bit Field	Name	Description
15:8	Reserved	Reserved, the reset value must be maintained.
7:1	ADDR2[7:1]	Interface address

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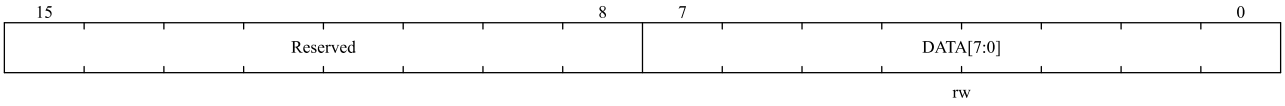
		7~1 bits of address in dual address mode.
0	DUALEN	Dual addressing mode enable 0: Disable dual address mode, only OADDR1 is recognized; 1: Enable dual address mode, both OADDR1 and OADDR2 are recognized. *Note: valid only for 7-bit address mode*

14.5.6 I²C Data Register (I2C_DAT)

Address offset: 0x10

Reset value: 0x0000

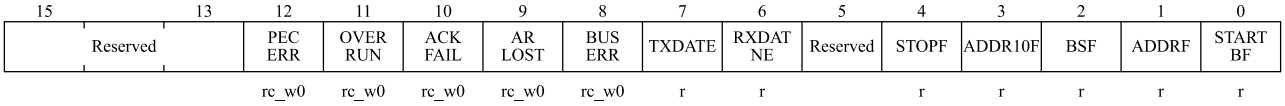


Bit Field	Name	Description
15:8	Reserved	Reserved, the reset value must be maintained.
7:0	DATA[7:0]	8-bit data register Send or receive data buffer. *Note: in the slave mode, the address will not be copied into the data register.* *Note: if* I2C_STS1.*TXDATE =0, data can still be written into the data register.* *Note: if the ARLOST event occurs when processing the ACK pulse, the received byte will not be copied into the data register, so it cannot be read.*

14.5.7 I²C Status Register 1 (I2C_STS1)

Address offset: 0x14

Reset value: 0x0000



Bit Field	Name	Description
15:13	Reserved	Reserved, the reset value must be maintained.
12	PECERR	PEC Error in reception Writing '0' to this bit by software can clear it, or it is cleared by hardware when I2C_CTRL1.EN=0. 0: No PEC error: receiver will returns ACK (if the I2C_CTRL1.ACKEN bit is enabled) 1: PEC error: receiver will returns NACK (It doesn't matter if I2C_CTRL1.ACKEN is enabled or not)
11	OVERRUN	Overrun/Underrun Writing '0' to this bit by software can clear it, or it is cleared by hardware when I2C_CTRL1.EN=0. 0: No Overrun/Underrun 1: Overrun/Underrun

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Bit Field	Name	Description
		Set by hardware in slave mode when I2C_CTRL1.NOEXTEND=1, and when receiving a new byte in receiving mode, if the data within DAT register has not been read yet, over-run occurs, and the new received byte will be lost. When transmitting a new byte in transmit mode, but there is not new data that has not been written in DAT register, under-run occurs which leads that the same byte will be send twice.
10	ACKFAIL	Acknowledge failure Writing '0' to this bit by software can clear it, or it is cleared by hardware when I2C_CTRL1.EN=0. 0: No acknowledge failed; 1: Acknowledge failed.
9	ARLOST	Arbitration lost (master mode) Writing '0' to this bit by software can clear it, or it is cleared by hardware when I2C_CTRL1.EN=0. 0: No arbitration lost; 1: Arbitration lost. When the interface loses control of the bus, the hardware will set this bit to '1', and the I2C interface will automatically switch back to slave mode (I2C_STS2.MSMODE=0).
8	BUSERR	Bus error Writing '0' to this bit by software can clear it, or it is cleared by hardware when I2C_CTRL1.EN=0. 0: No start or stop condition error 1: Start or stop condition error
7	TXDATE	Data register empty (transmitters) Writing data to DAT register by software can clear this bit; or after a start or stop condition occurs, or automatically cleared by hardware when I2C_CTRL1.EN=0. 0: Data register is not empty; 1: Data register is empty. When sending data, this bit is set to' 1' when the data register is empty, and it is not set at the address sending stage. If a NACK is received, or the next byte to be sent is PEC(I2C_CTRL1.PEC=1), this bit will not be set. *Note: after the first data to be sent is written, or data is written when BSF is set, the TXDATE bit cannot be cleared, because the data register is still empty.*
6	RXDATNE	Data register not empty(receivers) This bit is cleared by software reading and writing to the data register, or cleared by hardware when I2C_CTRL1.EN=0. 0: Data register is empty; 1: Data register is not empty. During receiving data, this bit is set to' 1' when the data register is not empty, and it is not set at the address receiving stage. RXDATNE is not set when the ARLOST event occurs.

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Bit Field	Name	Description
		Note: when BSF is set, the RXDATNE bit cannot be cleared when reading data, because the data register is still full.
5	Reserved	Reserved, the reset value must be maintained.
4	STOPF	Stop detection (slave mode) After the software reads the STS1 register, the operation of writing to the CTRL1 register will clear this bit, or when I2C_CTRL1.EN=0, the hardware will clear this bit. 0: No stop condition is detected; 1: Stop condition is detected. After a ACK, the hardware sets this bit to' 1' when the slave device detects a stop condition on the bus. *Note: I2C_STS1.STOPF bit is not set after receiving NACK.*
3	ADDR10F	10-bit header sent (Master mode) After the software reads the STS1 register, the operation of writing to the CTRL1 register will clear this bit, or when I2C_CTRL1.EN=0, the hardware will clear this bit. 0: No ADD10F event; 1: Master has sent the first address byte. In 10-bit address mode, when the master device has sent the first byte, the hardware sets this bit to' 1'. *Note: after receiving a NACK, the I2C_STS1.ADDR10F bit is not set.*
2	BSF	Byte transfer finished After the software reads the STS1 register, reading or writing the data register will clear this bit, or after sending a start or stop condition in transfer, or when I2C_CTRL1.EN=0, this bit is cleared by hardware. 0: Byte transfer does not finish. 1: Byte transfer finished. When I2C_CTRL1.NOEXTEND =0, the hardware sets this bit to' 1' in the following cases: In receiving mode, when a new byte (including ACK pulse) is received and the data register has not been read (I2C_STS1.RXDATNE=1). In sending mode, when a new data is to be transmitted and the data register has not been written the new data (I2C_STS1.TXDATE=1). *Note: after receiving a NACK, the BSF bit will not be set.* *If the next byte to be transferred is PEC (I2C _STS2.TRF is' 1' and I2C_CTRL1.PEC is' 1'), the BSF bit will not be set.*
1	ADDRF	Address sent (master mode) / matched (slave mode) After the STS1 register is read by software, reading the STS2 register will clear this bit, or when I2C_CTRL1.EN=0, it will be cleared by hardware. 0: Address mismatch or no address received(slave mode) or address sending did not end(master mode); 1: Received addresses matched(slave mode) or address sending ends(master mode) In master mode: In 7-bit address mode, this bit is set to' 1' after receiving the ACK of the address.In 10-bit address mode, this bit is set to' 1' after receiving the ACK of the second byte of the address.

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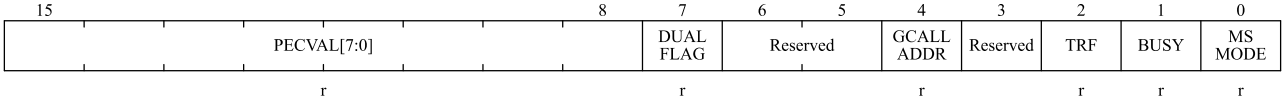
Bit Field	Name	Description
		In slave mode: Hardware sets this bit to' 1' (when the corresponding setting is enabled) when the received slave address matches the content in the OADDR register, or a general call is recognized. *Note: after receiving NACK, the I2C_STS1.ADDRF bit will not be set.*
0	STARTBF	Start bit (Master mode) After the STS1 register is read by software, writing to the data register will clear this bit, or when I2C_CTRL1.EN=0, the hardware will clear this bit. 0: Start condition was not sent; 1: Start condition has been sent. This bit is set to' 1' when the start condition is sent.

14.5.8 I²C Status Register 2 (I2C_STS2)

Address offset: 0x18

Reset value: 0x0000



Bit Field	Name	Description
15:8	PECVAL[7:0]	Packet error checking register Stores the internal PEC value When I2C_CTRL1.PECEN =1.
7	DUALFLAG	Dual flag(Slave mode) Hardware clears this bit when a stop condition or a repeated start condition is generated, or when I2C_CTRL1.EN=0. 0: Received address matches the content in OADDR1; 1: Received address matches the content in OADDR2.
6:5	Reserved	Reserved, the reset value must be maintained.
4	GCALLADDR	General call address(Slave mode) Hardware clears this bit when a stop condition or a repeated start condition is generated, or when I2C_CTRL1.EN=0. 0: No general call address was received; 1: when I2C_CTRL1.GCEN=1, general call address was received.
3	Reserved	Reserved, the reset value must be maintained.
2	TRF	Transmitter/receiver After detecting the stop condition (I2C_STS1.STOPF=1), repeated start condition or bus arbitration loss (I2C_STS1.ARLOST=1), or when I2C_CTRL1.EN=0, the hardware clears it. 0: Data receiving mode 1: Data transmission mode; At the end of the whole address transmission stage, this bit is set according to the R/W bit of the address byte.
1	BUSY	Bus busy Hardware clears this bit when a stop condition is detected.

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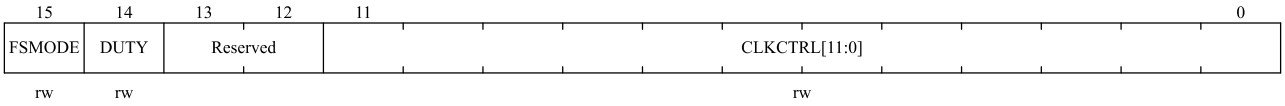
Bit Field	Name	Description
		0: No data communication on the bus; 1: Data communication on the bus. When detecting that SDA or SCL is low level, the hardware sets this bit to' 1'; *Note: this bit indicates the bus communication currently in progress, and this information is still updated when the interface is disabled (I2C_CTRL1.EN=0).*
0	MSMODE	Master/slave mode Hardware clears this bit when a stop condition is detected on the bus, arbitration is lost (I2C_STS1.ARLOST=1), or when I2C_CTRL1.EN=0. 0: In slave mode; 1: In master mode. When the interface is in the master mode (I2C_STS1.STARTBF=1), the hardware sets this bit.

14.5.9 I²C Clock Control Register (I2C_CLKCTRL)

Address offset: 0x1c

Reset value: 0x0000

Note: the CLKCTRL register can only be set when I²C is turned off (I2C_CTRL1.EN=0)



Bit Field	Name	Description
15	FSMODE	I²C mode selection 0: I²C in standard mode (duty cycle default 1/1); 1: I²C in fast mode (duty cycle configurable).
14	DUTY	Duty cycle in fast mode 0: Tlow/Thigh = 2; 1: Tlow/Thigh = 16/9
13:12	Reserved	Reserved, the reset value must be maintained.
11:0	CLKCTRL[11:0]	Clock control register in Fast/Standard mode (Master mode) This division factor is used to set the SCL clock in the master mode. • If duty cycle = Tlow/Thigh = 1/1: CLKCTRL = f_{PCLK}(Hz)/100000/2 Tlow = CLKCTRL ×T_{PCLK} Thigh = CLKCTRL ×T_{PCLK} • If duty cycle = Tlow/Thigh = 2/1: CLKCTRL = f_{PCLK}(Hz)/100000/3 Tlow = 2 ×CLKCTRL×T_{PCLK} Thigh = CLKCTRL×T_{PCLK} • If duty cycle = Tlow/Thigh = 16/9: CLKCTRL = f_{PCLK}(Hz)/100000/25 Tlow = 16 ×CLKCTRL×T_{PCLK}

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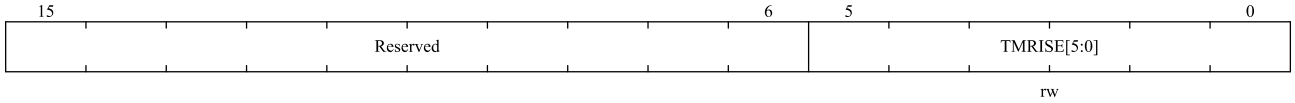
Bit Field	Name	Description
		Thigh = 9 ×CLKCTRL×T_{PCLK} For example, if f_{PCLK}(Hz) = 8MHz, duty cycle = 1/1, CLKCTRL = 8000000/100000/2 = 0x28. *Note:* *(1) the minimum setting value is 0x04 in standard mode and 0x01 in fast mode;* *(2) T_{high}= $T_{r(SCL)}$+$T_{w(SCLH)}$. Refer to the definitions of these parameters in the data sheet for details;* *(3) T_{low}= $T_{f(SCL)}$+$T_{w(SCLL)}$, refer to the definitions of these parameters in the data sheet for details.*

14.5.10 I²C Rise Time Register (I2C_TMRISE)

Address offset: 0x20

Reset value: 0x0002

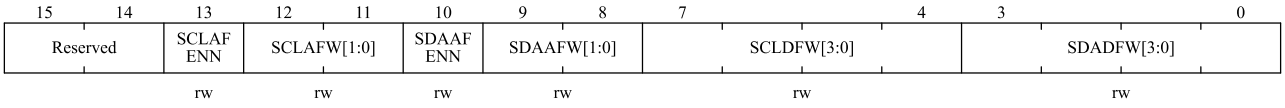


Bit Field	Name	Description
15:6	Reserved	Reserved, the reset value must be maintained.
5:0	TMRISE[5:0]	Maximum rise time in fast/standard mode (master mode). These bits must be set to the maximum SCL rising time given in the I2C bus specification, and incremented step is 1. For example, the maximum allowable SCL rise time in standard mode is 1000ns. if the value in I2C_CTRL2.CLKFREQ [5:0] is equal to 0x08(8MHz) and T_{PCLK}=125ns, 09h(1000ns/125 ns + 1) must be written in TMRISE[5:0] . If the result is not an integer, write the integer part to TMRISE[5:0] to ensure the t_{HIGH} parameter. *Note: TMRISE[5:0] can only be set when I²C is disabled (I2C_CTRL1.EN=0).*

14.5.11 I²C Filter Control Register (I2C_GFLTRCTRL)

Address offset: 0x24

Reset value: 0x0000



Bit field	Name	Description
15:14	Reserved	Reserved
13	SCLAFENN	SCL analog filter enable. 0: Enable 1: Disable
12:11	SCLAFW[1:0]	SCL analog filter width selection 00: 5ns

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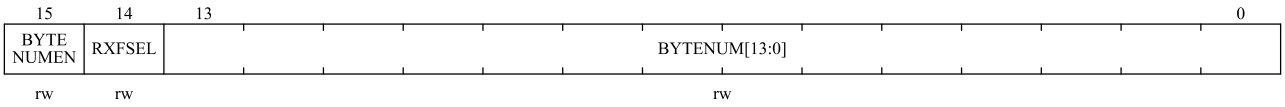
Bit field	Name	Description
		01: 15ns 10: 25ns 11: 35ns
10	SDAAFENN	SDA analog filter enable 0: Enable 1: Disable
9:8	SDAAFW[1:0]	SDA analog filter width selection 00: 5ns 01: 15ns 10: 25ns 11: 35ns
7:4	SCLDFW[3:0]	SCL digital filter width selection 0000: Disable SCL digital filter Others: Filter width is SCLDFW * T_{PCLK}
3:0	SDADFW[3:0]	SDA digital filter width selection 0000: Disable SDA digital filter Others: Filter width is SDADFW * T_{PCLK}

14.5.12 I²C Master Receive Byte Register (I2C_BYTENUM)

Address offset: 0x28

Reset value: 0x0000



Bit field	Name	Description
15	BYTENUMEN	Master receive byte control enable 0: Disable 1: Enable
14	RXFSEL	Receive end send condition selection 0: master sends a STOP condition after receiving all bytes 1: master sends a START condition after receiving all bytes
13:0	BYTENUM	Master receives bytes configuration *Note: if you need to reconfigure BYTENUM after receiving all bytes, you need to wait for I2C_STS2.BUSY is 0 and re-enabled I2C_CTRL1.ACKEN*

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15 Universal Asynchronous Receiver Transmitter (UART)

15.1 Introduction

UART is a full-duplex universal asynchronous serial transceiver module. This interface is a highly flexible serial communication device that can perform full-duplex data exchange with external devices.

The UART has programmable transmit and receive baud rates. It also supports single-wire half-duplex communication and multi-processor communication.

15.2 Main Features

- Full-duplex asynchronous communication
- Supports NRZ standard format
- Supports single-wire half-duplex communication
- Configurable baud rate
- Supports serial data frame structure with 8 or 9 data bits, 1 or 2 stop bits
- Supports generation and checking parity bits
- Supports multi-processor communication mode, can enter mute mode, wake up by idle detection or address mark detection
- Supports data overflow error detection, frame error detection, noise error detection, parity error detection
- 8 interrupt requests:
  - Transmit data register empty
  - Transmit complete
  - Receive data register full
  - Idle line detected
  - Data overflow detected
  - Frame error
  - Noise error
  - Parity error

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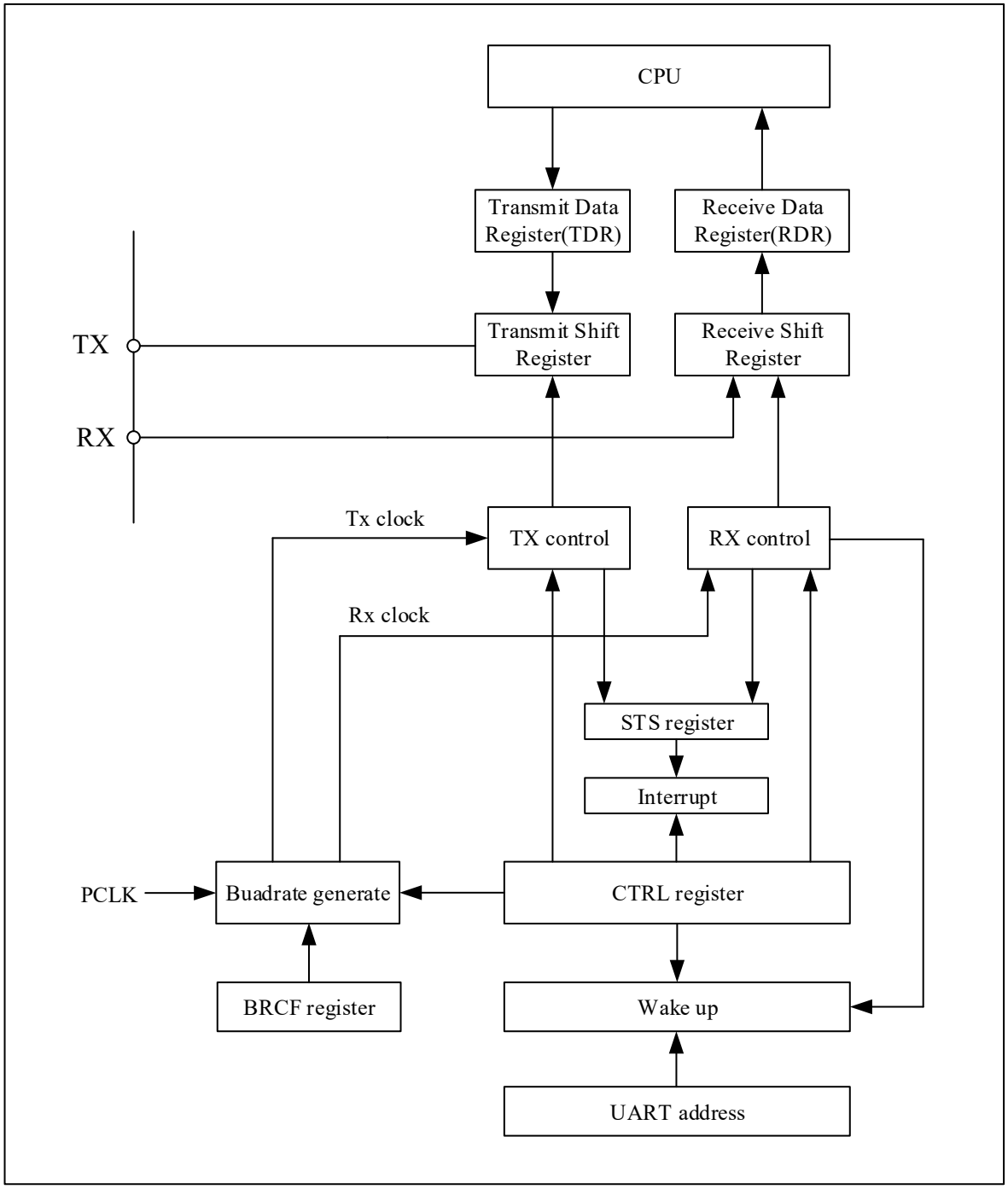
15.3 Functional Block Diagram

Figure 15-1 UART Block Diagram



15.4 Function Description

As shown in the Figure 15-1, any UART bidirectional communication needs to use the RX and TX pins to connect to external devices. TX is the output pin for serial data transmission. When the transmitter is active and not sending data, the TX pin is pulled high. When the transmitter is inactive, the TX pin reverts to the I/O port configuration. RX

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is an input pin for serial data reception, and data is recovered by oversampling technique.

The data packets of serial communication are transmitted from the sending device to the RX interface of the receiving device through its own TX interface.The bus is in an idle state when there is not data transmission and reception . Frame format is: 1 start bit + 8 or 9 data bits (least significant bit first) + 1 parity bit (optional) + 1 or 2 stop bit.

Transmit and receive baud rates can be configured by the fractional baud rate generator.

15.4.1 UART Frame Format

Start bit: 1 bit, active low. Data bits: Configurable via UART_CTRL1.WL bit as 8 or 9 bits, with the LSB first. Stop bit: Active high. Idle frame: A complete data frame consisting entirely of '1's, including the start bit.

Break frame: A complete data frame consisting entirely of '0's, including the stop bit. At the end of the break frame, the transmitter inserts 1 or 2 stop bits ('1') to acknowledge the start bit.

Figure 15-2 Word Length = 8 Setting

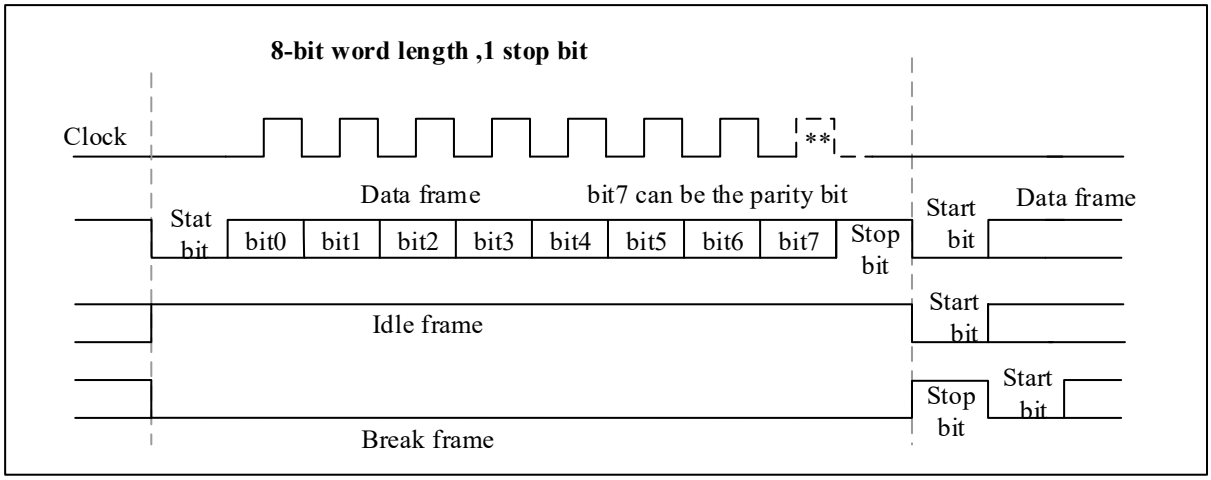
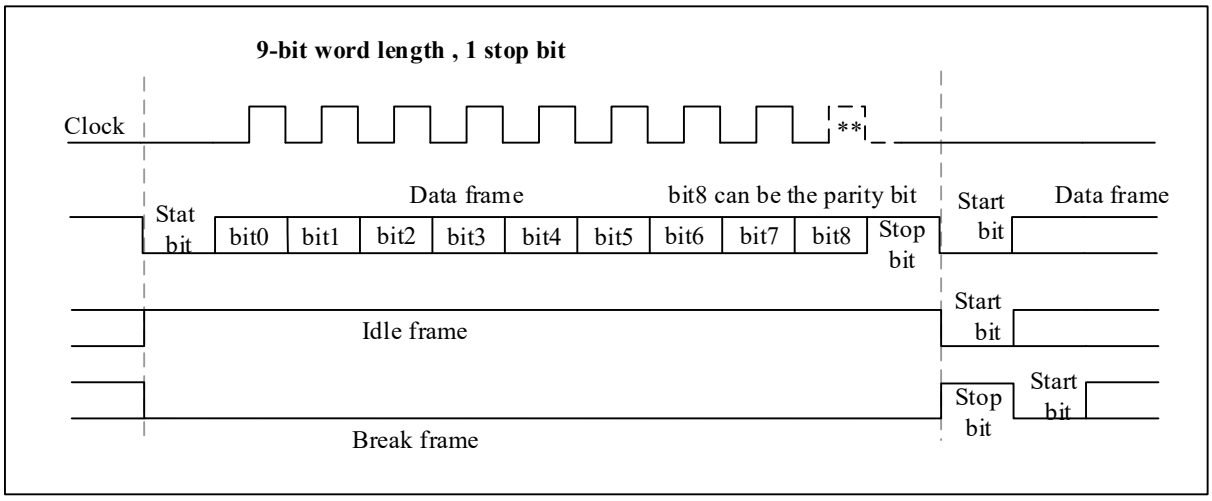


Figure 15-3 Word Length = 9 Setting



15.4.2 Transmitter

After the transmitter is enabled, the data in the transmit shift register is transmitted out through the TX pin.

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15.4.2.1 Idle frame

Setting UART_CTRL1.TXEN will cause the UART to transmit an idle frame before the first data frame.

15.4.2.2 Character transmission

Idle frames are followed by characters transmission. Each character is preceded by a start bit (low level). The transmitter transmits 8-bit or 9-bit data according to the configuration of the data bit length, with the least significant bit first. If UART_CTRL1.TXEN is reset during a data transfer, it will cause the baud rate counter to stop counting and the data being transferred will be corrupted.

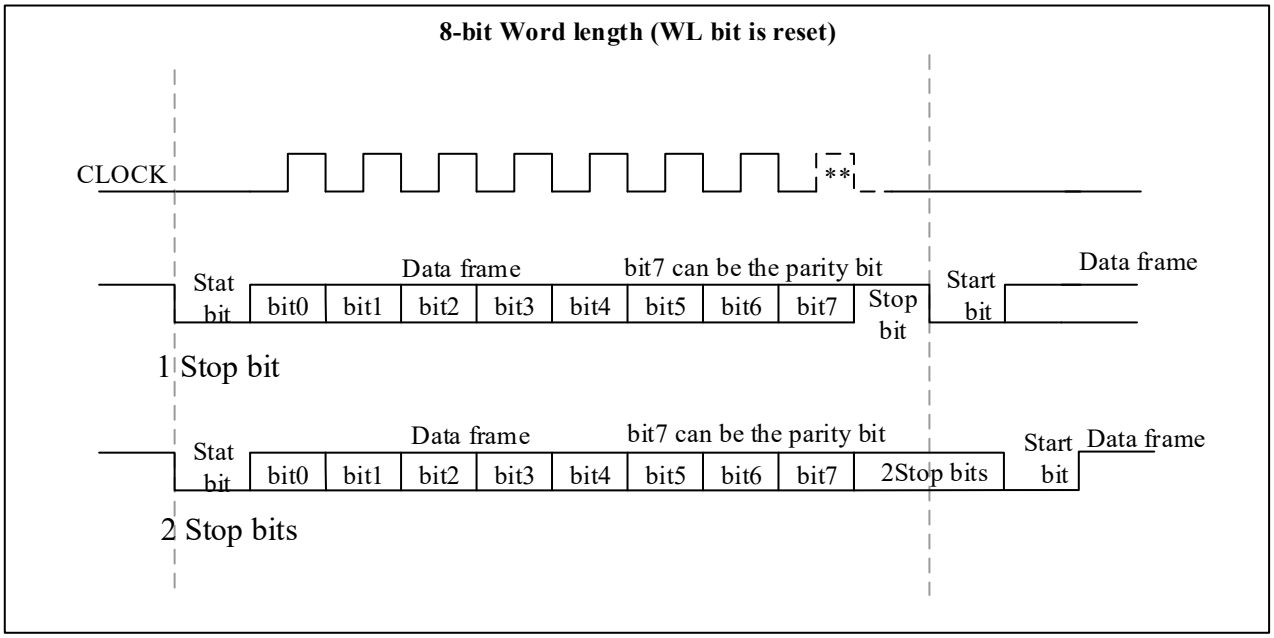
15.4.2.3 Stop bit

The characters are followed by stop bits, the number of which can be configured by setting UART_CTRL2. STPB[1:0] bits.

Table 15-1 Stop Bit Configuration

UART_CTRL2.STPB[1:0]	Stop Bit Length (Bits)	Functional Description
00	1	Default
10	2	General UART mode, single-wire mode and modem mode.

Figure 15-4 Stop Bit Configuration



15.4.2.4 Break frame

UART_CTRL1.SDBRK can be set to transmit the break frame. When data length is 8-bit data, the break frame consists of 10 bits of low level, followed by a stop bit; when data length is 9-bit data, the break frame consists of 11 bits of low level, followed by a stop bit (high level).

After the break frame is transmitted, UART_CTRL1.SDBRK is cleared by hardware, and the stop bit of the break frame is automatically transmitted. Therefore, to transmit a second break frame, UART_CTRL1.SDBRK should be set after the stop bit of the previous break frame has been transmitted.

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If software resets the UART_CTRL1.SDBRK bit before starting to transmit the break frame, the break frame will not be transmitted.

15.4.2.5 Transmitter process

1. Enable UART_CTRL1.UEN to activate UART;
2. Configure the transmitter's baud rate, data bit length, parity bit (optional), the number of stop bits;
3. Activate the transmitter (UART_CTRL1.TXEN);
4. Write each data to be transmitted to the UART_DAT register through the CPU, and the write operation to the UART_DAT register will clear UART_STS.TXDE;
5. After writing the last data to the UART_DAT register, wait for UART_STS.TXC =1, which indicates the end of the transmission of the last data frame.

15.4.2.6 Single byte communication

Writing to the UART_DAT register clears the UART_STS.TXDE bit.

The UART_STS.TXDE bit is set by hardware when the data in the TDR register is transferred to the transmit shift register (indicating that data is being transmitted). An interrupt will be generated if UART_CTRL1.TXDEIEN is set. At this point, the next data can be write to the UART_DAT register because the TDR register has been cleared and will not overwrite the previous data.

Write operation to UART_DAT register:

- When the transmit shift register is not transmitting data and is in an idle state, the data is directly put into the shift register for transmission, and the UART_STS.TXDE bit is set by hardware;
- When the transmit shift register is transmitting data, the data is stored in the TDR register, and after the current transmission is completed, the data is put into the transmit shift register.

When a frame containing data is sent and UART_STS.TXDE=1, the UART_STS.TXC bit is set to '1' by hardware. An interrupt is generated if UART_CTRL1.TXCIEN is '1'. UART_STS.TXC bit is cleared by a software sequence (read UART_STS register first, then write UART_DAT register).

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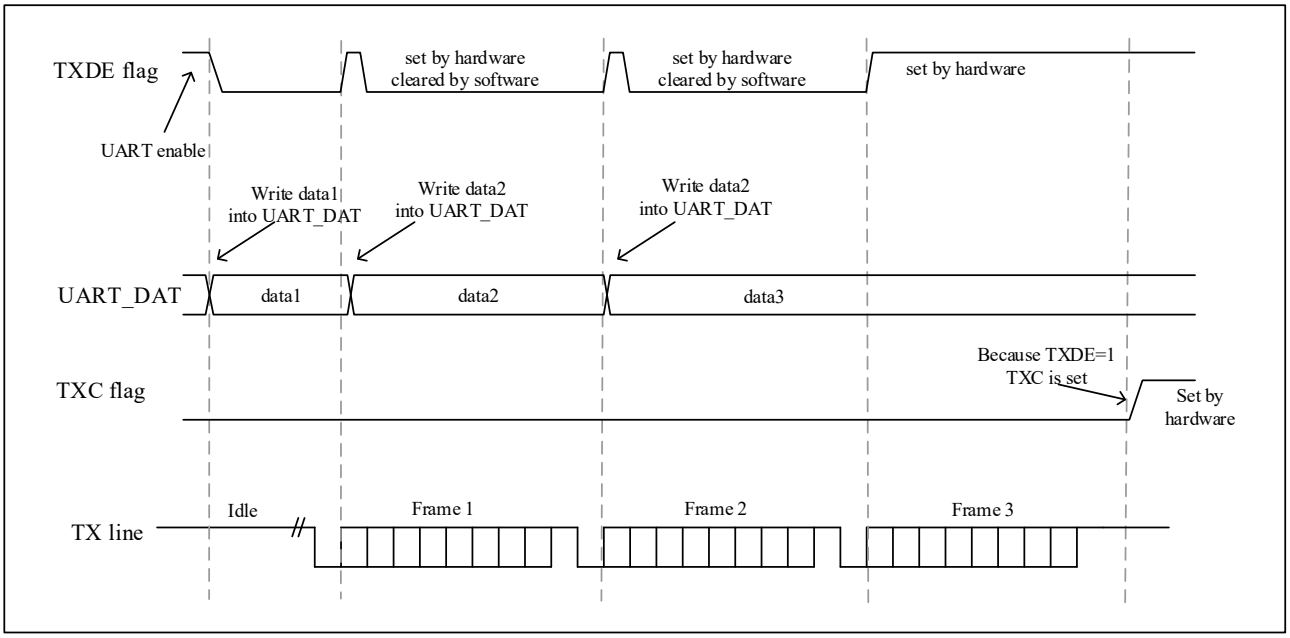
Figure 15-5 TXC/TXDE Changes During Transmission



15.4.3 Receiver

15.4.3.1 Start bit detection

When the received sampling sequence is: 1 1 1 0 X 0 X 0 X 0 0 0 0, it is considered that a start bit is detected.

If there are three ‘0’ samples at the 3rd, 5th, and 7th bits, and three ‘0’ samples at the 8th, 9th, and 10th bits, the start bit is confirmed. The UART_STS.RXDNE flag bit is set, and if UART_CTRL1.RXDNEIEN=1, an interruption occurs, but it will not set the NEF noise flag.

If there are two ‘0’ samples at the 3rd, 5th, and 7th bits, and two ‘0’ samples at the 8th, 9th, and 10th bits, the start bit is confirmed, but it will set bit NEF noise flag.

If there are three ‘0’ samples at the 3rd, 5th, and 7th bits, and two ‘0’ samples at the 8th, 9th, and 10th bits, the start bit is confirmed, but it will set NEF noise flag.

If there are two ‘0’ samples of the 3rd, 5th, and 7th bits, and three ‘0’ samples at the 8th, 9th, and 10th bits, the start bit is confirmed, but it will set NEF noise flag.

If the sampling values in the 3rd, 5th, 7th, 8th, 9th and 10th bits cannot meet the above four requirements, the UART receiver thinks that it has not received the correct start bit, and will exit the start bit detection and return to idle state and wait for falling edge.

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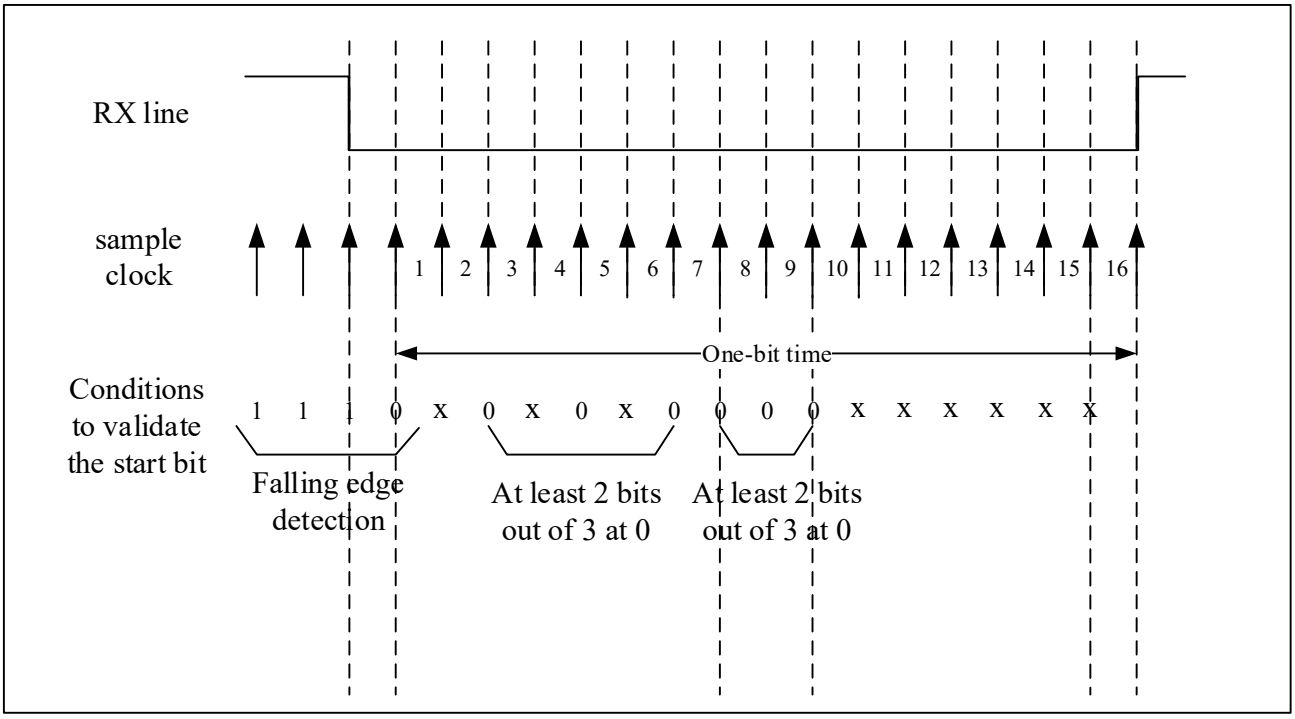
Figure 15-6 Start Bit Detection



15.4.3.2 Stop bit description

The number of data stop bits can be configured by the UART_CTRL2.STPB[1:0] bits. In normal mode, 1 or 2 stop bits can be selected.

1. **1 stop bit:** the sampling of 1 stop bit is done on the 8th, 9th and 10th samples.
2. **2 stop bits:** the sampling of 2 stop bits is done on the 8th, 9th and 10th samples of the first stop position. If a frame error is detected during the first stop bit, the frame error flag is set. The second stop bit is not detected for framing error. The UART_STS.RXNE flag will be set at the end of the first stop bit.

15.4.3.3 Receiver process

1. Enable UART_CTRL1.UEN to activate UART;
2. Configure the receiver's baud rate, data bit length, parity bit (optional), stop bit number;
3. Activate the receiver (UART_CTRL1.RXEN) and start searching for the start bit;
4. The receiver receives 8-bit or 9-bit data according to the configuration of the data bit length, and the least significant bit of the data is first shifted from the RX pin into the receive shift register;
5. When the data of the received shift register is moved to the RDR register, UART_STS.RXDNE is set, and the data can be read out. If UART_CTRL1.RXDNEIEN is 1, an interrupt will be generated;
6. When an overflow error, noise error, or frame error is detected in the received frame, the corresponding error flag status bit will be set. If UART_CTRL1.RXEN is reset during data transmission, the data being received will be lost;
7. UART_STS.RXDNE is set after receiving data, and a read operation to UART_DAT can clear this bit: in single-

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buffer communication, it is cleared by software reading the UART_DAT register.

15.4.3.4 Idle frame detection

When an idle frame is detected, UART_STS.IDLEF sets to 1. An interrupt is generated if UART_CTRL1.IDLEIEN is '1'. UART_STS.IDLEF bit is cleared by a software sequence (read UART_STS register first, then read UART_DAT register).

15.4.3.5 Break frame detection

The frame error flag(UART_STS.FEF) is set by hardware when the receiver detects a break frame. It can be cleared by a software sequence (read UART_STS register first, then read UART_DAT register).

15.4.3.6 Framing error

A framing error occurs when a stop bit is not received and recognized at the expected time. At this time, the frame error flag UART_STS.FEF will be set by hardware, and the invalid data will be transferred from the shift register to the UART_DAT register. In single-byte communication, no framing error interrupt will be generated because UART_STS.RXDNE flag is set and the hardware will generate an interrupt.

15.4.3.7 Overrun error

When UART_STS.RXDNE is still '1', and the data currently received in the shift register needs to be transferred to the RDR register, an overflow error flag (UART_STS.OREF) will be set by hardware. When this bit is set, the value in the RDR register is not lost, but the data in the shift register is overwritten. It is cleared by a software sequence (read UART_STS register first, then write UART_DAT register).

When an overflow error occurs, UART_STS.RXDNE is '1', and an interrupt is generated.

15.4.3.8 Noise error

UART_STS.NEF is set by hardware when noise is detected on a received frame. It is cleared by software sequence (read UART_STS register first, then write UART_DAT register). In single-byte communication, no noise interrupt generated because it occurs with UART_STS.RXDNE and the hardware will generate an interrupt when the UART_STS.RXDNE flag is set.

Table 15-2 Data Sampling For Noise Detection

Sample Value	NE Status	Received Bits	Data Validity
000	0	0	Valid
001	1	0	be invalid
010	1	0	be invalid
011	1	1	be invalid
100	1	0	be invalid
101	1	1	be invalid
110	1	1	be invalid
111	0	1	Valid

15.4.4 Generation of Fractional Baud Rate

The baud rate of the UART can be configured in the UART_BRCF register. This register defines the integer and fractional parts of the baud rate divider. The baud rate of the transmitter and receiver should be configured to the

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same value. The UART_BRCF register should not be changed during communication, because the baud rate counter will be replaced by the new value of the baud rate register.

$$\text{TX / RX baud rate} = f_{CK} /(16 * \text{UARTDIV})$$

where f_{CK} is the clock provided to the peripheral: PCLK is used for UART1/2, up to 48MHz. UARTDIV is an unsigned fixed-point number.

15.4.4.1 UARTDIV and UART_BRCF register configuration

Example 1:

If UARTDIV = 27.75, then:

DIV_Decimal = 16*0.75 = 12 = 0x0C

DIV_Integer = 27=0x1B

So UART_BRCF = 0x1BC

Example 2:

If UARTDIV = 20.98, then:

DIV_Decimal = 16*0.98 = 15.68

Nearest integer: DIV_Decimal = 16 = 0x10, which is out of configurable range, so a carry to integer is required

So DIV_Integer = 20 + 1 = 21 = 0x15

DIV_Decimal = 0x0

So UART_BRCF = 0x150

Example 3:

If UART_BRCF = 0x19B:

DIV_Integer = 0x19 = 25

DIV_Decimal = 0x0B = 11

So UARTDIV = 25 + 11/16 = 25.6875

Table 15-3 Error Calculation when Setting Baud Rate

Baud Rate		f_{ck}=48M		
Serial Number	Kbps	Reality	Value programmed in Baud Rate Register	Error%
1	2.4	2.4	1250	0%
2	9.6	9.6	312.5	0%
3	19.2	19.2	156.25	0%
4	57.6	57.623	52.0625	0.04%
5	115.2	115.1	26.0625	0.08%
6	230.4	230.769	13	0.16%
7	460.8	461.538	6.5	0.16%

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8	921.6	923.076	3.25	0.16%
9	2250	2285.714	1.3125	1.58%
10	3000	3000	1	0%

Note: The lower the clock frequency of the CPU, the lower the error for a particular baud rate.

15.4.5 Receiver's Tolerance Clock Deviation

Variations due to transmitter errors (including transmitter side oscillator variations), receiver side baud rate rounding errors, receiver side oscillator variations, variations due to transmission lines (usually due to the inconsistency between the low-to-high and the high-to-low transition timing of the transceiver), these factors will affect the overall clock system variation. Only when the sum of the above four changes is less than the tolerance of the UART receiver, the UART asynchronous receiver can work normally.

When receiving data normally, the tolerance of the UART receiver depends on the selection of the data bit length and whether fractional baud rate divisors are used. The tolerance of the UART receiver is equal to the maximum tolerable variation.

Table 15-4 When DIV_Decimal = 0. Tolerance of UART Receiver

WL Bit	NF is an Error	NF is Don't Care
0	3.75%	4.375%
1	3.41%	3.97%

Table 15-5 When DIV_Decimal != 0. Tolerance of UART Receiver

WL bit	NF is an Error	NF is Don't Care
0	3.33%	3.88%
1	3.03%	3.53%

15.4.6 Parity Control

Parity can be enabled by configuring the UART_CTRL1.PCEN bit. When the parity bit is enabled for transmission, a parity bit is generated, and parity check is performed on reception.

Table 15-6 Frame Format

WL Bit	PCEN Bit	UART Frame
0	0	| Start bit | 8-bit data | Stop bit |
0	1	| Start bit | 7 bits of data | Parity bit | Stop bit |
1	0	| Start bit | 9-bit data | Stop bit |
1	1	| start bit | 8-bit data | Parity bit | Stop bit |

Even parity

Configure UART_CTRL1.PSEL to 0 to enable even parity.Even parity means that the number of '1' in the transmitted data frame (including parity bit) is an even number. For example: if Data=1100 0101, there are 4 '1's, then the parity bit will be '0' (4 '1' in total). After the data and parity bit are sent to the receiver, the receiver calculates the number of '1's in the data again. If it is an even number, the check is passed, indicating that no errors occurred during the transmission process. If it is not an even number, it means that an error has occurred, the UART_STS.PEF flag is set to '1', and if UART_CTRL1.PEIEN is enabled, an interrupt is generated.

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Odd parity

Configure UART_CTRL1.PSEL to 1 to enable odd parity.Odd parity means the number of '1' in the transmitted data frame (including parity bit) is an odd number.For example: if Data=11000101, there are 4 '1's, then the parity bit will be '1' (5 '1' in total). After the data and parity bit are sent to the receiver, the receiver calculates the number of '1's in the data again. If it is an odd number, the check is passed, indicating that no errors occurred during the transmission process. If it is not an odd number, it means that an error has occurred, the UART_STS.PEF flag is set to '1', and if UART_CTRL1.PEIEN is enabled, an interrupt is generated.

15.4.7 Multiprocessor Communication

UART allows multiprocessor communication. When multiple processors communicate through UART, and it is necessary to determine who is the master device, and the remaining processors are all slave devices. The TX output of the master device is directly connected to the RX port of all slave device. The TX outputs of the slaves are logically AND together and connected to the RX inputs of the master.

When multiprocessor communication is performed, the slave devices are all in mute mode, the master uses a specific method to wake up a slave device to communicate when needed, so that the slave device is in an active state and transmits data with the master device.

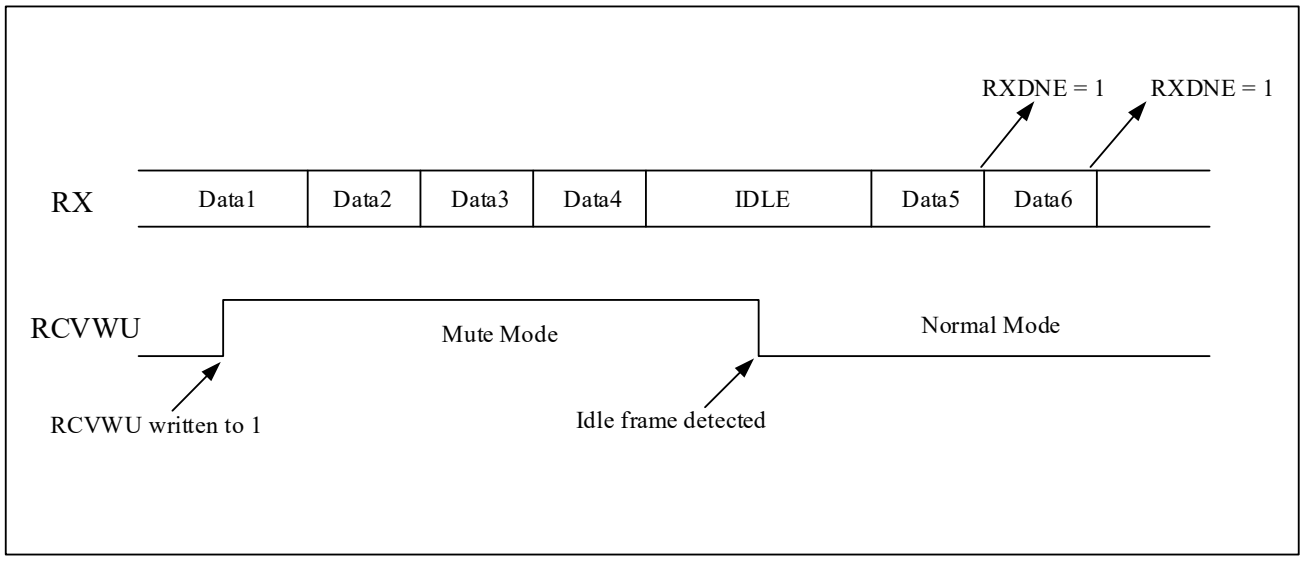
The UART can wake up from mute mode by idle line detection or address mark detection.

15.4.7.1 Idle line detection

The idle line detection configuration process is as follows:

1. Configure the UART_CTRL1.WUM bit to 0, and the UART performs idle line detection;
2. When UART_CTRL1.RCVWU is set (which can be automatically controlled by hardware or written by software under certain conditions), UART enters mute mode. In mute mode, none of the receive status bits are set, and all receive interrupts are disabled;
3. As shown in the Figure 15-7 below, when an idle frame is detected, UART is woken up, and then UART_CTRL1.RCVWU is cleared by hardware. At this time, UART_STS.IDLEF is not set.

Figure 15-7 Mute Mode Using Idle Line Detection



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15.4.7.2 Address mark detection

By configuring the UART_CTRL1.WUM bit to 1, the UART performs address mark detection. The address of the receiver is programmable through the UART_CTRL2.ADDR[3:0] bits. If the MSB is 1, the byte is considered as an address, otherwise it is considered as data.

In this mode, the UART can enter mute mode by:

- When the receiver does not contain data, UART_CTRL1.RCVWU can be written to 1 by software, and UART enters mute mode;

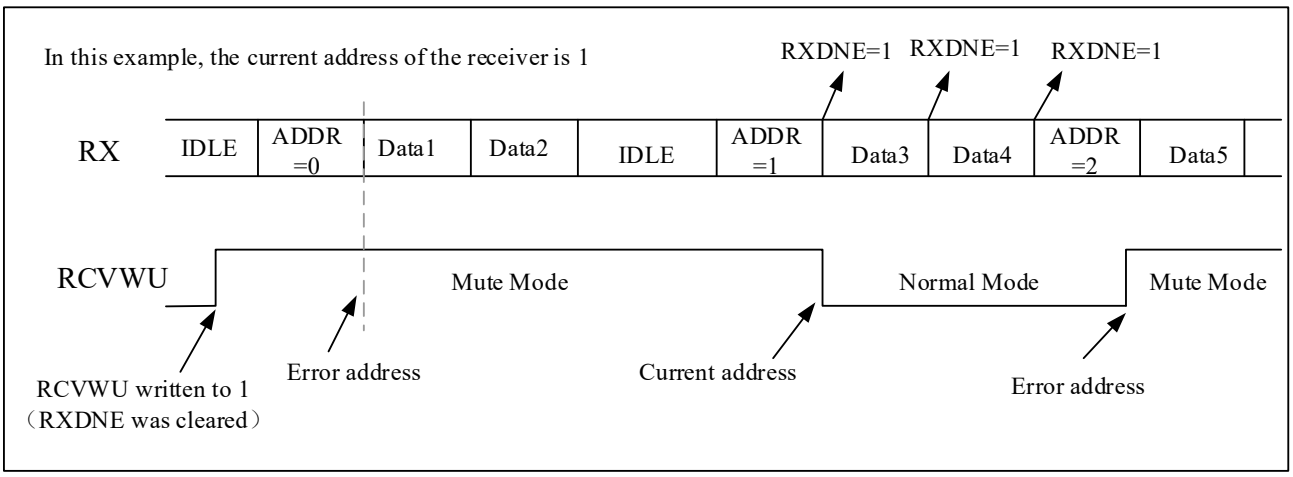
  Note: when the receive buffer contains no data (UART_STS.RXDNE = 0), the UART_CTRL1.RCVWU bit can be written to 0 or 1. Otherwise, the write operation is ignored.

- When the received address does not match the address of the UART_CTRL2.ADDR[3:0] bits, UART_CTRL1.RCVWU is written to 1 by hardware.

In mute mode, none of the receive status bits are set and all receive interrupts are disabled.

When the received address matches the address of the UART_CTRL2.ADDR[3:0] bits, the UART is woken up and UART_CTRL1.RCVWU is cleared. The UART_STS.RXDNE bit will be set when this matching address is received, and then data can then be transmitted normally.

Figure 15-8 Mute Mode Detected Using Address Mark



15.4.8 Single-line Half-duplex Communication

UART supports single-wire half-duplex communication, allowing data to be transmitted in both directions, but only allows data to be transmitted in one direction at the same time. Communication conflicts are managed by software. Through the UART_CTRL3.HDMEN bit, user can choose whether to enable half-duplex mode.

After the half-duplex mode is turned on, the TX pin and the RX pin are interconnected inside the chip, and the RX pin is no longer used. When there is no data to be transmitted, TX is always released. Therefore, when not driven by the UART, the TX pin must be configured as a floating input or an open-drain output high.

15.5 Interrupt Request

The various interrupt events of UART are logical OR relations. If the corresponding enable control bit is set, these

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events can generate their own interrupts, but only one interrupt request can be generated at the same time.

Table 15-7 UART Interrupt Request

Interrupt Function	Interrupt Event	Event Flag	Enable Bit
UART global interrupt	Transmission data register is empty.	TXDE	TXDEIEN
	Transmission complete	TXC	TXCIEN
	Receive data ready to be read	RXDNE	RXDNEIEN
	Data overrun error detected.	OREF	
	Idle line detected	IDLEF	IDLEIEN
	Parity error	PEF	PEIEN

15.6 UART Mode Configuration

Table 15-8 UART Mode Setting(1)

Communication Mode	UART1	UART2
Asynchronous mode	Y	Y
Hardware flow control mode	N	N
DMA communication mode	N	N
Multiprocessor	Y	Y
Smartcard mode	N	N
Single-wire half duplex mode	Y	Y
IrDA infrared mode	N	N
LIN	N	N

(1) Y = support this mode, N = do not support this mode

15.7 UART Registers

15.7.1 UART Register Map

Table 15-9 UART Register Map and Reset Values

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
000h	UART_STS	Reserved																								TXDE	TXC	RXDNE	IDLEF	OREF	NEF	FEF	PEF
	Reset Value																									1	1	0	0	0	0	0	0
004h	UART_DAT	Reserved																							DATV[8:0]								
	Reset Value																								0	0	0	0	0	0	0	0	0
008h	UART_BRCF	Reserved																DIV_Integer[11:0]												DIV_Decimal [3:0]			
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
00Ch	UART_CTRL1	Reserved																		UEN	WL	WUM	PCEN	PSEL	PEIEN	TXDEIEN	TXCIEN	RXDNEIEN	IDLEIEN	TXEN	RXEN	RCVWU	SDBRK
	Reset Value																			0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
010h	UART_CTRL2	Reserved																		STPB [1:0]		Reserved								ADDR[3:0]			
	Reset Value																			0	0									0	0	0	0
014h	UART_CTRL3	Reserved																												HDMEN	Reserved		
	Reset Value																													0			

15.7.2 UART Status Register (UART_STS)

Address offset: 0x00

Reset value: 0x0000 00C0

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								TXDE	TXC	RXDNE	IDLEF	OREF	NEF	FEF	PEF
								r	rc_w0	rc_w0	r	r	r	r	r

Bit Field	Name	Description
31:8	Reserved	Reserved, the reset value must be maintained
7	TXDE	The Transmit data register empty. Set to 1 after power-on reset or transmit data has been sent to the shift register. Setting UART_CTRL1.TXDEIEN will generate an interrupt. This bit is cleared to 0 when the software writes the data into UART_DAT. 0: Send data buffer is not empty. 1: The transmitting data buffer is empty.
6	TXC	Transmission complete. This bit is set to 1 after power-on reset. If UART_STS.TXDE is set, this bit is set when the current data transmission is completed. Setting UART_CTRL1.TXCIEN bit will generate an interrupt. This bit is cleared by software sequence (a read from the UART_STS register followed by a write to the UART_DAT register) or software writes 0. 0: Transmission is not complete. 1: Transmission is completed.
5	RXDNE	The read data register not empty. This bit is set when the read data buffer receives data from the shift register. When UART_CTRL1.RXDNEIEN bit is set, an interrupt will be generated. Software can clear this bit by writing 0 to it or reading the UART_DAT register. 0: The read data buffer is empty. 1: The read data buffer is not empty.
4	IDLEF	IDLE line detected flag. Within one frame time, if the idle state is detected at the RX pin, this bit is set to 1. When UART_CTRL1.IDLEIEN bit is set, an interrupt will be generated.

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Bit Field	Name	Description
		The software can clear this bit by reading UART_STS first and then reading UART_DAT. 0: No idle frame detected. 1: idle frame detected. *Note: UART_STS.IDLEF bit will not be set high again until UART_STS.RXDNE bit is set (that is, an idle line is detected again)*
3	OREF	Overrun error With UART_STS.RXDNE set, this bit is set if the UART_DAT register receives data from the shift register. When UART_CTRL1.RXDNEIEN bit is set, an interrupt will be generated. The software can clear this bit by reading UART_STS first and then reading UART_DAT. 0: No overrun error was detected. 1: Overflow error detected. *Note: When this bit is set, the RDR register content will not be lost but the shift register will be overwritten.*
2	NEF	Noise error flag. When noise is detected in the received frame, this bit is set by hardware. It is cleared by the software sequence (read UART_STS first, and then read UART_DAT). 0: No noise error detected. 1: Noise error detected. *Note: this bit will not generate an interrupt because it appears with UART_STS.RXDNE, and the hardware will generate an interrupt when setting the UART_STS.RXDNE flag.*
1	FEF	Framing error. This bit is set by hardware when synchronization dislocation, excessive noise or break character is detected. It is cleared by the software sequence (read UART_STS first, and then read UART_DAT). 0: No framing errors were detected. 1: A framing error or a Break Character detected. *Note: this bit will not generate an interrupt because it appears with UART_STS.RXDNE, and the hardware will generate an interrupt when setting the UART_STS.RXDNE flag. If the currently transmitted data has both framing errors and overload errors, the hardware will continue to transmit the data and only set the UART_STS.OREF flag bit.*
0	PEF	Parity error. This bit is set when the parity bit of the received data frame is different from the expected check value. If UART_CTRL1.PEIEN=1, it will generate an interrupt. The software can clear this bit by reading UART_STS first and then reading UART_DAT. Before clear UART_STS.PEF bit, software must wait for UART_STS.RXDNE =1. 0: No parity error detected. 1: Parity error detected.

15.7.3 UART Data Register (UART_DAT)

Address offset: 0x04

Reset value: undefined (uncertain value)

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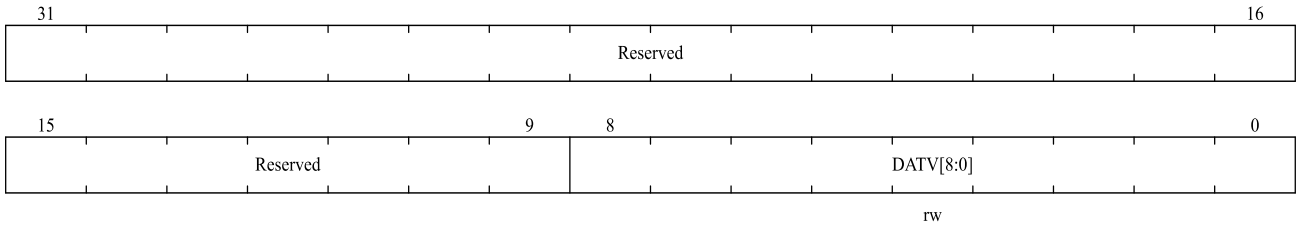


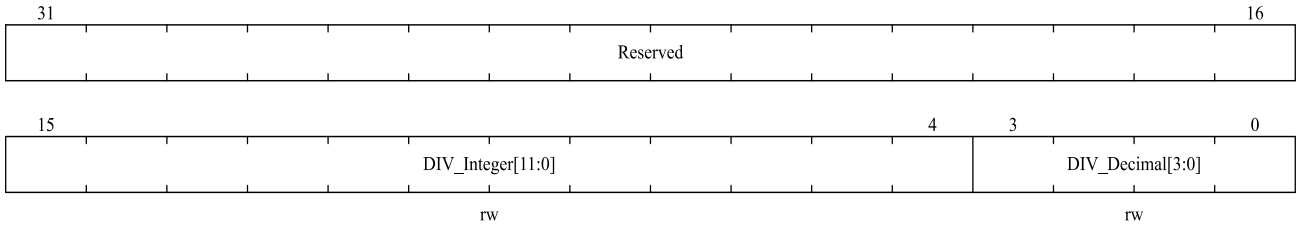
Bit Field	Name	Description
31:9	Reserved	Reserved, the reset value must be maintained
8:0	DATV[8:0]	Data value Contains the data sent or received; Software can change the transmitted data by writing these bits, or read to obtain the received data. If parity is enabled, when the transmitted data is written into the register, the highest bit of the data (the 7th or 8th bit depends on UART_CTRL1.WL bit) will be replaced by the parity bit.

15.7.4 UART Baud Rate Configuration Register (UART_BRCF)

Address offset: 0x08

Reset value: 0x0000 0000

Note: The baud counter stops counting if UART_CTRL1.TXEN or UART_CTRL1.RXEN are disabled respectively.

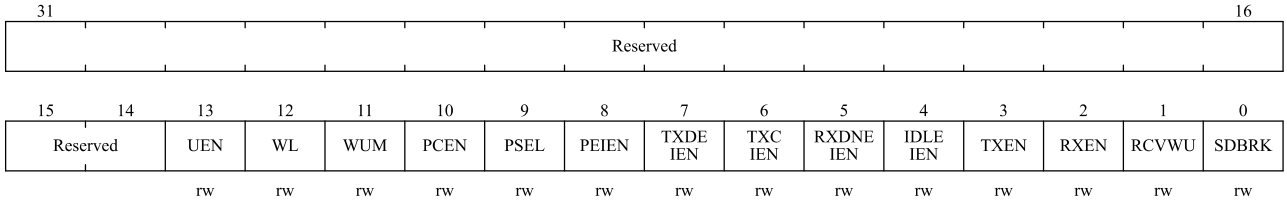


Bit Field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained
15:4	DIV_Integer [11:0]	Integer part of baud rate divider
3:0	DIV_Decimal[3:0]	Fractional part of baud rate divider

15.7.5 UART Control Register 1(UART_CTRL1)

Address offset: 0x0C

Reset value: 0x0000 0000



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Bit Field	Name	Description
31:14	Reserved	Reserved, the reset value must be maintained
13	UEN	UART enable When this bit is cleared, the divider and output of UART stop working after the current byte transmission is completed to reduce power consumption. Software can set or clear this bit. 0:UART is disabled. 1:UART is enabled.
12	WL	Word length. 0: 8 data bits. 1: 9 data bits. *Note: if data is transmitting, this bit cannot be configured.*
11	WUM	Wake up mode from mute mode. 0: Idle frame wake-up. 1: Address identifier wake-up.
10	PCEN	Parity control enable 0: Parity control is disabled. 1: Parity control is enabled.
9	PSEL	Parity selection. 0: Even parity. 1: Odd parity.
8	PEIEN	PE interrupt enable If this bit is set to 1, an interrupt is generated when UART_STS.PEF bit is set. 0: Parity error interrupt is disabled. 1: Parity error interrupt is enabled.
7	TXDEIEN	TXDE interrupt enable If this bit is set to 1, an interrupt is generated when UART_STS.TXDE bit is set. 0: Send buffer empty interrupt is disabled. 1: Send buffer empty interrupt is enabled.
6	TXCIEN	Transmit complete interrupt enable. If this bit is set to 1, an interrupt is generated when UART_STS.TXC is set. 0: Transmission completion interrupt is disabled. 1: Transmission completion interrupt is enabled.
5	RXDNEIEN	RXDNE interrupt enable If this bit is set to 1, an interrupt is generated when UART_STS.RXDNE or UART_STS.OREF is set. 0: Data buffer non-empty interrupt and overrun error interrupt are disabled. 1: Data buffer non-empty interrupt and overrun error interrupt are enabled.
4	IDLEIEN	IDLE interrupt enable. If this bit is set to 1, an interrupt is generated when UART_STS.IDLEF is set. 0: IDLE line detection interrupt is disabled. 1: IDLE line detection interrupt is enabled.
3	TXEN	Transmitter enable. 0: The transmitter is disabled.

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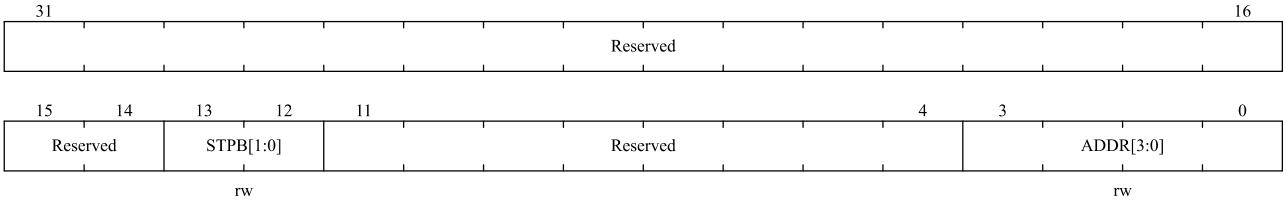
Bit Field	Name	Description
		1:The transmitter is enabled.
2	RXEN	Receiver enable 0: The receiver is disabled. 1: The receiver is enabled.
1	RCVWU	The receiver wakes up Software can set this bit to 1 to make UART enter mute mode, and clear this bit to 0 to wake up UART. In idle frame wake-up mode (UART_CTRL1.WUM=0), this bit is cleared by hardware when an idle frame is detected. In address wake-up mode (UART_CTRL1.WUM=1), when an address matching frame is received, this bit is cleared by hardware. When an address mismatch frame is received, it is set to 1 by hardware. 0: The receiver is in normal operation mode. 1: The receiver is in mute mode.
0	SDBRK	Send break frame. The software transmits a break frame by setting this bit to 1. This bit is cleared by hardware during stop bit of the break frame transmission. 0: No break frame is transmitted. 1: break frame will be transmitted

15.7.6 UART Control Register 2(UART_CTRL2)

Address offset: 0x10

Reset value: 0x0000 0000



Bit Field	Name	Description
31:14	Reserved	Reserved, the reset value must be maintained
13:12	STPB[1:0]	STOP bits. 00: 1 stop bit 10: 2 stop bit Other: reserved
11:4	Reserved	Reserved, the reset value must be maintained
3:0	ADDR[3:0]	UART address. Used in the mute mode of multiprocessor communication, using address identification to wake up a UART device. In address wake-up mode (UART_CTRL1.WUM=1), if the lower four bits of the received data frame are not equal to the ADDR[3:0] value, UART will enter the mute mode;

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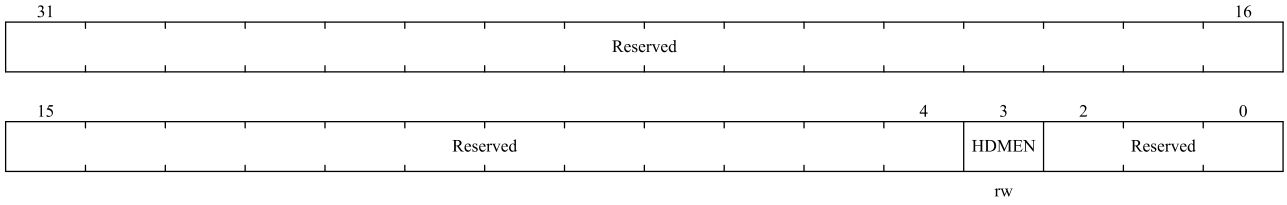
Bit Field	Name	Description
		If the lower four bits of the received data frame are equal to the ADDR[3:0] value, UART will be awakened.

15.7.7 UART Control Register 3(UART_CTRL3)

Address offset: 0x14

Reset value: 0x0000 0000



Bit Field	Name	Description
31:4	Reserved	Reserved, the reset value must be maintained.
3	HDMEN	Half-duplex mode enable. This bit is used to enable half-duplex mode. 0: Half-duplex mode is disabled. 1: Half-duplex mode is enabled.
2:0	Reserved	Reserved, the reset value must be maintained.

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16 Serial Peripheral Interface (SPI)

16.1 SPI Introduction

The serial peripheral interface (SPI) is able to work in master or slave mode, and supports full-duplex and simplex high-speed communication mode.

16.2 SPI Main Features

- Full-duplex mode and half-duplex synchronous mode
- Supports master mode, slave mode and multi-master mode
- Supports 8-bit or 16-bit data frame format
- Data bit sequence programmable
- NSS management by hardware or software
- Clock polarity and phase programmable

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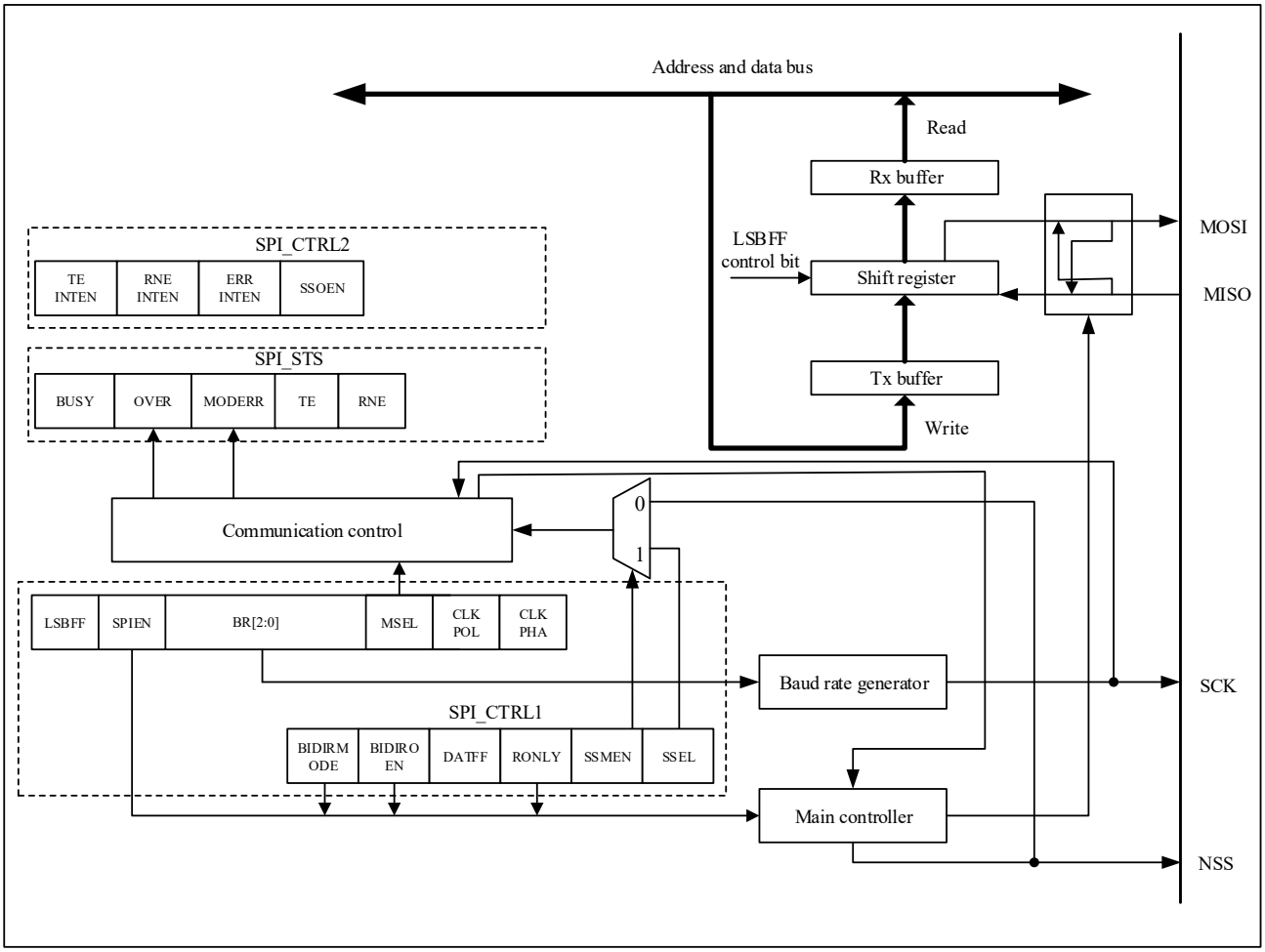
16.3 SPI Function Description

16.3.1 General Description

Figure 16-1 SPI Block Diagram



To connected external devices, SPI has four pins, which are as follows:

- SCK: serial clock pin. Serial clock signal is output from the SCK pin of master device and input to SCK pin of slave device.
- MISO: master input/slave output pin. Data is received from the MISO pin of master device and transmitted by the MISO pin of slave device.
- MOSI: master output/slave input pin. Data is transmitted by the MOSI pin of master device and received from the MOSI pin of slave device.
- NSS: chip select pin. There are two types of NSS pin, internal pin and external pin. If the internal pin detects a high level, SPI works in the master mode. Conversely, SPI works in the slave mode. Users can use a standard I/O pin of the master device to control the NSS pin of the slave device.

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16.3.1.1 Software NSS mode

The software slave device management is enabled when SPI_CTRL1.SSMEN=1.

The NSS pin is not used in software NSS mode. In this mode, the internal NSS signal level is driven by writing the SPI_CTRL1.SSEL bit (SPI_CTRL1.SSEL=1 in master mode, and SPI_CTRL1.SSEL=0 in slave mode).

16.3.1.2 Hardware NSS mode

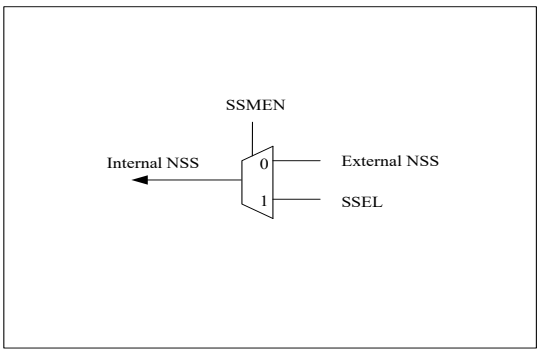
The software slave device management is disabled when SPI_CTRL1.SSMEN=0.

Input mode: The NSS output of the master device is disabled (SPI_CTRL1.MSEL=1, SPI_CTRL2.SSOEN=0), allowing operation in multi-master mode. The master should connect NSS pin to the high level and the slave should connect NSS pin to the low level during the entire data frame transfer.

Output mode: The NSS output of the master device is enable (SPI_CTRL1.MSEL=1, SPI_CTRL2.SSOEN=1). SPI as the master device must pull the NSS pin to low level, and all device which connected to the master device and set to NSS hardware mode, will detect low level and enter the slave mode automatically. If the master device cannot pull the NSS pin to low level, device will enter the slave mode and generates the master mode failure error.

Note: the choice of software mode or hardware mode depends on whether NSS control is needed in the communication protocol. If not, you can choose the software mode, and release a GPIO pin for other purposes.

Figure 16-2 Slave Selects Management of Hardware/Software



The following figure is an example of the interconnection of single master and single slave devices

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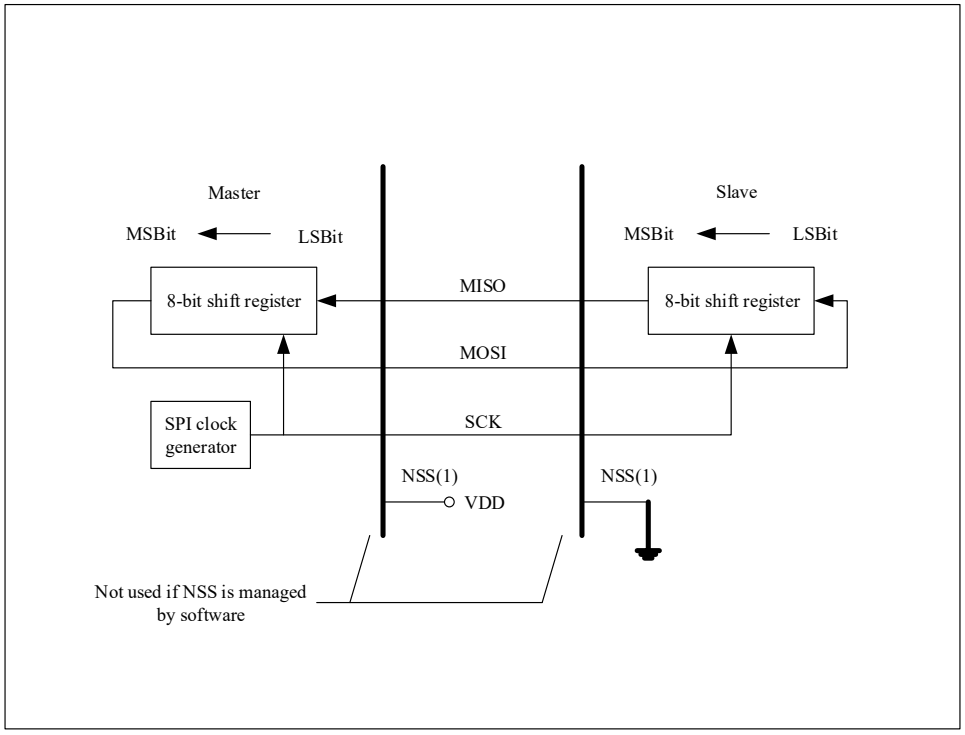
Figure 16-3 Master and Slave Applications



Note: NSS pin is set as input

SPI is a ring bus structure, and the master device outputs a synchronous clock signal through SCK pin, and the MOSI pin of master device is connected with the MOSI pin of slave device, and the MISO pin of master device is connected with the MISO pin of slave device. Serial transfer of data between master device and slave device, through MOSI pin to transmit data to slave device, through MISO pin transmit the highest bit of the shift register of the slave device to lowest bit of the shift register of the master device. When the second bit of data is transmitted, the lowest bit data of the shift register of the slave device will be shifted to the left by one bit and the data of the new highest bit int the shift register will be sent to the master device by MISO pin, and the lowest bit data of the shift register of the master device will be shifted to the left by one bit and the new data that the master device has been received will be stored in the lowest bit of the shift register.

16.3.1.3 SPI timing mode

User can selects the clock edge of data capture by setting SPI_CTRL1.CLKPOL bit and SPI_CTRL1.CLKPHA bit.

- When CLKPOL = 0, CLKPHA = 0, the SCK pin will keep low in idle state, and the data will be sampled at the first edge, which is rising edge.
- When CLKPOL = 0, CLKPHA = 1, the SCK pin will keep low in idle state, and the data will be sampled at the second edge, which is falling edge.
- When CLKPOL = 1, CLKPHA = 0, the SCK pin will keep high in idle state, and the data will be sampled at the first edge, which is falling edge.
- When CLKPOL = 1, CLKPHA = 1, the SCK pin will keep high in idle state, and the data will be sampled at the second edge, which is rising edge.

Regardless of the timing mode used, the master and slave configuration must be the same.

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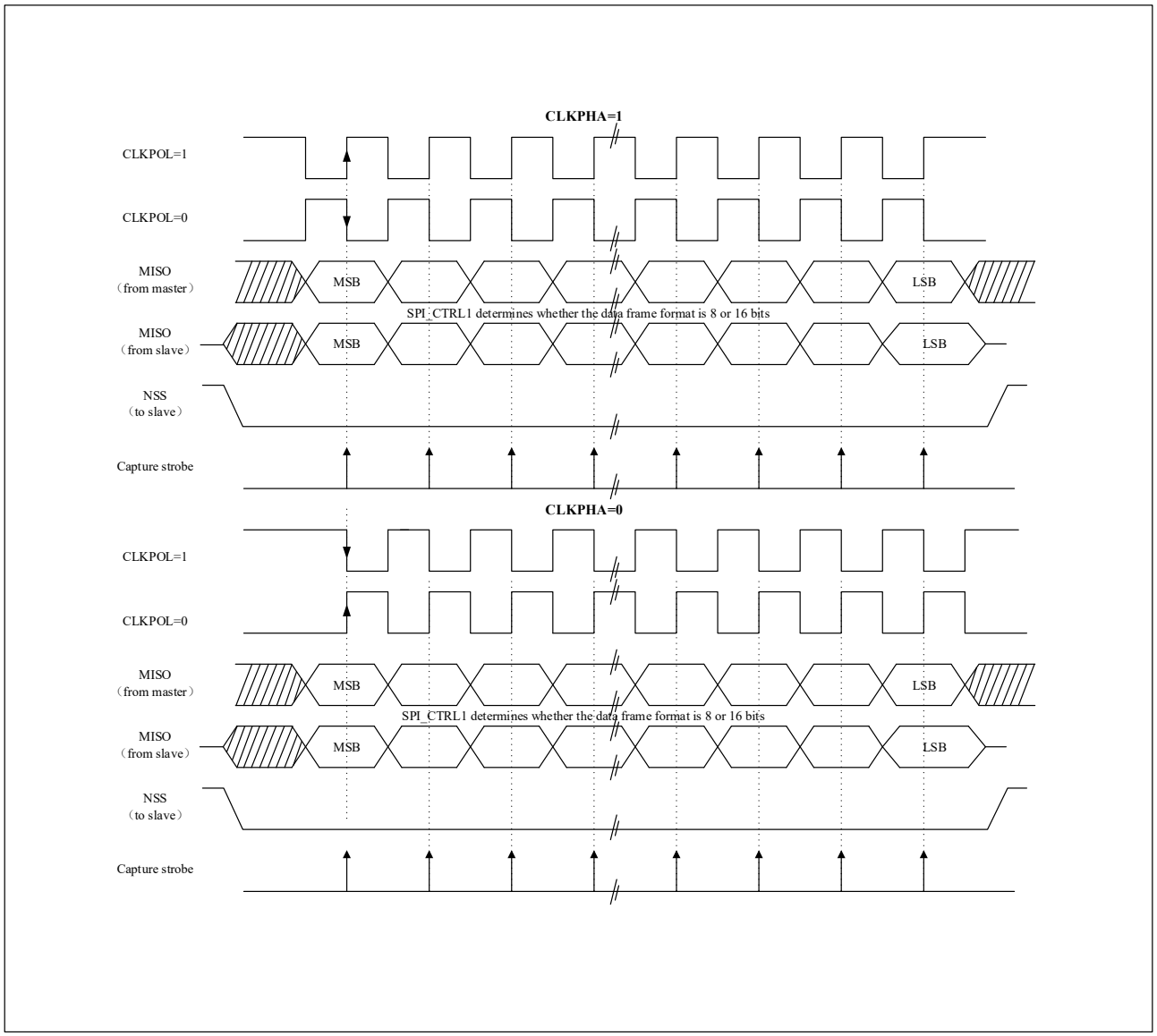
Figure 16-4 is the timing of 4 combinations of CLKPHA and CLKPOL bits in SPI transmission when the SPI_CTRL1.LSBFF=0.

Figure 16-4 Data Clock Timing Diagram



16.3.1.4 Data format

User can selects the data bit order by setting the SPI_CTRL1.LSBFF bit. When SPI_CTRL1.LSBFF = 0, SPI will transmit the most significant bit (MSB) first; When SPI_CTRL1.LSBFF = 1, SPI will transmit the less significant bit (LSB) first.

User can selects the data frame format by setting the SPI_CTRL1.DATFF bit. When SPI_CTRL1.DATFF = 0, SPI data frame length is 8-bit; When SPI_CTRL1.DATFF = 1, SPI data frame length is 16-bit.

16.3.2 SPI Operating Mode

16.3.2.1 Master full duplex mode

Master full duplex mode (SPI_CTRL1.MSEL=1 (master), SPI_CTRL1.BIDIRMODE=0 (two-wire unidirectional),

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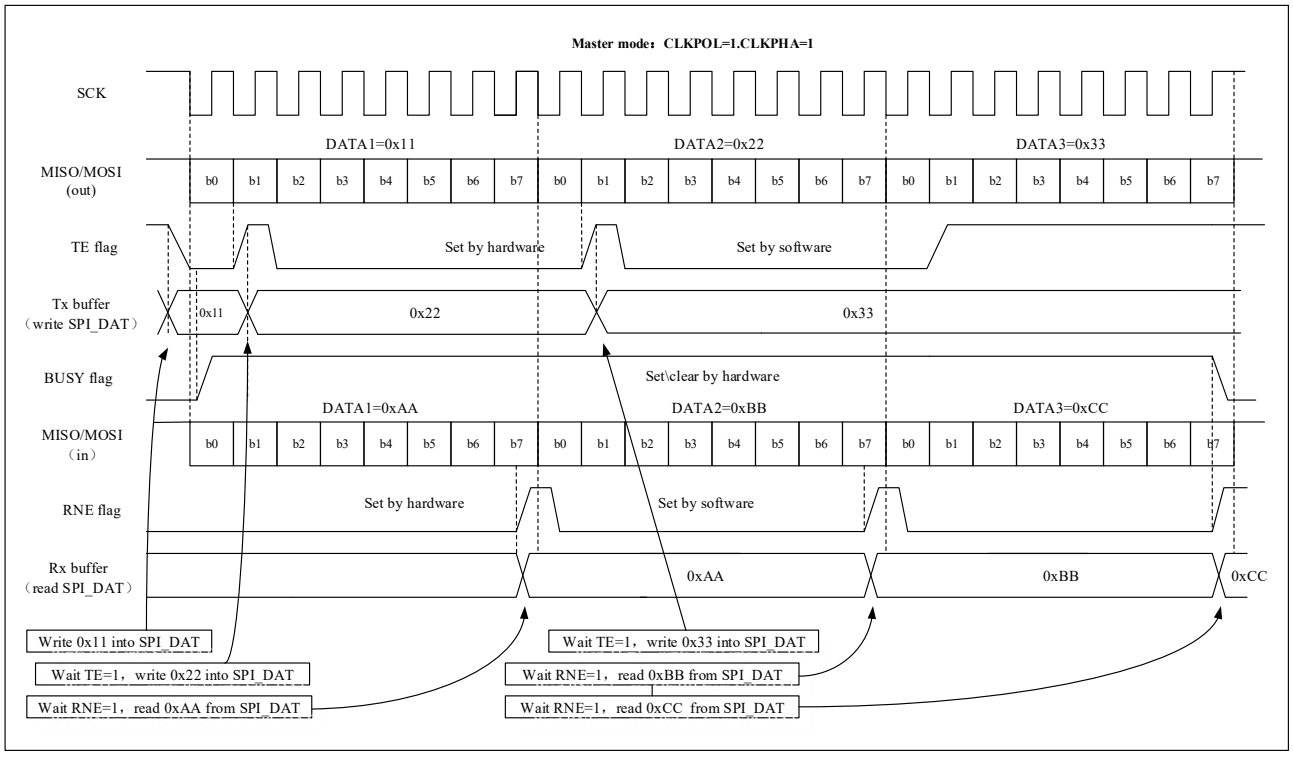
SPI_CTRL1.RONLY=0 (transmitting mode and receiving mode)). After the first data is written to the SPI_DAT register, the transmission will start. When the first bit of the data is sent, the data bytes are loaded from the data register into the shift register in parallel, and then according to the configuration of the SPI_CTRL1.LSBFF bit, the data bits follow the MSB or LSB order is serially shifted to the MOSI pin. At the same time, the data received on the MISO pin is serially shifted into the shift register in the same order and then loaded into the SPI_DAT register in parallel. The software operation process is as follows:

1. Enable SPI module by setting SPI_CTRL1.SPIEN = 1.
2. Write the first data to be sent into SPI_DAT register (this operation will clear SPI_STS.TE bit).
3. Wait for SPI_STS.TE bit to be set to '1', and write the second data to be transmitted into SPI_DAT. Wait for SPI_STS.RNE bit to be set to '1', read SPI_DAT to get the first received data, and the SPI_STS.RNE bit will be cleared by hardware while reading SPI_DAT. Repeat the above operation, sending subsequent data and receiving n-1 data at the same time;
4. Wait for SPI_STS.RNE bit to be set to '1' to receive the last data;
5. Wait for SPI_STS.TE to be set to '1', then wait for SPI_STS.BUSY bit to be cleared and turn off SPI module.

The process of data transmitting and data receiving can also be implemented in the interrupt handler generated by the rising edge of the SPI_STS.RNE or SPI_STS.TE flag.

Figure 16-5 Schematic Diagram of the Change of TE/RNE/BUSY when the Master is Continuously Transmitting in Full Duplex Mode



16.3.2.2 Master two-wire unidirectional transmit-only mode

Master two-wire unidirectional transmit-only mode (SPI_CTRL1.MSEL = 1(master), SPI_CTRL1.BIDIRMODE = 0(two-wire unidirectional), SPI_CTRL1.RONLY = 0(transmitting mode and receiving mode)). Master two-wire

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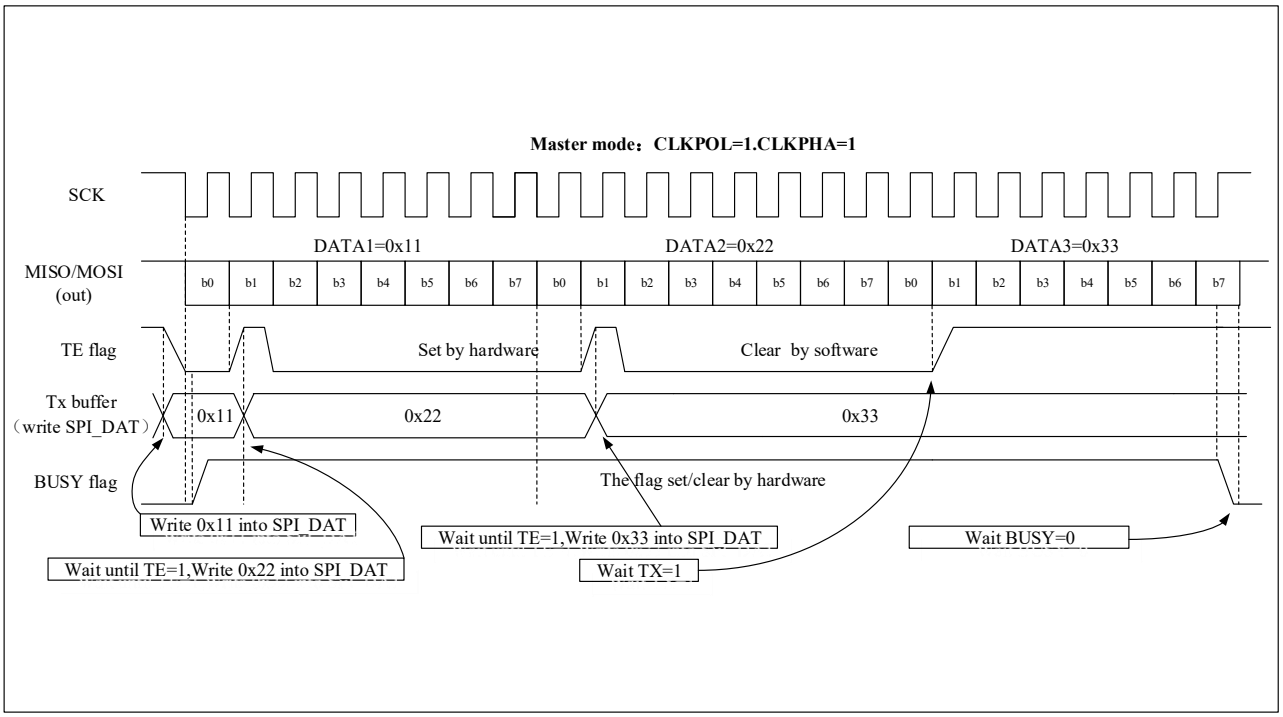
unidirectional send-only mode is similar to master full-duplex mode. The difference is that this mode will not read the received data, so the SPI_STS.OVER bit will be set to '1', and the software will ignore it. The software operation process is as follows:

1. Enable SPI module by setting SPI_CTRL1.SPIEN = 1.
2. Write the first data to be transmitted into SPI_DAT register (this operation will clear SPI_STS.TE bit).
3. Wait for SPI_STS.TE bit to be set to '1', and write the second data to be sent into SPI_DAT. Repeat this operation to send subsequent data;
4. After writing the last data to SPI_DAT, wait for SPI_STS.TE bit to set '1'; then wait for SPI_STS.BUSY bit to be cleared to complete the transmission of all data.

The process of data transmitting can also be implemented in the interrupt handler generated by the rising edge of the SPI_STS.TE flag.

Figure 16-6 Schematic Diagram of TE/BUSY Change when the Host Transmits Continuously in Unidirectional Only Mode



16.3.2.3 Master two-wire unidirectional receive-only mode

Master two-wire unidirectional receive-only mode (SPI_CTRL1.MSEL = 1(master), SPI_CTRL1.BIDIRMODE = 0(two-wire unidirectional), SPI_CTRL1.RONLY = 1(receive-only mode)). When SPI_CTRL1.SPIEN=1, the receiving process starts. The data bits from the MISO pin are sequentially shifted into the shift register and then loaded into the SPI_DAT register(receive buffer) in parallel. The software operation process is as follows:

1. Enable the receive-only mode (SPI_CTRL1.RONLY=1).
2. Enable SPI module by setting SPI_CTRL1.SPIEN=1:
   - In master mode, SCK clock signal is generated immediately, and serial data is continuously received before

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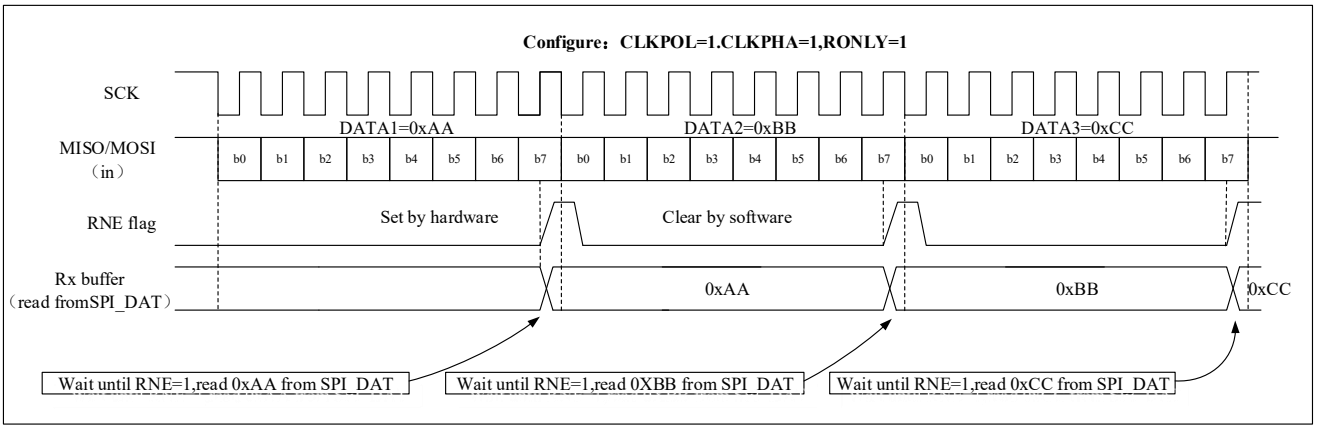
SPI is turned off(SPI_CTRL1.SPIEN=0);

- In slave mode, serial data is continuously received when the SPI master device pulls low the NSS signal and generates SCK clock.

3. Wait for SPI_STS.RNE bit to be set to '1', read the SPI_DAT register to get the received data, and the SPI_STS.RNE bit will be cleared by hardware while reading SPI_DAT register. Repeat this operation to receive all data.

The process of data receiving can also be implemented in the interrupt handler generated by the rising edge of the SPI_STS.RNE flag.

Figure 16-7 Schematic Diagram of RNE Change when Continuous Transmission Occurs in Receive-only Mode (BIDIRMODE=0 and RONLY=1)



16.3.2.4 Master one-wire bidirectional transmit mode

Master one-wire bidirectional transmit mode (SPI_CTRL1.MSEL = 1(master), SPI_CTRL1.BIDIRMODE = 1(one-wire bidirectional), SPI_CTRL1.BIDIROEN = 1(transmit-only mode), SPI_CTRL1.RONLY = 0(transmitting mode and receiving mode)). After the data is written to the SPI_DAT register (transmit buffer), the transmission process starts. This mode does not receive data. At the same time as the first data bit is transmitted, the data to be transmitted is loaded into the 8-bit shift register in parallel, and then according to the configuration of the SPI_CTRL1.LSBFF bit, the SPI serially shifts the data bits to the MOSI pin in MSB or LSB order.

The software operation flow of the master one-wire bidirectional send mode is the same as that of the send-only mode.

16.3.2.5 Master one-wire bidirectional receive mode

Master one-wire bidirectional receive mode (SPI_CTRL1.MSEL = 1(master), SPI_CTRL1.BIDIRMODE = 1(one-wire bidirectional), SPI_CTRL1.BIDIROEN = 0(receive-only mode), SPI_CTRL1.RONLY = 0(transmitting mode and receiving mode)). When SPI_CTRL1.SPIEN=1 , the receiving process starts. There is no data output in this mode, the received data bits are sequentially and serially shifted into the shift register, and then loaded into the SPI_DAT register (receive buffer) in parallel

The software operation flow of the master one-wire bidirectional receive mode is the same as that of the receive-only mode.

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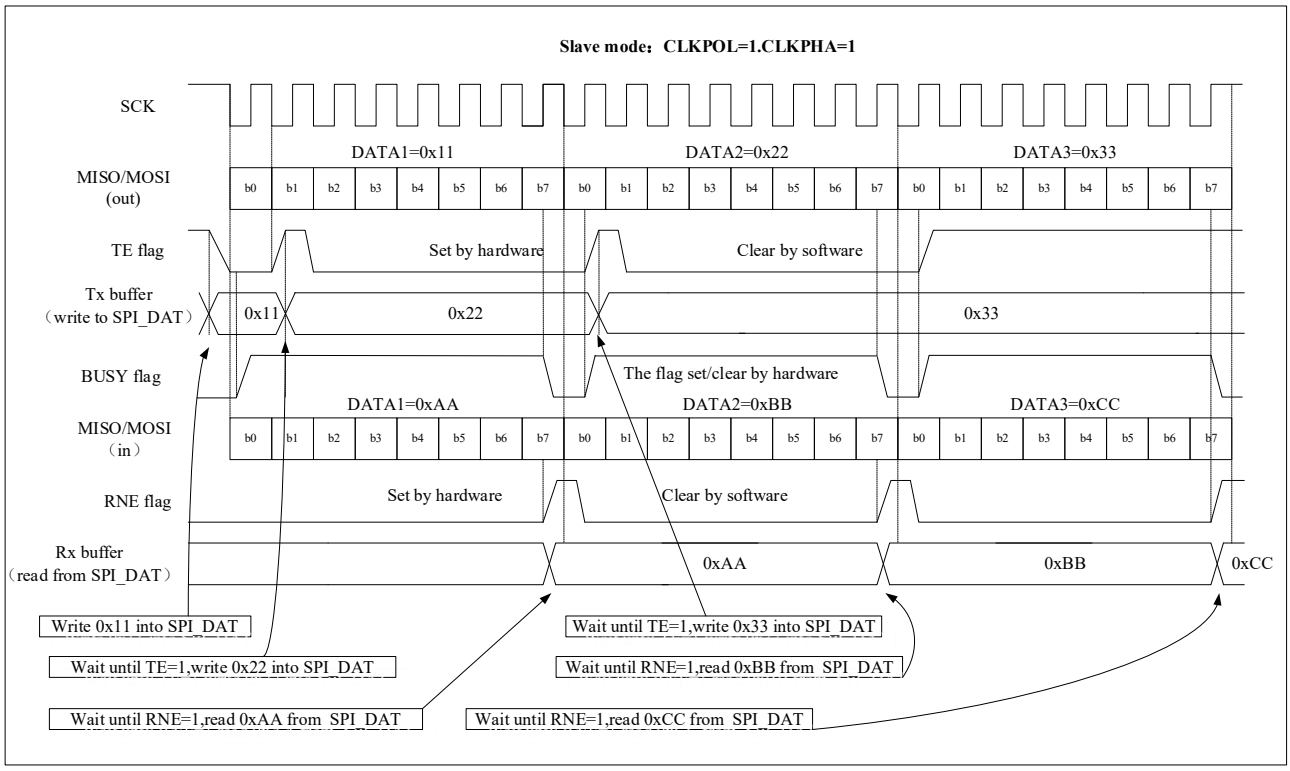
16.3.2.6 Slave full duplex mode

Slave full duplex mode (SPI_CTRL1.MSEL = 0(slave), SPI_CTRL1.BIDIRMODE = 0(two-wire unidirectional) and SPI_CTRL1.RONLY = 0(transmitting mode and receiving mode)). The data transfer process begins when the slave device receives the first clock edge. Before the master starts data transfer, software must ensure that the data to be transmitted is written to the SPI_DAT register.

Figure 16-8 Schematic Diagram of the Change of TE/RNE/BUSY when the Slave is Continuously Transmitting in Full Duplex Mode



16.3.2.7 Slave two-wire unidirectional transmit-only mode

Slave two-wire unidirectional transmit-only mode (SPI_CTRL1.MSEL = 0(slave), SPI_CTRL1.BIDIRMODE = 0(two-wire unidirectional) and SPI_CTRL1.RONLY = 0(transmitting mode and receiving mode)).

Figure 16-9 Schematic Diagram of TE/BUSY Change During Continuous Transmission in Slave Unidirectional

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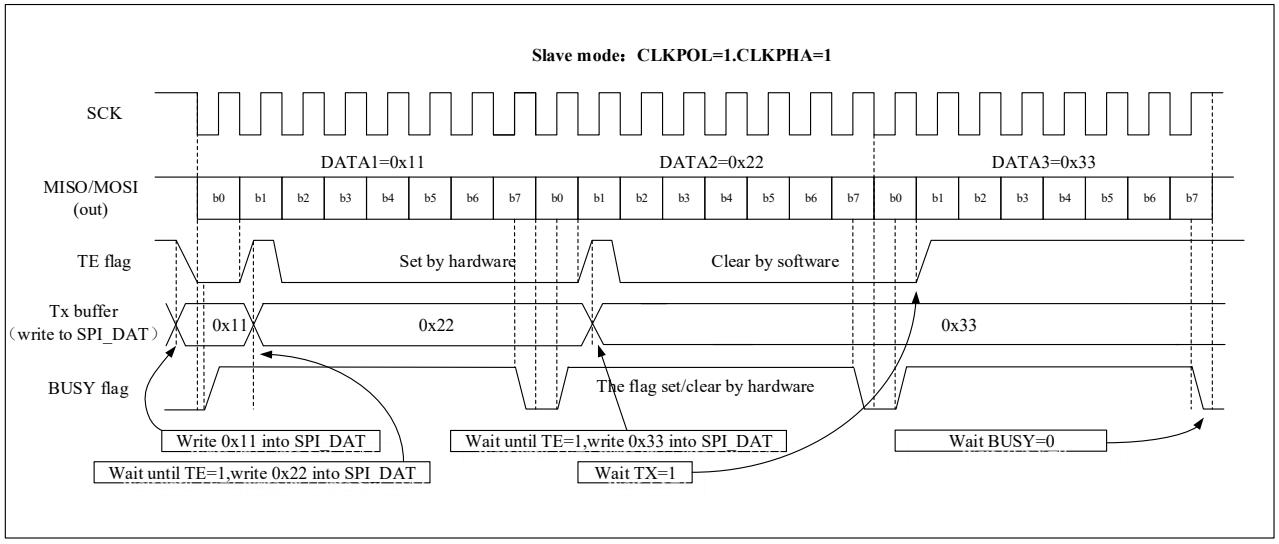
Transmit-only Mode



16.3.2.8 Slave two-wire unidirectional receive-only mode

Slave two-wire unidirectional receive-only mode (SPI_CTRL1.MSEL = 0(slave), SPI_CTRL1.BIDIRMODE = 0(two-wire unidirectional) and SPI_CTRL1.RONLY = 1(receive-only mode)).The data receiving process begins when the slave device receives the clock signal and the first data bit from the MOSI pin. The received data bits are sequentially and consecutively shifted serially into the shift register and then loaded into the SPI_DAT register (receive buffer) in parallel.

16.3.2.9 Slave one-wire bidirectional send mode

Slave one-wire bidirectional transmit mode (SPI_CTRL1.MSEL = 0(slave), SPI_CTRL1.BIDIRMODE = 1(one-wire bidirectional) and SPI_CTRL1.BIDIROEN = 1(send-only mode)). When the slave device receives the first edge of the clock signal, the sending process starts. No data is received in this mode, and the software must ensure that the data to be transmitted has been written in the SPI_DAT register before the SPI master device starts data transmission.

16.3.2.10 Slave one-wire bidirectional receive mode

Slave one-wire bidirectional receive mode (SPI_CTRL1.MSEL = 0(slave), SPI_CTRL1.BIDIRMODE = 1(one-wire bidirectional) and SPI_CTRL1.BIDIROEN = 0(receive-only mode)). Data receiving begins when the slave device receives the first clock edge and a data bit from the MISO pin. There is no data output in this mode, the received data bits are sequentially and consecutively shifted serially into the shift register, and then loaded into the SPI_DAT register (receive buffer) in parallel.

Note: The software operation process of the slave can refer to the master.

16.3.2.11 SPI initialization process

1. The baud rate of serial clock is defined by the SPI_CTRL1.BR[2:0] bits (this step is ignored if it is operating in slave mode).
2. Select SPI_CTRL1.CLKPOL bit and SPI_CTRL1.CLKPHA bit to define the phase relationship between data transmission and serial clock.

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3. Set SPI_CTRL1.DATFF bit to define 8-bit or 16-bit data frame format.
4. Configure SPI_CTRL1.LSBFF bit to define whether the sequence of transmitting data bits is LSB or MSB.
5. Configure the NSS mode.
6. Configured SPI_CTRL1.MSEL bit, SPI_CTRL1.BIDIRMODE bit, SPI_CTRL1.BIDIROEN bit and SPI_CTRL1.RONLY bit to define run mode.
7. Set the SPI_CTRL1.SPIEN=1 to enable SPI.

16.3.2.12 Basic transmit and receive process

When SPI transmits a data frame, it firstly loads the data frame from the Tx buffer into the shift register, and then starts to transmit the loaded data. When the data is transferred from the Tx buffer to the shift register, the Tx buffer empty flag is set (SPI_STS.TE=1), and the next data can be loaded into the Tx buffer; if the SPI_CTRL2.TEINTEN bit is set, an interrupt will be generated; writing data to the SPI_DAT register will clear the SPI_STS.TE bit.

At the last edge of the sampling clock, when the data is transferred from the shift register to the Rx buffer, the Rx buffer non-empty flag is set (SPI_STS.RNE=1); at this time the data is ready and can be read from the SPI_DAT register; if the Rx buffer non-empty interrupt is enabled (SPI_CTRL2.RNEINTEN=1), an interrupt will be generated; the SPI_STS.RNE bit can be cleared by reading the SPI_DAT register data.

In master mode, the transmitting process starts when data is written to the Tx buffer. If the next data has been written into the SPI_DAT register before the current data frame transmitting is completed, the continuous transmitting function can be achieved.

In slave mode, the NSS pin level is low, and the transmitting process starts when the first edge of the clock signal comes. To avoid accidental data transfers, software must write data to the Tx buffer before the data transmitting (it is recommended to enable the SPI slave before the master sends the clock).

In some configurations, when the last data is sent, the SPI_STS.BUSY flag can be used to wait for the end of the data transmitting.

16.3.2.12.1 Continuous and discontinuous transmission

When transmitting data in master mode, if the software is fast enough to detect each SPI_STS.TE rising edge (or TE interrupt), and the data is written to the SPI_DAT register immediately before the end of the ongoing transmission. At this time, the SPI clock remains continuous between the transmission of data items, and the SPI_STS.BUSY bit will not be cleared, continuous communication can be achieved.

If the software is not fast enough, it will result in discontinuous communication; in this case, the SPI_STS.BUSY bit is cleared between the transmission of each data items(refer to Figure 16-10).

In master receive-only mode (SPI_CTRL1.RONLY=1), communication is always continuous and the SPI_STS.BUSY flag is always high.

In slave mode, the continuity of communication is determined by the SPI master device. However, even if the communication is continuous, the SPI_STS.BUSY flag will be low for at least one SPI clock cycle between each data item (refer to Figure 16-9).

Figure 16-10 Schematic Diagram of TE/BUSY Change when BIDIRMODE = 0 and RONLY = 0 are Transmitted

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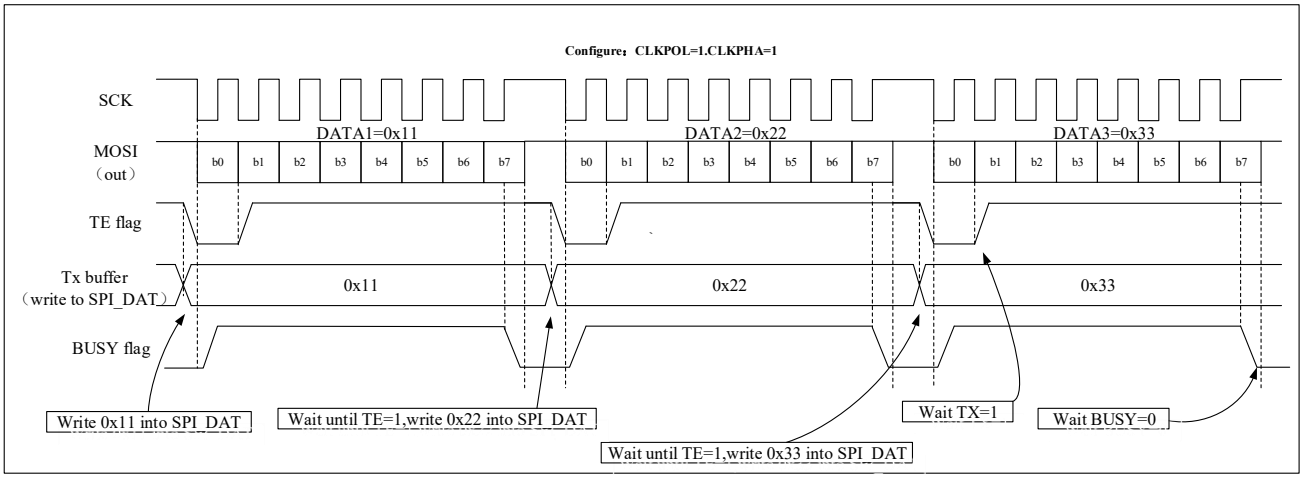
Discontinuously



16.3.3 Status Flag

The SPI_STS register has 3 flag bits to monitor the status of the SPI:

16.3.3.1 Send buffer empty flag bit (TE)

When the Tx buffer is empty, the SPI_STS.TE flag is set to 1, which means that new data can be written into the SPI_DAT register. When the Tx buffer is not empty, the hardware will clear this flag to 0.

16.3.3.2 Receive buffer non-empty flag bit (RNE)

When the Rx buffer is not empty, the SPI_STS.RNE flag is set to 1, so the user knows that there is data in the Rx buffer. After reading the SPI_DAT register, the hardware will clear this flag to 0.

16.3.3.3 BUSY flag bit (BUSY)

When the transmission starts, the hardware sets the SPI_STS.BUSY flag to 1, and after the transmission ends, the hardware clears the SPI_STS.BUSY flag to 0.

Only when the device is in the master one-wire bidirectional receive mode, the SPI_STS.BUSY flag will be set to 0 when the communication is on going.

The SPI_STS.BUSY flag will be cleared to 0 in the following cases:

- End of transmission (except for continuous communication in master mode);
- Turn off the SPI module (SPI_CTRL1.SPIEN=0);
- The master mode error occurs (SPI_STS.MODERR=1)

When the communication is discontinuous: the SPI_STS.BUSY flag is cleared to '0' between the transmission of each data item.

When communication is continuous: in master mode, the SPI_STS.BUSY flag remains high during the entire transfer process; in slave mode, the SPI_STS.BUSY flag will be low for 1 SPI clock cycle between each data item transfer. So do not use the SPI_STS.BUSY flag to handle the transmitting and receiving of each data item.

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16.3.4 Turn Off the SPI

In order to turn off the SPI module, different operation modes require different operation steps:

16.3.4.1 Master or slave full duplex mode

1. Wait for the SPI_STS.RNE flag to be set to 1 and the last byte to be received;
2. Wait for the SPI_STS.TE flag to be set to 1;
3. Wait for the SPI_STS.BUSY flag to be cleared to 0;
4. Turn off the SPI module (SPI_CTRL1.SPIEN=0).

16.3.4.2 One-wire transmit-only mode or bidirectional transmit mode for master or slave

1. After writing the last byte to the SPI_DAT register, wait for the SPI_STS.TE flag to be set to 1;
2. Wait for the SPI_STS.BUSY flag to be cleared to 0;
3. Turn off the SPI module (SPI_CTRL1.SPIEN=0).

16.3.4.3 One-wire receive-only mode or bidirectional receive mode for master

1. Wait for the last second SPI_STS.RNE to be set to 1;
2. Before closing the SPI module (SPI_CTRL1.SPIEN=0), wait for 1 SPI clock cycle (using software delay);
3. Wait for the last SPI_STS.RNE to be set before entering shutdown mode (or turning off the SPI module clock).

16.3.4.4 Unidirectional receive-only mode or bidirectional receive mode for slave

1. The SPI module can be turned off at any time (SPI_CTRL1.SPIEN=0), and after the current transfer is completed, the SPI module will be turned off;
2. If you want to enter the shutdown mode, you must wait for the SPI_STS.BUSY flag to be set to 0 before entering the shutdown mode (or turn off the SPI module clock).

16.3.5 Error Flag

16.3.5.1 Master mode failure error (MODERR)

The following two conditions will cause the master mode failure error:

- NSS pin hardware management mode, the master device NSS pin is pulled low;
- NSS pin software management mode, the SPI_CTRL1.SSEL bit is set to 0.

When a master mode failure error occurs, the SPI_STS.MODERR bit is set to 1. An interrupt is generated if the user enables the corresponding interrupt (SPI_CTRL2.ERRINTEN=1). The SPI_CTRL1.SPIEN bit and SPI_CTRL1.MSEL bit will be write protected and both are cleared by hardware. SPI is turned off and forced into slave mode.

Software performs a read or write operation to the SPI_STS register, and then writes to the SPI_CTRL1 register to clear the SPI_STS.MODERR bit (in multi-master mode, the master's NSS pin must be pulled high first).

Normally, the SPI_STS.MODERR bit of the slave cannot be set to 1. However, in a multi-master configuration, the slave's SPI_STS.MODERR bit may be set to 1. In this case, the SPI_STS.MODERR bit indicates that there is a multi-master collision. The interrupt routine can perform a reset or return to the default state to recover from an error state.

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16.3.5.2 Overflow error (OVER)

When the SPI_STS.RNE bit is set to 1, but there is still data sent into the Rx buffer, an overflow error will occur. At this time, the overflow flag SPI_STS.OVER bit is set to 1. An interrupt is generated if the user enables the corresponding interrupt (SPI_CTRL2.ERRINTEN=1). All received data is lost, and the SPI_DAT register retains only previously unread data.

Read the SPI_DAT register and the SPI_STS register in turn to clear the SPI_STS.OVER bit.

16.3.6 SPI Interrupt

Table 16-1 SPI Interrupt Request

Interrupt Event	Event Flag Bit	Enable Control Bit
Send buffer empty flag	TE	TEINTEN
Receive buffer non empty flag	RNE	RNEINTEN
Master mode failure event	MODERR	ERRINTEN
Overflow error	OVER	

16.4 SPI Register

16.4.1 SPI Register Overview

Table 16-2 SPI Register Overview

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
000h	SPI_CTRL1	Reserved																BIDIRMODE	BIDIROEN	Reserved		DATFF	RONLY	SSMEN	SSEL	LSBFF	SPIEN	BR[2:0]			MSEL	CLKPOL	CLKPHA
	Reset Value																	0	0			0	0	0	0	0	0	0	0	0	0	0	0
004h	SPI_CTRL2	Reserved																								TEINTEN	RNEINTEN	ERRINTEN	Reserved		SSOEN	Reserved	
	Reset Value																									0	0	0			0		
008h	SPI_STS	Reserved																								BUSY	OVER	MODERR	Reserved			TE	RNE
	Reset Value																									0	0	0				1	0
00Ch	SPI_DAT	Reserved																DAT[15:0]															
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

16.4.2 SPI Control Register 1 (SPI_CTRL1)

Address: 0x00

Reset value: 0x0000

15	14	13 12	11	10	9	8	7	6	5 3	2	1	0
BIDIR MODE	BIDIR OEN	Reserved	DATFF	RONLY	SSMEN	SSEL	LSBFF	SPIEN	BR[2:0]	MSEL	CLKPOL	CLKPHA
rw	rw		rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Bit Field	Name	Description
15	BIDIRMODE	Bidirectional data mode enable 0: Select the "two-wire unidirectional" mode.

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Bit Field	Name	Description
		1: Select the "one-wire bidirectional" mode.
14	BIDIROEN	Output enable in bidirectional mode 0: Output disable (receive-only mode). 1: Output enabled (transmit-only mode). In master mode, the "one-wire" data line is the MOSI pin, and in slave mode, the "one-wire" data line is the MISO pin.
13:12	Reserved	Reserved, the reset value must be maintained.
11	DATFF	Data frame format 0: 8-bit data frame format is used for transmitting/receiving. 1: 16-bit data frame format is used for transmitting/receiving. *Note: this bit can only be written when SPI is disabled (SPI_CTRL1.SPIEN=0), otherwise an error will occur.*
10	RONLY	Only receive mode This bit, together with the SPI_CTRL1.BIDIRMODE bit, determines the transfer direction in two-wire unidirectional mode. In the application scenario of multiple slave devices, this bit is only set to 1 by the accessed slave device, and only the accessed slave device can output, so as to avoid data line conflicts. 0: Full duplex (transmitting mode and receiving mode). 1: Disable output (receive-only mode).
9	SSMEN	Software slave device management When the SPI_CTRL1.SSMEN bit is set to 1, the NSS pin level is determined by the value of the SPI_CTRL1.SSEL bit. 0: Disable software slave device management. 1: Enable software slave device management.
8	SSEL	Internal slave device selection This bit only has meaning when the SPI_CTRL1.SSMEN bit is set. It determines the NSS level, and I/O operations on the NSS pin have no effect.
7	LSBFF	Frame format 0: Send MSB first. 1: Send LSB first. *Note: this bit cannot be changed during communication.*
6	SPIEN	SPI enable 0: Disable SPI device. 1: Enable SPI device. *Note: when turning off the SPI device, please follow Section 16.3.4 Section's procedure operation.*
5:3	BR[2:0]	Baud rate control 000: fPCLK/2 001: fPCLK/4 010: fPCLK/8 011: fPCLK/16 100: fPCLK/32

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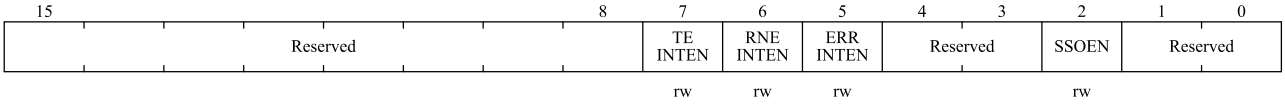
Bit Field	Name	Description
		101: fPCLK/64 110: fPCLK/128 111: fPCLK/256 *Note: this bit cannot be changed during communication.*
2	MSEL	Master device selection 0: Configure as the slave device. 1: Configure as the master device. *Note: this bit cannot be changed during communication.*
1	CLKPOL	Clock polarity 0: In idle state, SCK remains low. 1: In idle state, SCK remains high. *Note: this bit cannot be changed during communication.*
0	CLKPHA	Clock phase 0: Data is sampled on the first clock edge. 1: Data is sampled on the second clock edge. *Note: this bit cannot be changed during communication.*

16.4.3 SPI Control Register 2 (SPI_CTRL2)

Address: 0x04

Reset value: 0x0000



Bit Field	Name	Description
15:8	Reserved	Reserved, the reset value must be maintained.
7	TEINTEN	Tx buffer empty interrupt enable 0: Disable TE interrupt. 1: Enable TE interrupt, and interrupt request is generated when SPI_STS.TE flag is set to '1'.
6	RNEINTEN	Rx buffer non-empty interrupt enable 0: Disable RNE interrupt. 1: Enable RNE interrupt, and generate interrupt request when SPI_STS.RNE flag is set to ‘1’.
5	ERRINTEN	Error interrupt enable When an error (SPI_STS.OVER, SPI_STS.MODERR) is generated, this bit controls whether an interrupt is generated 0: Disable error interrupt. 1: Enable error interrupt.
4:3	Reserved	Reserved, the reset value must be maintained.
2	SSOEN	NSS output enable 0: Disable NSS output in master mode, the device can work in multi-master mode. 1: Enable NSS output in the master mode. The device cannot work in the multi-master device mode.

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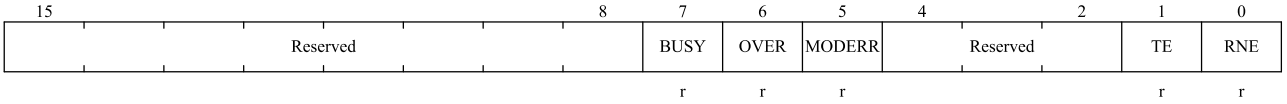
Bit Field	Name	Description
1:0	Reserved	Reserved, the reset value must be maintained.

16.4.4 SPI Status Register (SPI_STS)

Address: 0x08

Reset value: 0x0002

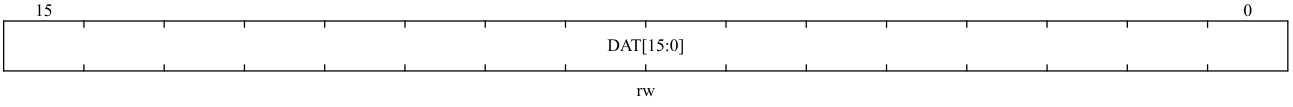


Bit Field	Name	Description
15:8	Reserved	Reserved, the reset value must be maintained.
7	BUSY	Busy flag 0: SPI is not busy. 1: SPI is busy with communication, or the Tx buffer is not empty. This bit is set or reset by hardware. *Note: special attention should be paid to the use of this sign,* refer to *Section 16.3.3 and Section 16.3.4 for details..*
6	OVER	Overflow flag 0: No overflow error. 1: An overflow error occurred. *Note:this bit is set by hardware and cleared according to the sequence of software operations. For more information about software sequences, refer to Section 16.3.5 for details.*
5	MODERR	Mode error 0: No mode error. 1: A mode error occurred. *Note: this bit is set by hardware and cleared according to the sequence of software operations. For more information about software sequences, refer to Section 16.3.5 for details.*
4:2	Reserved	Reserved, the reset value must be maintained.
1	TE	The Tx buffer is empty 0: The send buffer is not empty. 1: The send buffer is empty.
0	RNE	The Rx buffer is not empty 0: The receive buffer is empty. 1: The receive buffer is not empty.

16.4.5 SPI Data Register (SPI_DAT)

Address: 0x0C

Reset value: 0x0000



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Bit Field	name	Description
15:0	DAT[15:0]	Data register Data to be transmitted or received The data register corresponds to two buffers: one for write (Tx buffer); The other is for read (Rx buffer).Write operation writes data to Tx buffer; The read operation will return the data in the Rx buffer. *Note on SPI mode: according to the selection of the data frame format by the SPI_CTRL1.DATFF bit, the data sending and receiving can be 8-bit or 16-bit. To ensure correct operation, the data frame format needs to be determined before enabling the SPI.* **For 8-bit data frame format:** the buffer is 8-bit, and only SPI_DAT[7:0] is used when transmitting and receiving. When receiving, SPI_DAT[15:8] is forced to 0. **For 16-bit data frame format:** the buffer is 16-bit, and the entire data register is used when transmitting and receiving, that is, SPI_DAT[15:0].

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17 Beeper

17.1 Introduction

The Beeper module supports complementary outputs and can generate periodic signals to drive external passive Beeper, and can be used to generate a prompt tone or an alarm sound.

17.2 Function Description

Beeper as an independent module, is mounted on the APB bus, and its operating clock source is LSI.

- Single or dual outputs can be configured
- Supports two complementary outputs
- Output frequency can be configured: 1kHz, 2kHz, 4kHz, 8kHz

17.3 Beeper Registers

These peripheral registers must be operated in word (32-bit) mode.

17.3.1 Beeper Register Overview

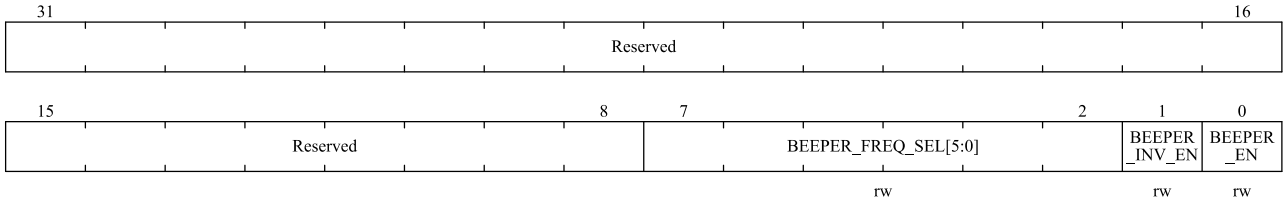
Table 17-1 Beeper Register Overview

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
000h	BEEPER_CTRL	Reserved																									BEEPER_FREQ_SEL[5:0]					BEEPER_INV_EN	BEEPER_EN
	Reset Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

17.3.2 Beeper Control Register (BEEPER_CTRL)

Address offset: 0x00

Reset value: 0x0000 0000



Bit Field	Name	Description
31:8	Reserved	Reserved, the reset value must be maintained.
7:2	BEEPER_FREQ_SEL[5:0]	Beeper output frequency selection: 000001: 8kHz 000011: 4kHz

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Bit Field	Name	Description
		000111: 2kHz 001111: 1kHz Others: reserved
1	BEEPER_INV_EN	Beeper complementary output enable 0: Only one output, the other output is off. 1: Two outputs are turned on and the outputs are complementary
0	BEEPER_EN	Beeper enable 0: Beeper disable(*Note: after BEEPER_EN=0, the Beeper output can be turned off immediately by disabling the RCC_APBPCLKEN.BEEPEREN*) 1: Beeper enable

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18 Debug Support (DBG)

18.1 Overview

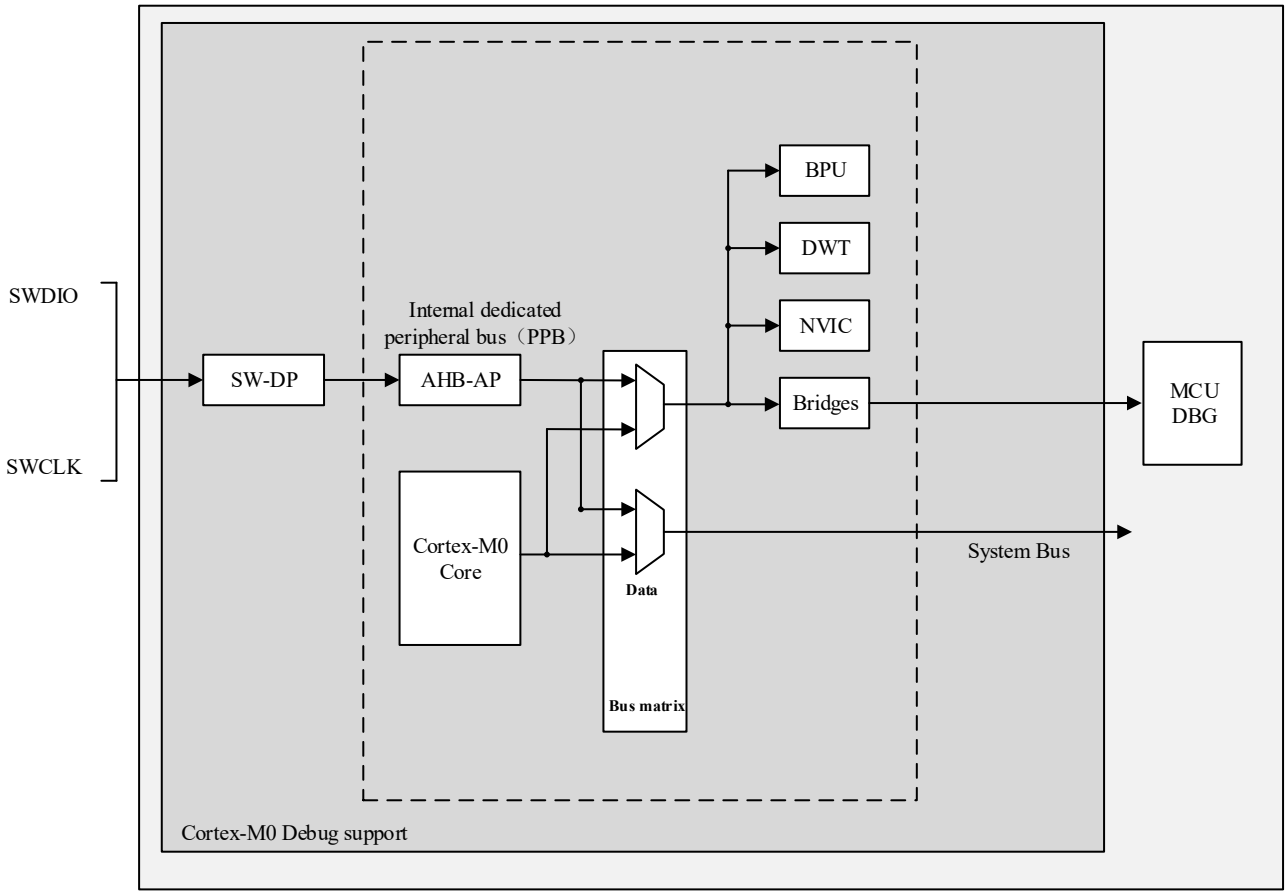
N32G003 uses Cortex®-M0 core, which integrates hardware debugging module supporting instruction breakpoint (stop when instruction fetches value) and data breakpoint (stop when data access). When the core is stopped, the user can view the internal state of the core and the external state of the system. After the user's query operation is completed, the core and peripherals can be restored, and the corresponding program can continue to be executed.

The hardware debugging module of the N32G003 core can be used when it is connected to the debugger (when it is not disabled).

N32G003 supports the following debugging interfaces:

- Serial wire interface

Figure 18-1 N32G003 Level and Cortex®-M0 Level Debugging Block Diagram



ARM Cortex®-M0 core hardware debugging module can provide the following debugging functions:

- SW-DP: Serial wire debugging port
- AHB-AP: AHB access port
- BPU: Break point unit

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- DWT: Data watchpoint trigger

Reference:

- Cortex®-M0 Technical Reference Manual (TRM)
- ARM debug interface V5 structure specification
- ARM CoreSight development tool set (r1p0 version) technical reference manual

18.2 SWD Function

The debugging tool can call the debugging function through the above-mentioned SWD debugging interface.

18.2.1 Pin Assignment

SWD (serial debug) interface consists of two pins: SWCLK (clock pin) and SWDIO (data input and output pin).

The pin assignment of SWD debug interface is shown in the following table:

Table 25-1 Debug Port Pin

Debug Port	Pin Assignment
SWDIO	PA8
SWCLK	PA9

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19 Unique device serial number (UID)

19.1 Introduction

MCU series products have two built-in unique device serial numbers with different lengths, namely 96-bit UID (Unique device ID) and 128-bit UCID (Unique Customer ID). These two device serial numbers are stored in the system configuration block of the Flash memory, and the information is programmed during manufacture, and any MCU microcontroller is guaranteed to be unique under any circumstances. It can be read by user applications or external devices through CPU or SWD interface and cannot be modified.

UID is 96 bits, which is usually used as serial number or password. When writing Flash memory, this unique identifier is combined with software encryption and decryption algorithm to further improve the security of code in Flash memory.

UCID is 128 bits and complies with the definition of the Nsing Technologies chip serial number. It contains information about chip production and version.

In addition to the above two device serial numbers, there is also a 32-bit DBGMCU_ID, which contains the chip version number, chip model, and Flash/SRAM capacity information.

19.2 UID Register

Start address: 0x1FFF_F4FC, 96 bits in length.

19.3 UCID Register

Start address: 0x1FFF_F4D0, 128 bits in length.

19.4 DBGMCU_ID Register

Start address: 0x1FFF_F508, 32 bits in length.

For different bytes, the low byte comes first and the high byte follows; for the same byte, the high bit comes first and the low bit follows.

Table 19-1 DBGMCU_ID Bit Description

Description	Size	Remark
Chip version number	4bit	The lower 4 bits of the chip version number.
	4bit	The upper 4 bits of the chip version number.
Chip model	4bit	The upper 4 bits of the chip model. The chip model is composed of 12 bits, divided to high, middle and low bits.
	4bit	The middle 4 bits of the chip model.
	4bit	The lower 4 bits of the chip model.
Flash capacity	4bit	Flash capacity indicator. In unit of 2KB, FLASH size = N * 2KB

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		Note: 0x8 indicates capacity16KB; 0xF indicates capacity 29.5KB
SRAM capacity	4bit	SRAM capacity indicator. In unit of 1KB, SRAM size = N * 1KB
Reserved	4bit	Keep it all 1.

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20 Version History

Version	Date	Changes
V1.0	2022.10.10	Initial release
V1.1.0	2023.07.07	1. Section 5.2.5.4.2: PA9 adds UART2_RX multiplexing function 2. Section 2.2.1.6: the option byte adds USER3[6] LVR reset enable bit and the corresponding FLASH_USER register read-only bit 3. Table 2-5: modify SWD access rights for L1 level 4. Table 19-1: modify Flash capacity note

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