N32G031x Series Errata Sheet

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1 Errata List

Table 1-1 Overview Of Errata

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			B
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Ch 3: Reset and Clock Control (RCC)	3.1: When running the program, the LSI has deviation		●
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Ch 7: I2C Interface	7.1: Handling Software events before current byte transferring		●
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	10.3: RTC calendar function cannot be initialized multiple times within 1 second		●
	10.4: RTC mistakenly triggers TISOVF flag bit		●
	10.5: RTC_DATA register lock		●

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2 Power Control (PWR)

2.1 Power On After Power Off

Description:

When the power supply voltage drops to around 1.6V (not completely power down) and then returns to the normal operating voltage, there may be a possibility of unsuccessful power-up.

Workaround:

When the MCU is powered off, it is necessary to ensure that the chip's VDD voltage drops to below 100mV, and then powered on to the normal operating voltage.

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3 Reset and Clock Control (RCC)

3.1 When Running The Program, The LSI Has Deviation

Description:

When running the program, the LSI has high jitter, the average frequency (1S time) is 30K±1KHz, and the instantaneous frequency is 20K~45KHz.

Workaround:

For precise timing, it is recommended that customers use LSE instead of LSI.

3.2 LSE Is Affected By Toggling Of Adjacent Pins

Description:

LSE is affected by toggling of adjacent pins.

Workaround:

Avoid toggling of adjacent pins of LSE

3.3 HSE Instability Causes Chips to Run Off

Description:

When HSE is enabled, running the code directly after the HSE Ready flag is set, then the system program may run away due to the unstable HSE clock.

Workaround:

After enabling HSE, add a software delay of about 10 milliseconds, then wait for the HSE Ready flag to be set before running the code.

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4 GPIO And AFIO

4.1 GPIO Analog Function

Description:

When the 4 GPIOs (PA1/PA2/PA3/PA4) are in the high-level output state, and they switch to the analog function, there will be a transient output voltage drop of about 30mv during the switching process.

Workaround:

Avoid the above usage methods.

4.2 IO Reverse Current

Description:

If the IO that does not support failsafe function is powered on before VDD, an exception may occur at this time, and the external pin reset cannot return to normal after the exception.

Workaround:

It is recommended that customers use the power-on of VDD prior to the power-on of IO.

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5 Analog/Digital Conversion (ADC)

5.1 When the Injection Channel is Triggered, The Regular Channel is Also Triggered

Description:

When performing ADC continuous conversion with external triggering disabled for regular channels, and an injection channel conversion is triggered by software or hardware, The regular channels may be triggered for conversion, and the corresponding status bits for the regular channels will be set.

Workaround:

Ignore the flags and data generated by the regular channels.

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6 Serial Peripheral Interface (SPI)

6.1 SPI Interface

6.1.1 SPI Baud Rate Setting When CRC Is Enabled

Description:

When the CRC function is turned on, depending on the operating environment of the SPI interface, such as board-level delay, ambient temperature, etc., CRC errors may occur for both the SPI master and slave.

In an ideal laboratory environment at room temperature, when the SPI clock is greater than 14MHz, an abnormal CRC check error may occur.

Workaround:

When the CRC function is enabled, it is recommended to configure the CRC clock frequency to not exceed 14MHz.

When a CRC exception error occurs, it is recommended to reduce the configuration SPI baud rate.

6.1.2 Checking Slave Mode CRC

Description:

In SPI operating in slave mode with CRC validation enabled, even if the NSS pin is at a high level, CRC calculation continues if the SPI receives a clock signal.

Workaround:

1. Before using CRC validation, clear the CRC data register to ensure synchronization between the CRC checks of the master and slave devices. The clearing steps are as follows: reset the SPI enable bit (set to 0).
2. Reset the CRC validation bit (set to 0).
3. Set the CRC validation bit (set to 1).
4. Set the SPI enable bit (set to 1).

6.1.3 When The Power Supply Voltage Is 1.8V~2.0V, The SPI Data Rate May Not Reach 18Mbps

Description:

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When the power supply voltage is 1.8V~2.0V, the SPI data rate may not reach 18Mbps depending on the IO and board-level wiring delay characteristics.

The highest communication rate measured in the ideal environment of the laboratory is:

-25℃ ~ 45℃: rate up to 18Mbps.

-40℃ ~ -25℃, 45℃-105℃: rate up to 12Mbps.

Workaround:

If customers have SPI communication requirements at high or low temperatures with a 1.8V power supply, it is recommended to contact the technical support of NSING TECHNOLOGIES PTE.LTD.

6.2 I2S Interface.

6.2.1 PCM Long Frame Mode

Description:

When I2S operates in master mode, PCM long frame mode, and the data format is "32bit" or "16bit extended to 32bit", the WS signal is one cycle per 16bit instead of 32bit.

Workaround:

When I2S is the master mode and the long frame mode must be used, the 16bit data mode should be used.

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7 I2C Interface

7.1 Handling Software Events Before Current Byte Transferring.

Description:

In the occurrence of events EV7, EV7_1, EV6_1, EV6, EV2, EV8, and EV3, it is essential to handle the events before the current byte transfer to prevent issues such as reading an extra byte, obtaining duplicate data, or losing data. If the software fails to read the N-1 data before the stop signal generation, the data in the shift register for the Nth byte may become corrupted (shifted left by one bit).

Workaround:

1. When transferring more than one byte in I2C, consider using DMA if possible.
2. When using I2C interrupts, set the interrupt priority to the highest priority in the application.
3. When the read data reaches the N-1 byte:
   a) Check that BSF (Byte Shift Flag) is set to 1.
   b) Configure SCL as a GPIO open-drain output and set it to 0.
   c) Set STOPGEN to 1.
   d) Read the N-1 byte.
   e) Configure SCL back to I2C multiplex open-drain output mode.
   f) Read the last byte.

7.2 Attentions When Reading A Single Byte At Time

Description:

In master read mode, errors in reading data may occur when reading single-byte.

Workaround:

Single byte Read:

a) Upon receiving ADDRF.
b) Set ACKEN to 0.
c) Clear ADDRF bit (by reading STS1 first and then STS2).
d) Set STOPGEN to 1.
e) Read one byte of data.

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8 Universal Synchronous Asynchronous Receiver Transmitter (USART)

8.1 Parity Error Flag

Description:

During the reception of a byte of data, if a parity error is detected before receiving the stop bit, the parity error flag is set. During this period, the parity error flag cannot be cleared through software (by reading the status register and then reading the data register). If the parity error interrupt is enabled, it may repeatedly enter the parity error interrupt handling function.

Workaround:

When the read data buffer flag is set, clear the parity error flag after receiving the data. If the parity error interrupt is enabled, to avoid multiple entries into the interrupt handling function, disable the parity error interrupt upon the first entry into the parity error interrupt, and then re-enable the parity error interrupt after receiving the data.

8.2 RTS Hardware Flow Control

Description:

When the RTS (Request to Send) hardware flow control is enabled, and a USART receives a frame of data, the RTS signal is automatically asserted (pulled high) upon receiving the first byte of data. If this first byte is not promptly read from the data register, upon receiving the next byte of data, the RTS signal is de-asserted (pulled low) again, and the USART waits for the reception of the next frame of data.

Workaround:

Before the next new data is received, the data is read out from the data register in time.

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9 Timer (TIM)

9.1 TIM Overcapture

Description:

When reading the capture data register data (normally, reading the data register will clear the capture flag), if an external trigger capture occurs, even if the previous capture has been correctly read and the new capture data has been accurately sent to the register, the repeat capture flag is still detected. The system is critical for overcapture, but no capture data is lost.

Workaround:

None

9.2 ADTIM And GPTIM Cannot Generate Compare Events Under Certain Circumstances

Description:

In edge-aligned mode, and up-counting PWM1 mode, when CCDATx shadow register value is greater than or equal to AR value in current PWM cycle, and if the CCDATx shadow register value cycle is equal to 0 in the next PWM cycle. No compare event will occur when the count value of the PWM period counter is equal to the value of the CCDATx shadow register is 0.

Workaround:

If it is not required that "the compare event is generated at the time when the count value = the shadow register of the comparison value =0", the compare event can be generated through another channel.

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10 Real Time Clock (RTC)

10.1 RTC Subsecond Match

Description:

When using the RTC programmable alarm clock, disable the matching of date, hour, minute, and second mode, only enable the matching of the sub-seconds mode. This means that an alarm interrupt is generated when the sub-seconds match every second. However, the alarm interrupt is not generated at the first sub-seconds match after enabling RTC alarm, and the alarm interrupt is generated for each sub-second match after that.

Workaround:

None.

10.2 RTC Second Match

Description:

When the RTC alarm is configured in second match mode, the chip enters SLEEP mode. If an alarm interrupt wakes up the chip from SLEEP mode and the interrupt handling function is executed (only clearing the interrupt flag), and the chip immediately enters STOP mode, the next alarm interrupt cannot wake up the chip from STOP mode.

Workaround:

Before configuring the RTC time, it is necessary to enter the RTC initialization mode. Before entering this mode, ensure that the sub-second register value is less than the synchronous prescaler value and not equal to 0.

10.3 RTC Calendar Function Cannot Be Initialized Multiple Times Within 1 Second

Description:

Multiple initializations of the RTC calendar function within 1 second will result in the inability to generate RTC alarm interrupts.

Workaround:

The interval between two initializations of the RTC calendar function should be more than 1 second.

10.4 RTC Mistakenly Triggers TISOVF Flag Bit

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When the system wakes up from STANDBY mode or reset by IWDG timeout, TISOVF flag in RTC may be set incorrectly.

Workaround:

Before entering STANDBY mode or when the system is reset by IWDG timeout, when the SHOPF flag is 0, configure RTC_SCTRL.SUBF[14:0] register once, and the SHOPF flag will be set to 1. When the SHOPF flag is 0 again, it should configure RTC_SCTRL.SUBF[14:0] register for the second time. This will solve the issue.

Note: that NRST cannot be triggered during above process.

10.5 RTC_DATE Register Lock

Description:

1. Before the system software reset, if the RTC_DATE register is not read after reading the RTC_SUBS or RTC_TSH shadow register, and after the system software reset, if the RTC is initialized without configuring or reading the RTC_DATE register, then the RTC_DATE register will revert to its default value;
2. When reading the calendar, after reading the RTC_SUBS or RTC_TSH shadow register, the value of the RTC_DATE register remains unchanged.

Workaround:

1. Read the RTC_DATE register before initializing the RTC;
2. After reading the RTC_SUBS or RTC_TSH shadow register, then read the RTC_DATE register.

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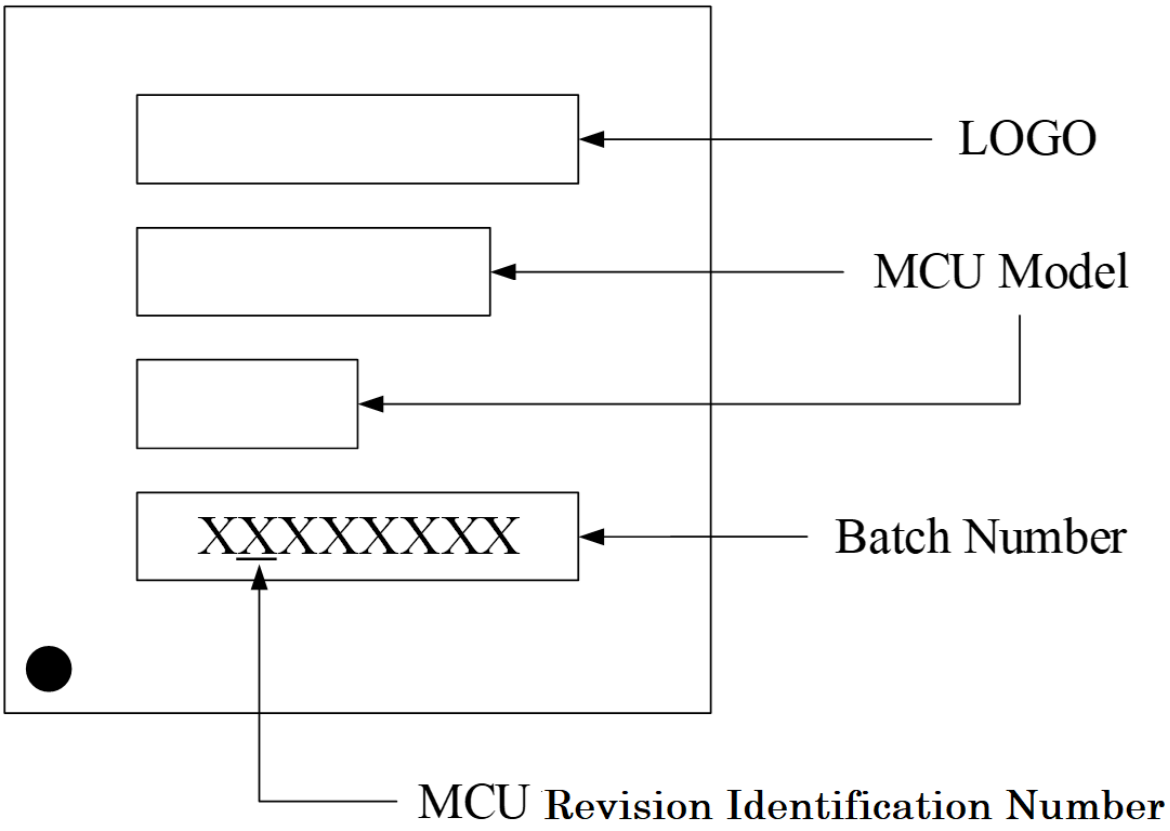
11 Chip Marking And Revision Description



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12 Version History

Version	Date	Changes
V1.1	2022.6.14	Initial version
V1.2.0	2023.7.31	1. Add section 3.1、3.3 2. Add section 6.1.3 3. Modify 6.1.1 4. Add section 2.1 5. Add section 10.4、10.5

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